HD3SS3412 4チャネルの高性能差動スイッチ

1 特長

- PCI Express Gen IIIおよびUSB 3.0を含む、最高12Gbpsの複数のインターフェイス標準と互換
- 8GHzを超える広い-3dB差動BW
- 優れた動的特性(4GHz時)
  - クロストーク＝－35dB
  - オフ絶縁＝－19dB
  - 挿入損失＝－1.5dB
  - 反射損失＝－11dB
- 双方向「マルチプレクサ/デマルチプレクサ」型差動スイッチ
- VDD動作範囲: 3.3V±10%
- 小型の3.5mm×9.0mm、42ピンWQFNパッケージ
- 共通の業界標準ピン配置
- XAUIおよびSGMIIのサポート

2 アプリケーション

- デスクトップPCおよびノートPC
- サーバーおよびストレージ・エリア・ネットワーク
- PCI Expressバックプレーン
- 共有I/Oポート

3 概要

HD3SS3412デバイスは、PCまたはサーバーで1つのソースから2つのターゲットのいずれかに接続するために2つのフルPCI Express x1レーンを使用するアプリケーションなど、4つの差動チャネルのスイッチングに対応した高速パッシブ・スイッチです。HD3SS3412は双方向型なので、2つのプラットフォーム間で共有するペリフェラルなど、1つのターゲット・デバイスと2つのソース・デバイスとの接続を可能にするアプリケーションもサポートしています。HD3SS3412には1つの制御線(SELピン)があり、これを使用してポートAと、ポートBまたはポートCとの間の信号経路を制御できます。

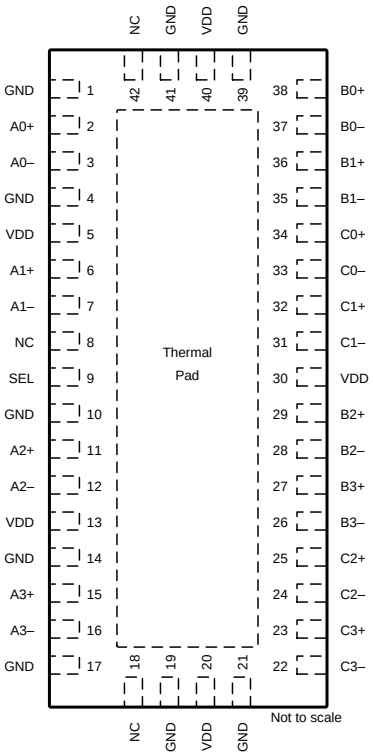
HD3SS3412は、他の複数のベンダと共通の実装サイズを持つ、業界標準の42ピンWQFNパッケージで供給されます。このデバイスは、-40℃～85℃の温度範囲全体にわたって、3.3Vの単一電源で動作が規定されています。

製品情報(1)

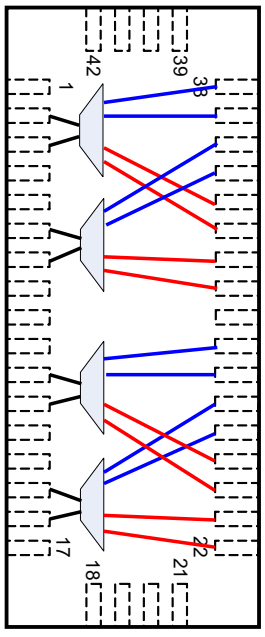
型番	パッケージ	本体サイズ(公称)
HD3SS3412	WQFN (42)	9.00mm×3.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

HD3SS3412のピン配置



HD3SS3412スイッチのフロースルー配線



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (January 2015) から **Revision F** に変更 **Page**

- 温度範囲を「0℃～70℃」から「-40℃～85℃」に変更 ... 1
- Changed T_A To: –40°C MIN and 85°C MAX From: 0°C MIN and 70°C MAX in the *Recommended Operating Conditions* table ... 7
- Changed the P_D values From: MIN = 15.5, MAX = 21.6 To: MIN = 2.8, MAX = 4.4 in the *Dissipation Ratings* table ... 8

Revision D (December 2015) から **Revision E** に変更 **Page**

- Changed "over the full industrial temperature range of –40°C to 70°C" To: "over the commercial temperature range of 0°C to 70°C" in the *Overview* section ... 13

Revision C (July 2015) から **Revision D** に変更 **Page**

- Changed "full industrial temperature range of –40°C to 85°C" To: "full industrial temperature range of 0°C to 70°C" in the *Overview* section ... 13

Revision B (November 2013) から **Revision C** に変更 **Page**

- 「*ピン構成および機能*」セクション、「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- 「*注文情報*」表を削除 ... 1

Revision A (February 2012) から **Revision B** に変更 **Page**

- 追加機能: 双方向「マルチプレクサ/デマルチプレクサ」型差動スイッチ 追加 ... 1
- デバイスがXAUIおよびSGMIIをサポートすることを追記 ... 1
- 「*概要*」セクションで「産業用」を削除し、温度範囲を「-40℃～85℃」から「0℃～70℃」に 変更 ... 1
- Changed pin description of NC From: Electrically not connected. To: Electrically not connected. May connect to

VDD or GND, or leave unconnected 6
- Added the *Application Information* section 15

2012年1月発行のものから更新 **Page**

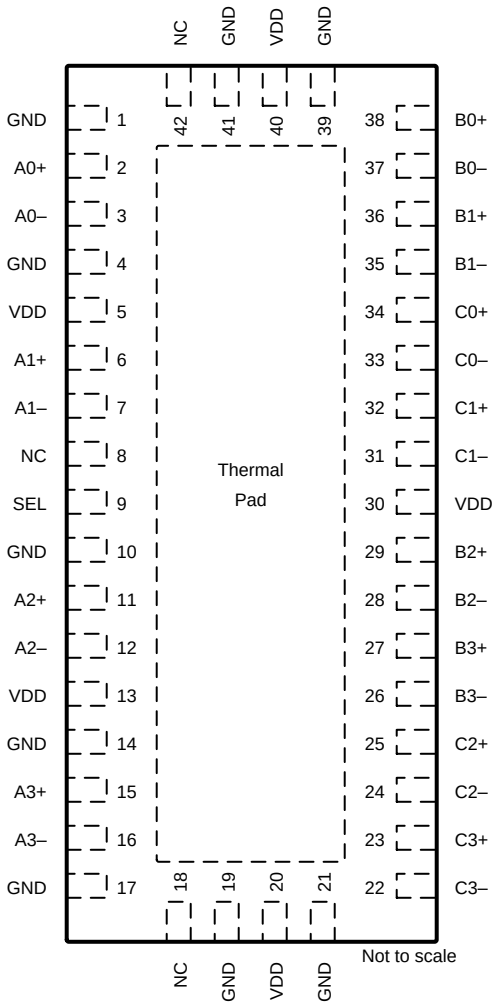
- 差動BWの箇条書き項目を「7.5GHZ」から「8GHz」に 変更 1
- 「特長」の動的特性についての箇条書き副項目を「絶縁」から「オフ絶縁」に 変更 1
- 動的特性についての箇条書き副項目の反射損失を「-9dB」から「-11dB」に 変更 1
- 動的特性についての箇条書き副項目「最大ペア内(ビット-ビット)スキュー」を 削除 1
- Changed ESD, Human body model, MAX voltage from "±2000" to "±4,000" in Absolute Maximum Ratings table 7
- Changed I_{LK} spec (Diff I/O pins) MAX value from "4 µA" to "130 µA" and added [Ports B and C] and [Port A] to Conditions statements. 8
- Changed t_{PD} spec MAX delay from "50" ps to "85" ps in Device Parameters table 8
- Changed SEL-to-switch T_{on} and T_{off} spec TYP values from "175" ns to "70" ns; in the Device Parameters table 8
- Changed T_{SKEW_Inter} and T_{SKEW_Intra} spec MAX values from "5 ps" and "4 ps" respectively, to "20 ps" and "8 ps" respectively, in Electrical Characteristics table 8
- Changed R_L spec TYP value from "–25" and "–9" dB to "–28" and "–11" dB for f=0.3 MHz and f=4000 MHz, respectively, in Electrical Characteristics table. 8
- Changed O_{IRR} spec TYP value from "–70" to "–75" dB for f=0.3 MHz, in Electrical Characteristics table. 8
- Changed BW spec TYP value from "7.5" GHz to "8" GHz in Electrical Characteristics table. 8
- Changed graphic image for Figure 3. 10
- Changed graphic image for Figure 4 10

5 概要（続き）

HD3SS3412は、回路基板における2点間の高速信号のルーティングに使用可能な、汎用4チャネル高速マルチプレクサ/デマルチプレクサ型スイッチです。PCI Express Gen IIIアプリケーション専用に設計されていますが、ほかにもUSB 3.0やDisplayPort 1.2など、差動振幅1800mVpp未満、同相電圧2V未満のいくつかの高速データ・プロトコルをサポートしています。このデバイスにある1つのセレクト(SEL)入力ピンは、システム内で利用可能なGPIOピンにより、またはマイクロコントローラから簡単に制御できます。

6 Pin Configuration and Functions

RUA Package
42-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCH PORT A			
A0+	2	I/O	Port A, Channel 0, High-Speed Positive Signal
A0–	3	I/O	Port A, Channel 0, High-Speed Negative Signal
A1+	6	I/O	Port A, Channel 1, High-Speed Positive Signal
A1–	7	I/O	Port A, Channel 1, High-Speed Negative Signal
A2+	11	I/O	Port A, Channel 2, High-Speed Positive Signal
A2–	12	I/O	Port A, Channel 2, High-Speed Negative Signal
A3+	15	I/O	Port A, Channel 3, High-Speed Positive Signal
A3–	16	I/O	Port A, Channel 3, High-Speed Negative Signal
SWITCH PORT B			
B0+	38	I/O	Port B, Channel 0, High-Speed Positive Signal
B0–	37	I/O	lPort B, Channel 0, High-Speed Negative Signal

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
B1+	36	I/O	Port B, Channel 1, High-Speed Positive Signal
B1–	35	I/O	Port B, Channel 1, High-Speed Negative Signal
B2+	29	I/O	Port B, Channel 2, High-Speed Positive Signal
B2–	28	I/O	Port B, Channel 2, High-Speed Negative Signal
B3+	27	I/O	Port B, Channel 3, High-Speed Positive Signal
B3–	26	I/O	Port B, Channel 3, High-Speed Negative Signal
SWITCH PORT C			
C0+	34	I/O	Port C, Channel 0, High-Speed Positive Signal
C0–	33	I/O	Port C, Channel 0, High-Speed Negative Signal
C1+	32	I/O	Port C, Channel 1, High-Speed Positive Signal
C1–	31	I/O	Port C, Channel 1, High-Speed Negative Signal
C2+	25	I/O	Port C, Channel 2, High-Speed Positive Signal
C2–	24	I/O	Port C, Channel 2, High-Speed Negative Signal
C3+	23	I/O	Port C, Channel 3, High-Speed Positive Signal
C3–	22	I/O	Port C, Channel 3, High-Speed Negative Signal
CONTROL, SUPPLY, AND NO CONNECT			
NC	8	—	Electrically not connected. May connect to VDD or GND, or leave unconnected.
	18		
	42		
GND	1	Supply	Negative power supply voltage
	4		
	10		
	14		
	17		
	19		
	21		
	39		
	41		
	Center Pad		
SEL	9	I	Select between port B or port C. Internally tied to GND through a 100-kΩ resistor
VDD	5	Supply	Positive power supply voltage
	13		
	20		
	30		
	40		

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage (V_{DD})	Absolute minimum/maximum supply voltage	–0.5	4	V
Voltage	Differential I/O	–0.5	4	V
	Control pin (SEL)	–0.5	VDD + 0.5	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Typical values for all parameters are at V_{DD} = 3.3 V and T_A = 25°C. (Temperature limits are specified by design)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3	3.3	3.6	V
V_{IH}	Input high voltage (SEL pin)		2		VDD	V
V_{IL}	Input low voltage (SEL pin)		–0.1		0.8	V
V_{I/O_Diff}	Differential voltage (differential pins)	Switch I/O diff voltage	0		1.8	VPP
V_{I/O_CM}	Common voltage (differential pins)	Switch I/O common-mode voltage	0		2	V
T_A	Operating free-air temperature	Ambient temperature	-40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		HD3SS3412 RUA (WQFN) 42 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	27.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
I_{IH}	Input High Voltage (SEL)	V_{DD} = 3.6 V; V_{IN} = VDD			95	µA
I_{IL}	Input Low Voltage (SEL)	V_{DD} = 3.6 V; V_{IN} = GND			1	µA
I_{LK}	Leakage Current (Differential I/O pins)	V_{DD} = 3.6 V; V_{IN} = 0 V; V_{OUT} = 2 V (I_{LK} On OPEN outputs) [Ports B and C]			130	µA
		V_{DD} = 3.6 V, V_{IN} = 2 V; V_{OUT} = 0 V (I_{LK} On OPEN outputs) [Port A]			4	
I_{DD}	Supply Current	V_{DD} = 3.6 V; SEL = V_{DD}/GND; Outputs Floating		4.7	6	mA
C_{ON}	Outputs ON Capacitance	V_{IN} = 0 V; Outputs Open; Switch ON		1.5		pF
C_{OFF}	Outputs OFF Capacitance	V_{IN} = 0 V; Outputs Open, Switch OFF		1		pF
R_{ON}	Output ON resistance	V_{DD} = 3.3 V; V_{CM} = 0.5 V to 1.5 V ; I_O = –8 mA		5	8	Ω
ΔR_{ON}	ON-resistance match between channels	V_{DD} = 3.3 V ; –0.35 V ≤ V_{IN} ≤ 1.2 V; I_O = –8 mA			2	Ω
	ON-resistance match between pairs of the same channel	V_{DD} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 1.2 V; I_O = –8 mA			0.7	Ω
R_{FLAT_ON}	ON-resistance flatness ($R_{ON(MAX)}$ – $R_{ON(MAIN)}$)	V_{DD} = 3.3 V; –0.35 V ≤ V_{IN} ≤ 1.2 V			1.15	Ω
t_{PD}	Switch propagation delay	Rsc and R_{LOAD} = 50 Ω			85	ps
	SEL-to-switch T_{ON}	Rsc and R_{LOAD} = 50 Ω		70	250	ns
	SEL-to-switch T_{OFF}			70	250	
T_{SKEW_Inter}	Inter-pair output skew (CH-CH)	Rsc and R_{LOAD} = 50 Ω			20	ps
T_{SKEW_Intra}	Intra-pair output skew (bit-bit)	Rsc and R_{LOAD} = 50 Ω			8	ps
R_L	Differential return loss (VCM = 0 V) Also see *Typical Characteristics*	f = 0.3 MHz		–28		dB
		f = 2500 MHz		–12		
		f = 4000 MHz		–11		
X_{TALK}	Differential Crosstalk (VCM = 0 V) Also see *Typical Characteristics*	f = 0.3 MHz		–90		dB
		f = 2500 MHz		–39		
		f = 4000 MHz		–35		
O_{IRR}	Differential Off-Isolation (VCM = 0 V) Also see *Typical Characteristics*	f = 0.3 MHz		–75		dB
		f = 2500 MHz		–22		
		f = 4000 MHz		–19		
I_L	Differential Insertion Loss (VCM = 0 V) Also see *Typical Characteristics*	f = 0.3 MHz		–0.5		dB
		f = 2500 MHz		–1.1		
		f = 4000 MHz		–1.5		
BW	Bandwidth	At –3 dB		8		GHz

7.6 Dissipation Ratings

		MIN	MAX	UNIT
P_D	Power Dissipation	2.8	4.4	mW

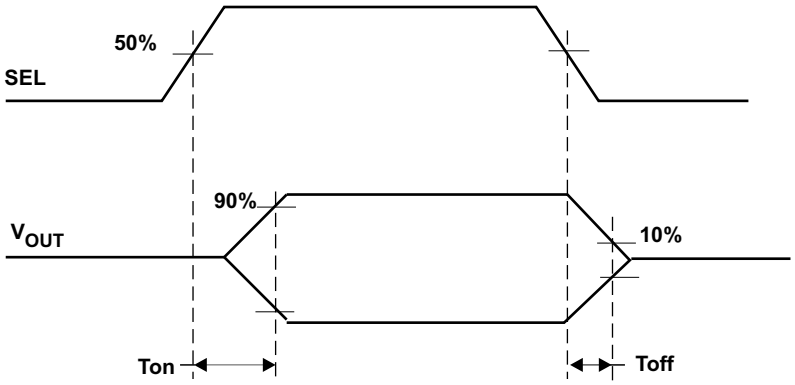
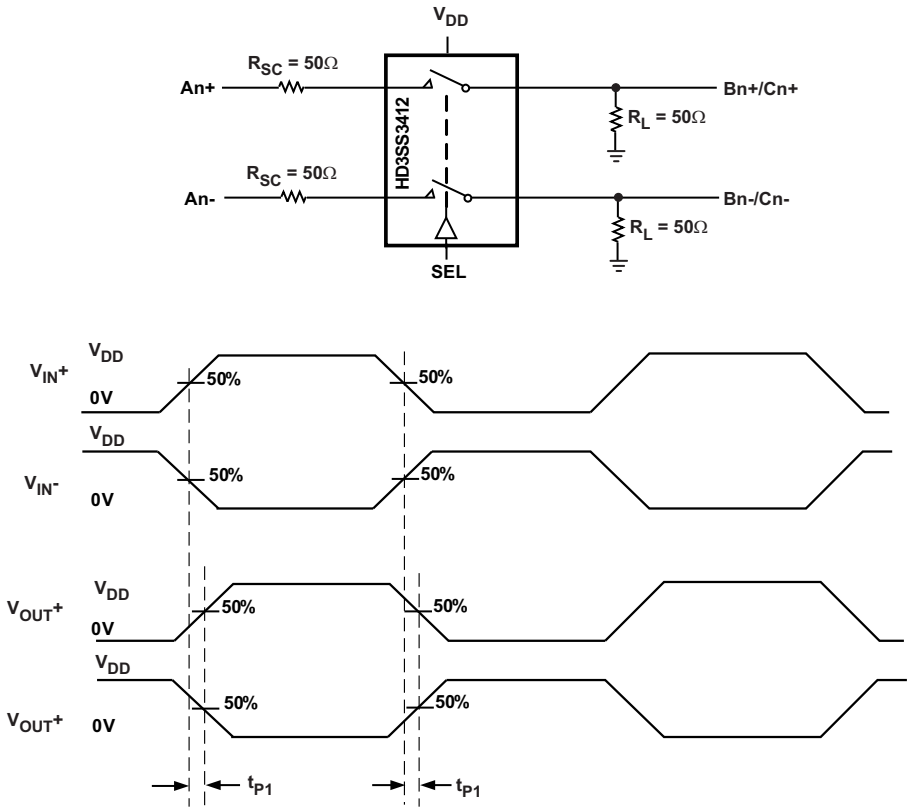


Figure 1. Switch ON and OFF Timing Diagram



$T_{SKEWInter}$ = Difference between t_{PD} for any two pairs of outputs

$T_{SKEWIntra}$ = Difference between t_{P1} and t_{P2} of same pair

Figure 2. Propagation Delay Timing Diagram and Test Setup

7.7 Typical Characteristics

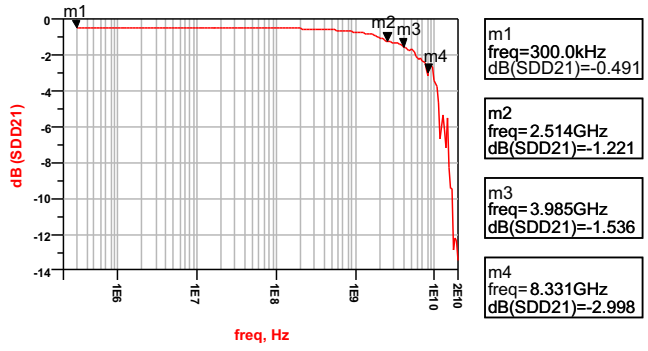


Figure 3. Differential Insertion Loss

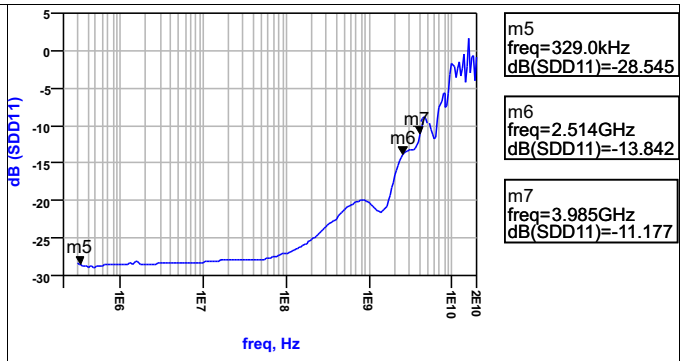


Figure 4. Differential Return Loss

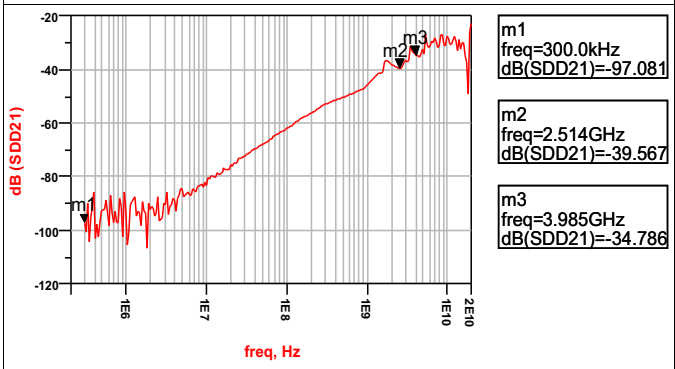


Figure 5. Differential Crosstalk

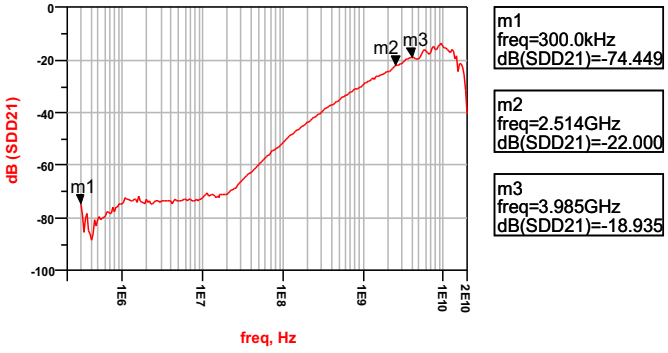


Figure 6. Differential Off Isolation

8 Parameter Measurement Information

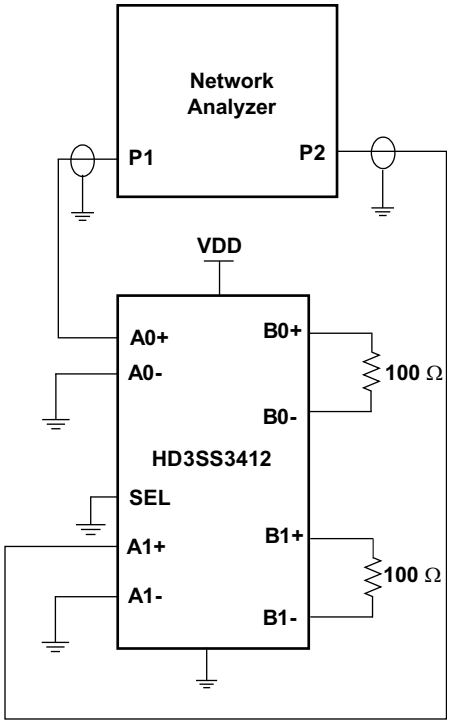


Figure 7. Cross Talk Measurement Setup

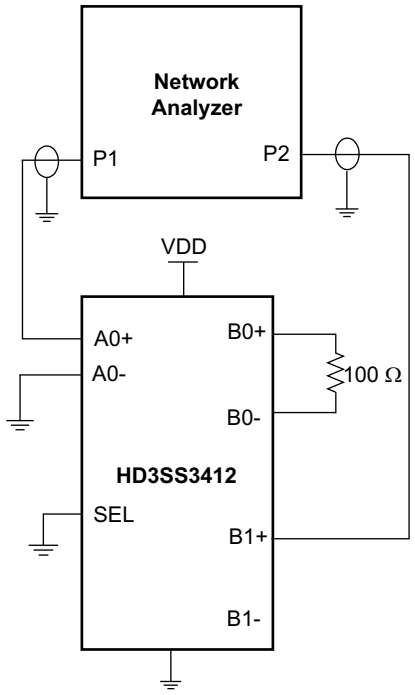


Figure 8. Off Isolation Measurement Setup

Parameter Measurement Information (continued)

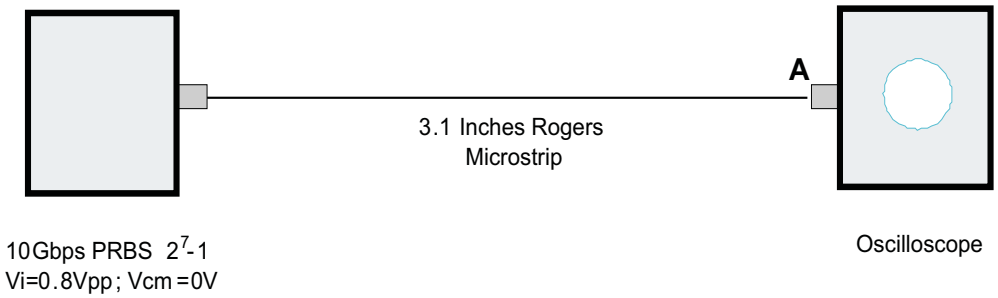


Figure 9. Source Eye Diagram Test Setup

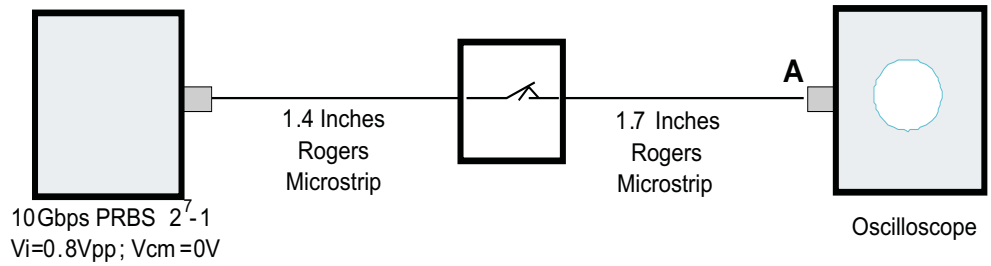


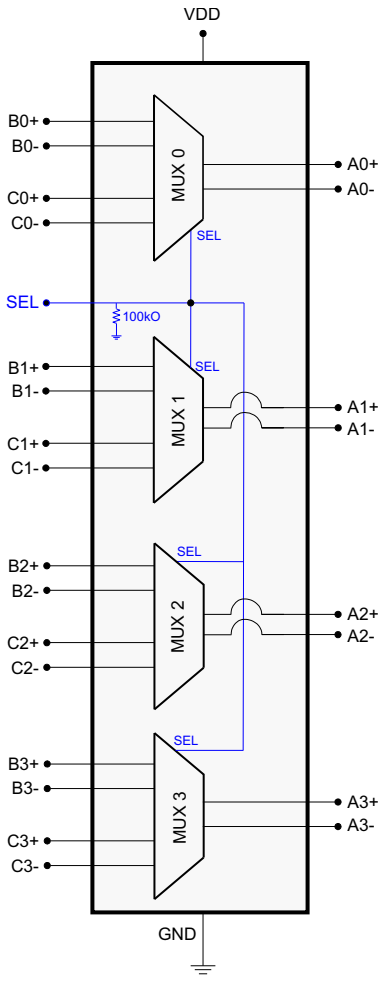
Figure 10. Output Eye Diagram Test Setup

9 Detailed Description

9.1 Overview

The HD3SS3412 is a high-speed passive switch offered in an industry standard 42-pin WQFN package available in a common footprint shared by several other vendors. The device is specified to operate from a single supply voltage of 3.3 V over the commercial temperature range of 0°C to 70°C. The HD3SS3412 is a generic 4-CH high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. Although it was designed specifically to address PCI Express Gen III applications, the HD3SS3412 will also support several other high-speed data protocols with a differential amplitude of < 1800 mVpp and a common-mode voltage of < 2.0 V, as with USB 3.0 and DisplayPort 1.2. The device's one select input (SEL) pin can easily be controlled by an available GPIO pin within a system or from a microcontroller.

9.2 Functional Block Diagram



9.3 Feature Description

The HD3SS3412 has a single control line (SEL Pin) which can be used to control the signal path between Port A and either Port B or Port C. The one select input (SEL) pin of the device can easily be controlled by an available GPIO pin within a system or from a microcontroller. The input signal is selected using the SEL pin.

Table 1. Mux Pin Connections(1)

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0+	B0+	C0+
A0–	B0–	C0–
A1+	B1+	C1+
A1–	B1–	C1–
A2+	B2+	C2+
A2–	B2–	C2–
A3+	B3+	C3+
A3–	B3–	C3–

(1) The HD3SS3412 can tolerate polarity inversions for all differential signals on Ports A, B, and C. Take care to ensure the same polarity is maintained on Port A versus Port B/C.

9.4 Device Functional Modes

Table 2 lists the functional modes for the HD3SS3412.

Table 2. HD3SS3412 Control Logic

CONTROL PIN (SEL)	PORT A TO PORT B CONNECTION STATUS	PORT A TO PORT C CONNECTION STATUS
L (Default State)	Connected	Disconnected
H	Disconnected	Connected

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 AC Coupling Caps

Many interfaces require AC coupling between the transmitter and receiver. The 0402 capacitors are the preferred option to provide AC coupling, and the 0603 size capacitors also work. The 0805 size capacitors and C-packs should be avoided. When placing AC coupling capacitors symmetric placement is best. A capacitor value of 0.1 µF is best and the value should be match for the ± signal pair. The placement should be along the TX pairs on the system board, which are usually routed on the top layer of the board.

There are several placement options for the AC coupling capacitors. Because the switch requires a bias voltage, the capacitors must only be placed on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. A few placement options are shown below. In Figure 11, the coupling capacitors are placed between the switch and endpoint. In this situation, the switch is biased by the system/host controller.

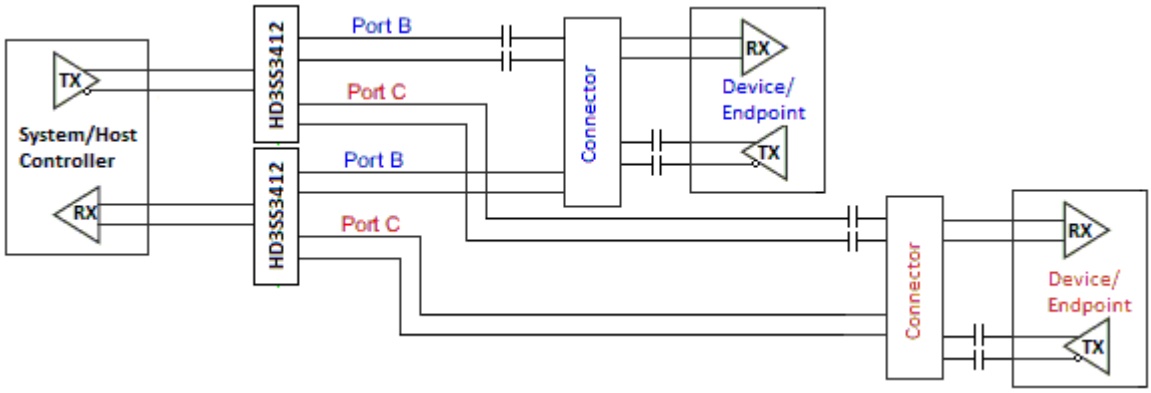


Figure 11. AC Coupling Capacitors Between Switch Tx and Endpoint Tx

In Figure 12, the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on the top is biased by the endpoint and the lower switch is biased by the host controller.

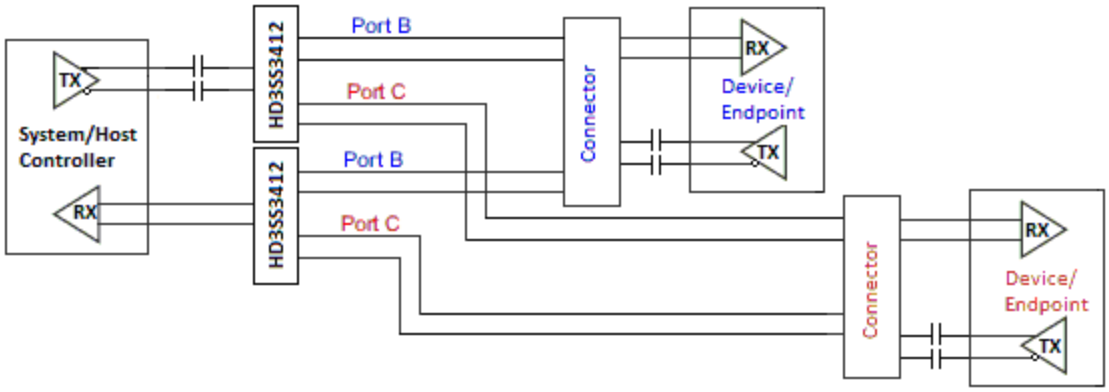


Figure 12. AC Coupling Capacitors on Host Tx and Endpoint Tx

Application Information (continued)

If the common-mode voltage in the system is higher than 2 V, the coupling capacitors are placed on both sides of the switch (shown in Figure 13). A biasing voltage of less than 2 V is required in this case.

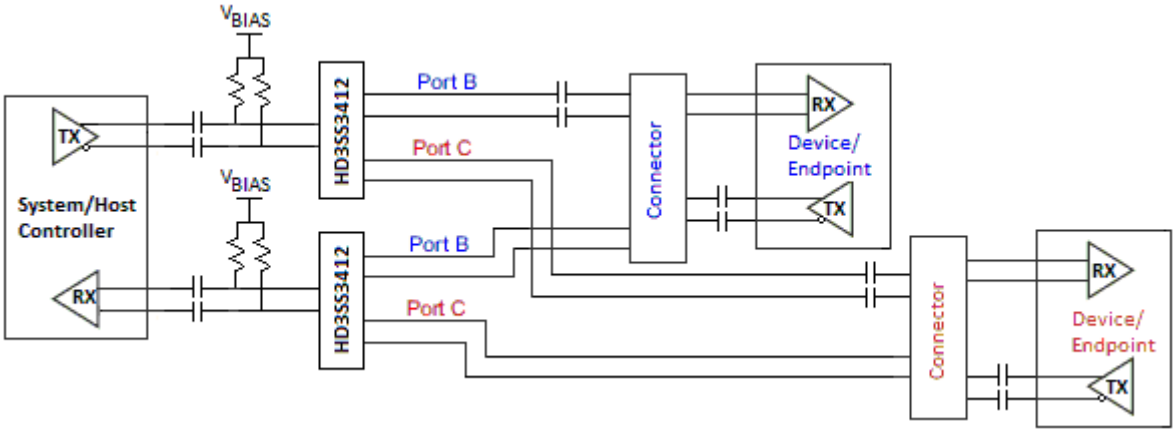


Figure 13. AC Coupling Capacitors on Both Sides of Switch

10.2 Typical Application

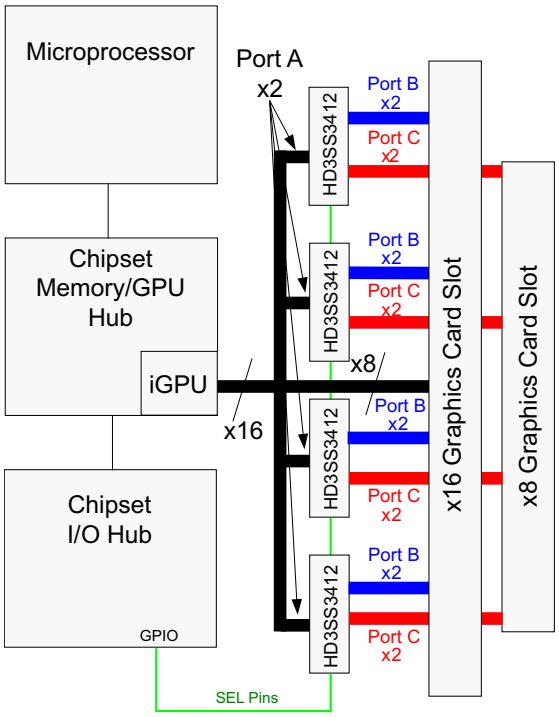


Figure 14. Typical Application Block Diagram

Typical Application (continued)

10.2.1 Design Requirements

Table 3 lists the design parameters of this example.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	3.3 V
Decoupling capacitors	0.1 µF
AC capacitors	75 nF – 200 nF (100 nF shown) USBAA TX p and n lines require AC capacitors. Alternate mode signals may or may not require AC capacitors

10.2.2 Detailed Design Procedure

- Connect VDD and GND pins to the power and ground planes of the printed circuit board, with 0.1-uF bypass capacitor
- Use +3.3-V TTL/CMOS logic level at SEL
- Use controlled-impedance transmission media for all the differential signals
- Ensure the received complimentary signals are with a differential amplitude of <1800 mVpp and a common-mode voltage of <2 V

10.2.3 Application Curves

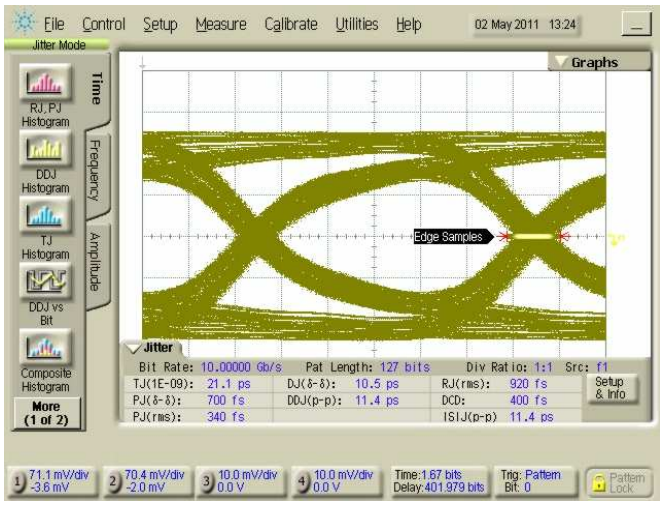


Figure 15. 10-gbps Source Eye Diagram at a: V_{ID} = 800 Mvpp; 2^7–1 Prbs; V_{CM}= 0 V

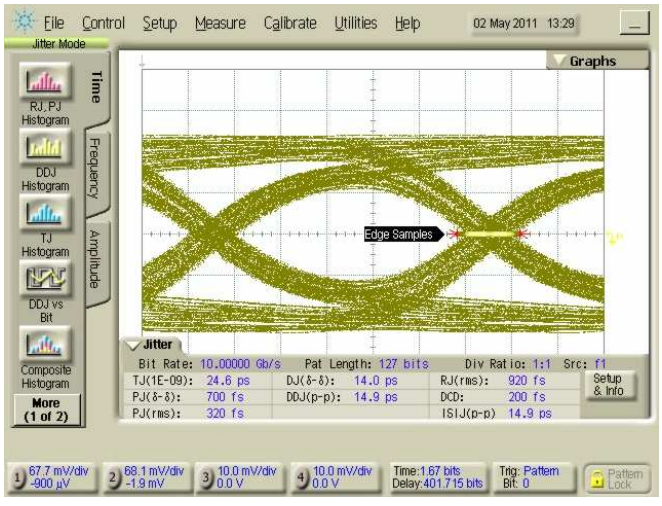


Figure 16. 10-gbps Output Eye Diagram at a: V_{ID} = 800 Mvpp; 2^7–1 Prbs; V_{CM}= 0v; V_{DD}= 3.3 V; Sel= 0 V

11 Power Supply Recommendations

The HD3SS3412 requires +3.3-V digital power sources. VDD 3.3 supply must have 0.1-μF bypass capacitors to VSS (ground) in order for proper operation. The recommendation is one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors like 0.01-μF are also recommended on the digital supply terminals.

12 Layout

12.1 Layout Guidelines

- Decoupling caps should be placed next to each power terminal on the HD3SS3412. Take care to minimize the stub length of the race connecting the capacitor to the power pin.
- Avoid sharing vias between multiple decoupling caps
- Place vias as close as possible to the decoupling cop solder pad
- Widen VDD/GND planes to reduce effect if static and dynamic IR drop
- The VBUS traces/planes must be wide enough to carry maximum of 2-A current

12.2 Layout Example

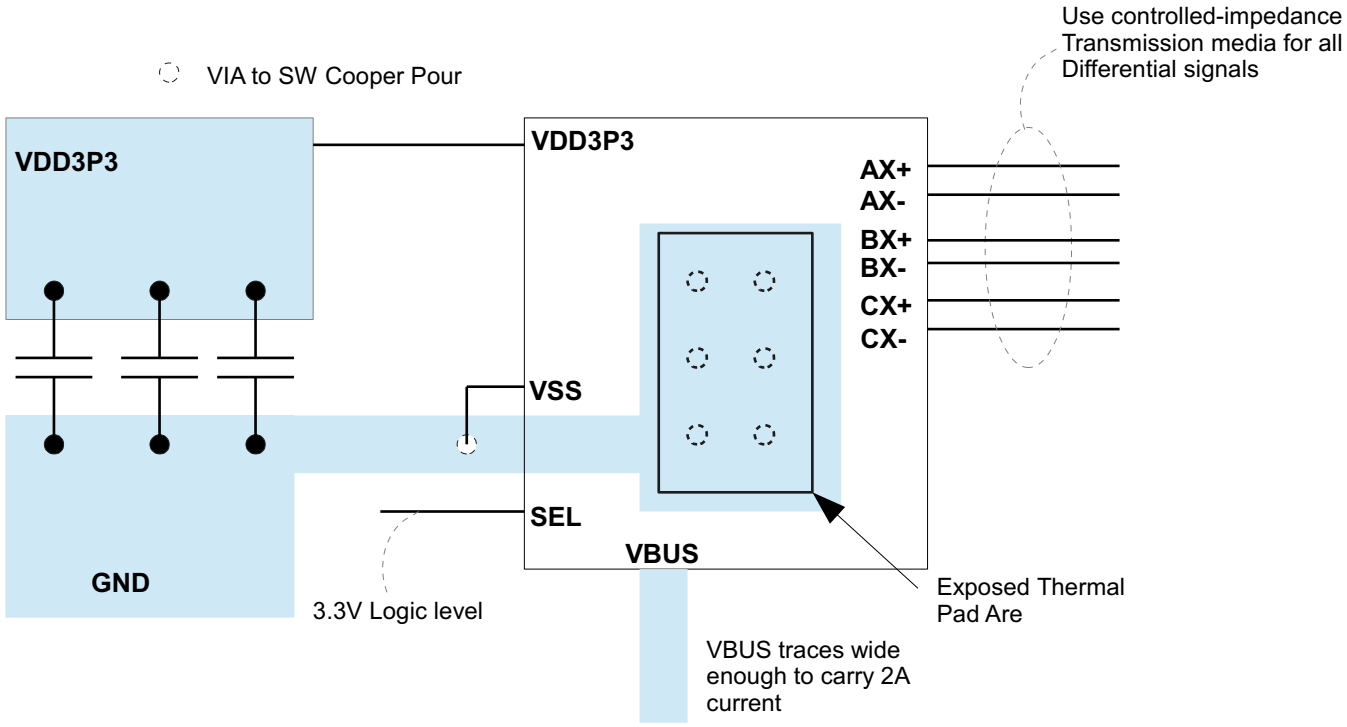


Figure 17. Layout Example

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*****エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

13.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
HD3SS3412RUAR	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HD3SS3412
HD3SS3412RUAT	Active	Production	WQFN (RUA) | 42	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	XHD3SS3412 HD3SS3412

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

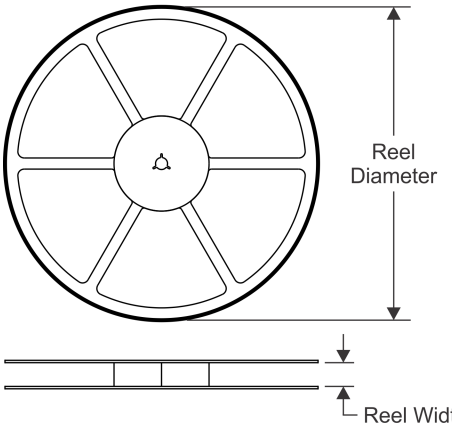
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

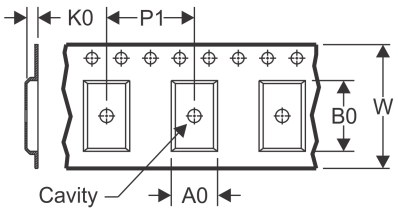
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

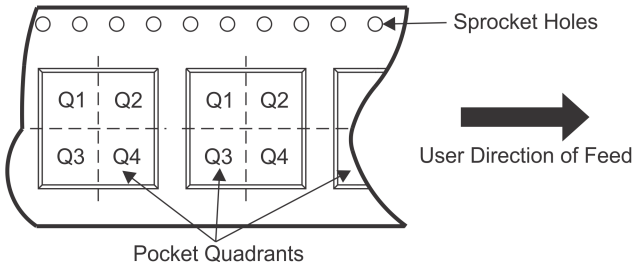


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

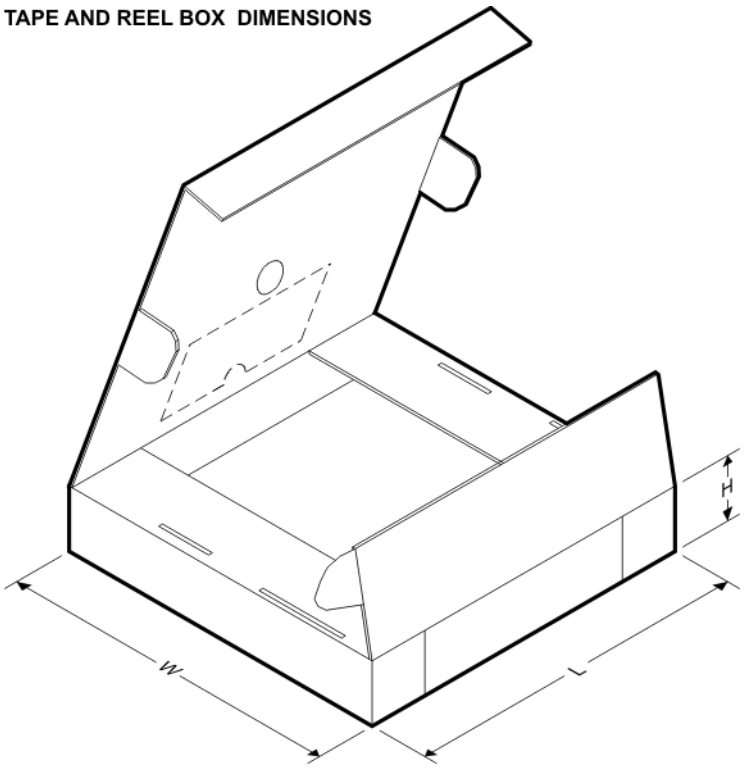
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS3412RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
HD3SS3412RUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS3412RUAR	WQFN	RUA	42	3000	367.0	367.0	38.0
HD3SS3412RUAT	WQFN	RUA	42	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

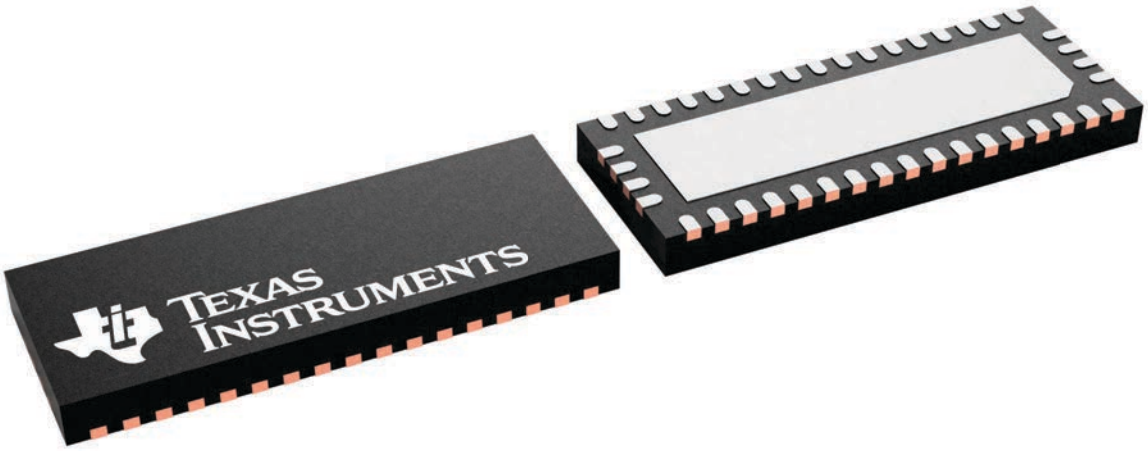
RUA 42

WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

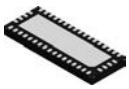
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226504/A

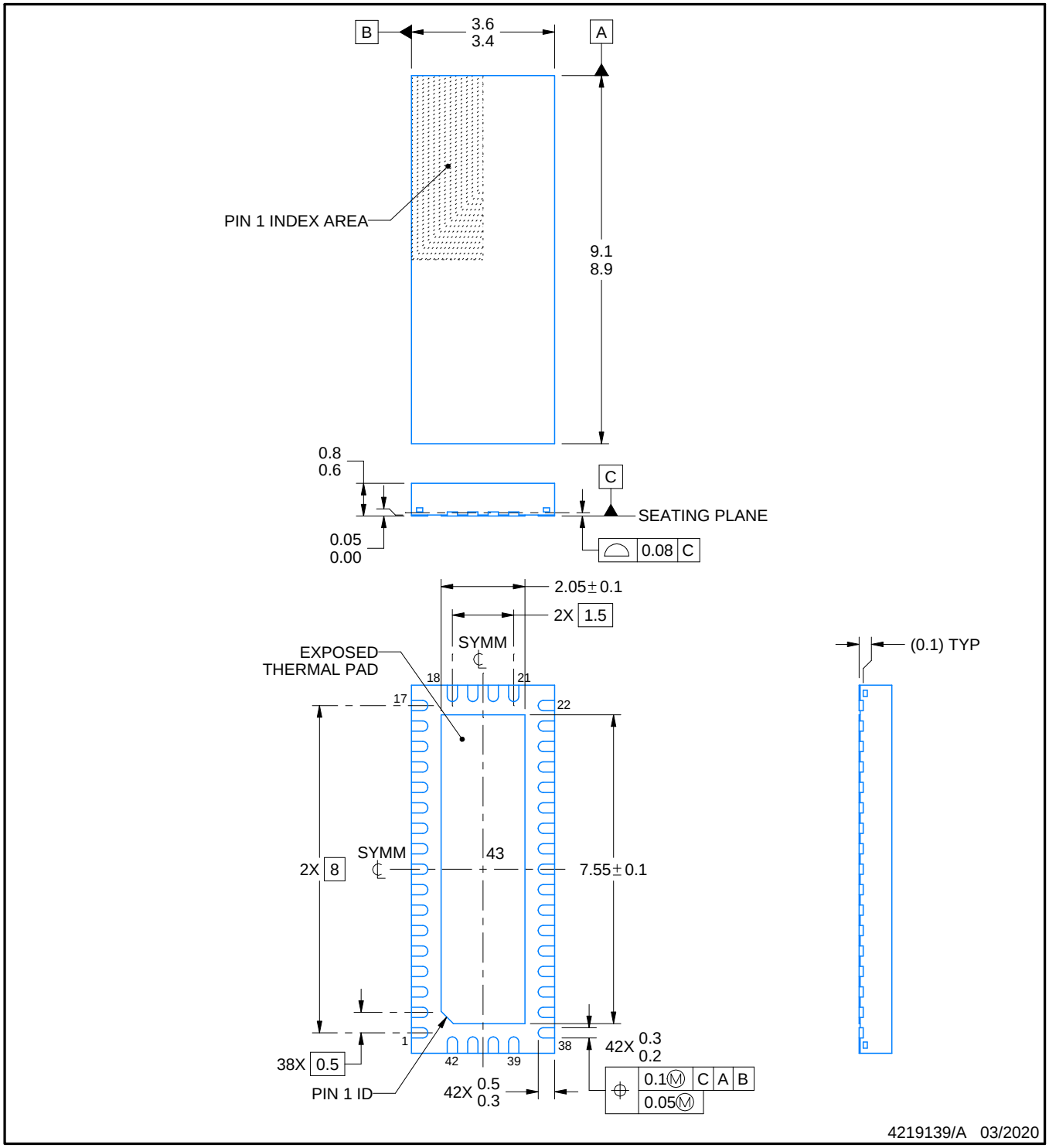
PACKAGE OUTLINE

RUA0042A



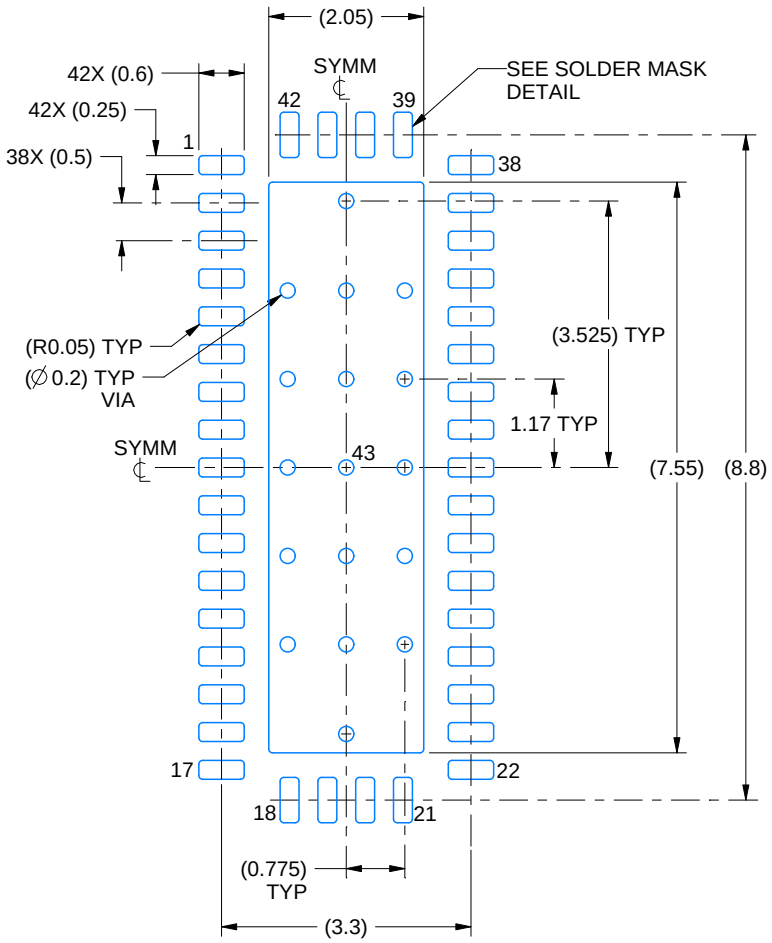
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

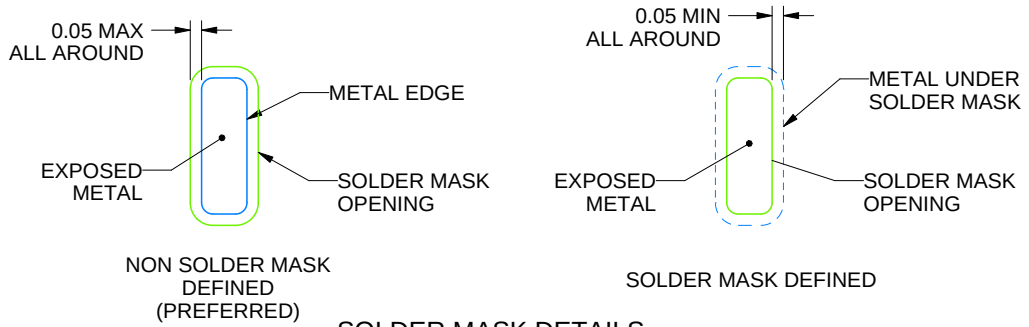


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4219139/A 03/2020

NOTES: (continued)

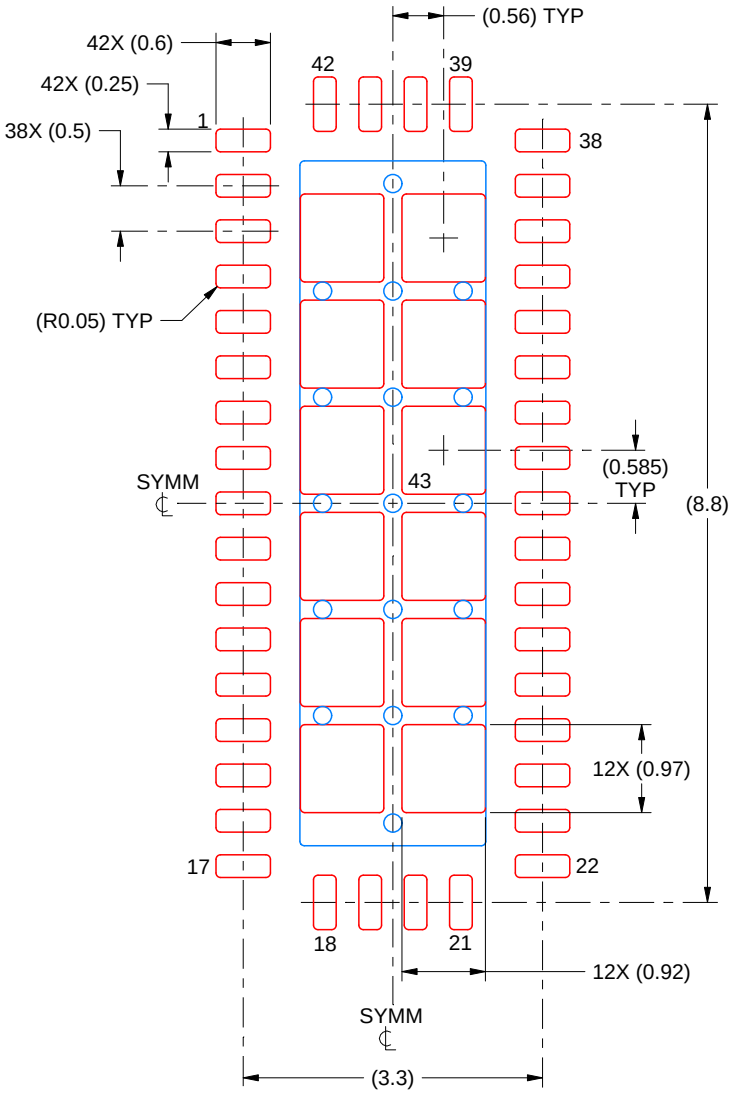
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219139/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月