INA4230 I²C インターフェイスを備えた 48V、4 チャネル、16 ビット、電流、電圧、電力、電力量モニタ

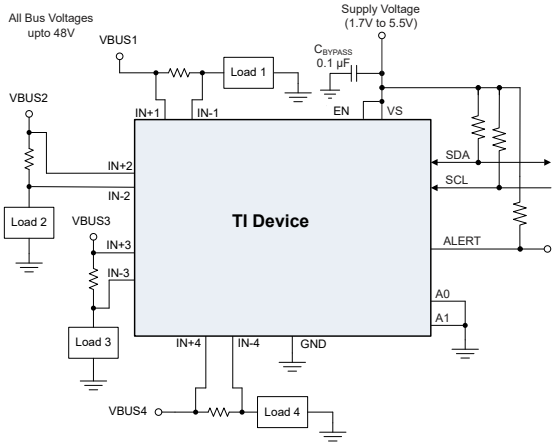
1 特長

- ハイサイドまたはローサイド電流センシング
- 1.7V～5.5V 電源で動作
- 電流、電圧、電力、電力量を報告
- プログラム可能なフルスケール レンジ：20mV/80mV
- 入力同相範囲：-0.3V～48V
- 電流監視精度：
  - 16 ビット ADC 分解能
  - ゲイン誤差 0.75% 以下
  - オフセット 75µV 以下
- 電力監視精度：
  - フルスケールの 1.5% 以下
- 電力量監視精度：
  - フルスケールの 2% 以下
- 低い入力バイアス電流：5nA (最大値)
- 小さい無効化時電流：1µA 以下
- 平均化オプションを構成可能
- アラート限界値による過電流および低電流イベント
- 1.2V 互換の I²C、SMBus インターフェイス
- ピンで選択可能な 16 つのアドレス
- DSBGA-16 パッケージ (1.5mm × 1.5mm)

2 アプリケーション

- ノート PC
- セキュリティ カメラ
- リテール オートメーション
- パワー・マネージメント
- バッテリ セル モニタとバランサ
- ラック サーバー

代表的なアプリケーション



3 概要

INA4230 デバイスは、1.2V～5V のデジタル バス電圧に対応した I²C/SMBus 互換インターフェイスを備えたクワッド チャネル 16 ビット デジタル電流モニタです。このデバイスは、外付けの検出抵抗の両端の電圧を監視し、各チャネルのシャント電圧、バス電圧、電流、電力、電力量の値を報告します。

INA4230 は、プログラム可能な ADC 変換時間と、すべてのチャネルに共通する平均化機能を特長としています。各チャネルはプログラム可能な較正値と内蔵乗算器を持っているため、電流 (A)、電力 (W)、電力量 (J) の数値を直接読み出すことができます。各チャネルは、IN– ピンに現れるバス電圧を監視し、過電流および低電流状態と過電圧および低電圧状態の発生時に警報を出すことができます。電流測定モードでは入力インピーダンスが高いため、値の小さいシステム電流を測定するのに必要とされる、より大きな電流検出抵抗を使用できます。

INA4230 は、電源電圧とは無関係に、-0.3V～48V の同相バス電圧の電流を検出できます。本デバイスは 1.7V～5.5V の単一電源で動作し、通常動作時に 400µA (標準値) の電源電流を消費します。本デバイスは、動作電流が 2.5µA (標準値) の低消費電力スタンバイ モードに移行させることができ、イネーブル ピンを使って完全に無効化することで、1µA 未満の消費電流を実現できます。このデバイスは -40℃～125℃の動作温度範囲で動作が規定されており、最大 16 つのアドレスをプログラム可能です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
INA4230	YBJ (DSBGA、16)	1.5mm × 1.5mm

(1) 供給されているすべてのパッケージについては、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

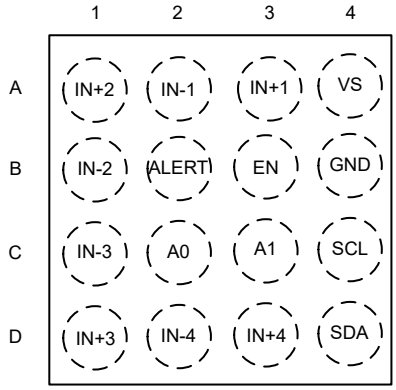

図 4-1. YBJ Package 16-Bump DSBGA (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	YBJ (DSBGA)		
A0	C2	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. 表 6-1 lists the pin settings and corresponding addresses.
A1	C3	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. 表 6-1 lists the pin settings and corresponding addresses.
ALERT	B2	Digital output	Multifunctional alert, open-drain output. This pin alerts to report fault conditions or can be configured to notify host when a conversion is complete.
EN	B3	Digital input	Enable pin. A logic high level enables the device; a logic low level disables the device.
GND	B4	Ground	Ground for both analog and digital.
IN–1	A2	Analog input	Channel 1 current sensing negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor. Bus voltage measurements are made with respect to this pin.
IN+1	A3	Analog input	Channel 1 current sensing positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
IN–2	B1	Analog input	Channel 2 current sensing negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor. Bus voltage measurements are made with respect to this pin.
IN+2	A1	Analog input	Channel 2 current sensing positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
IN–3	C1	Analog input	Channel 3 current sensing negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor. Bus voltage measurements are made with respect to this pin.
IN+3	D1	Analog input	Channel 3 current sensing positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
IN–4	D2	Analog input	Channel 4 current sensing negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor. Bus voltage measurements are made with respect to this pin.
IN+4	D3	Analog input	Channel 4 current sensing positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
SCL	C4	Digital input	Serial bus clock line, open-drain input.
SDA	D4	Digital input/output	Serial bus data line, open-drain input/output
VS	A4	Power Supply	Power supply, 1.7V to 5.5V

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply Voltage		6	V
V_{IN+}, V_{IN-}	Differential (V_{IN+}) - (V_{IN-})	–26	26	V
	Common - mode	GND – 0.3	50	V
V_{IO}	SDA, SCL, ALERT, A0, A1, EN	GND – 0.3	6	V
	Input current into any pin		5	mA
	Open-drain digital output current (SDA, ALERT)		10	mA
T_A	Operating Temperature	–55	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range	GND – 0.3		48	V
V_S	Operating supply range	1.7		5.5	V
T_A	Ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		INA4230 DSBGA 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Y_{JB}	Junction-to-board characterization parameter	21.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

at T_A = 25°C, V_S = 3.3V, V_{SENSE} = V_{IN+} - V_{IN-} = 0mV, V_{IN-} = V_{BUS} = 12V, for all channels (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
CMRR	Common-mode rejection	V_{CM} = –0.3V to 48V, T_A = –40°C to 125°C	110	120		dB
	Shunt voltage input range	ADCRANGE = 0	–81.9175		81.92	mV
		ADCRANGE = 1	–20.4794		20.48	mV
V_{os}	Shunt offset voltage	V_{CM} = 12 V		±10	±75	µV
dV_{os}/dT	Shunt offset voltage drift	T_A = –40°C to 125°C		±0.1	±0.5	µV/°C
V_{os_b}	IN- bus offset Voltage			±5	±30	mV
dV_{os_b}/dT	IN- bus offset voltage drift	T_A = –40°C to 125°C		±10	±30	µV/°C
$PSRR_{SH}$	Power supply rejection ratio (Current measurments)	V_S = 1.7V to 5.5V, T_A = –40°C to 125°C		±0.2	±2.5	µV/V
$PSRR_{BUS}$	Power supply rejection ratio (Voltage measurments)	V_S = 1.7V to 5.5V, T_A = –40°C to 125°C		±0.5	±2.5	mV/V
Z_{IN-}	IN- input impedance	Bus Voltage Measurement Mode		1.05		MΩ
I_B	Input bias current	IN+, IN-, Current Measurment Mode		0.1	5	nA
DC ACCURACY						
R_{DIFF}	Differential Input Impedance (IN+ to IN-)	V_{IN+} - V_{IN-} < 82mV		140		kΩ
	ADC Resolution	T_A = –40°C to 125°C		16		Bits
	1 LSB step size	Shunt Voltage		2.5		µV
		Bus Voltage		1.6		mV
	ADC Conversion-time (T_A = –40°C to 125°C)	CT bit = 000		140		µs
		CT bit = 001		204		µs
		CT bit = 010		332		µs
		CT bit = 011		588		µs
		CT bit = 100		1.100		ms
		CT bit = 101		2.116		ms
		CT bit = 110		4.156		ms
		CT bit = 111		8.244		ms
	Internal Oscillator Frequency	T_A = +25°C		500		kHz
	Internal Oscillator Tolerance	T_A = +25°C			0.5	%
		T_A = –40°C to +125°C			1	%
G_{SERR}	Shunt voltage gain error			±0.02	±0.75	%
G_{S_DRFT}	Shunt voltage gain error drift	T_A = –40°C to +125°C			50	ppm/°C
G_{BERR}	V_{IN-} voltage gain error			±0.02	±0.75	%
G_{B_DRFT}	V_{IN-} voltage gain error drift	T_A = –40°C to +125°C			50	ppm/°C
P_{TME}	Power total measurement error	At full scale voltage and current		±0.04	±1.5	%
E_{TME}	Energy total measurement error	At full scale voltage and current		±0.3	±2	%
INL	Integral Non-Linearity	ADCRANGE = 0, Linear best fit,T_A = –40°C to +125°C		±2	±6	m%
DNL	Differential Non-Linearity			±0.1		LSB

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at T_A = 25°C, V_S = 3.3V, V_{SENSE} = V_{IN+} - V_{IN-} = 0mV, V_{IN-} = V_{BUS} = 12V, for all channels (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE						
I_{EN}	Input leakage current	0 V ≤ V_{EN} ≤ V_S		1	50	nA
V_{IH}	Logic input level, high	V_S = 1.7V to 3.6V, T_A = –40°C to +125°C	1.1		5.5	V
V_{IH}	Logic input level, high	V_S = 3.6V to 5.5V, T_A = –40°C to +125°C	1.3		5.5	V
V_{IL}	Logic input level, low	V_S = 1.7V to 5.5V, T_A = –40°C to +125°C	0		0.4	V
V_{HYS}	Hysteresis			50		mV
POWER SUPPLY						
I_Q	Quiescent current			400	500	µA
		I_Q vs temperature, T_A = –40°C to +125°C			600	µA
		Shutdown		2.5	4	µA
I_Q	Quiescent current disabled	V_{EN} = 0V		0.15	1	µA
V_{POR}	Power-on reset threshold	V_S falling		0.95		V
SMBUS						
	SMBUS timeout			28	35	ms
	Input capacitance			3		pF
DIGITAL INTERFACE						
V_{IH}	Logic input level, high	V_S = 1.7V to 5.5V, T_A = –40°C to +125°C	0.9		5.5	V
V_{IL}	Logic input level, low	V_S = 1.7V to 5.5V, T_A = –40°C to +125°C	0		0.4	V
V_{HYS}	Hysteresis			130		mV
V_{OL}	Logic output level, low	I_{OL} = 3mA, V_S = 1.7V to 5.5V, T_A = –40°C to +125°C	0		0.3	V
	Digital leakage input current	0 ≤ V_{INPUT} ≤ V_S			±50	nA

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5.6 Timing Requirements (I^2C)

		MIN	NOM	MAX	UNIT
I^2C BUS (FAST MODE)					
$F_{(SCL)}$	I^2C clock frequency	1		400	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	600			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		900	ns
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1300			ns
$t_{(HIGH)}$	SCL clock high period	600			ns
t_F	Data fall time			300	ns
t_F	Clock fall time			300	ns
t_R	Clock rise time			300	ns
t_R	Clock rise time (SCLK ≤ 100 kHz)			1000	ns
I^2C BUS (HIGH-SPEED MODE)					
$F_{(SCL)}$	I^2C clock frequency	10		2940	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	160			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		125	ns
$t_{(SUDAT)}$	Data setup time	20			ns
$t_{(LOW)}$	SCL clock low period	200			ns
$t_{(HIGH)}$	SCL clock high period	60			ns
t_F	Data fall time			80	ns
t_F	Clock fall time			40	ns
t_R	Clock rise time			40	ns

5.7 Timing Diagram

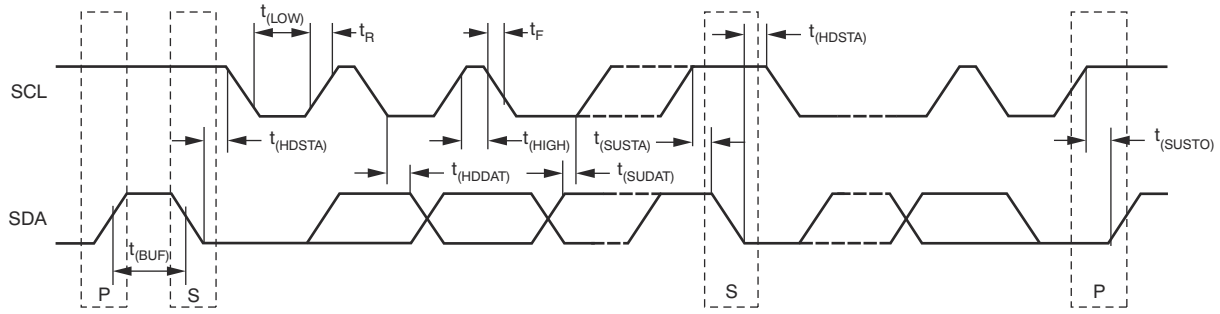

図 5-1. I^2C Timing Diagram

5.8 Typical Characteristics

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV (unless otherwise noted)

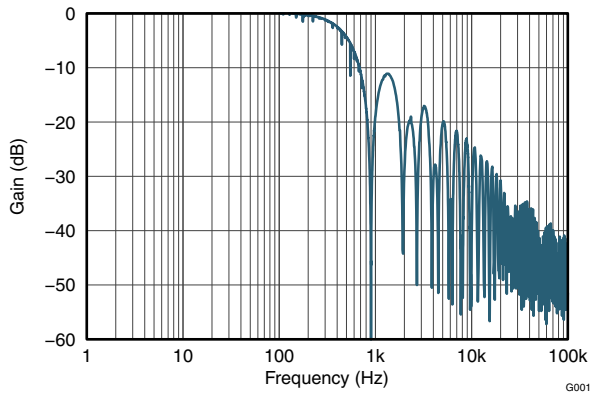

図 5-2. Frequency Response

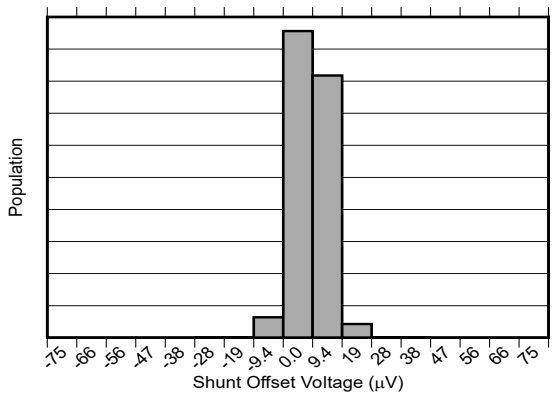

図 5-3. Shunt Input Offset Voltage Production Distribution

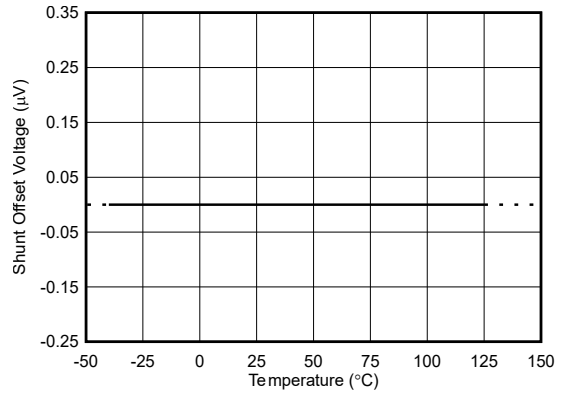

図 5-4. Shunt Input Offset Voltage vs. Temperature

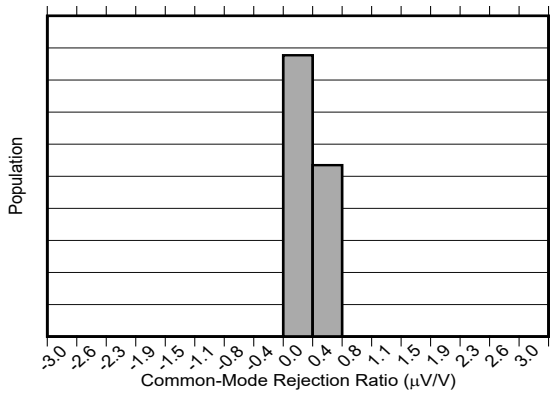

図 5-5. CMRR Production Distribution

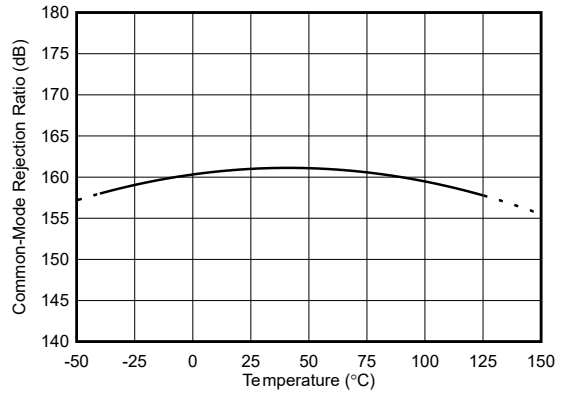

図 5-6. Shunt Input CMRR vs. Temperature

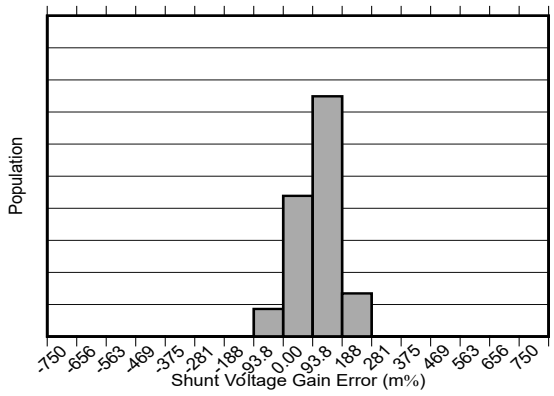

図 5-7. Shunt Voltage Gain Error Production Distribution

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV (unless otherwise noted)

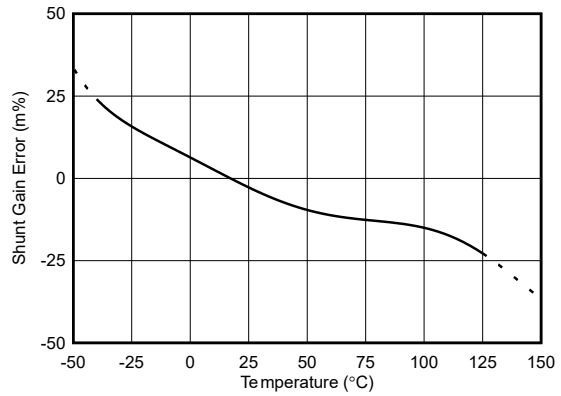

図 5-8. Shunt Gain Error vs. Temperature

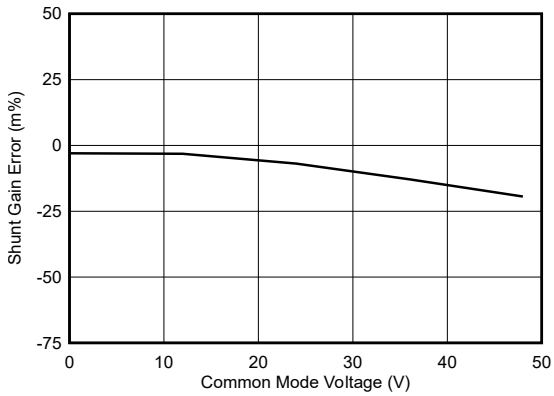

図 5-9. Shunt Gain Error vs. Common-Mode Voltage

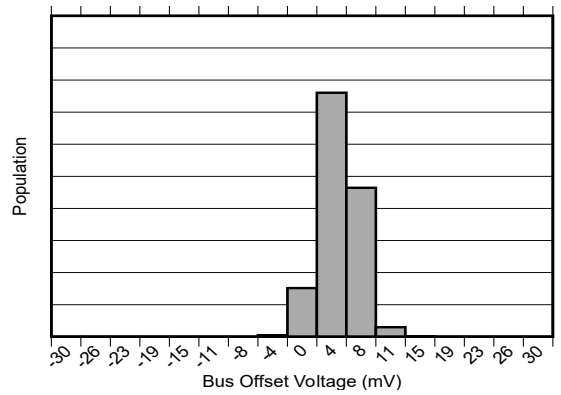

図 5-10. Bus Offset Voltage (V_{IN-}) Production Distribution

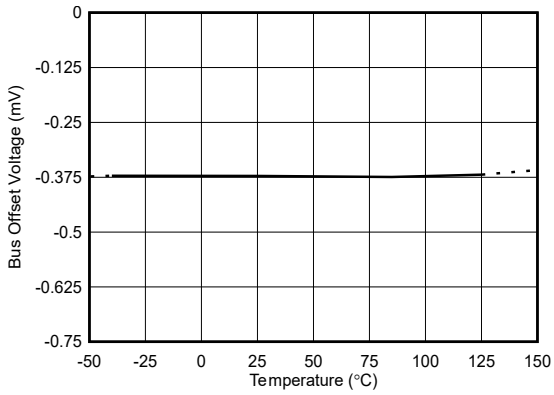

図 5-11. Bus Offset Voltage (V_{IN-}) vs. Temperature

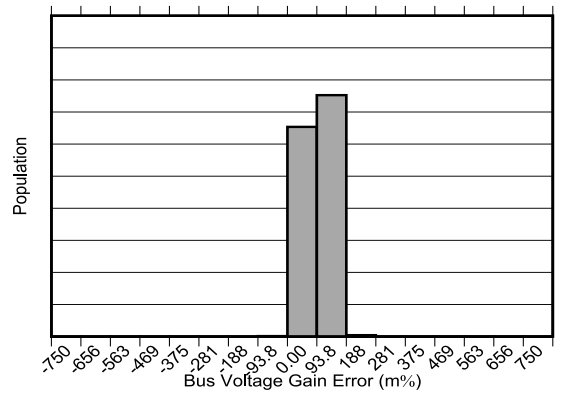

図 5-12. Bus Voltage (V_{IN-}) Gain Error Production Distribution

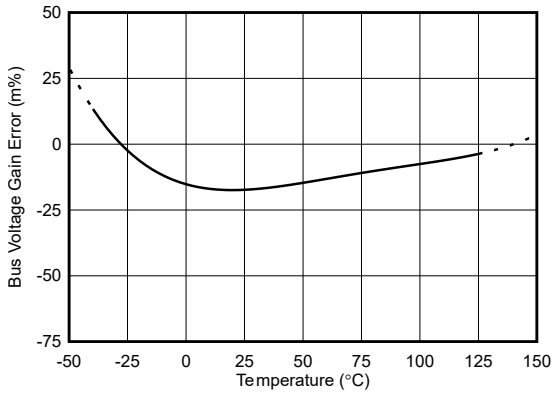

図 5-13. Bus Voltage (V_{IN-}) Gain Error vs. Temperature

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV (unless otherwise noted)

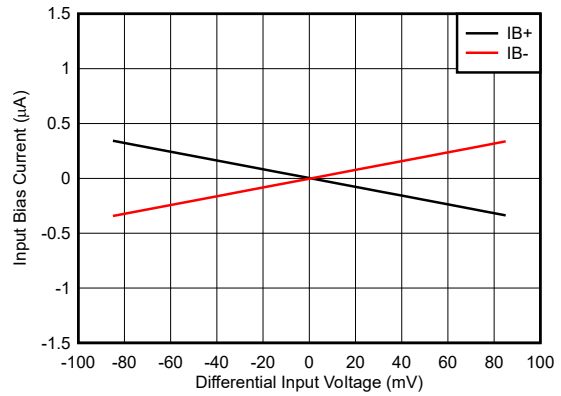

図 5-14. Input Bias Current vs. Differential Voltage

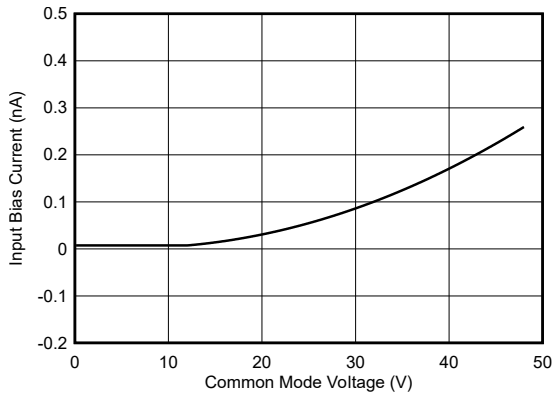

図 5-15. Input Bias Current vs. Common-Mode Voltage (IB+, IB-)

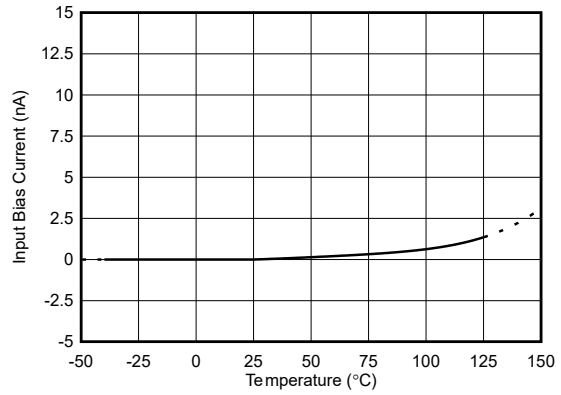

図 5-16. Input Bias Current vs. Temperature

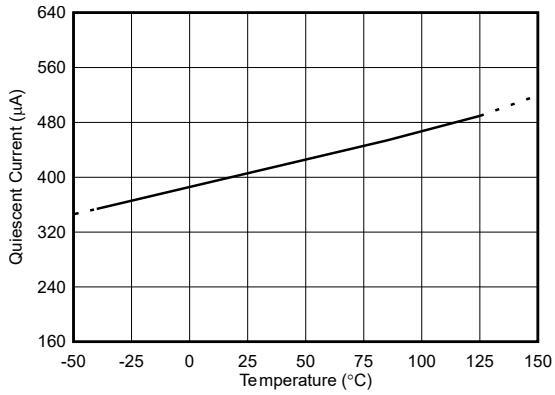

図 5-17. Quiescent Current vs. Temperature

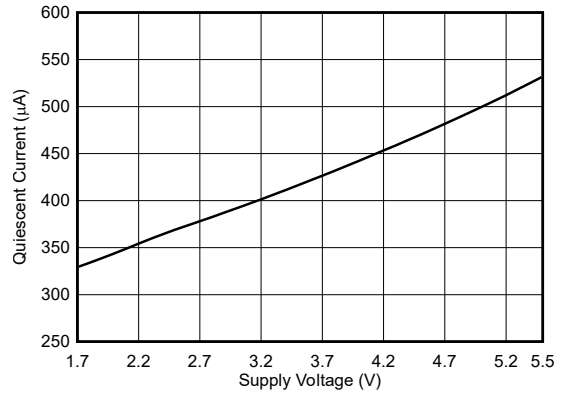

図 5-18. Quiescent Current vs. Supply Voltage

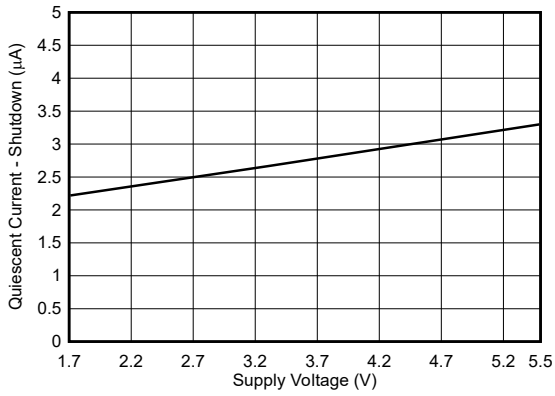

図 5-19. Quiescent Current - Shutdown vs. Supply Voltage

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3V, V_{CM} = 12V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV (unless otherwise noted)

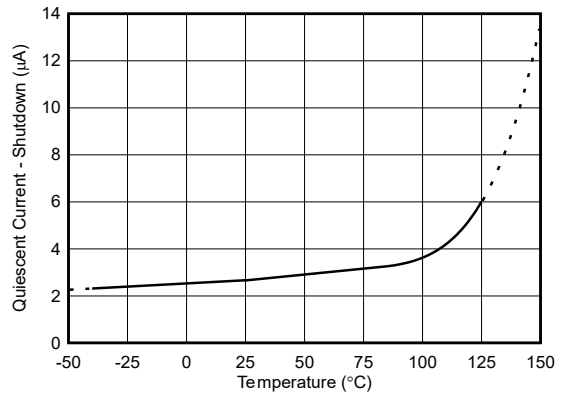

図 5-20. Quiescent Current - Shutdown vs. Temperature

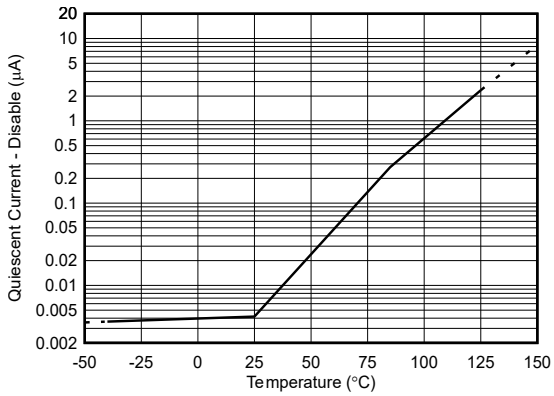

図 5-21. Quiescent Current - Disabled vs. Temperature

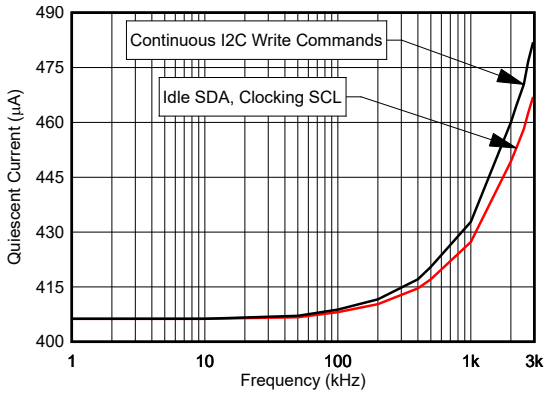

図 5-22. Quiescent Current vs. Clock(SCL) Frequency

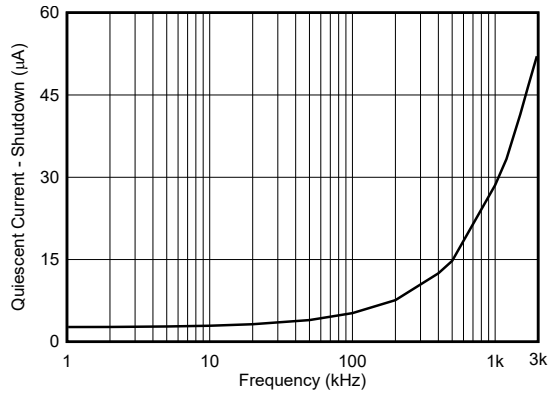

図 5-23. Quiescent Current - Shutdown vs. SCL Frequency

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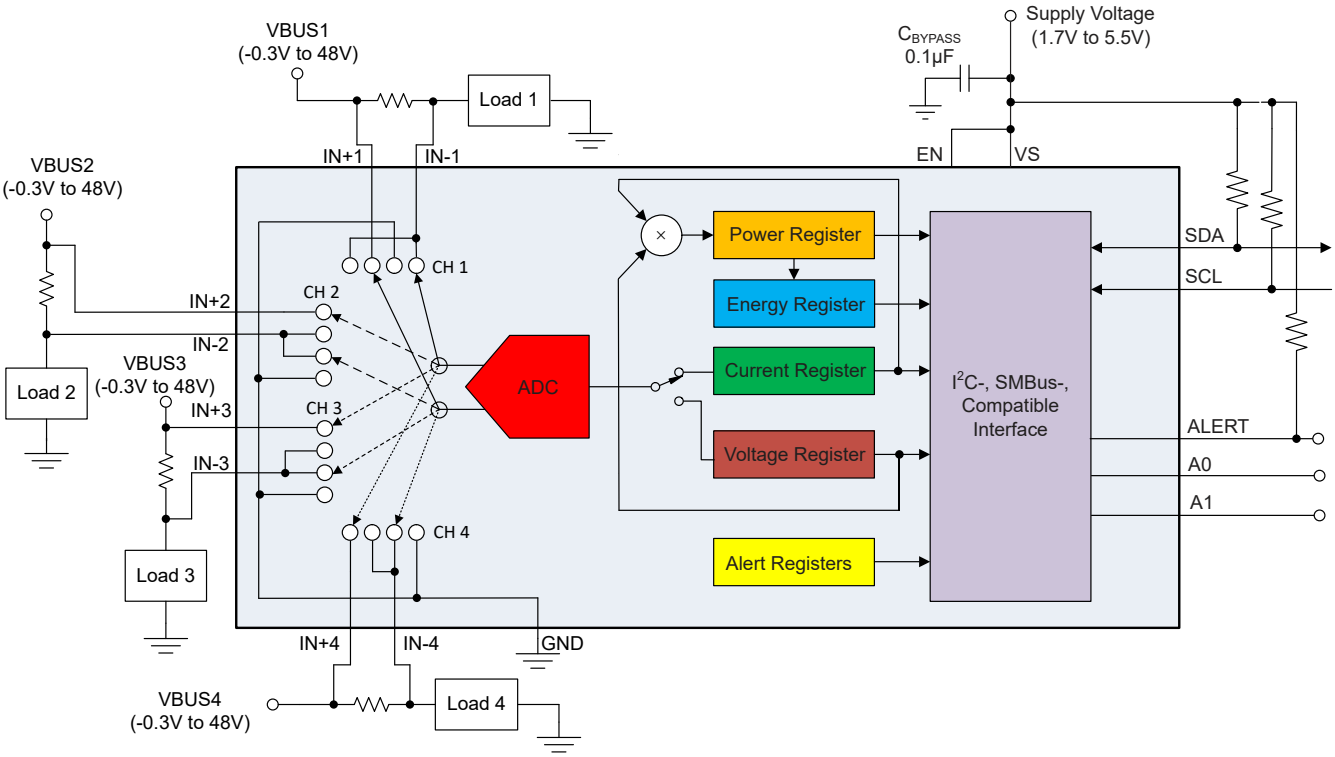
6 Detailed Description

6.1 Overview

The INA4230 is a multichannel digital current-sense amplifier with an I²C- and SMBus-compatible interface. The device reports current, voltage, power, and energy for each of the channels and features programmable out-of-range limits to issue alerts when selected parameters are outside the normal range of operation. The integrated analog-to-digital converter (ADC) can be set to different averaging modes and configured for continuous-versus-triggered operation. *Device Registers* provides detailed register information for the INA4230.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Integrated Analog-to-Digital Converter (ADC)

The INA4230 integrates a low offset 16-bit delta-sigma (ΔΣ) ADC. This ADC is multiplexed for each channel to process both the shunt voltage and bus voltage measurements. Bus voltage measurements are made with respect to IN- and GND. The shunt voltage measurement is a differential measurement of the voltage developed when the load current flows through a shunt resistor between the IN+ and IN– pins for each channel. The shunt voltage measurement has a maximum offset voltage of only 75µV and a maximum gain error of 0.75%. The low offset voltage of the shunt voltage measurement allows for increased accuracy at light load conditions for a given shunt resistor value. Another advantage of low offset is the ability to sense a lower voltage drop across the sense resistor accurately, thus allowing for a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current-sense circuit and help improve the power efficiency of the end application.

There are no special considerations for power-supply sequencing because the bus common-mode at the IN+ and IN- pins and power-supply voltage at the VS pin are independent of each other; therefore, the bus common-mode voltage can be present with the supply voltage off, and so forth.

6.3.2 Internal Measurement and Calculation Engine

The internal round robin measurement scheme for the INA4230 is shown in 図 6-1. For each channel the current, power, and energy registers are calculated from the shunt and bus voltage measurements and are not

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directly affected by ADC conversion times. Register values are updated for each channel before preceding to the next channel. When averaging is enabled, the registers for each channel updates once the number of averages is complete. Fault conditions are compared immediately after conversions or calculations based on the ADC conversion time and are independent of the number of averages set. Reducing the conversion times result in faster alert responses but at lower effective resolutions due to noise. Longer conversion times slow the alert response but are less sensitive to noise. Channels or measurements that are disabled are skipped in the round robin cycle. The conversion ready flag is set at the end of conversions after the selected number of averages are met.

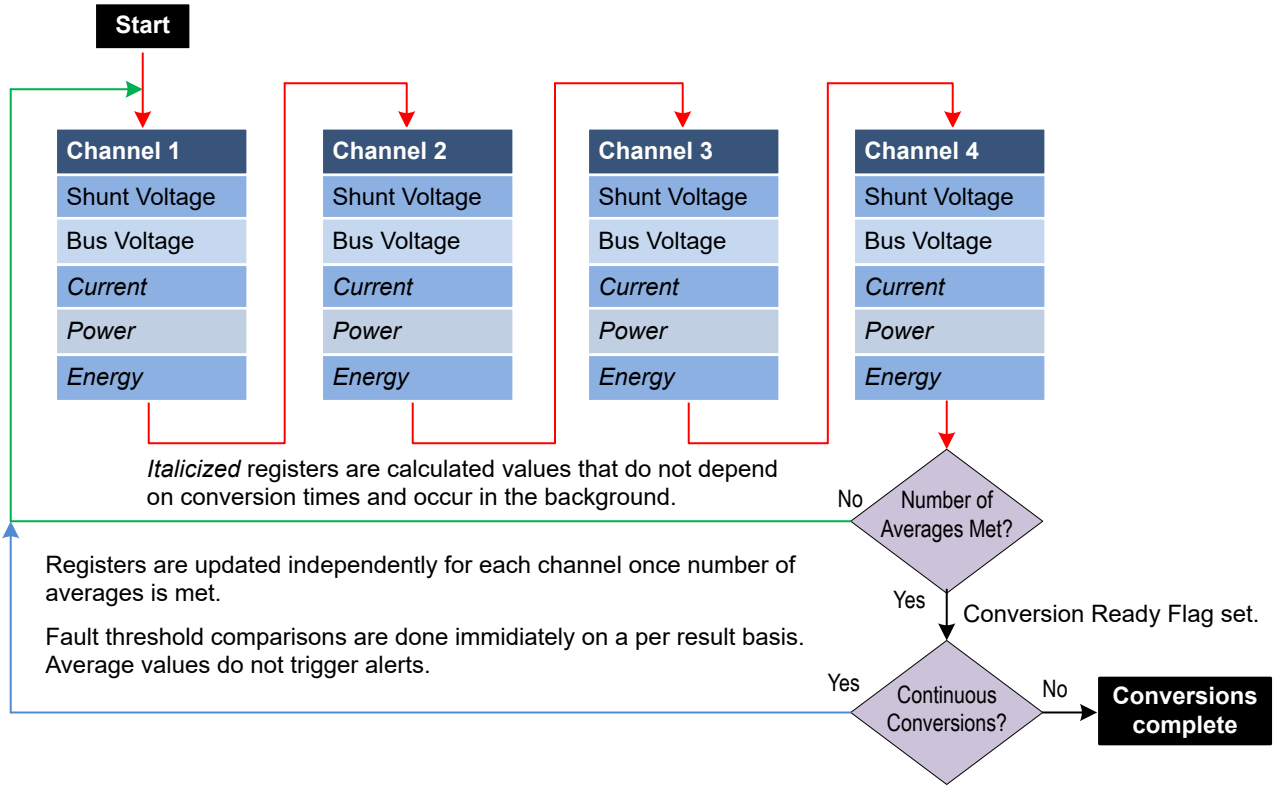

図 6-1. Internal Measurement and Calculation Scheme

Current is calculated from the shunt voltage measurements and the value entered in the corresponding calibration register. Power is calculated based on the previous current calculation and the latest bus voltage measurement. Energy is accumulated by adding the previous power calculation multiplied by the current timebase interval. If the value loaded into the corresponding calibration register is zero, current, power, and energy values are reported as zero also. When the averaging is enabled, register values are updated once the number of averages are met. These calculations are performed in the background and do not add to the overall conversion time.

6.3.3 Low Bias Current

When performing a current measurement, the INA4230 features very low input bias current which provides several benefits. The low input bias current of the INA4230 reduces the current consumed by the device in both active and shutdown state. Another benefit of low bias current is that low bias current allows the use of input filters to reject high-frequency noise before the signal is converted to digital data. In traditional digital current-sense monitors, the addition of input filters comes at the cost of reduced accuracy. However, as a result of the low bias current, the reduction in accuracy due to input filters is minimized. An additional benefit of low bias current is the ability to use a larger shunt resistor to accurately sense smaller currents. Use of a larger value for the shunt resistor allows the device to accurately monitor currents in the sub-mA range.

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The bias current in the INA4230 is the smallest when the sensed current is zero. As the current starts to increase, the differential voltage drop across the shunt resistor increases which results in an increase in the bias current (see 図 5-14).

The INA4230 has low bias current only when making a current measurement. When bus voltage measurements are made, the impedance of the IN- pins decrease. During bus voltage measurements the IN- pins are connected to an internal resistor divider with an impedance of approximately 1MΩ. Configuring the internal multiplexer to perform only current measurements allows the device to always have low bias current.

6.3.4 Low Voltage Supply and Wide Common-Mode Voltage Range

The supply voltage range of the INA4230 is 1.7V to 5.5V. The ability to operate at 1.7V enables the device to be used in 1.8V supply rails. Even with a supply voltage of 1.7V, the device can monitor currents on voltage rails as high as 48V. This wide common-mode range of operation allows the device to be used in many applications where the common-mode voltage exceeds the supply voltage rail.

6.3.5 ALERT Pin

The INA4230 has four Alert Configuration Registers that can be assigned to the four channels as needed. Each alert register has a channel assignment field as well as an alert mask field. The alert mask field allows the selection from one of the five available functions for the alert response. Based on the function being monitored, a value can then be entered into the Alert Limit Registers to set the corresponding threshold value that asserts the ALERT pin.

The ALERT pin allows for one of several available alert functions to be monitored to determine if a user-defined threshold has been exceeded. The five alert functions that can be monitored are:

- Shunt voltage overlimit (SOL)
- Shunt voltage underlimit (SUL)
- Bus voltage overlimit (BOL)
- Bus voltage underlimit (BUL)
- Power overlimit (POL)

The ALERT pin is an open-drain output. This pin is asserted when the alert function selected in the Alert Configuration registers exceeds the value programmed into the Alert Limit register. Up to four alert functions can be enabled and monitored at a time.

The conversion-ready state of the device can also be monitored at the ALERT pin to inform the user when the device has completed the previous conversion and is ready to begin a new conversion. The conversion ready flag (CVRF) bit can be monitored at the ALERT pin along with one of the alert functions.

If the alert function is not used, the ALERT pin can be left floating without impacting the operation of the device.

The alert function compares the programmed alert limit value to the result of each corresponding conversion. Therefore, an alert can be issued during a conversion cycle where the averaged value of the signal does not exceed the alert limit. Triggering an alert based on this intermediate conversion allows for out-of-range events to be detected faster than the averaged output data registers are updated. This fast detection can be used to create alert limits for quickly changing conditions through the use of the alert function, as well as to create limits to longer-duration conditions through software monitoring of the averaged output values.

6.4 Device Functional Modes

6.4.1 Continuous Versus Triggered Operation

The INA4230 has two operating modes, continuous and triggered, that determine how the ADC operates after these conversions. When the INA4230 is in the normal operating mode (that is, the MODE bits of the CONFIG1 register are set to '111'), the device continuously converts a shunt voltage reading followed by a bus voltage reading for each channel.

In triggered mode, writing any of the triggered convert modes into the セクション 7.1.1 (that is, the MODE bits of the CONFIG1 register are set to 001, 010, or 011) triggers a single-shot conversion of the selected parameters.

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This action produces a single set of measurements. To trigger another single-shot conversion, the Configuration register must be written to again, even if the mode does not change.

Although the INA4230 can be read at any time, and the data from the last conversion remain available, the conversion ready flag bit (CVRF bit, FLAGS register) is provided to help coordinate single-shot or triggered conversions. The CVRF bit is set after all conversions, averaging, and multiplication operations are complete for a single round robin cycle.

The CVRF bit clears under these conditions:

1. Writing to the CONFIG1 register, except when configuring the MODE bits for power-down mode; or
2. Reading the FLAGS register.

6.4.2 Device Low Power Modes

In addition to the two operating modes (continuous and triggered), the INA4230 also has two low power modes. In shutdown the device reduces the quiescent current and input bias current but is able to process I^2C bus communications. In this state the quiescent current is reduced to less than 4µA. Full recovery from shut-down mode requires 40µs. The device remains in shut-down mode until one of the active modes settings are written into the Configuration register. An even lower power mode is the disabled mode, which is initiated by forcing a logic low on the enable pin. In this mode the quiescent current is the lowest, with the device only drawing 1µA (max) of supply current, but the device does not recognize any I2C bus communications in this state. Also the device configuration gets reset when in the disabled state and needs to be reprogrammed when enabled. Recovery from the disabled state requires 100µs.

6.4.3 Power-On Reset

Power-on reset (POR) is asserted when V_S drops below 0.95V (typical) at which point all of the registers are reset to the default values. The default power-up register values are shown in the reset column for each register description.

6.4.4 Averaging and Conversion Time Considerations

The INA4230 has programmable conversion times for both the shunt voltage and bus voltage measurements that are applied across all channels. The conversion times for these measurements can be selected from as fast as 140µs to as long as 8.244ms. The conversion time settings, along with the programmable averaging mode, allow the INA4230 to be configured to optimize the available timing requirements in a given application. The INA4230 can also be configured with a different conversion time setting for the shunt and bus voltage measurements. This type of approach is common in applications where the bus voltage tends to be relatively stable. This situation allows for the time spent measuring the bus voltage to be reduced relative to the shunt voltage measurement.

There are trade-offs associated with the conversion time settings and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal. This approach allows the INA4230 to reduce noise in the measurement that can be caused by noise coupling into the signal. A greater number of averages enables the INA4230 to be more effective in reducing the noise component of the measurement.

The conversion times selected can also have an effect on the measurement accuracy. 図 6-2 shows multiple conversion times to illustrate the effect of noise on the measurement. To achieve the highest accuracy measurement possible, use a combination of the longest allowable conversion times and highest number of averages, based on the timing requirements of the system.

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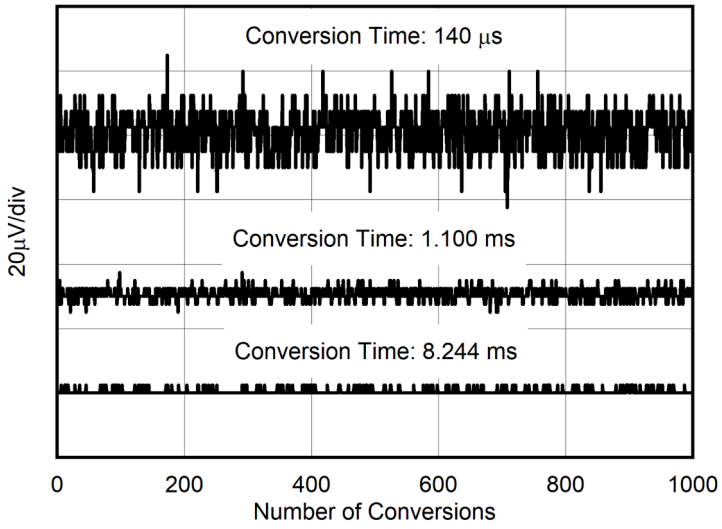

図 6-2. Noise vs. Conversion Time

6.5 Programming

6.5.1 I²C Serial Interface

The INA4230 operates only as a target on both the SMBus and I²C interfaces. Connections to the bus are made through the open-drain SDA and SCL lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device integrates spike suppression into the digital I/O lines, proper layout techniques help minimize the amount of coupling into the communication lines. This noise introduction can occur from capacitive coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a printed circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielded communication lines reduce the possibility of unintended noise coupling into the digital I/O lines that can be incorrectly interpreted as start or stop commands.

The INA4230 supports the transmission protocol for fast mode (1kHz to 400kHz) and high-speed mode (1kHz to 2.94MHz). All data bytes are transmitted most significant byte first and follow the SMBus 3.0 transfer protocol.

To communicate with the INA4230, the controller must first address targets through a target address byte. The target address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device has two address pins, A0 and A1. 表 6-1 lists the pin connections required for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin state before any activity on the interface occurs.

表 6-1. Address Pins and Target Addresses

A1	A0	TARGET DEVICE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111

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表 6-1. Address Pins and Target Addresses (続き)

A1	A0	TARGET DEVICE ADDRESS
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

6.5.2 Writing to and Reading Through the I²C Serial Interface

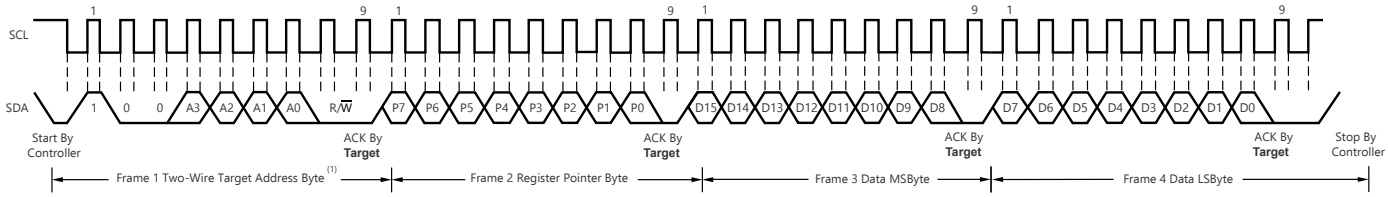
Accessing a specific register on the INA4230 is accomplished by writing the appropriate value to the register pointer. Refer to *Register Maps* for a complete list of registers and corresponding addresses. The value for the register pointer (see 図 6-5) is the first byte transferred after the target address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the controller. This byte is the target address, with the R/$\overline{W}$ bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the controller is the address of the register to be accessed. This register address value updates the register pointer to the desired internal device register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The controller can terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a target address byte with the R/$\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The controller then generates a start condition and sends the address byte for the target with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the target and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the controller; then the target transmits the least significant byte. The controller can or can not acknowledge receipt of the second data byte. The controller can terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, continually sending the register pointer bytes is not necessary. The device retains the register pointer value until the value is changed by the next write operation.

図 6-3 shows the write operation timing diagram. 図 6-4 shows the read operation timing diagram. These diagrams are shown for reading/writing to 16 bit registers.

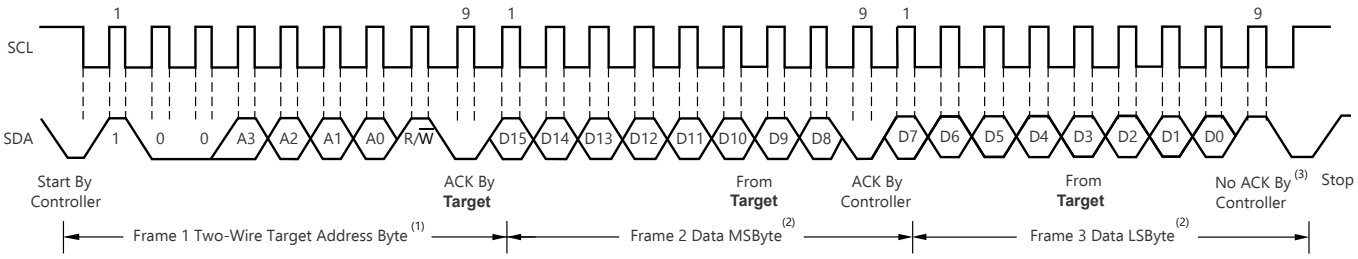
Register bytes are sent most-significant byte first, followed by the least significant byte.



A. The value of the Target Address byte is determined by the setting of the A0 address pin. Refer to 表 6-1.

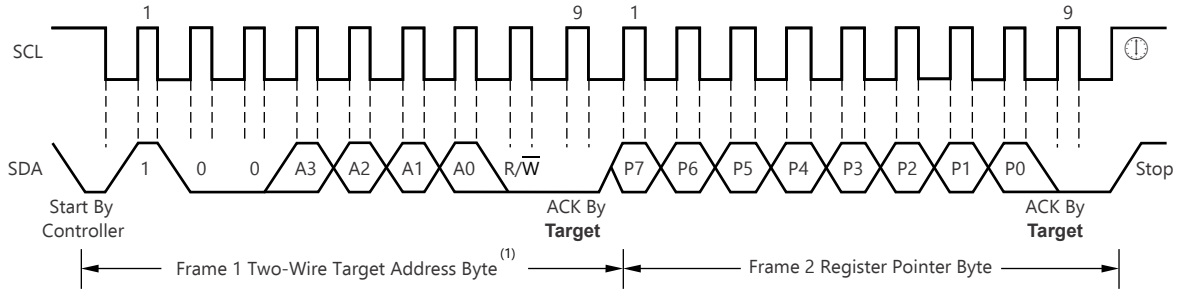
B. The device does not support packet error checking (PEC) or perform clock stretching.

図 6-3. Timing Diagram for Write Word Format



A. The value of the Target Address byte is determined by the setting of the A0 address pin. Refer to 表 6-1.
B. Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See 図 6-5.
C. ACK by the controller can also be sent.
D. The device does not support packet error checking (PEC) or perform clock stretching.

図 6-4. Timing Diagram for Read Word Format



A. The value of the Target Address byte is determined by the setting of the A0 address pin. Refer to 表 6-1.

図 6-5. Typical Register Pointer Set

6.5.3 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors. The controller generates a start condition followed by a valid serial byte containing high-speed (HS) controller code *00001XXX*. This transmission is made in fast (400kHz) or standard (100kHz) (F/S) mode at no more than 400kHz. The device does not acknowledge the HS controller code, but does recognize the code and switches the internal filters to support 2.94MHz operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94MHz are allowed. Instead of using a stop condition, use repeated start conditions to maintain the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

6.5.4 General Call Reset

A general call reset to multiple devices is implemented by addressing the general call address 0000 000, with the last R/$\overline{W}$ bit set to 0. This is then followed by the following data byte 0000 0110 (06h).

On receiving this 2-byte sequence, all devices designed to respond to the general call address are reset. All INA4230 devices on the bus perform a soft reset operation and return to the default power-up conditions

6.5.5 SMBus Alert Response

The INA4230 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple targets. When an Alert occurs, the controller can broadcast the Alert Response target address (0001 100) with the Read/Write bit set high. Following this Alert Response, any target that generates an alert is identified by acknowledging the Alert Response and sending the address on the bus.

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The Alert Response can activate several different target devices simultaneously, similar to the I²C General Call. If more than one target attempts to respond, bus arbitration rules apply. The device that is not prioritized during arbitration does not generate an acknowledge. The device continues to hold the Alert line lows until the device is prioritized as a result of the arbitration.

7 Register Maps

7.1 Device Registers

表 7-1 lists the INA4230 registers. All register locations not listed in the table are considered as reserved locations and the register contents must not be modified.

表 7-1. INA4230 Register Overview

Register Name	Address	Register Type	Register Size (bits)	Default Value
CONFIG1	0x20	R/W	16	0xF127
CONFIG2	0x21	R/W	16	0x0000
CALIBRATION_(CH1 - CH4)	0x05,0x0D, 0x15. 0x1D	R/W	16	0x0000
ALERT_CONFIG(1 - 4)	0x07, 0x0F, 0x17, 0x1F	R/W	16	0x0000
ALERT_LIMIT(1 - 4)	0x06, 0x0E, 0x16, 0x1E	R/W	16	0x0000
SHUNT_VOLTAGE_(CH1 - CH4)	0x00, 0x08, 0x10, 0x18	R	16	0x0000
BUS_VOLTAGE_(CH1 - CH4)	0x01, 0x09, 0x11,0x19	R	16	0x0000
CURRENT_(CH1 - CH4)	0x02, 0x0A, 0x12, 0x1A	R	16	0x0000
POWER_(CH1 - Ch4)	0x03, 0x0B, 0x13, 0x1B	R	16	0x0000
ENERGY_(CH1 - CH4)	0x04, 0x0C, 0x14, 0x1C	R	32	0x0000
FLAGS	0x22	R	16	0x0000
MANUFACTURER_ID	0x7E	R	16	0x5449 ("TI" in ASCII)

Complex bit access types are encoded to fit into small table cells. 表 7-2 shows the codes that are used for access types in this section.

表 7-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

7.1.1 CONFIG1 Register (Address = 0x20h) [reset = F127h]

The configuration register is shown in 表 7-3.

表 7-3. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	ACTIVE_CHANNEL	R/W	1111b	These 4 bits determine which channels are active. Set this bit to '1' to enable each channel. Disabled channels are skipped in the round robin cycle. Bit15 = Channel 4 measurement enable/disable. Bit14 = Channel 3 measurement enable/disable. Bit13 = Channel 2 measurement enable/disable. Bit12 = Channel 1 measurement enable/disable. Power up default: **1111b = All channels active**

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表 7-3. CONFIG1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
11-9	AVG	R/W	000b	Sets the number of ADC conversion results to be averaged. The read-back registers are updated after averaging is completed. **000b = 1** 001b = 4 010b = 16 011b = 64 100b = 128 101b = 256 110b = 512 111b = 1024
8-6	VBUSCT	R/W	100b	Sets the conversion time of the VBUS measurement 000b = 140µs 001b = 204µs 010b = 332µs 011b = 588µs **100b = 1100µs** 101b = 2116µs 110b = 4156µs 111b = 8244µs
5-3	VSHCT	R/W	100b	Sets the conversion time of the SHUNT measurement 000b = 140µs 001b = 204µs 010b = 332µs 011b = 588µs **100b = 1100µs** 101b = 2116µs 110b = 4156µs 111b = 8244µs
2-0	MODE	R/W	111b	Operating mode, modes can be selected to operate the device either in Shutdown mode, continuous mode or triggered mode. The mode also allows user to select mux settings to set continuous or triggered mode on bus voltage, shunt voltage measurement. 000b = Shutdown 001b = Shunt voltage triggered, single shot 010b = Bus voltage triggered, single shot 011b = Shunt voltage and Bus voltage triggered, single shot 100b = Shutdown 101b = Continuous shunt voltage 110b = Continuous bus voltage **111b = Continuous shunt and bus voltage**

Return to the Summary Table.

7.1.2 CONFIG2 Register

The configuration register is shown in 表 7-4.

表 7-4. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0b	Set this bit to '1' to generate a system reset that is the same as power-on reset. Resets all registers to default values and then self-clears.

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表 7-4. CONFIG2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
14-12	Reserved	R	000b	These bits always read 0.
11-8	ACC_RST	R/W	0000b	Writing a one to these bits resets the energy registers and clears any overflow flags. Bit11 = Channel 4 energy reset, overflow clear. Bit10 = Channel 3 energy reset, overflow clear. Bit9 = Channel 2 energy reset, overflow clear. Bit8 = Channel 1 energy reset, overflow clear. Power up default: **0000b = All channels active** Bits are reset back to 0 after write.
7	CNVR_MASK	R/W	0b	Setting this bit high configures the ALERT pin to be asserted when conversions are complete. 0b = Disable conversion ready flag on ALERT pin 1b = Enables conversion ready flag on ALERT pin ALERT remains asserted until the CVRF field in the flags register is read.
6	ENOF_MASK	R/W	0b	When set to 1, the Alert pin toggles when an energy overflow condition occurs on any of the enabled channels
5	ALERT_LATCH	R/W	0b	When set to 1 the state of the Alert pin latches during fault conditions. To clear the alert the alert flags register must be read and the fault condition removed.
4	ALERT_POL	R/W	0b	When this bit is set to 1, the alert pin toggles from low to high during a fault condition. When set to 0 (default), the alert pin toggles from high to low during faults.
3-0	RANGE	R/W	0000b	Enables the selection of the shunt full scale input range for each channel. Bit3 = Channel 4 range selection. Bit2 = Channel 3 range selection. Bit1 = Channel 2 range selection. Bit0 = Channel 1 range selection. range selection bit = 0 selects ±81.92mV range selection bit = 1 selects ±20.48mV **0000b = all channels set to ±81.92mV range**

Return to the Summary Table.

7.1.3 CALIBRATION Registers

The calibration registers shown in 表 7-5 must be programmed to receive valid current, power, and energy results after initial power up, power cycle events, or on device enable.

表 7-5. INA4230 Calibration Registers

Address	Register Name	Register Type	Register Size (bits)
0x05	CALIBRATION_CH1	R/W	16
0x0D	CALIBRATION_CH2	R/W	16
0x15	CALIBRATION_CH3	R/W	16
0x1D	CALIBRATION_CH4	R/W	16

This register provides the device with the value of the shunt resistor that are present to create the measured differential voltage. This register also sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB.

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表 7-6. Calibration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	
14-0	SHUNT_CAL	R/W	0000h	Programmed value needed for doing the shunt voltage to current conversion.

Return to the Summary Table.

7.1.4 Alert Configuration Registers

The alert configuration registers are shown in 表 7-7.

表 7-7. INA4230 ALERT_CONFIG Registers

Address	Register Name	Register Type	Register Size (bits)
0x07	ALERT1	R/W	16
0x0F	ALERT2	R/W	16
0x17	ALERT3	R/W	16
0x1F	ALERT4	R/W	16

The format of each alert configuration register is shown in 表 7-8.

These registers configure what triggers an alert for each of the channels. The alert mask field sets the active alert. Up to 4 alerts can be assigned to a given channel or spread equally across all channels depending on the needs of the application.

表 7-8. Alert Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	Reserved	R	000000000000b	Reserved
4-3	CHANNEL	R/W	00b	Selects 00b = Channel 1 01b = Channel 2 10b = Channel 3 11b = Channel 4
2-0	ALERT_MASK	R/W	000b	Sets the active alert for the assigned channel 000b = reserved, no effect 001b = Shunt Voltage over limit (SOL) 010b = Shunt Voltage under limit (SUL) 011b = Bus Voltage over limit (BOL) 100b = Bus Voltage under limit (BUL) 101b = Power over limit (POL) 110b = reserved, no effect 111b = reserved, no effect

The alert configuration registers set what triggers an alert for each of the channels. The alert mask field sets the active alert. Up to 4 alerts can be assigned to a given channel or spread as required across all channels depending on the application.

Return to the Summary Table.

7.1.5 Alert Limit Registers

The alert limit registers shown in 表 7-9 must be programmed to set the desired fault limit threshold.

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表 7-9. INA4230 ALERT_LIMIT Registers

Address	Register Name	Register Type	Reset	Register Size (bits)
0x06	LIMIT1	R/W	0000h	16
0x0E	LIMIT2	R/W	0000h	16
0x16	LIMIT3	R/W	0000h	16
0x1E	LIMIT4	R/W	0000h	16

The format of the alert limit register follows the format of the corresponding result register.

Shunt voltage limits are represented as signed 16 bit, bus voltage limits are unsigned 15 bit, and power limits are unsigned 16 bit values.

Return to the Summary Table.

7.1.6 Shunt Voltage Registers

The Shunt Voltage Registers store the current shunt voltage reading, V_{SHUNT}. The shunt voltage measurement for each channel has a unique address as shown in 表 7-10.

表 7-10. INA4230 SHUNT_VOLTAGE Registers

Address	Register Name	Register Type	Register Size (bits)
0x00	SHUNT_VOLTAGE_CH1	R	16
0x08	SHUNT_VOLTAGE_CH2	R	16
0x10	SHUNT_VOLTAGE_CH3	R	16
0x18	SHUNT_VOLTAGE_CH4	R	16

The format of each shunt voltage register is shown in 表 7-11.

If averaging is enabled, these registers contain the averaged shunt voltage value.

表 7-11. Shunt Voltage Register Field Description

Bit	Field	Type	Reset	Description
15-0	VSHUNT	R	0000h	Differential voltage measured across the shunt output. 2's complement value.

Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. An MSB = '1' denotes a negative number.

Example: For a value of V_{SHUNT} = –80mV:

1. Take the absolute value: 80mV
2. Translate this number to a whole decimal number (80mV ÷ 2.5µV) = 32000
3. Convert this number to binary = 0111 1101 0000 0000
4. Complement the binary result = 1000 0010 1111 1111
5. Add '1' to the complement to create the two's complement result = 1000 0011 0000 0000 = 8300h

Return to the Summary Table.

7.1.7 Bus Voltage Registers

The bus voltage registers store the voltage measured at the bus pin for each of the channels. Bus voltage measurements are stored in an unique register addresses as shown in 表 7-12.

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表 7-12. INA4230 BUS_VOLTAGE Registers

Address	Register Name	Register Type	Register Size (bits)
0x01	BUS_VOLTAGE_CH1	R	16
0x09	BUS_VOLTAGE_CH2	R	16
0x11	BUS_VOLTAGE_CH3	R	16
0x19	BUS_VOLTAGE_CH4	R	16

The format of each bus voltage register is shown in 表 7-13.

The bus voltage registers only return positive values. If averaging is enabled, this register displays the averaged value.

表 7-13. BUS_VOLTAGE Register Field Description

Bit	Field	Type	Reset	Description
15-0	VBUS	R	0000h	Bus voltage output. 2's complement value, however always positive.

Return to the Summary Table.

7.1.8 CURRENT Registers

The current registers store the calculated current value for each of the channels. Current measurements are stored in an unique register addresses as shown in 表 7-14.

表 7-14. INA4230 CURRENT Registers

Address	Register Name	Register Type	Register Size (bits)
0x02	CURRENT_CH1	R	16
0x0A	CURRENT_CH2	R	16
0x12	CURRENT_CH3	R	16
0x1A	CURRENT_CH4	R	16

The format of each bus current register is shown in 表 7-15.

If averaging is enabled, this register displays the averaged value. The value of the Current Register is calculated by multiplying the decimal value in the Shunt Voltage Register with the decimal value of the Calibration Register.

表 7-15. CURRENT Register Field Description

Bit	Field	Type	Reset	Description
15-0	CURRENT	R	0000h	Calculated current output in Amperes. 2's complement value.

Return to the Summary Table.

7.1.9 POWER Registers

The power registers store the multiplied value of the bus voltage and current for each of the channels. Power measurements are stored in an unique register addresses as shown in 表 7-16.

表 7-16. INA4230 POWER Registers

Address	Register Name	Register Type	Register Size (bits)
0x03	POWER_CH1	R	16
0x0B	POWER_CH2	R	16
0x13	POWER_CH3	R	16
0x1B	POWER_CH4	R	16

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The format of each bus power register is shown in 表 7-17.

If averaging is enabled, this register displays the averaged value. The Power Register records power in Watts by multiplying the decimal values of the Current Register with the decimal value of the Bus Voltage Register. This is an unsigned result.

表 7-17. POWER Register Field Description

Bit	Field	Type	Reset	Description
15-0	POWER	R	0000h	This bit returns a calculated value of power in the system. This is an unsigned result.

Return to the Summary Table.

7.1.10 Energy Registers

The energy registers accumulate data from the power registers and with the internal precision timebase calculate and store the energy for each of the channels. Energy measurements are stored in an unique register addresses as shown in 表 7-18.

表 7-18. INA4230 ENERGY Registers

Address	Register Name	Register Type	Register Size (bits)
0x04	ENERGY_CH1	R	32
0x0C	ENERGY_CH2	R	32
0x14	ENERGY_CH3	R	32
0x1C	ENERGY_CH4	R	32

The format of each bus power register is shown in 表 7-19.

The Energy register records energy in Joules and utilizes the precision oscillator as a timebase. This is an unsigned result.

表 7-19. Energy Register Field Description

Bit	Field	Type	Reset	Description
31-0	ENERGY	R	00000000h	This bit returns a calculated value of energy in the system. This is an unsigned result.

Return to the Summary Table.

7.1.11 Flags Register

The Flags Register is shown in 表 7-20.

表 7-20. Flags Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LIMIT4_ALERT	R	0b	Indicates the fourth alert limit has been exceeded. This alert is independent of channel.
14	LIMIT3_ALERT	R	0b	Indicates the third alert limit has been exceeded. This alert is independent of channel.
13	LIMIT2_ALERT	R	0b	Indicates the second alert limit has been exceeded. This alert is independent of channel.
12	LIMIT1_ALERT	R	0b	Indicates the first alert limit has been exceeded. This alert is independent of channel.
11	ENERGYOF_CH4	R	0b	Indicates an the energy register has overflowed for channel 4

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表 7-20. Flags Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
10	ENERGYOF_CH3	R	0b	Indicates an the energy register has overflowed for channel 3
9	ENERGYOF_CH2	R	0b	Indicates an the energy register has overflowed for channel 2
8	ENERGYOF_CH1	R	0b	Indicates an the energy register has overflowed for channel 1
7	CVRF (Conversion Ready Flag)	R	0b	Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 1.) Writing to the Configuration Register (except for Power-Down selection) 2.) Reading the Flags Register
6	OVF (Math Over-flow)	R	0b	This bit is set to '1' if an arithmetic operation results in an overflow error. This bit indicates that current and power data can be invalid.
5-0	Reserved	-	000000b	Reserved

Return to the Summary Table.

7.1.12 Manufacturer ID Register (Address = 7Eh)

The manufacturer ID register is shown in 表 7-21.

表 7-21. MANUFACTURE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MANUFACTURE_ID	R	5449h	Reads back TI in ASCII

Return to the Summary Table.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The INA4230 is a multi-channel current shunt monitor with an I^2C- and SMBus-compatible interface. The device monitors a shunt voltage drop to calculate the current and bus voltage at IN- pin to determine power and energy for up to four measurement channels. Programmable calibration value, conversion times, and averaging (combined with an internal multiplier) enable direct readouts of current in amperes, power in watts, and energy in joules.

8.1.1 Device Measurement Range and Resolution

The INA4230 device supports two input ranges for the shunt voltage measurements for each channel. The supported full scale differential input across the IN+ and IN– pins can be either ±81.92mV or ±20.48mV depending on the RANGE field in the CONFIG2 Register register. The range for the bus voltage measurement at the IN- pins is from 0V to 52.42V, but is limited by process ratings to the maximum operating voltage.

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表 8-1 provides a description of full scale voltage on shunt and bus voltage measurements, along with the associated resolution.

表 8-1. ADC Full Scale Values

PARAMETER	FULL SCALE VALUE	RESOLUTION
Shunt voltage	±81.92mV (ADCRANGE = 0)	2.5µV/LSB
	±20.48mV (ADCRANGE = 1)	625nV/LSB
Bus voltage	0V to 52.4V (Limit usable range to recommended operating voltage)	1.6mV/LSB

The device shunt voltage and bus voltage measurements are read through the Shunt Voltage registers and Bus Voltage registers, respectively. The digital output in shunt voltage and bus voltage registers is 16 bits. The shunt voltage measurement can be positive or negative due to bidirectional currents in the system; therefore the data value in shunt voltage register can be positive or negative. The bus voltage register data value is always positive. The output data can be directly converted into voltage by multiplying the digital value by the respective resolution size.

Furthermore, the device provides the flexibility to report calculated current in Amperes, power in Watts, as described in *Current and Power Calculations*.

8.1.2 Current and Power Calculations

For the INA4230 to report current values in Amperes, a constant conversion value must be written in each of the calibration registers that is dependent on the selected CURRENT_LSB and the shunt resistance used in the application for each channel. The value of the calibration register is calculated based on 式 1. The term CURRENT_LSB is the chosen LSB step size for the CURRENT register where the current is stored. 式 2 shows the minimum value of CURRENT_LSB is based on the maximum expected current, and the equation directly defines the maximum resolution of the CURRENT register. While the smallest CURRENT_LSB value yields highest resolution, this value is common for selecting a higher round-number (no higher than 8x) value for the CURRENT_LSB to simplify the conversion of the CURRENT.

The R_{SHUNT} term is the resistance value of the external shunt used to develop the differential voltage across the IN+ and IN– pins. Use 式 1 for ADCRANGE = 0. For ADCRANGE = 1, the value of SHUNT_CAL must be divided by 4.

$$\text{SHUNT\_CAL} = \frac{0.00512}{\text{Current\_LSB} \times R_{SHUNT}} \tag{1}$$

where

- 0.00512 is an internal fixed value used to verify that scaling is maintained properly.
- CURRENT_LSB is a selected value for the current step size in amperes. Must be greater than or equal to CURRENT_LSB (minimum), but less than 8 x CURRENT_LSB(minimum) to reduce resolution loss.
- The value of SHUNT_CAL must be divided by 4 for ADCRANGE = 1.

$$\text{CURRENT\_LSB (minimum)} = \frac{\text{Maximum Expected Current}}{2^{15}} \tag{2}$$

Note that the current is calculated following a shunt voltage measurement based on the value set in the SHUNT_CAL field. If the value loaded into the SHUNT_CAL field is zero, the current value reported through the CURRENT register is also zero.

After programming the SHUNT_CAL field with the calculated value, the measured current in Amperes can be read from the CURRENT register. Use 式 3 to calculate the final value scaled by the CURRENT_LSB:

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$$\text{Current [A]} = \text{CURRENT\_LSB} \times \text{CURRENT} \quad (3)$$

where

- CURRENT is the value read from the CURRENT register

The power value can be read from the POWER register as an unsigned 16-bit value. Use 式 4 to convert the power to Watts:

$$\text{Power [W]} = 32 \times \text{CURRENT\_LSB} \times \text{POWER} \quad (4)$$

where

- POWER is the value read from the POWER register.
- CURRENT_LSB is chosen lsb size for the selected channel.

The energy values can be read from the each ENERGY register as a 32-bit unsigned value. Use 式 5 to convert the energy to Joules:

$$\text{Energy [J]} = 32 \times \text{CURRENT\_LSB} \times \text{ENERGY} \quad (5)$$

where

- ENERGY is the value read from the each ENERGY register.
- CURRENT_LSB is chosen lsb size for the selected channel.

8.2 Typical Application

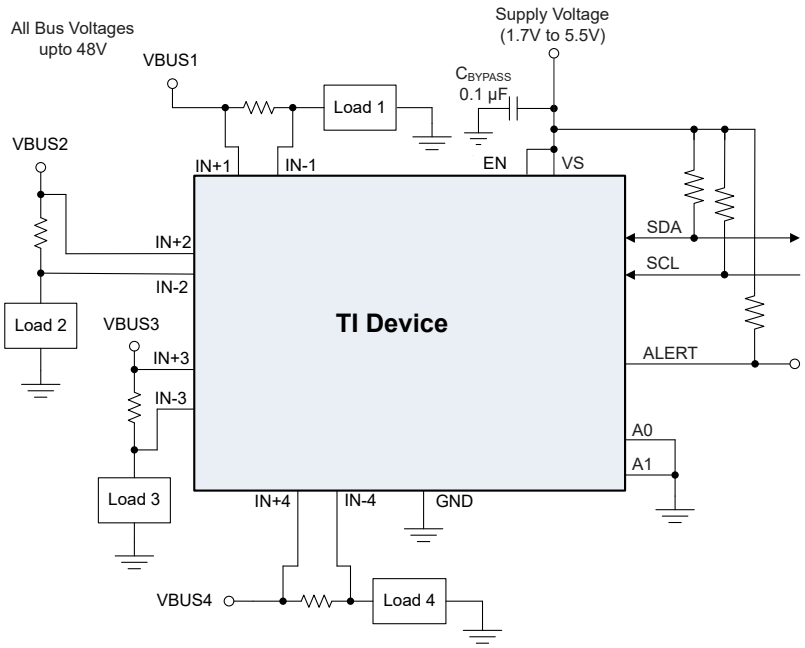

図 8-1. Typical High-Side Sensing Circuit Configuration, INA4230

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8.2.1 Design Requirements

The INA4230 features 4 channels that measure the voltage developed across a current-sensing resistor (R_{SHUNT}) when current passes through the resistor. The device also measures the bus supply voltage and calculates power and energy for each channel. The device also comes with alert capability, where the alert pin can be programmed to respond to a user-defined event or a conversion ready notification.

表 8-2 lists the design requirements for a single channel of the circuit shown in 図 8-1.

表 8-2. Design Parameters for Channel 1

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	3.3V
Bus supply rail (V_{CM})	12V
Average Current	6A
Overcurrent fault threshold	9A
Maximum current monitored (I_{MAX})	10A
ADC Range Selection (V_{SENSE_MAX})	±81.92mV
Energy Accumulation Period	1 hour

8.2.2 Detailed Design Procedure

This design example walks through the process of selecting the shunt resistor, programming the calibration register, setting the correct fault thresholds, and how to properly scale returned values from the device for channel 1 of the device. The configuration of additional channels is similar with calculated values programmed into the registers corresponding to the appropriate channel.

8.2.2.1 Select the Shunt Resistor

Using values from 表 8-2, the maximum value of the shunt resistor is calculated based on the value of the maximum current to be sensed (I_{MAX}) and the maximum allowable sense voltage (V_{SENSE_MAX}) for the chosen ADC range. When operating at the maximum current, the differential input voltage must not exceed the maximum full scale range of the device, V_{SENSE_MAX}. Using 式 6 for the given design parameters, the maximum value for R_{SHUNT} is calculated to be 8.192mΩ. The closest standard resistor value that is smaller than the maximum calculated value is 8.0mΩ. Smaller resistors can be used to minimize power loss at the expense of reduced accuracy. The shunt resistor selected must have sufficient wattage to handle the power dissipation at maximum load at the desired operating temperature.

$$R_{SHUNT} < \frac{V_{SENSE\_MAX}}{I_{MAX}} \tag{6}$$

8.2.2.2 Configure the Device

The first step to program the INA4230 is to properly set the device configuration registers, CONFIG1 and CONFIG2. On initial power up, the configuration registers are set to the reset values (see 表 7-3 and 表 7-4). In the default power on state the device is set to measured on the ±81.92mV range with the ADC continuously converting the shunt and bus (voltage at IN–) voltages for all channels. If the default power up conditions do not meet the design requirements, these registers need to be set properly after each disable or V_S power cycle event.

8.2.2.3 Program the Shunt Calibration Registers

There are four shunt calibration registers for each channel that need to be correctly programmed after each power up for the device to properly report any result based on current. The first step to calculate the value for the calibration register is to calculate the minimum LSB value for the current by using 式 2. Applying this equation with the maximum expected current of 10A results in an minimum LSB size of 305.17578µA. The INA4230 allows selection of the CURRENT_LSB to be up to 8 times larger than the minimum LSB size. For this example a value of 500µA is used. Applying 式 1 to the Current_LSB and selected value for the shunt resistor results in a

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shunt calibration register setting of 1280d (500h). Failure to set the value of the shunt calibration registers results in a zero value for any result based on current for that channel. Programming these registers is not required for reading shunt voltage, bus voltage or setting corresponding alert limits.

8.2.2.4 Set Desired Fault Thresholds

The INA4230 has the ability to assert the alert pin on several different fault conditions as described in Alert Configuration Registers. The desired fault condition to assert the alert pin needs to be selected by appropriately programming the ALERT MASK field in the Alert Configuration Register. Fault thresholds are set by programming the desired trip threshold into the Alert Limit Registers.

For example, channel 1 can be configured to alert on an over current condition by setting the ALERT1 register CHANNEL field to channel 1(00b) with the ALERT MASK field set to shunt over voltage (001b). The desired threshold for the over current condition has to be programmed in the Limit1 Register. In this example, the over current threshold is 9.0A and the value of the current sense resistor is 8.0mΩ, which give a shunt voltage limit of 72mV. Once the shunt voltage limit is known, the value for the shunt over voltage limit register is calculated by dividing the shunt voltage limit by the shunt voltage LSB size.

For this case, the calculated value of the alert limit register is 72mV / 2.5µV = 28800d (7080h).

Values stored in the LIMIT1 to LIMIT4 registers are set to the default values when the device is disabled or V_S is power cycled.

Fault limits programmed into the LIMIT registers can be applied to a single channel or distributed to each of the 4 measurement channels. For example, if monitoring of the bus voltage was also required on channel 1, the CHANNEL field of the ALERT2 register can be also set to channel 1(00b) with the ALERT MASK field set to monitor over bus conditions (011b). The value for the over voltage fault can be set as desired in the LIMIT2 register.

8.2.2.5 Calculate Returned Values

Parametric values are calculated by multiplying the returned value by the LSB value. 表 8-3 shows the returned values for this application example, assuming the design requirements shown in 表 8-2.

表 8-3. Register Values

Register	Contents	LSB Value	Calculated Value
Shunt_Voltage_CH1 (00h)	19200d (4B00h)	2.5µV	19200 × 2.5µV = 0.048V
Bus_Voltage_CH1 (01h)	7500d (1D4Ch)	1.6mV	7500 × 1.6mV = 12V
Current_CH1 (02h)	12000d (2EE0h)	Current LSB = 500µA	12000 × 500µA = 6A
Power_CH1 (03h)	4500d (1194h)	Current LSB x 32 = 16mW	4500 × 16mW = 72W
Energy_CH1 (04h)	16200000d (00F7 3140h)	Current LSB x 32 = 16mJ	16200000 × 16mJ = 259.2kJ

Shunt Voltage and Current return values in two's complement format. In two's complement format a negative value in binary is represented by having a 1 in the most significant bit of the returned value. These values can be converted to decimal by first inverting all the bits and adding 1 to obtain the unsigned binary value. This value must then be converted to decimal with the negative sign applied.

8.2.3 Application Curves

図 8-2 and 図 8-3 show the ALERT pin response to a BUS over voltage fault with a conversion time of 140µs for the bus voltage measurements with averaging set to 1. For these scope shots, persistence was enabled on the ALERT channel to show the variation in the alert response for many sequential fault events. The alert response time can change depending on the value of the current before fault occurs as well as the how much the fault condition exceeds the programmed fault threshold. 図 8-2 shows the response time for an overcurrent fault when the fault condition greatly exceeds the programmed threshold. While 図 8-3 shows the over voltage response time when the fault slightly exceeds the programmed threshold. Variation in the alert response exists because

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the external fault event is not synchronized to the internal ADC conversion start. Also the ADC is constantly sampling to get a result, so the response time for fault events starting from zero are slower than fault events starting from values near the set fault threshold. In applications where the alert timing is critical, the worst-case alert response is equal to 2 × (t_{conv_shunt} + $t_{conv\_voltage}$) × number of channels enabled. When alerting on over power conditions, an additional 60µs needed to allow for background math calculations.

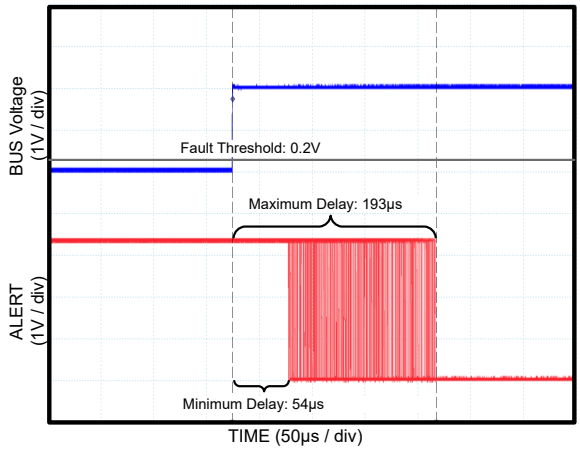

図 8-2. Alert Response Time (Sampled Values Significantly Above Threshold)

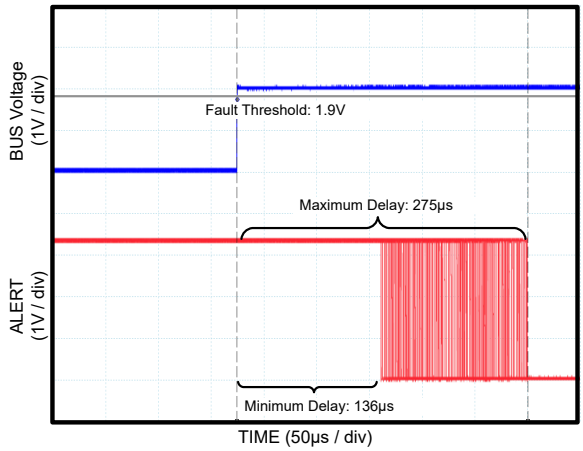

図 8-3. Alert Response Time (Sampled Values Slightly Above Threshold)

8.3 Power Supply Recommendations

図 8-1 shows that the device input circuitry can accurately measure signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the VS power supply pin can be 5V, whereas the bus power-supply voltage being monitored (the common-mode voltage) can be as high as 48V. The device can also withstand the full -0.3V to 48V range at the input pins, regardless of whether the device has power applied or not.

Place the required power-supply bypass capacitors as close as possible to the supply and ground pins of the device to provide stability. A typical value for this supply bypass capacitor is 0.1µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

8.4 Layout

8.4.1 Layout Guidelines

Connect all input pins (IN+X and IN–X) to the sensing resistor using a Kelvin connection or a 4-wire connection for each channel. These connection techniques verify that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

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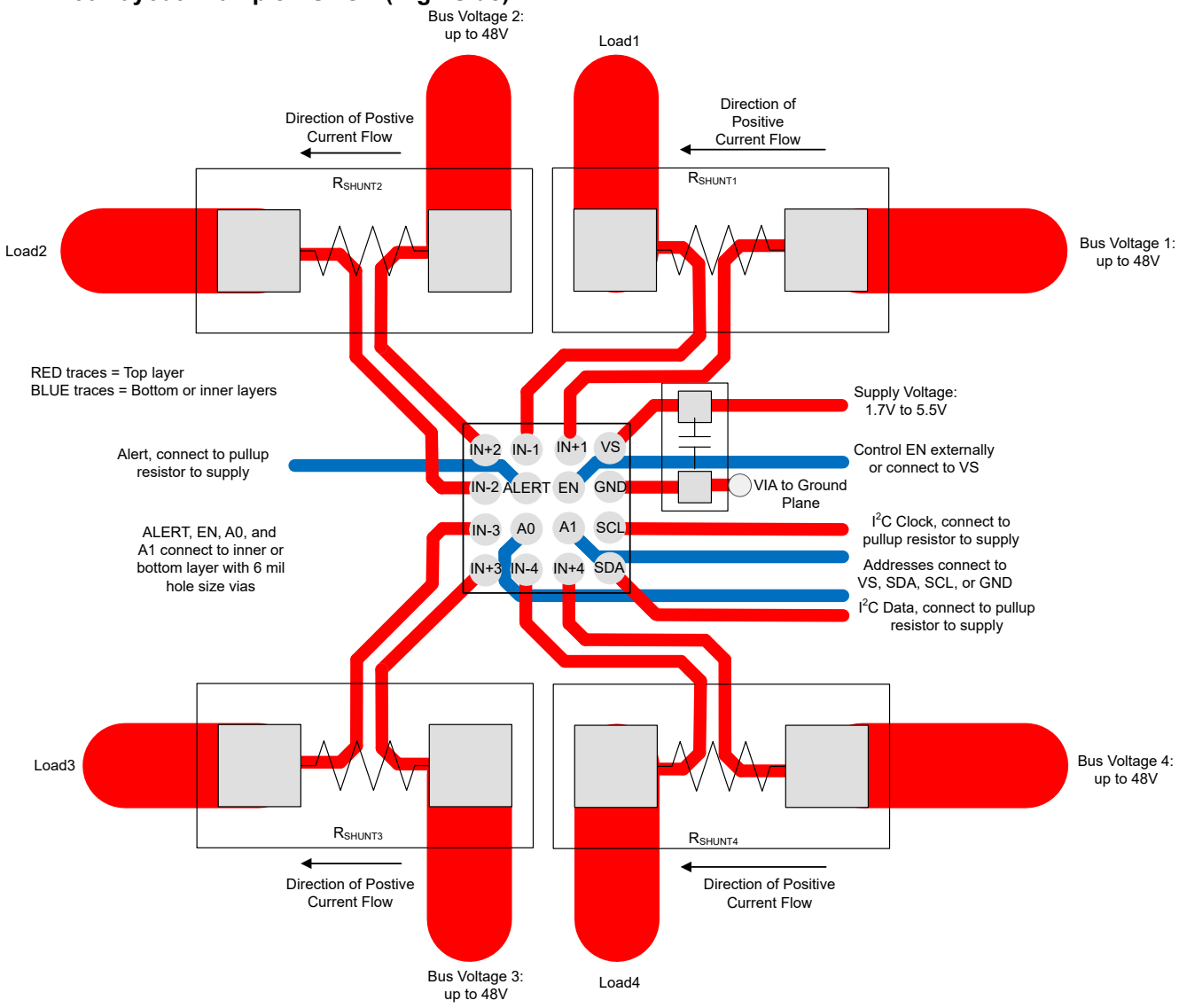
8.4.2 Layout Example

INA4230 Layout Example DSBGA (High Side)



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9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

For development support see the following:

INA234EVM and INA236EVM User's Guide

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Current Shunt Monitor with Transient Robustness Reference Design*, Design guide
- Texas Instruments, *INA234EVM and INA236EVM User's Guide*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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9.5 Trademarks

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9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

DATE	VERSION	NOTES
June 2024	*	Initial release.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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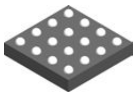
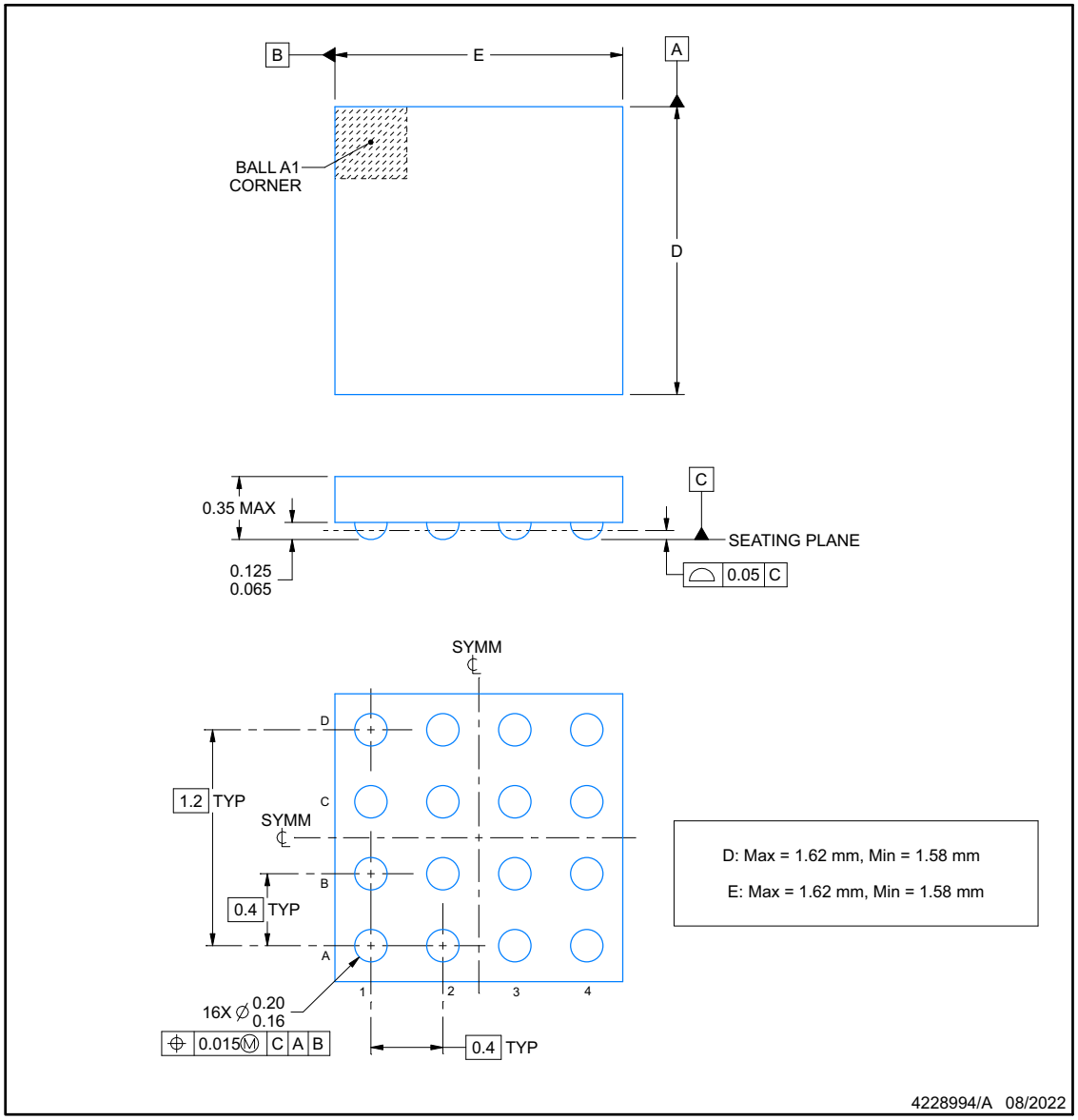


PACKAGE OUTLINE

YBJ0016-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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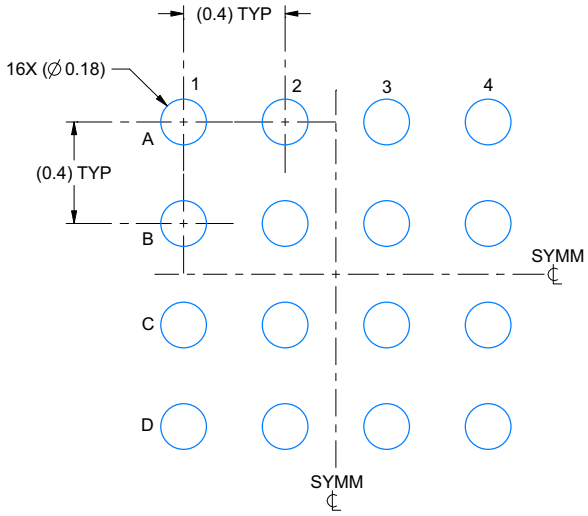
EXAMPLE BOARD LAYOUT

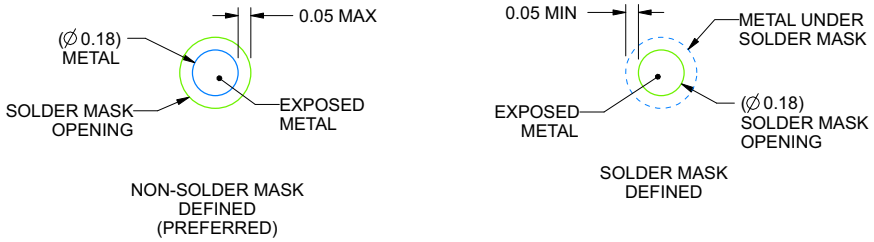
YBJ0016-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4228994/A 08/2022

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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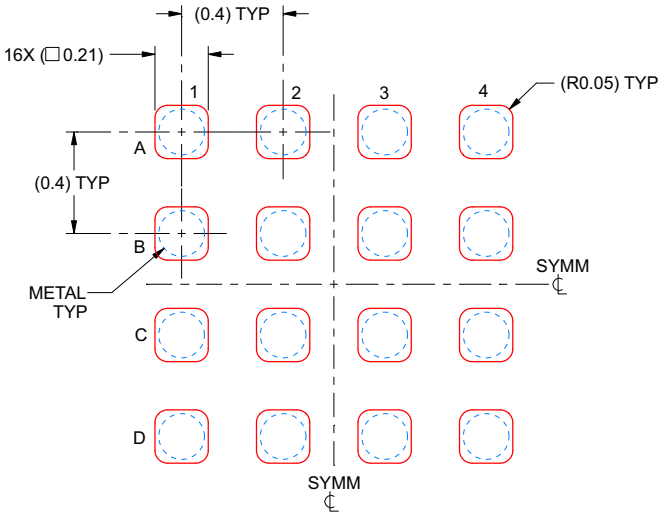
EXAMPLE STENCIL DESIGN

YBJ0016-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

4228994/A 08/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA4230AIYBJR	ACTIVE	DSBGA	YBJ	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	I4230	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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