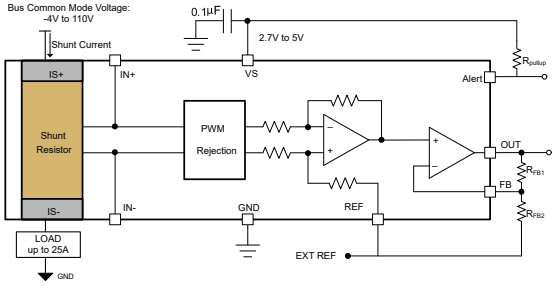
INA750x 強化 PWM 除去機能および 35A EZShunt™ テクノロジー搭載、-4V～110V、双方向、超高精度、電流センス アンプ

1 特長

- シャント抵抗内蔵の高精度ソリューション
  - 25℃で ±35A の連続電流
  - 125℃で ±25A の連続電流
  - シャント抵抗:800µΩ
  - シャント インダクタンス:2.5nH
- 広い同相電圧範囲:-4V～+110V
- スイッチング コモン モード電圧で動作するシステム向けに最適化された強化型 PWM 除去
  - 最大 125kHz のスイッチング周波数をサポート
- 非常に優れた CMRR
  - 160dB の DC CMRR
  - 50kHz で 114dB の AC CMRR
- 高い測定精度
  - システム ゲイン誤差 (最大値)
    - バージョン A:±0.35%、±35ppm/℃のドリフト
    - バージョン B:±1%、±100ppm/℃のドリフト
  - オフセット電圧 (最大値)
    - バージョン A:±15mA、±315µA/℃のドリフト
    - バージョン B:±125mA、±625µA/℃のドリフト
- 外付けの分圧抵抗回路でゲインを調整可能:
  - 40mV/A～800mV/A
- 160℃の T_J のオープン ドレイン温度アラート
- パッケージ オプション:VQFN-14

2 アプリケーション

- モーター ドライブ
- ソレノイドとアクチュエータ
- 射出成形機
- コードレス電動工具
- 医療用コードレス機器
- ドローンのプロペラ速度制御



代表的なアプリケーション

3 概要

INA750x は、800µΩ のシャント抵抗を内蔵した電圧出力、電流センス アンプです。INA750x は、電源電圧にかかわらず、-4V～+110V の同相電圧範囲で双方向の電流を監視するように設計されています。可変ゲイン オプションは、システムのダイナミック レンジの最適化に役立ちます。ケルビン接続シャント抵抗とゼロ ドリフトのチョップ アンプを内蔵しているため、較正と等価の測定精度、±35ppm/℃という非常に小さい温度ドリフト係数、センシング抵抗に最適化されたレイアウトが実現されています。

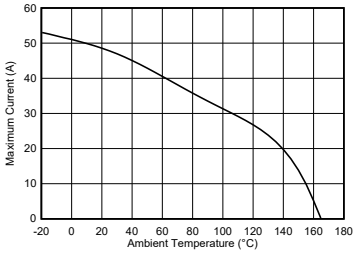
INA750x の設計には、強化された PWM 除去回路が組み込まれており、大きな (dv/dt) 同相過渡によるじょう乱を抑制し、スイッチング システムにおいてリアルタイムで連続的な電流測定が可能です。この連続測定は、モータ ドライブ アプリケーションにおけるインラインの電流測定や、ソレノイドのバルブ制御アプリケーションなどに不可欠なものです。

このデバイスは 2.7V～5.5V の単一電源で動作し、消費電流は最大 4.25mA です。どのバージョンも、拡張動作温度範囲 (-40℃～+125℃) で動作が規定され、14 ピン VQFN パッケージで供給されます。

パッケージ情報 (1)

部品番号	パッケージ	パッケージ サイズ(2)
INA750A、INA750B	REM (VQFN -14)	4.0mm × 5.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値で、該当する場合はピンも含まれます。



最大連続電流と周囲温度との関係

Table of Contents

4 Pin Configuration and Functions

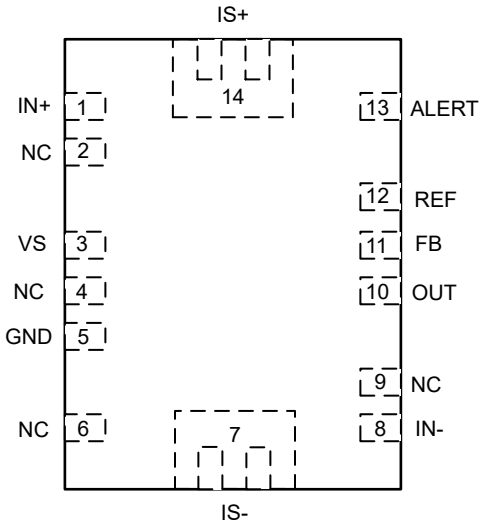


図 4-1. INA750x REM Package VQFN Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ALERT	13	Analog Out	Open drain temperature alert
FB	11	Analog Input	Gain adjustment feedback; connect to resistor divider to adjust device gain.
GND	5	Analog	Ground
IN–	8	Analog Input	Voltage input from load side of shunt resistor
IN+	1	Analog Input	Voltage input from supply side of shunt resistor
IS–	7	Analog Input	Connect to load
IS+	14	Analog Input	Connect to supply
NC	2	–	Connect to IN+ (pin 1).
NC	4, 6	–	Connect to ground or leave unconnected.
NC	9	–	Connect to IN– (pin 8).
OUT	10	Analog Output	Output voltage
REF	12	Analog Input	Reference voltage, 0 V to VS
VS	3	Analog	Power supply, 2.7 V to 5.5 V

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage (V_S)			6	V
Analog Inputs, V_{IN+}, V_{IN-} (2)	Differential (V_{IN+}) - (V_{IN-})	–12	12	V
	Common - mode	GND – 20	120	V
Analog input (REF)	Analog input (REF)	GND – 0.3	Vs + 0.3	V
Analog input (FB)	Analog input (FB)	GND – 0.3	Vs + 0.3	V
Analog output (OUT)	Analog output (OUT)	GND – 0.3	Vs + 0.3	V
Digital output (ALERT)	Temperature Alert Output	GND – 0.3	Vs + 0.3	V
T_A	Operating Temperature	–55	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range	–4		110	V
V_S	Operating supply range	2.7		5.5	V
I_{SENSE}	Continuous Current	–25		25	A
V_{REF}	Reference voltage range	0		V_S	V
V_{FB}	Feed-back voltage range	0		V_S	V
T_A	Ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		INA750x REM (VQFN) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(2)	13.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter(2)	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter(2)	13.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

(2) Thermal metrics are relative to the internal die and are conservative relative to the heating that occur from the package leadframe shunt. For more details on heating, see the Safe Operating Area section.

5.5 Electrical Characteristics

at T_A = 25 °C, V_S = 5V, I_{SENSE} = IS+ = 0A, V_{CM} = $V_{IN–}$ = 48V, V_{FB} = V_{OUT} (Adjustable Gain = 1), and V_{REF} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input range	V_{IN+} = –4V to 110V, I_{SENSE} = 0A, T_A = –40°C to +125°C	–4		110	V
CMRR	Common-mode rejection ratio	V_{IN+} = –4V to 110V, I_{SENSE} = 0A, T_A = –40°C to +125°C, INA750A		±12.5	±40	µA/V
		V_{IN+} = –4V to 110V, I_{SENSE} = 0A, T_A = –40°C to +125°C, INA750B		±400	±650	
CMRR	Common-mode rejection ratio	f = 50kHz		±28		mA/V
I_{os}	Input referred offset current error	I_{SENSE} = 0A, INA750A		±2.5	±15	mA
		I_{SENSE} = 0A, INA750B		±32	±125	
dI_{os}/dT	Input referred offset current error drift	I_{SENSE} = 0A, T_A = –40°C to +125°C, INA750A		±0.063	±0.4	mA/°C
		I_{SENSE} = 0A, T_A = –40°C to +125°C, INA750B		±0.125	±0.65	
PSRR	Power supply rejection ratio	V_S = 2.7V to 5.5V, VREF = 1V, I_{SENSE} = 0A, INA750A		±0.125	±2.5	mA/V
		V_S = 2.7V to 5.5V, VREF = 1V, I_{SENSE} = 0A, INA750B		±1.25	±12.5	
I_B	Total input bias current	I_{B+}+ I_{B-}, I_{SENSE} = 0A	45	66	90	µA
I_{FB}	Feed-back current	I_{SENSE} = 0A		±2		nA
		I_{SENSE} = 0A, T_A = –40°C to +125°C			±6	
INTEGRATED SHUNT RESISTOR						
R_{SHUNT}	Internal Kelvin shunt resistance	IN+ to IN-, T_A = 25 °C		0.8		mΩ
	Pin to pin package resistance	IS+ to IS-, T_A = 25 °C	0.800	960	1.200	mΩ
	Pin to pin package inductance	IS+ to IS-, T_A = 25 °C		2.5		nH
I_{SENSE}	Maximum Continuous Current	T_A = –40°C to +125°C			±25	A
	Shunt short time overload	I_{SENSE} = 55A for 5 seconds		± 0.01		%
	Shunt temperature cycle	–65°C to 150°C, 500 cycles		± 0.05		%
	Shunt resistance to solder heat	260°C solder, 10 seconds		± 0.1		%
	Shunt high temperature exposure	1000 hours, T_A = 150°C		± 0.015		%
OUTPUT						
G	Gain	INA750A , INA750B		40		mV/A
G	System Gain Error (shunt + amplifier)	GND + 50mV ≤ V_{OUT} ≤ V_S – 200mV, T_A = 25°C, I_{SENSE} = ±25A, INA750A		±0.05	±0.35	%
		GND + 50mV ≤ V_{OUT} ≤ V_S – 200mV, T_A = 25°C, I_{SENSE} = ±5A, INA750A		±0.05	±0.35	
		(1)GND + 50mV ≤ V_{OUT} ≤ V_S – 200mV, T_A = 25°C, I_{SENSE} = ±25A, INA750B		±0.3	±1	
		GND + 50mV ≤ V_{OUT} ≤ V_S – 200mV, T_A = 25°C, I_{SENSE} = ±5A, INA750B		±0.1	±0.625	
G	System Gain Error Drift (shunt + amplifier)	T_A = –40°C to +125°C, INA750A		±0.5	±35	ppm/°C
		T_A = –40°C to +125°C, INA750B		±10	±100	
	Power Coefficient Gain non-Linearity Error	(2)GND + 10mV ≤ V_{OUT} ≤ V_S – 200mV		6		ppm/A^2

at T_A = 25 °C, V_S = 5V, I_{SENSE} = IS+ = 0A, V_{CM} = $V_{IN–}$ = 48V, V_{FB} = V_{OUT} (Adjustable Gain = 1), and V_{REF} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RVRR	Reference voltage rejection ratio (input - referred)	V_{REF} = 0.5V to 4.5V		±1.15	±6.25	mA/V
	Maximum Capacitive Load	No sustained oscillation		0.5		nF
VOLTAGE OUTPUT						
	Swing to V_S Power Supply Rail	R_L = 10kΩ to GND, V_{REF} = V_S , Adjustable Gain = 4, T_A = –40°C to +125°C		V_S – 0.05	V_S – 0.1	V
	Swing to Ground	R_L = 10kΩ to GND, V_{REF} = GND, Adjustable Gain = 4, T_A = –40°C to +125°C		V_{GND} + 5	V_{GND} + 10	mV
	Swing to Ground	R_L = 10kΩ to GND, V_{REF} = GND, T_A = –40°C to +125°C		V_{GND} + 1	V_{GND} + 5	mV
FREQUENCY RESPONSE						
BW	Bandwidth (current sense amplifier only)	-3dB Bandwidth, V_{FB} = V_{OUT}		1		MHz
		-3dB Bandwidth, Adjustable Gain = 4		0.5		MHz
	Propagation delay(3)	V_{IN+}, V_{IN-} = 48V, Adjustable Gain = 1, V_{REF} = 150mV, Load Step = 0A to 20A, Output settles to 1%		0.250		µs
	Total Settling time (current in to out)	V_{IN+}, V_{IN-} = 48V, Adjustable Gain = 1, V_{REF} = 150mV, Load Step = 0A to 20A, Output settles to 1%		5		µs
SR	Slew Rate	V_{FB} = V_{OUT}		1.8		V/µs
		Adjustable Gain = 4		1.5		V/µs
NOISE						
	Current Noise Density			75		µA/√Hz
POWER SUPPLY						
I_Q	Quiescent current			3.5	4.25	mA
		T_A = –40°C to +125°C			4.5	mA
TEMPERATURE						
T_{Alert}	Thermal Alert Threshold	$R_{pull-up}$ = 10kΩ,		160		°C
VLO_{Alert}	Thermal Alert Low-level output voltage	$R_{pull-up}$ = 10kΩ,			200	mV

(1) This is inclusive of Power Coefficient Gain Non-linearity Error
(2) I_{SENSE} = ± 5A to ± 25A, V_{OUT} = V_{REF} ± 1V
(3) Propagation delay is difference of time between 10% of load step to 10% of final output settling value

5.6 Typical Characteristics

at T_A = 25°C, V_S = 5V, I_{SENSE} = IS+ = 0A, V_{CM} = 48V, V_{FB} = V_{OUT}, and V_{REF} = V_S / 2 (unless otherwise noted)

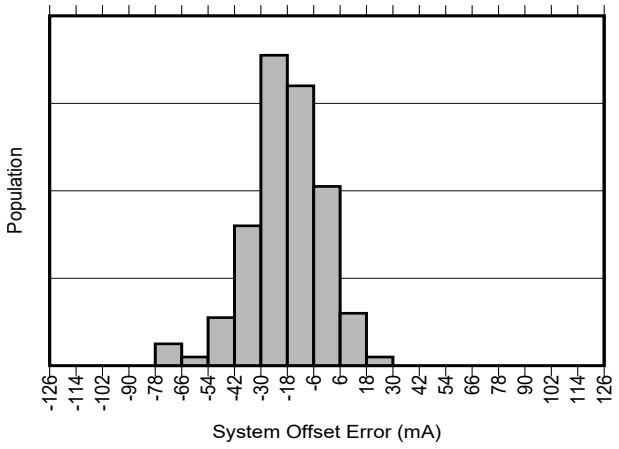


図 5-1. INA750 B Input Offset Current Production Distribution

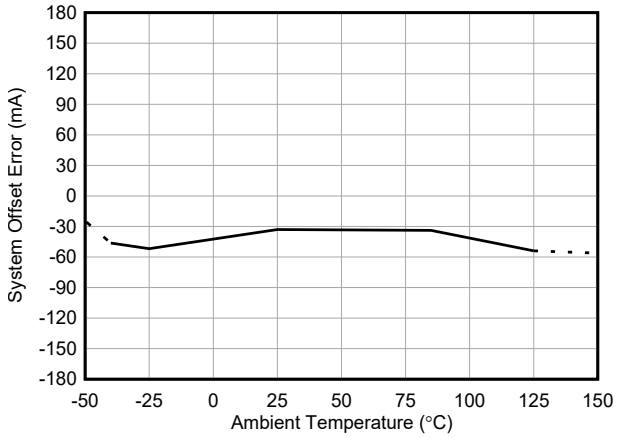


図 5-2. INA750 B Input Offset Current vs Temperature

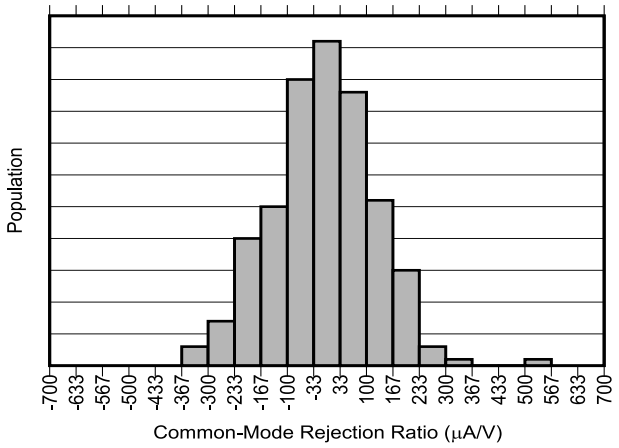


図 5-3. INA750 B Common-Mode Rejection Production Distribution

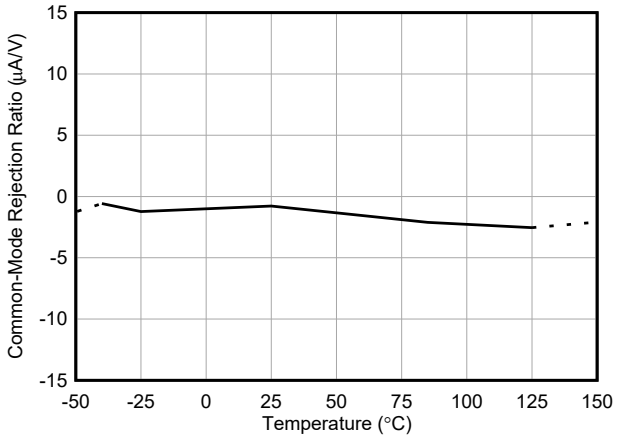


図 5-4. Common-Mode Rejection Ratio vs Temperature

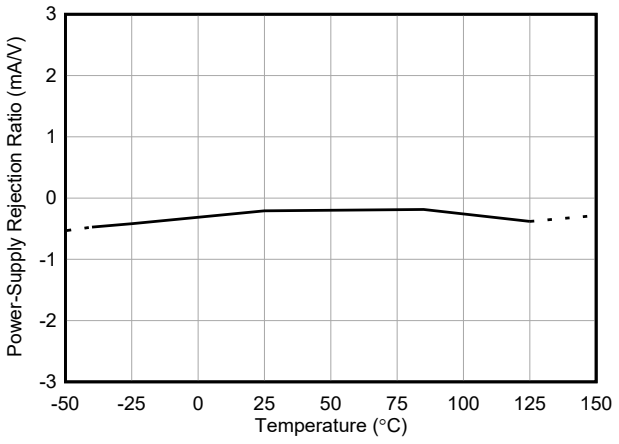


図 5-5. Power-Supply Rejection Ratio vs Temperature

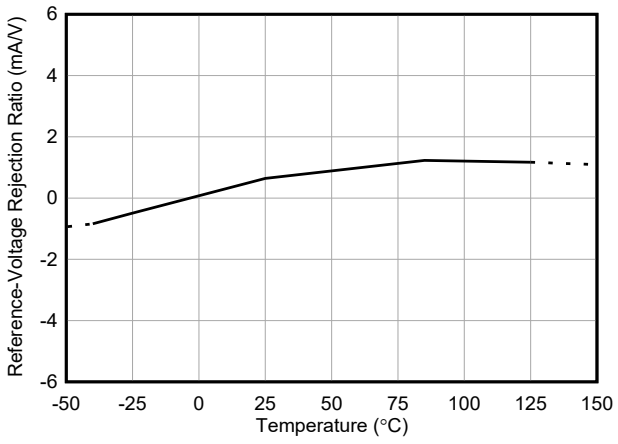


図 5-6. Reference Voltage Rejection Ratio vs Temperature

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, I_{SENSE} = IS+ = 0A, V_{CM} = 48V, V_{FB} = V_{OUT}, and V_{REF} = V_S / 2 (unless otherwise noted)

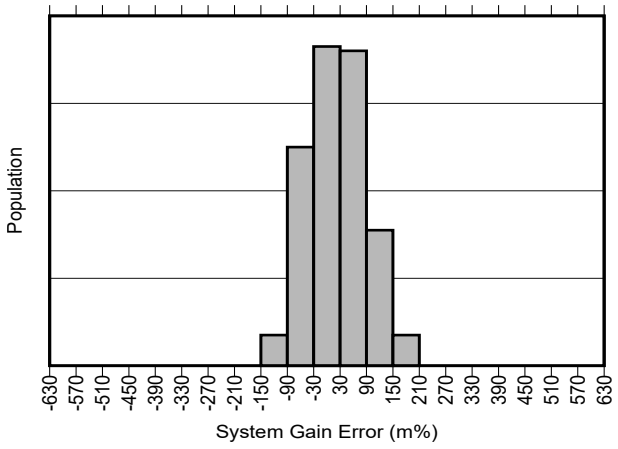


図 5-7. INA750 B Gain Error Production Distribution

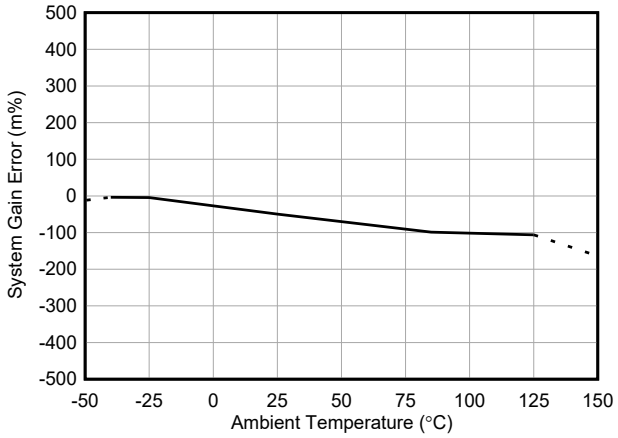


図 5-8. INA750 B Gain Error vs Temperature

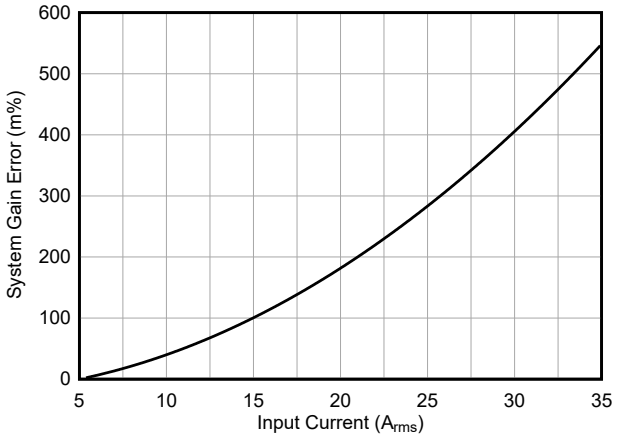


図 5-9. INA750 B System Gain Error vs Input Current

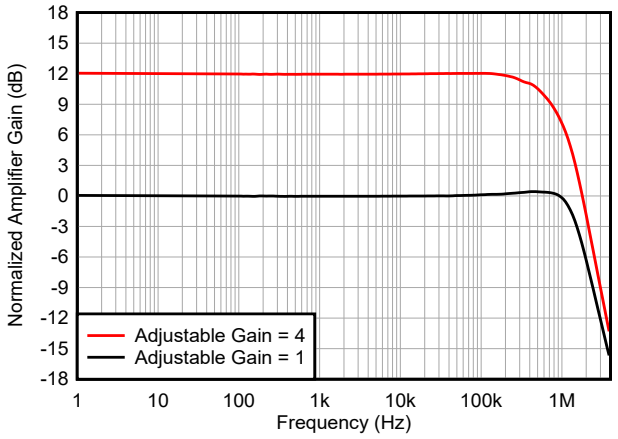


図 5-10. Current Sense Amplifier Gain vs Frequency

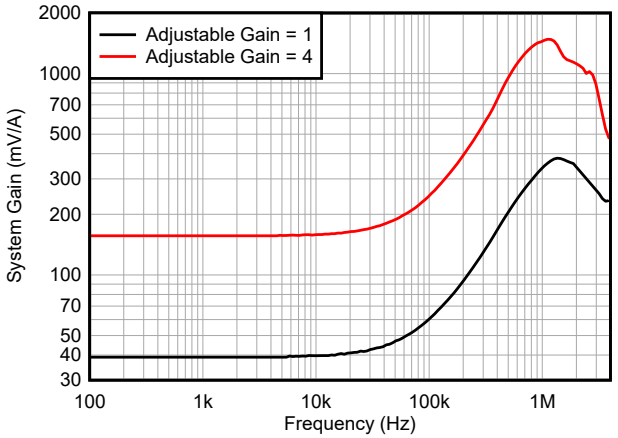


図 5-11. System Gain vs Frequency

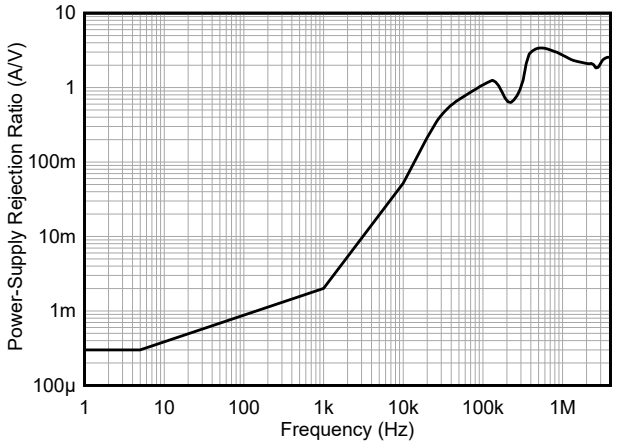


図 5-12. Power-Supply Rejection Ratio vs Frequency

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, I_{SENSE} = IS+ = 0A, V_{CM} = 48V, V_{FB} = V_{OUT}, and V_{REF} = V_S / 2 (unless otherwise noted)

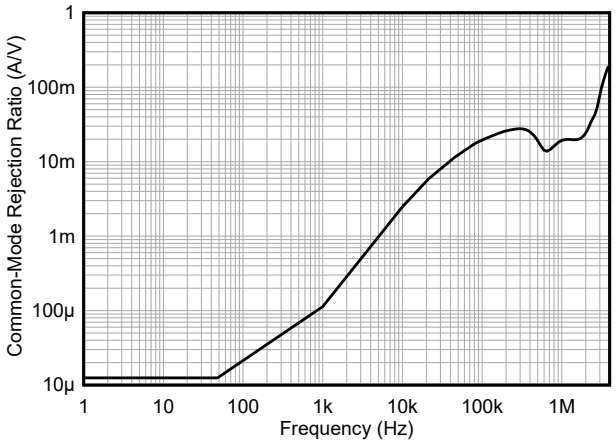
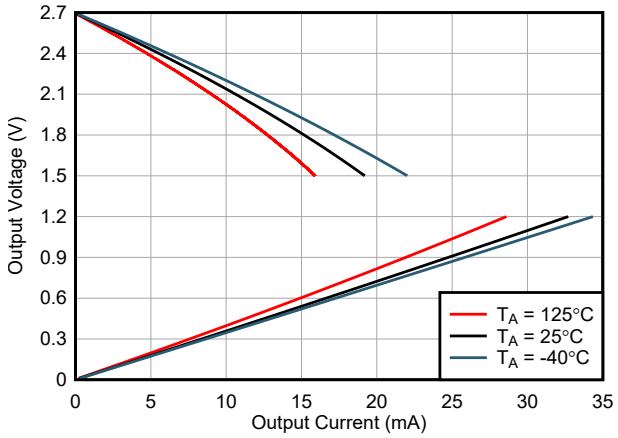
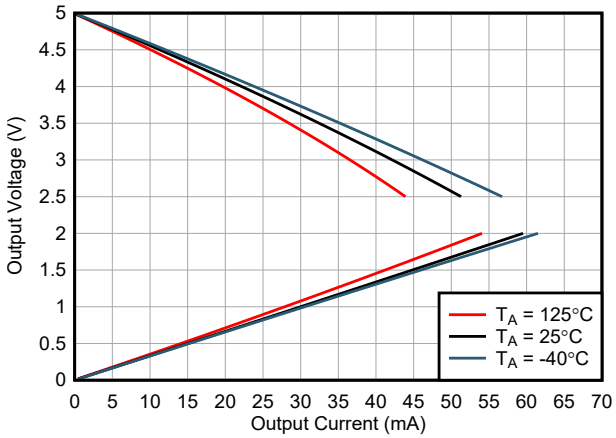


図 5-13. Common-Mode Rejection Ratio vs Frequency



V_S = 2.7V

図 5-14. Output Voltage Swing vs Output Current



V_S = 5V

図 5-15. Output Voltage Swing vs Output Current

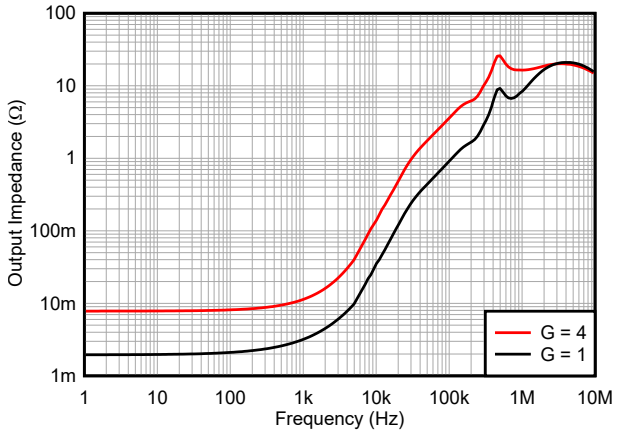
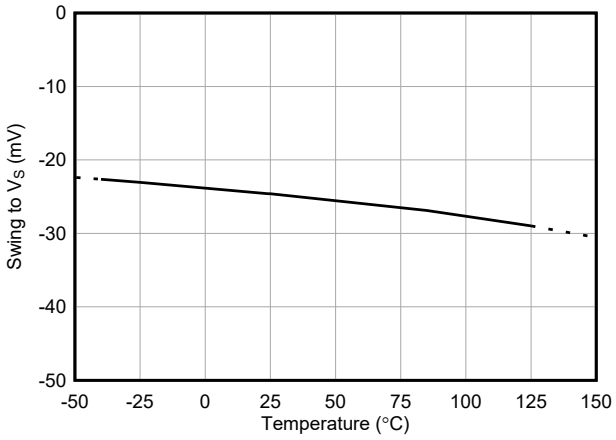
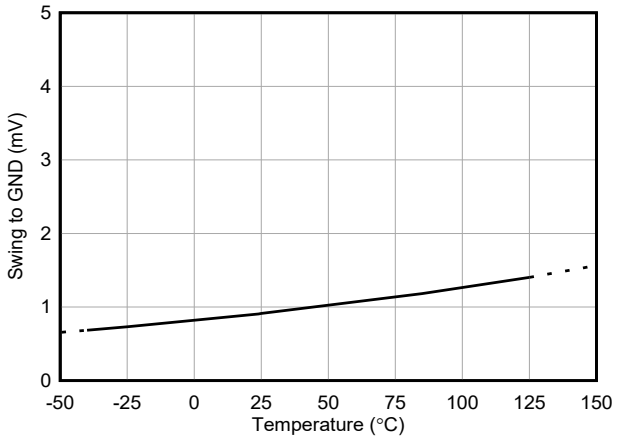


図 5-16. Output Impedance vs Frequency



Adjustable Gain = 4, V_{REF} = V_S

図 5-17. Output Voltage Swing High vs Temperature



Adjustable Gain = 1, V_{REF} = GND

図 5-18. Output Voltage Swing Low vs Temperature

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, I_{SENSE} = IS+ = 0A, V_{CM} = 48V, V_{FB} = V_{OUT}, and V_{REF} = V_S / 2 (unless otherwise noted)

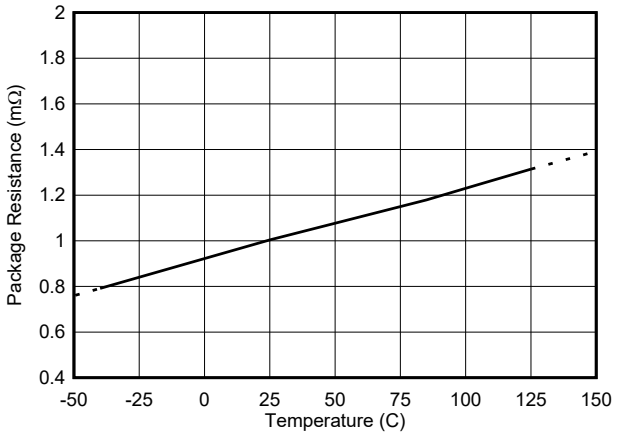


図 5-19. Package Resistance vs Temperature

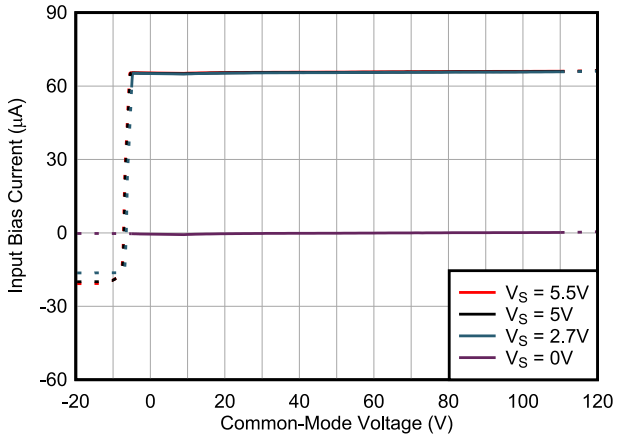


図 5-20. Total Input Bias Current vs Common-Mode Voltage

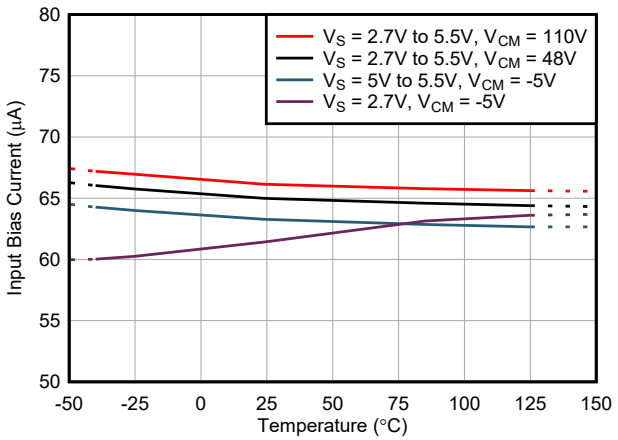


図 5-21. Total Input Bias Current vs Temperature

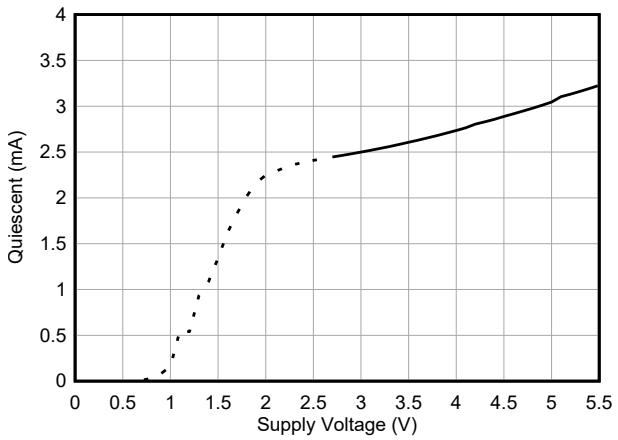


図 5-22. Quiescent Current vs Supply Voltage

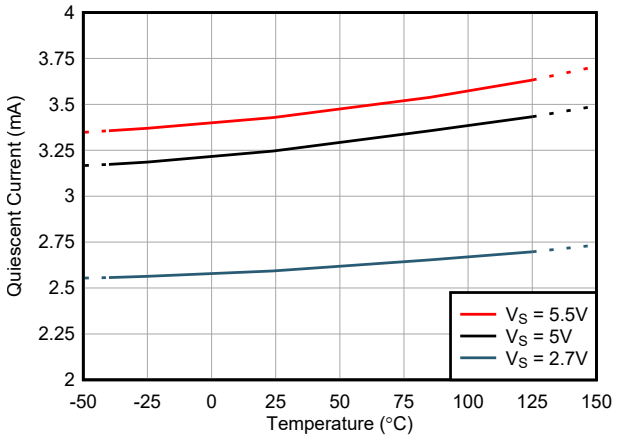


図 5-23. Quiescent Current vs Temperature

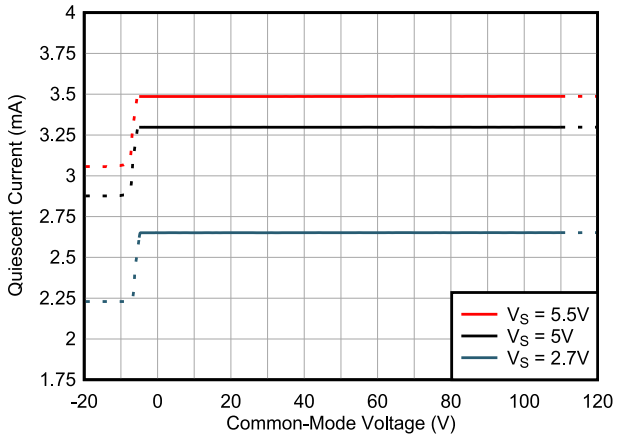


図 5-24. Quiescent Current vs Common-Mode Voltage

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5V, I_{SENSE} = IS+ = 0A, V_{CM} = 48V, V_{FB} = V_{OUT}, and V_{REF} = V_S / 2 (unless otherwise noted)

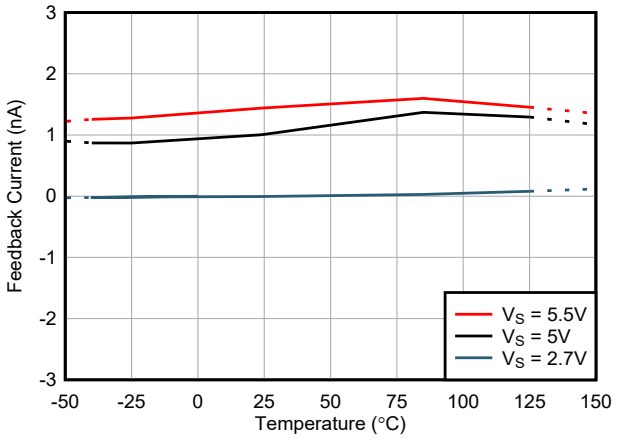


図 5-25. Feedback Current vs Temperature

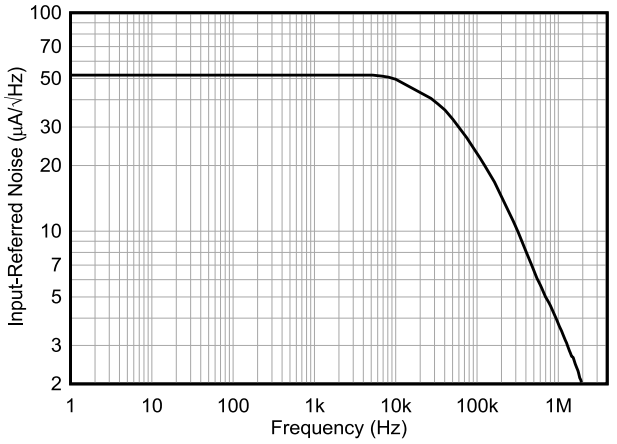


図 5-26. INA750 A Input-Referred Current Noise vs Frequency

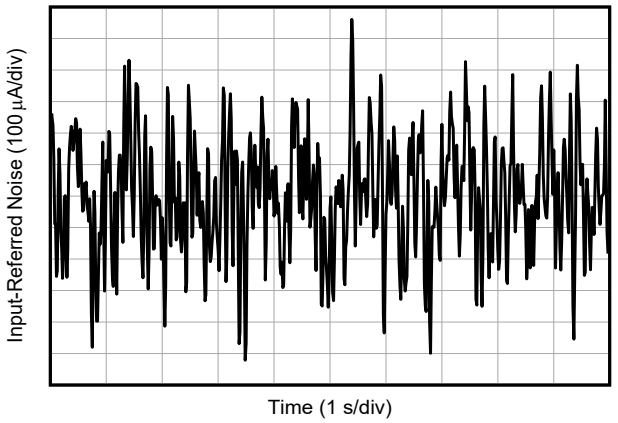
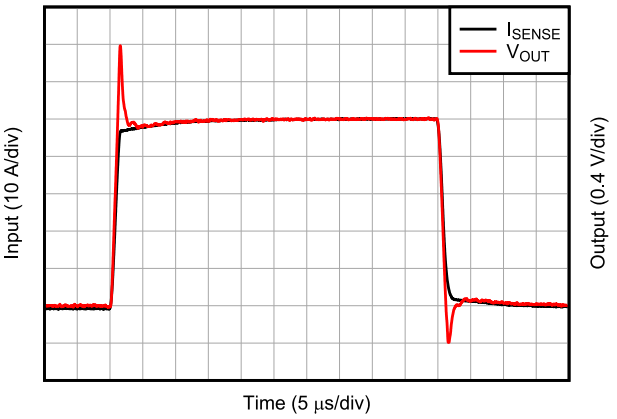
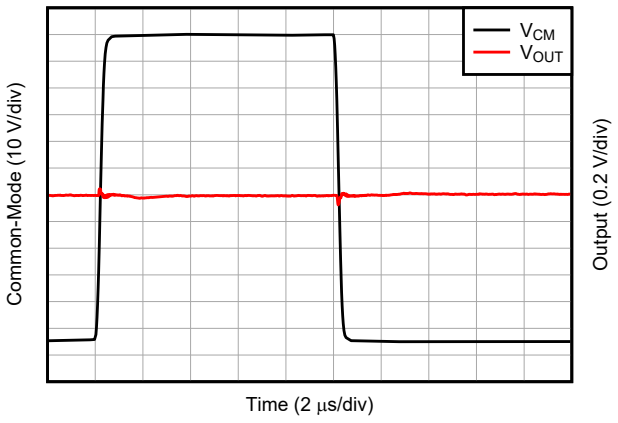


図 5-27. 0.1Hz to 10Hz Current Noise (Referred-to-Input)



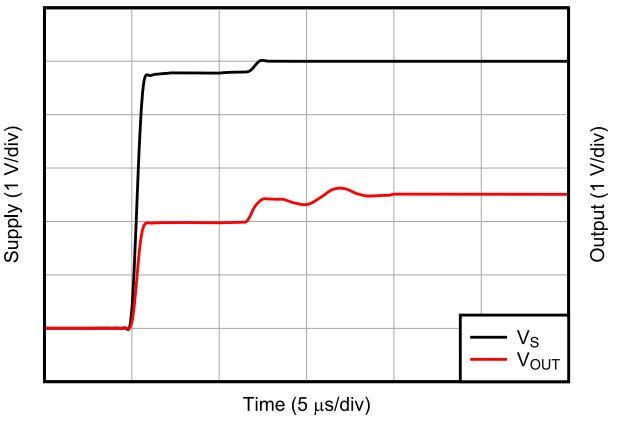
V_{REF} = 1V, 50A input step

図 5-28. Amplifier Step Response



INA750

図 5-29. Common-Mode Transient Response



V_{REF} = 0V

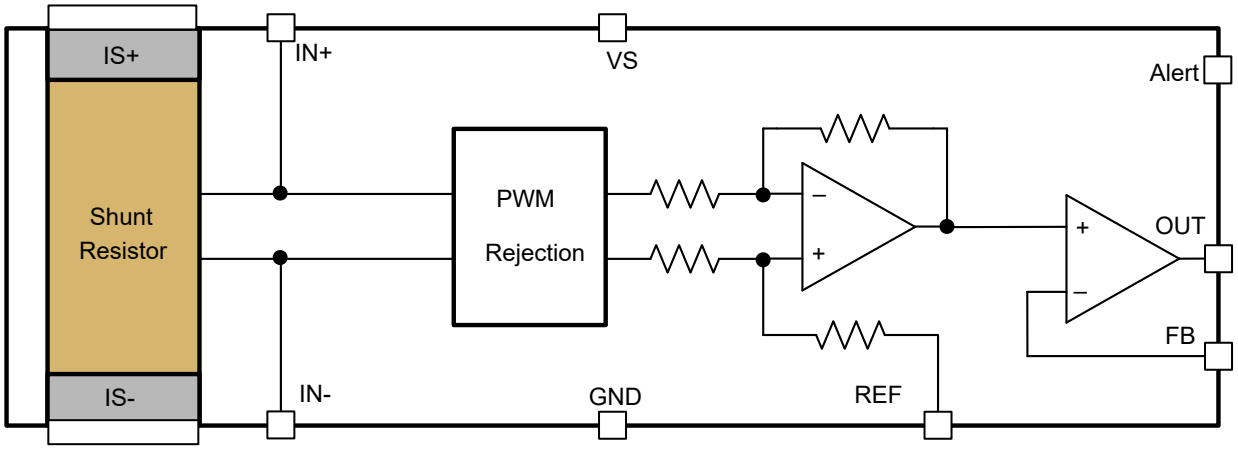
図 5-30. Start-Up Response

6 Detailed Description

6.1 Overview

The INA750x features a precision current sensing solution with 800µΩ current-sensing EZShunt™ technology resistor and supports common-mode voltages up to 110V. The internal amplifier features a precision zero-drift topology with excellent common-mode rejection ratio (CMRR) and enhanced pulse-width modulation (PWM) rejection. Enhanced PWM rejection reduces the effect of common-mode transients on the output signal that are associated with PWM signals in switching systems. High-precision measurements are enabled by matching the shunt resistor value and the current-sensing amplifier gain across temperature, thus providing a highly-accurate, system-calibrated method for measuring current. Flexibility of adjustable gain with two external resistors allows for the optimization of the desired full-scale output voltage based on the target current range expected in the application.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Integrated Shunt Resistor

The INA750x features an integrated EZShunt™ technology current-sensing resistor that provides accurate measurements over the entire specified temperature range of –40°C to +125°C. The integrated current-sensing resistor provides measurement stability over temperature, and simplifies printed circuit board (PCB) layout and board constraint difficulties common in high-precision measurements.

The onboard current-sensing resistor is designed as a 4-wire (or Kelvin) connected resistor that enables accurate measurements through a force-sense connection. Internally connected amplifier input pins (IN– and IN+) to the sense pins of the shunt resistor eliminates many instances of parasitic impedance commonly found in typical very-low sensing-resistor level measurements. The INA750x is system-calibrated to make sure that the current-sensing resistor and current-sensing amplifier are both precisely matched to one another. The in-package integrated sensing resistor must be used with the internal current-sensing amplifier to achieve the optimized system gain specification.

The INA750x has approximately 1mΩ of package resistance. Of this total package resistance, 800µΩ resistance from the Kelvin-connected current-sensing resistor is used by the amplifier. The power dissipation requirements of the system and package are based on the total 1mΩ package resistance between the IS+ and IS– pins.

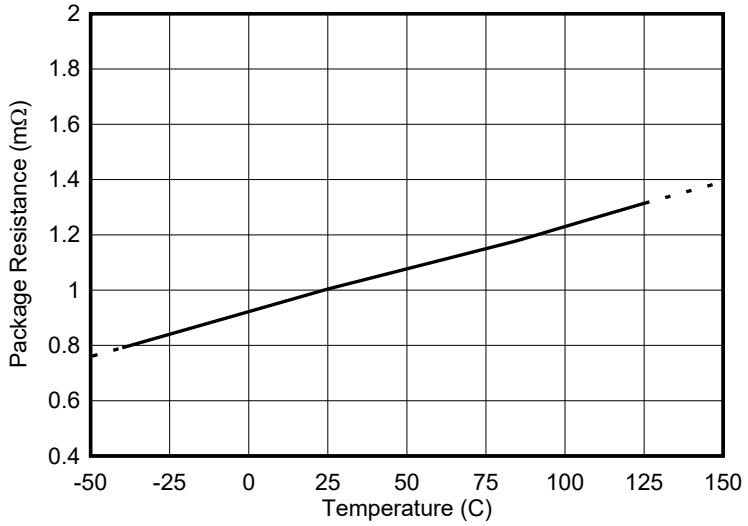


図 6-1. IS+ to IS– Package Resistance vs Temperature

6.3.2 Safe Operating Area

The heat dissipated across the package when current flows through the device ultimately determines the maximum current that can be safely handled by the package. The current consumption of the silicon is relatively low, leaving the total package resistance to carry the high load current as the primary contributor to the total power dissipation of the package. The maximum safe-operating current level shown in 図 6-2 is set to make sure that the heat dissipated across the package is limited so that no damage occurs to the resistor or the package, or that the internal junction temperature of the silicon does not exceed a 165°C limit.

External factors, such as ambient temperature, external air flow, and PCB layout, contribute to how effectively the device dissipates heat. The internal heat is developed as a result of the current flowing through the total package resistance of 1mΩ.

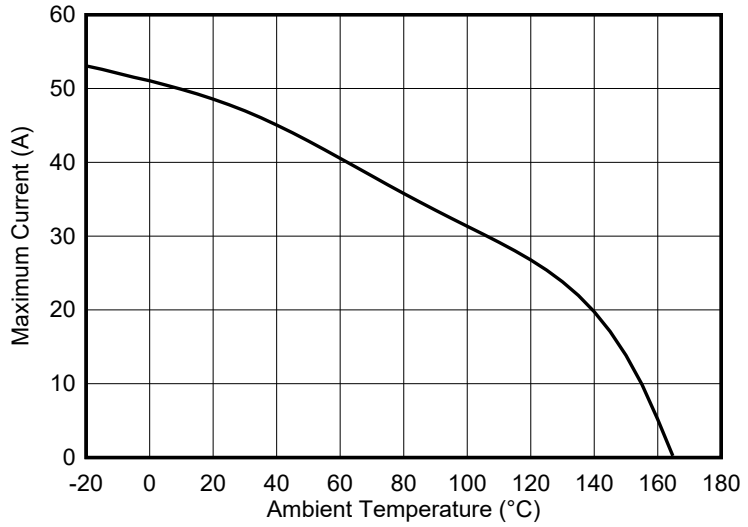


図 6-2. Maximum Continuous Current vs Ambient Temperature

6.3.3 Short-Circuit Duration

The INA750x features a physical shunt resistance that is able to withstand current levels higher than the continuous handling limit of 25A without sustaining damage to the current-sensing resistor or the current-sensing amplifier, if the excursions are brief. 図 6-3 shows the short-circuit duration curve for the INA750x .

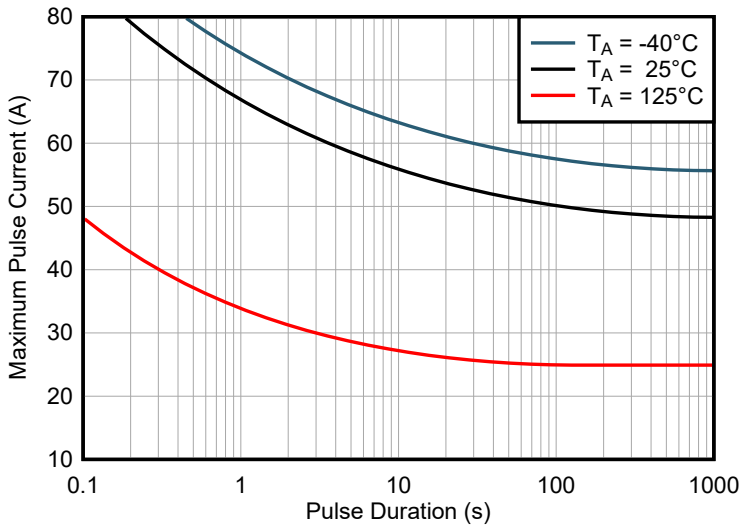


図 6-3. Maximum Pulse Current vs Pulse Duration (Single Event)

6.3.4 Temperature Drift Correction

System calibration is common for many industrial applications to eliminate initial component and system-level errors that can be present. A system-level calibration reduces the initial accuracy requirement for many of the individual components because the errors associated with these components are effectively eliminated through the calibration procedure. This calibration enables precise measurements at the temperature in which the system is calibrated. As the system temperature changes because of external ambient changes or self heating, measurement errors are reintroduced. Without accurate temperature compensation used in addition to the initial adjustment, the calibration procedure is not effective. The user must account for temperature-induced changes. The built-in programmed temperature compensation in the INA750x (including both the integrated current-sensing resistor and current-sensing amplifier) keep the device measurement accurate, even when the temperature changes throughout the specified temperature range of the device.

6.3.5 Enhanced PWM Rejection Operation

The enhanced PWM rejection feature of the INA750x provides increased attenuation of large common-mode ΔV/Δt transients. Large ΔV/Δt common-mode transients associated with PWM signals are employed in applications such as motor or solenoid drive and switching power supplies. The disturbances that can occur at the output of a current sense amplifier from common-mode transients causes erroneous measurements and impose limitations when the output is valid. The INA750x is designed with high common-mode rejection techniques to reduce large ΔV/Δt transients before the system is disturbed. As a result, this makes system design simple with INA750x . The high AC CMRR, in conjunction with signal bandwidth, allows the INA750x to minimize output disturbances and ringing during common-mode transitions when compared against traditional current-sensing amplifiers. 図 6-4 shows the INA750x PWM enhancement performance.

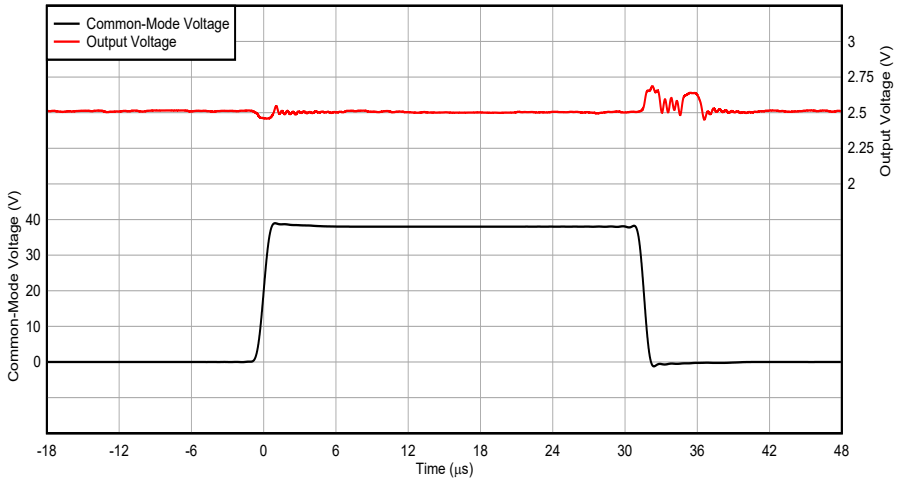


図 6-4. Enhanced PWM Rejection Performance

6.4 Device Functional Modes

6.4.1 Adjusting the Output With the Reference Pin

The INA750x output is configurable to allow for unidirectional or bidirectional operation. 図 6-5 shows a circuit for setting output with an external reference.

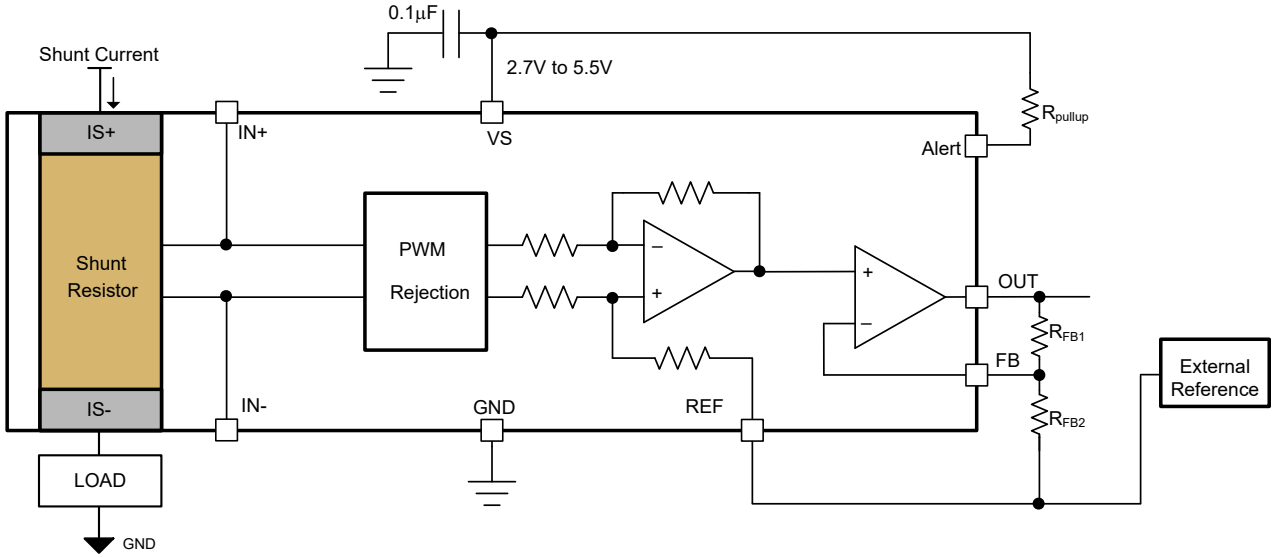


図 6-5. Adjusting the Output

The output voltage is set by applying a voltage from an external reference at REF. The reference input is connected to internal gain network. The external resistor network of R_{FB1} and R_{FB2}, connected to OUT, FB and REF pins, set up adjustable gain as explained in Adjustable Gain Set Using External Resistors. Output is set accurately at the voltage provided by external reference as shown in 式 1 when the resistor R_{FB2} is connected to the same voltage as REF pin. The voltage at REF pin can range between supply Vs and GND. For symmetric bidirectional current sensing REF is set at mid-supply which sets out at mid-supply as well.

$$V_{OUT} = G \times (I_{SHUNT}) + V_{REF} \quad (1)$$

6.4.1.1 Reference Pin Connections for Unidirectional Current Measurements

Unidirectional operation allows current measurements through a resistive shunt in one direction. For unidirectional operation, connect the device reference pin to the negative rail (see the Ground Referenced Output section) or positive rail, V_S. The required differential input polarity depends on the output voltage setting. The amplifier output moves away from the referenced rail proportional to the current passing through the internal shunt resistor.

6.4.1.2 Ground Referenced Output

When using the INA750x in unidirectional mode with a ground-referenced output, both REF input and resistor R_{FB2} are connected to ground. 図 6-6 shows how this configuration takes the output to ground when there is 0A flowing across the internal shunt.

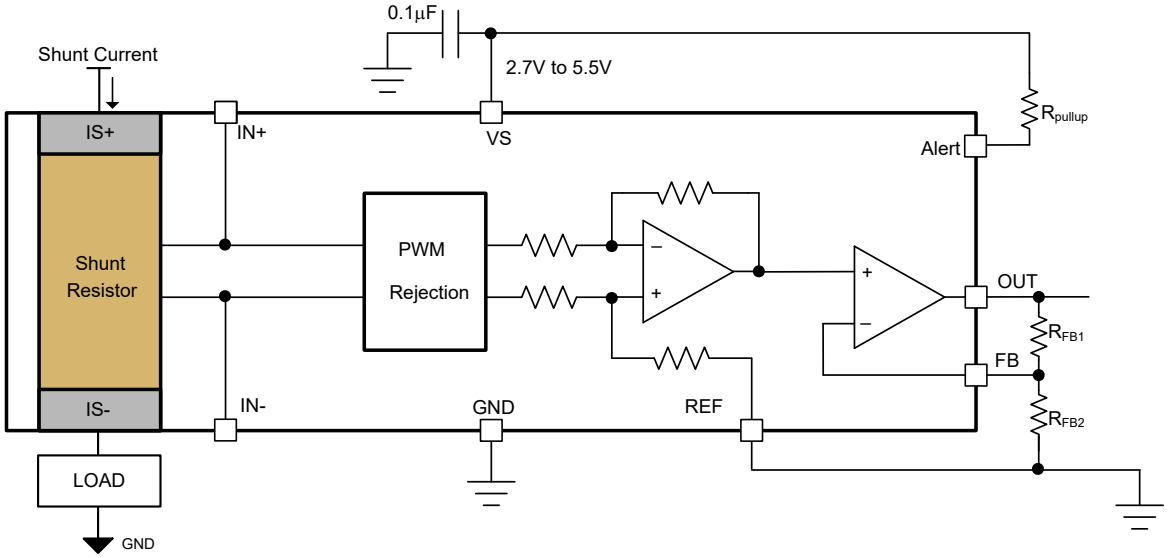


図 6-6. Ground-Referenced Output

6.4.1.3 Reference Pin Connections for Bidirectional Current Measurements

Bidirectional operation allows the INA750x to measure currents through a resistive shunt in two directions. For this case, set the output voltage anywhere within the reference input limits. A common configuration is to set the reference inputs at half-scale for equal range in both directions. However, the reference input can be set to a voltage other than half-scale when the bidirectional current is nonsymmetrical.

6.4.1.4 Output Set to Mid-Supply Voltage

図 6-7 shows two equal resistors R_1 and R_2 connected between VS and the GND pins divide the supply at half, and by connecting REF pin to the divided supply, output is set to mid-supply voltage. The mid-point of these resistors is buffered using external operational amplifier to avoid loading of resistors resulting in error. The output is set to middle of the supply when there is no differential input voltage or 0A current in shunt resistor. This method creates a ratiometric offset to the supply voltage, where the output voltage remains at VS / 2 when 0A of current flows through internal shunt resistor.

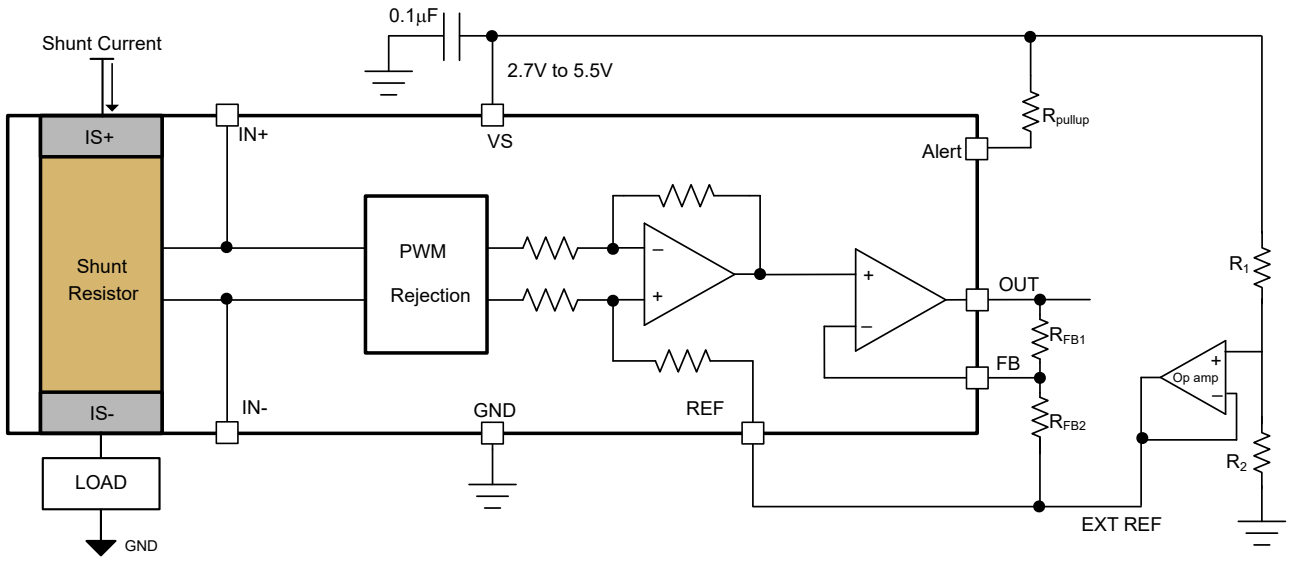


図 6-7. Mid-Supply Voltage Output

6.4.2 Adjustable Gain Set Using External Resistors

The INA750x features adjustable gain with two external resistor network. The default gain is 40mV/A, and with added external adjustable gain resistor network, total gain (G) can range up to 800mV/A. 図 6-8 shows two external resistors R_{FB1} and R_{FB2} configured for added external gain. 式 2 can be used for calculating external adjustable gain and 式 3 shows the total gain of the system with external adjustable gain. The REF pin and one end of resistor R_{FB2} is connected to external reference based on needed voltage at OUT pin as described in Adjusting the Output With the Reference Pin.

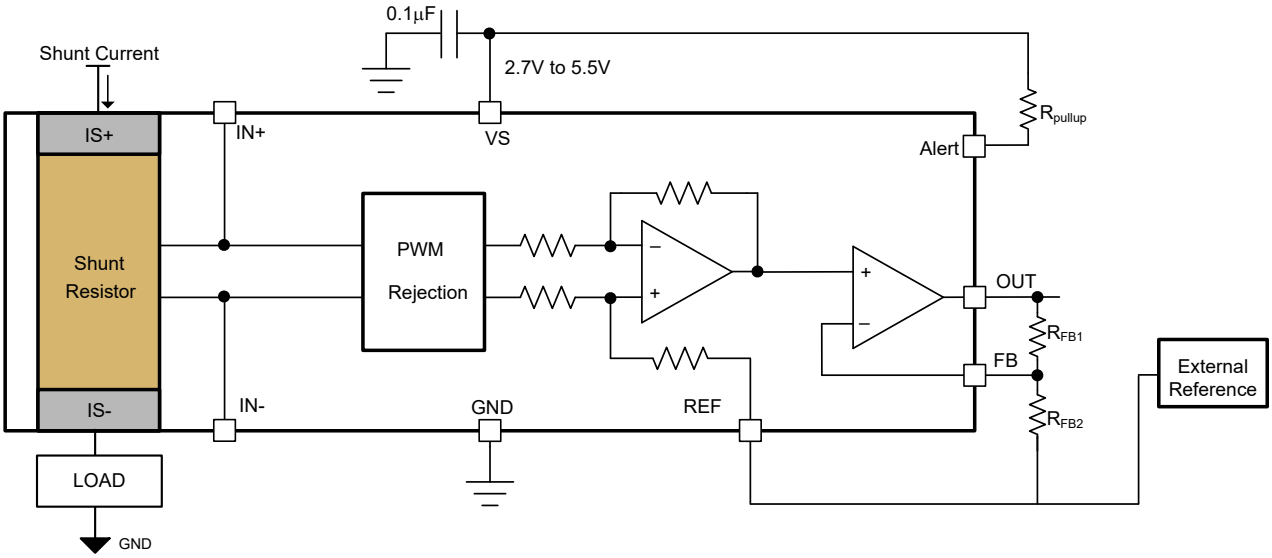


図 6-8. Adjustable Gain Setting With External Resistor Divider

$$\text{Adjustable Gain} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \quad (2)$$

$$G = 40\frac{mA}{V} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \quad (3)$$

The FB pin in INA750x has associated bias current, which can add to error when large values of adjustable gain resistor, R_{FB1}, is used. Alternatively, very low values of adjustable gain resistors load the output of the sense amplifier limiting the capability of the sense amplifier to get close to the supply rail. Keeping the sum of external resistors R_{FB1} and R_{FB2} between 10kΩ and 40kΩ is recommended when external adjustable gain is higher than 1. 表 6-1 shows recommended values of external gain resistors for the most common gains.

表 6-1. Recommended Values of External Resistors Setting Adjustable Gain

External Adjustable Gain	R_{FB1}	R_{FB2}	Total Gain (G)
1	0Ω (short)	Open	40mV/A
2	20kΩ	20kΩ	80mV/A
4	30kΩ	10kΩ	160mV/A
5	20kΩ	5kΩ	200mV/A

6.4.2.1 Adjustable Unity Gain

図 6-9 shows adjustable gain set to unity gain or 1. In this configuration OUT is connected to FB without any external resistor. This unity gain sets INA750x to default minimum gain of 40mV/A. 式 3 can be used to calculate the total gain of the system. The REF pin is connected to external reference based on needed output voltage setting as described in Adjusting the Output With the Reference Pin.

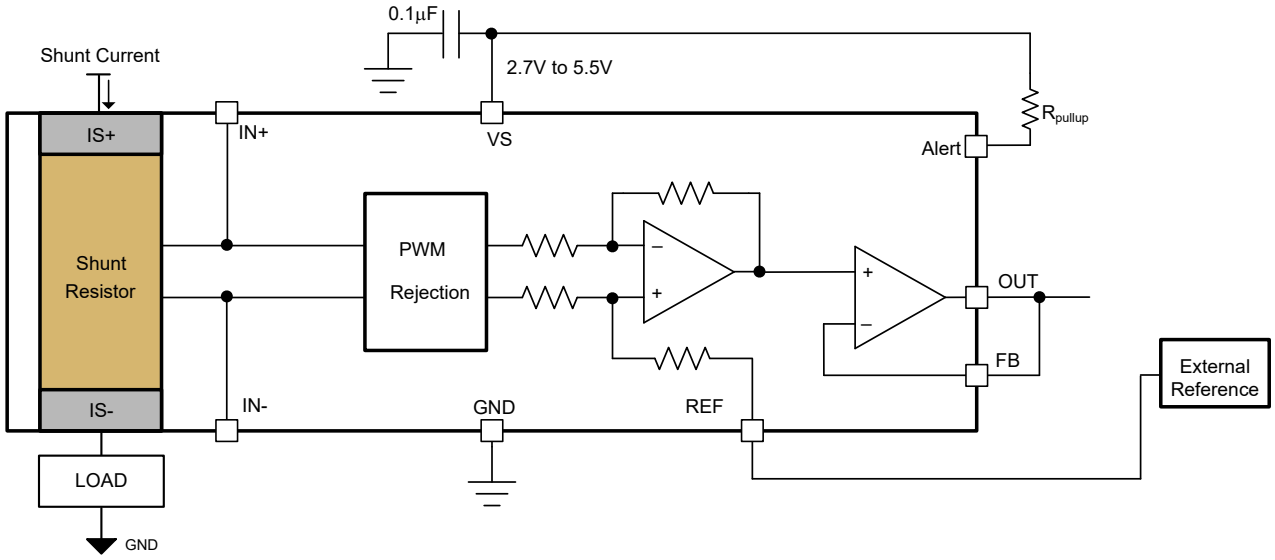


図 6-9. Adjustable Unity Gain Setting

6.4.3 Thermal Alert Function

The INA750x has thermal Alert function that provides an alert when internal shunt temperature reaches 160°C. The power dissipation as a result of internal shunt current causes the temperature to rise inside the package. Extended time at temperature higher than 150°C can cause permanent shift in device specification. Thermal alert function can be used to keep the temperature of INA750x below 150°C. 図 6-10 shows a circuit where R_{pullup} resistor is tied between open-drain Alert pin and the supply pin. When temperature of the INA750x reaches 160°C, the open-drain FET pulls Alert pin to the ground asserting thermal alert.

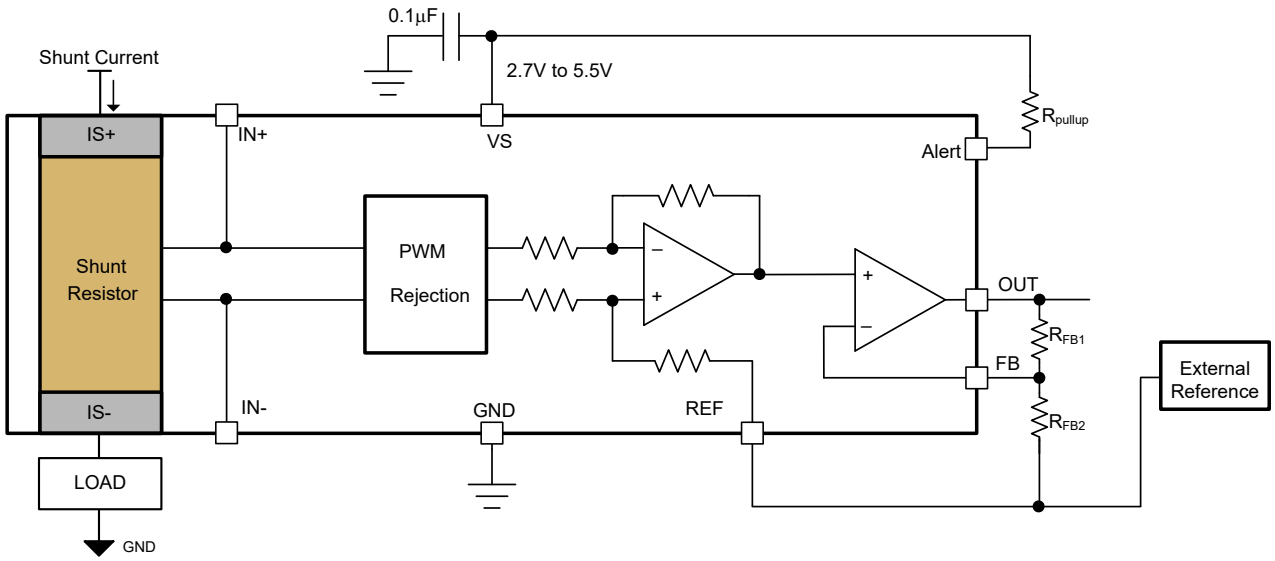


図 6-10. Thermal Alert Function

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The INA750x measures the voltage developed as current flows across the integrated current shunt. The device provides a reference pin to configure operation as either unidirectional or bidirectional output swing. When using the INA750x for inline motor current sense or measuring current in an H-bridge, the device is commonly configured for bidirectional operation.

7.1.1 Calculating Total Error

The INA750x electrical specifications セクション 5.5 include typical individual errors terms (such as gain error, offset error, and nonlinearity error). Total error, including all of these individual error components, is not specified in the table. To accurately calculate the expected error of the device, the user must first know the device operating conditions. This section discusses the individual error sources and how the device total error value can be calculated from the combination of these errors for specific conditions.

Three examples are provided in Total Error Example 1, Total Error Example 2, and Total Error Example 3 that detail how different operating conditions can affect the total error calculations. Typical and maximum calculations are shown as well to provide the user more information on how much error variance is present from device to device.

7.1.1.1 Error Sources

The typical error sources that have the largest effect on the total error of the device are gain error, nonlinearity, common-mode rejection ratio, and input offset error. For the INA750x , an additional error source (referred to as the *reference voltage rejection ratio*) is also included in the total error value.

7.1.1.2 Reference Voltage Rejection Ratio Error

Reference voltage rejection ratio refers to the amount of error induced by applying a reference voltage to the INA750x that deviates from the mid-point of the device supply voltage.

7.1.1.3 External Adjustable Gain Error

The INA750x features external adjustable gain with two external resistors as described in Adjustable Gain Set Using External Resistors. The tolerance of these external resistors contribute to the total gain error of the system. These resistors are recommended to be of same kind so that temperature drift of these resistor track closely. 式 4 can be used for calculating total error contributed by two external gain resistors.

$$Error_{G\_R} = \sqrt{2}*\left(Resistor_{Tolerance} + Resistor_{drift} \times \Delta\ T\right) \quad (4)$$

7.1.1.4 Total Error Example 1

表 7-1. Total Error Calculation: Example 1

TERM	SYMBOL	EQUATION(1)	MAX VALUE
Initial input offset with Temp drift	I_{OS_T}	$I_{OS} + \frac{dI_{os}}{dT} \times \Delta\ T$	15mA
Added input offset because of common-mode voltage	I_{OS_CM}	$CMRR \times \left\lvert (V_{CM} - 48\ V) \right\rvert$	0µA

表 7-1. Total Error Calculation: Example 1 (続き)

TERM	SYMBOL	EQUATION(1)	MAX VALUE
Added input offset because of reference voltage	I_{OS_REF}	$RVRR \times \left\lvert \left(\frac{V_S}{2} - V_{REF} \right) \right\rvert$	0µA
Total input offset Current	I_{OS_Total}	$\sqrt{(I_{OS\_T})^2 + (I_{OS\_CM})^2 + (I_{OS\_REF})^2}$	15mA
Error from input offset	$Error_{I_{OS}}$	$\frac{I_{OS\_Total}}{I_{Sense}} \times 100$	0.1%
Gain error with Gain drift	$Error_G$	$G_{Error} + G_{Error\_drift} \times \Delta T$	0.35%
Error due to Gain Nonlinearity	$Error_{Lin}$	$G_{Lin\_Error} \times I^2 * 100\%$	0.135%
Total error	—	$\sqrt{(Error_{I_{OS}})^2 + (Error_G + Error_{Lin})^2}$	0.495%

(1) The data for 表 7-1 is taken with the INA750x , V_S = 5V, V_{CM} = 48V, V_{REF} = V_S / 2, T = 25°C, External Unity Gain (G =40mV/A) and I_{SENSE} = 15A.

7.1.1.5 Total Error Example 2

表 7-2. Total Error Calculation: Example 2

TERM	SYMBOL	EQUATION(1)	MAX VALUE
Initial input offset with Temp drift	I_{OS_T}	$I_{OS} + \frac{dI_{os}}{dT} \times \Delta T$	55mA
Added input offset because of common-mode voltage	I_{OS_CM}	$CMRR \times \left\lvert (V_{CM} - 48V) \right\rvert$	1.4mA
Added input offset because of reference voltage	I_{OS_REF}	$RVRR \times \left\lvert \left(\frac{V_S}{2} - V_{REF} \right) \right\rvert$	15mA
Total input offset Current	I_{OS_Total}	$\sqrt{(I_{OS\_T})^2 + (I_{OS\_CM})^2 + (I_{OS\_REF})^2}$	57.2mA
Error from input offset	$Error_{I_{OS}}$	$\frac{I_{OS\_Total}}{I_{Sense}} \times 100$	0.381%
Gain error with Gain drift	$Error_G$	$G_{Error} + G_{Error\_drift} \times \Delta T$	0.7%
Error due to Gain Nonlinearity	$Error_{Lin}$	$G_{Lin\_Error} \times I^2 * 100\%$	0.135%
Total error	—	$\sqrt{(Error_{I_{OS}})^2 + (Error_G + Error_{Lin})^2}$	0.918%

(1) The data for 表 7-2 is taken with the INA750x , V_S = 5V, V_{CM} = 12V, V_{REF} = 0V, T = 125°C, External Unity Gain (G = 40mV/A) and I_{SENSE} = 15A.

7.1.1.6 Total Error Example 3

表 7-3. Total Error Calculation: Example 3

TERM	SYMBOL	EQUATION(1)	MAX VALUE
Initial input offset with Temp drift	I_{OS_T}	$I_{OS} + \frac{dI_{os}}{dT} \times \Delta T$	55mA
Added input offset because of common-mode voltage	I_{OS_CM}	$CMRR \times \left\lvert (V_{CM} - 48V) \right\rvert$	1.4mA
Added input offset because of reference voltage	I_{OS_REF}	$RVRR \times \left\lvert \left(\frac{V_S}{2} - V_{REF} \right) \right\rvert$	15.6mA
Total input offset Current	I_{OS_Total}	$\sqrt{(I_{OS\_T})^2 + (I_{OS\_CM})^2 + (I_{OS\_REF})^2}$	57.2mA

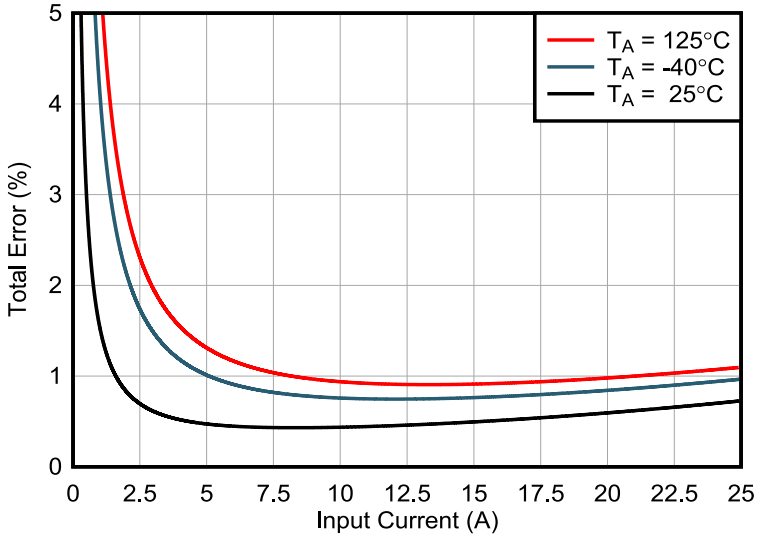
表 7-3. Total Error Calculation: Example 3 (続き)

TERM	SYMBOL	EQUATION(1)	MAX VALUE
Error from input offset	$Error_{I_{OS}}$	$\frac{I_{OS\_Total}}{I_{Sense}} \times 100$	0.381%
Gain error with Gain drift	$Error_G$	$G_{Error} + G_{Error\_drift} \times \Delta T$	0.7%
Error due to Gain Nonlinearity	$Error_{Lin}$	$G_{Lin\_Error} \times I^2 * 100\%$	0.135%
External Gain Resistor Error + Drift	$Error_{G\_R}$	式 4	0.707%
Total error	—	$\sqrt{(Error_{I_{OS}})^2 + (Error_{G\_R})^2 + (Error_G + Error_{Lin})^2}$	1.16%

(1) The data for *表 7-3* is taken with the INA750x , V_S = 5V, V_{CM} = 12V, V_{REF} = 0V, T = 125°C, External Gain = 4 (Total Gain = 160mV/A), External Resistor Tolerance = 0.25%, External Resistor Drift = 25ppm/°C and I_{SENSE} = 15A.

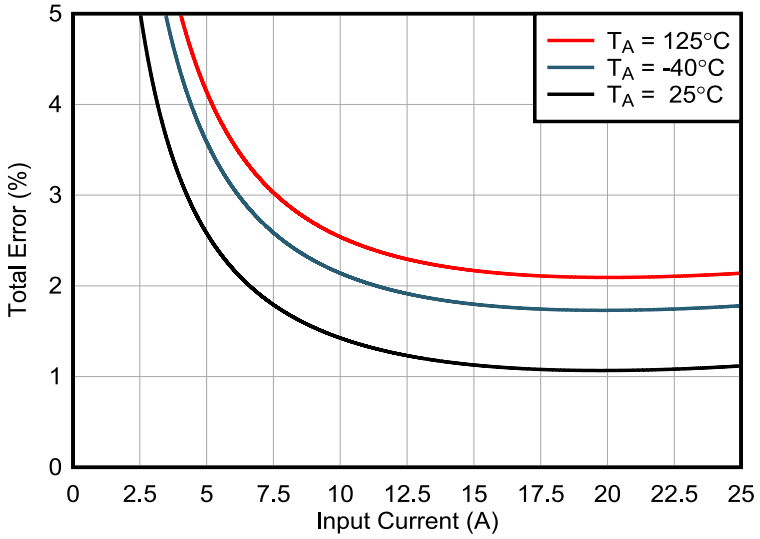
7.1.1.7 Total Error Curves

INA750A and INA750B Total Error Curve plots are generated using Total Error Examples for Adjustable Gain of 1 (unity gain).



V_{CM} = 48V, V_S = 5V, V_{REF} = 2.5V, Adjustable Gain = 1

図 7-1. INA750A Total Error vs Input Current



V_{CM} = 48V, V_S = 5V, V_{REF} = 2.5V, Adjustable Gain = 1

図 7-2. INA750B Total Error vs Input Current

7.2 Signal Filtering

Note that the integrated sensing element has inductance like all low-ohmic shunt resistors. Shunt inductance can lead to shunt voltage overshoots and AC gain peaking, which is undesirable if system requires linear and accurate current measurements when sensing small signal frequencies beyond 100kHz or when system can not tolerate overshoot from fast current step responses such as when comparators are tracking for fast overcurrent events. 図 7-3 shows INA750x shunt impedance vs frequency.

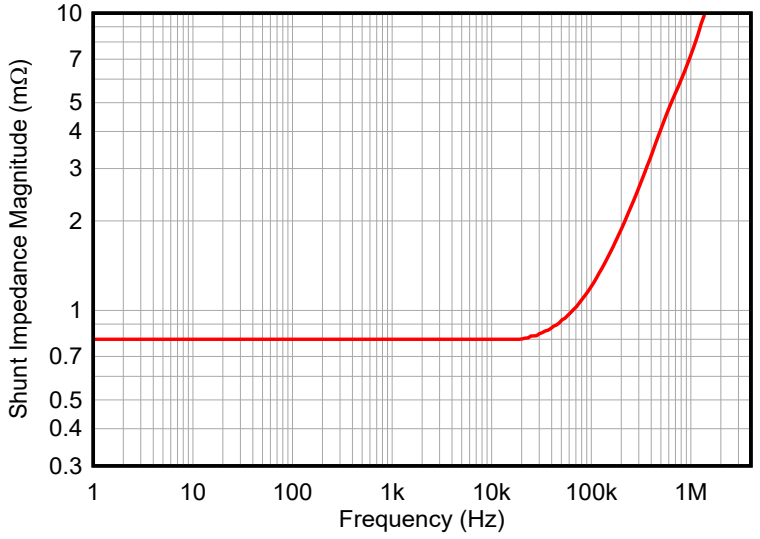


図 7-3. Shunt Impedance vs Frequency

Typically, inductance from low-Ohmic shunt resistors can be negated by adding a differential filter that creates a pole to flatten zero introduced from inductance. For the INA750x an internal short is provided from Kelvin sense connections to amplifier input to optimize noise, performance and quality. Thus, input resistance on these connections is very low and to apply an input filter, a capacitance between IN+ and IN- that is greater than 22µF is required. The filter capacitor must be placed as close as possible to IN+ and IN- pins. 図 7-4 shows gain response vs frequency with and without input filter capacitor.

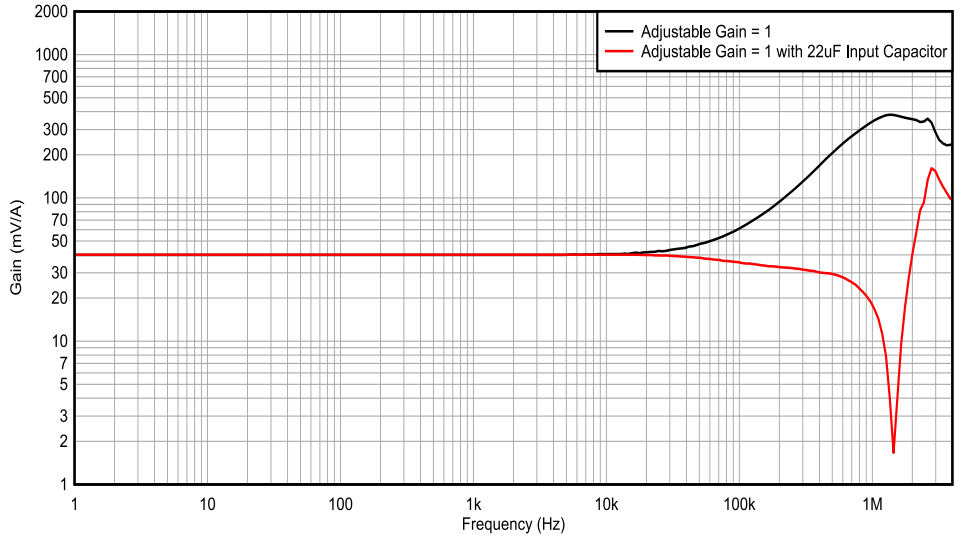


図 7-4. INA750x Gain vs Frequency Before and After Adding 22µF Input Capacitor

Another option to negate the shunt inductance is to introduce the zero in transfer function at the adjustable gain-setting output buffer with a circuit configuration referred to as a RISO Dual Feedback. This operational amplifier network provides a zero to cancel out shunt inductance without sacrificing overall bandwidth nor output impedance. 図 7-5 shows RISO Dual Feedback circuit configuration

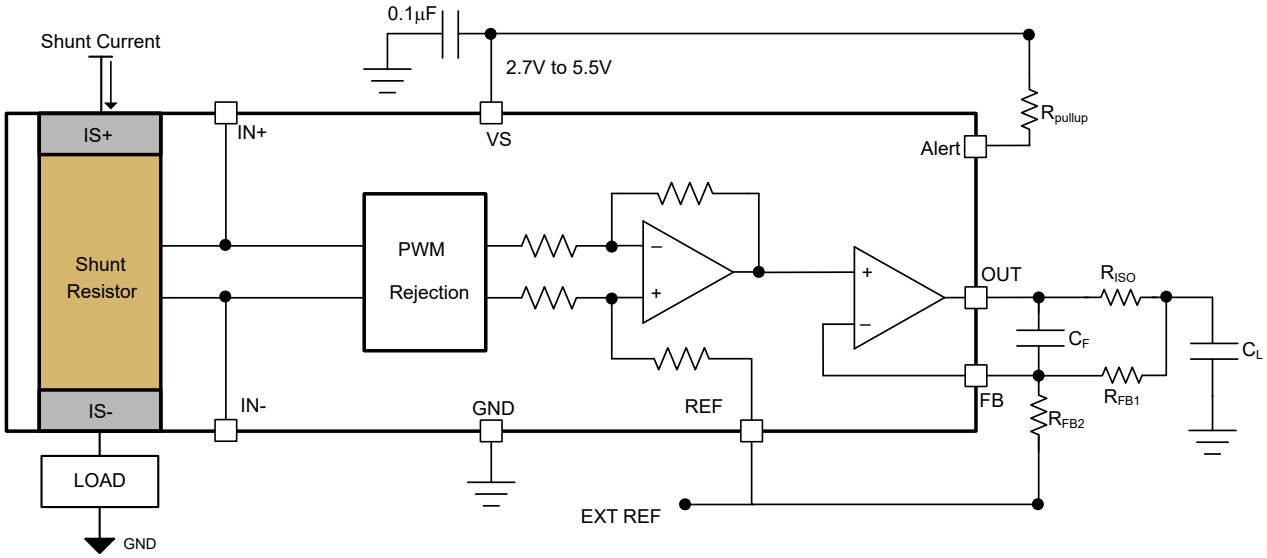


図 7-5. INA750x With RISO-Dual-Feedback

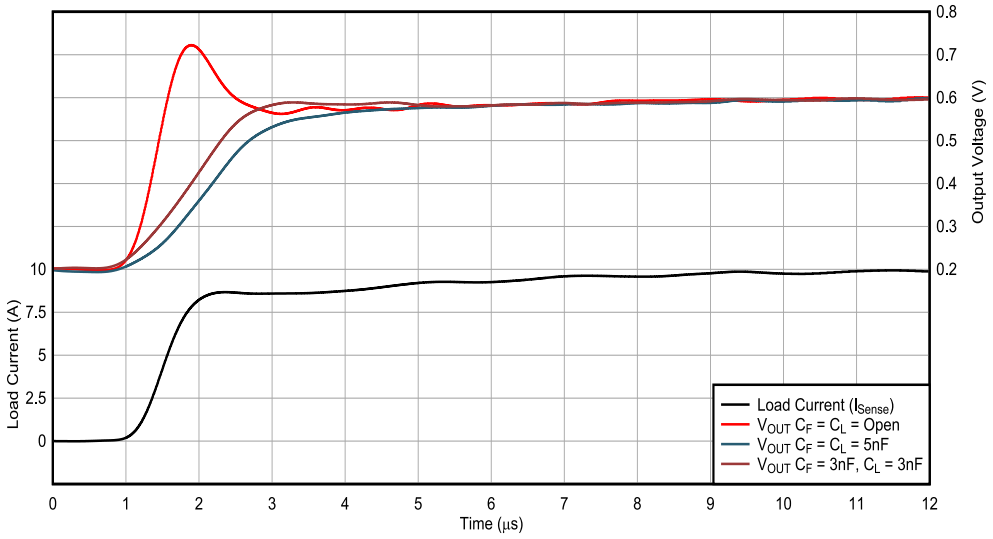
Based upon measured bandwidth and output impedance, 表 7-4 shows values for circuit components that can be used to achieve the circuit with the desired gain. Resistor tolerances under 2% is recommended. 図 7-6 and 図 7-7 show the load step responses with and without RISO Dual Feedback circuit with the component values in 表 7-4.

表 7-4. INA750x RISO Dual Feedback Values

Adjustable Gain	Total Gain (mV/A)	R_{FB1}	R_{FB2}	R_{ISO}	C_F	Min C_L
1	40	19.1kΩ	Open	200Ω	3nF	3nF
2	80	19.1kΩ	19.1kΩ	0Ω (Short)	50pF	Open
3	120	19.1kΩ	9.76kΩ	0Ω (Short)	50pF	Open

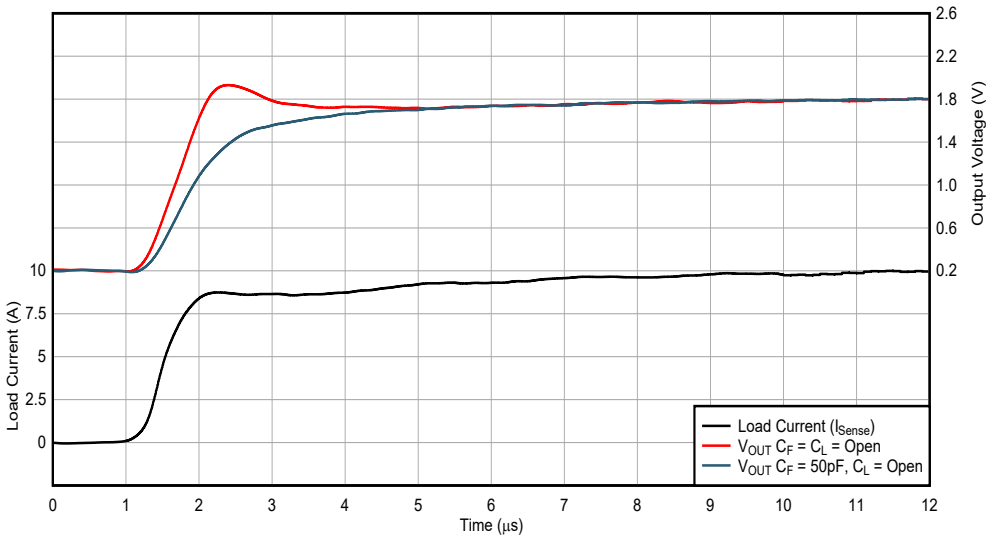
表 7-4. INA750x RISO Dual Feedback Values (続き)

Adjustable Gain	Total Gain (mV/A)	R_{FB1}	R_{FB2}	R_{ISO}	C_F	Min C_L
4	160	19.1kΩ	6.26kΩ	0Ω (Short)	50pF	Open
5	200	19.1kΩ	4.7kΩ	0Ω (Short)	50pF	Open



Adjustable Gain = 1, V_{CM} = 20V, V_S = 5V, V_{REF} = 0.2V

図 7-6. INA750x Load Step Responses Before and After RISO Dual Feedback for Adjustable Gain of 1



Adjustable Gain = 4, V_{CM} = 20V, V_S = 5V, V_{REF} = 0.2V

図 7-7. INA750x Load Step Responses Before and After RISO Dual Feedback for Adjustable Gain of 4

7.3 Typical Application

The INA750x offers advantages for multiple applications including the following:

- High common-mode range and excellent CMRR enables direct inline sensing
- Precision low-inductive, low-drift shunt eliminates the need for overtemperature system calibration

- Ultra-low offset and drift eliminates the necessity of calibration
- Wide supply range enables a direct interface with most microprocessors

7.3.1 High-Side, High-Drive, Solenoid Current-Sense Application

Challenges exist in solenoid drive current sensing that are similar to those in motor inline current sensing. In certain topologies, the current-sensing amplifier is exposed to the full-scale PWM voltage between ground and supply. The INA750x is an excellent choice for this type of application. The 800µΩ integrated shunt with a total system accuracy of 0.35% with a total system drift of 35ppm/°C provides system accuracy across temperature eliminating the need for system calibration at muliple temperatures.

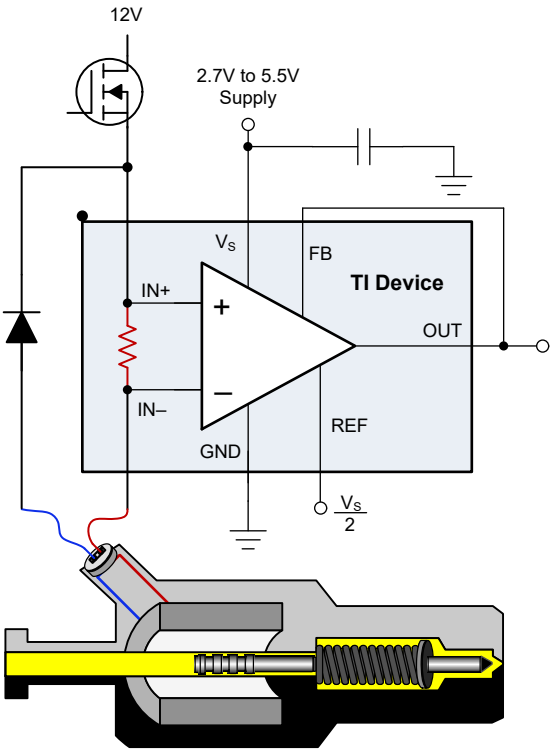


図 7-8. Solenoid Drive Application Circuit

7.3.1.1 Design Requirements

For this application, the INA750x measures current in the driver circuit of a 12V, 1A hydraulic valve.

表 7-5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Common-mode voltage	12V
Maximum sense current	1A
Power-supply voltage	5V

7.3.1.2 Detailed Design Procedure

To demonstrate the performance of the device, the INA750x , with total gain of 200mV/A, is selected for this design and powered from a 5V supply.

Using the information in *セクション 6.4.1.3*, the reference point is set to midscale by splitting the supply at mid point and connecting the REF.

7.3.1.3 Application Curve

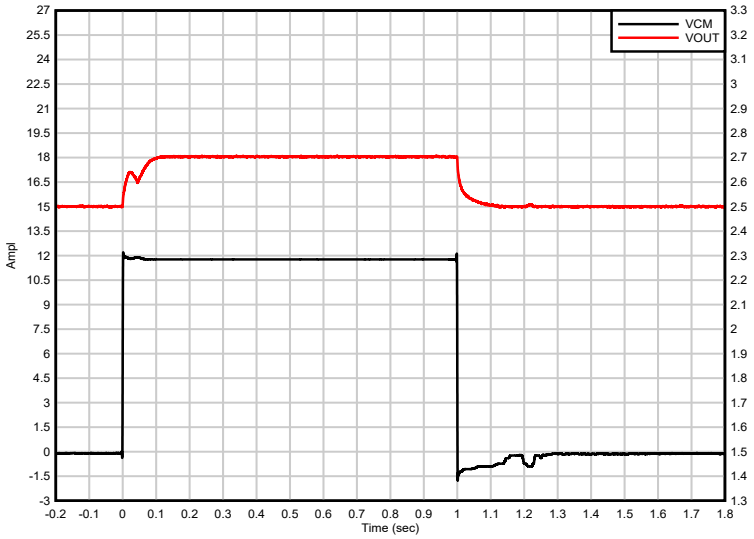


図 7-9. Solenoid Drive Current Sense Input and Output Signals

7.3.2 Speaker Enhancements and Diagnostics Using Current Sense Amplifier

CLASS-D audio amplifiers in conjunction with the INA750x provide accurate speaker load current. Speaker load current is used to determine speaker diagnostics, and can further be expanded to measure key speaker parameters, such as speaker coil resistance and speaker real-time ambient temperature.

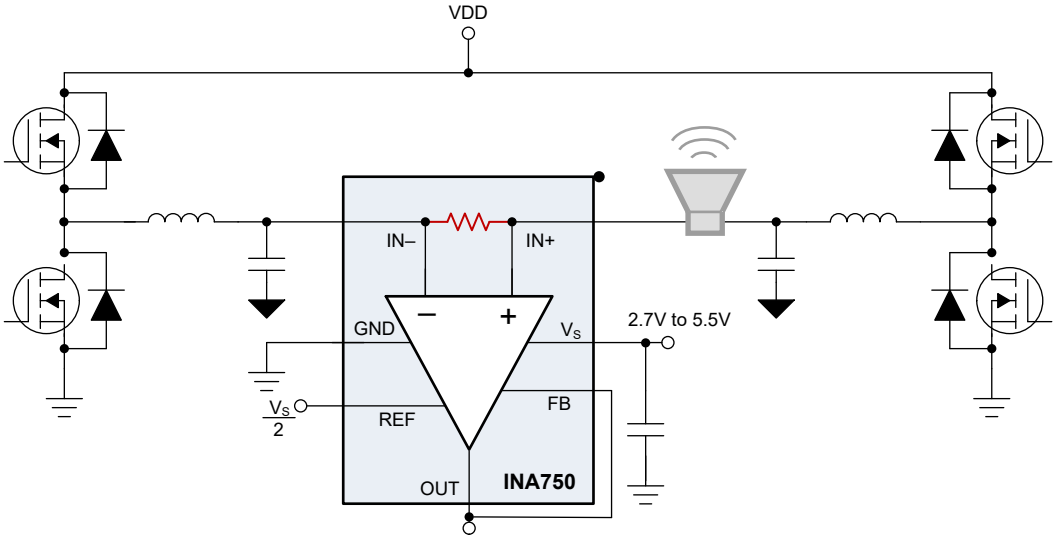


図 7-10. Current Sensing in a CLASS-D Subsystem

7.3.2.1 Design Requirements

表 7-6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Common-mode voltage	60V
Power-supply voltage	3.3V
Peak current	±15A
Frequency sweep	20Hz to 20kHz

7.3.2.2 Detailed Design Procedure

For this application, the INA750x measures current flowing through the speaker from the CLASS-D amplifier. The integrated shunt of 800µΩ with an inductance of only 2.5nH is an excellent choice for current sensing in speaker applications where low inductance is required. The low-inductive shunt enables accurate current sensing across frequencies over the audio range of 20Hz to 20kHz.

The INA750x is setup to support bidirectional currents with the reference set to mid-supply as shown in *セクション 6.4.1.4*. When the power supply to the INA750x is set at 3.3V and there is no current flowing in the speaker, the output of INA750x is at 1.65V. When operating with a gain of 80mV/A with peak-to-peak current of ±15A, the output of the INA750x swings from 0.45V to 2.85 V. In this application the output can be directly connected to an ADC input that has a full scale range of 3.3V. The INA750x can measure the impedance of the speaker and accurately measure the resonance frequency and peak impedance at resonance frequency. The INA750x can accurately track changes in the impedance in real-time.

7.3.2.3 Application Curves

図 7-11 shows the typical example output response of a speaker with 4Ω impedance measurement from 20Hz to 20kHz.

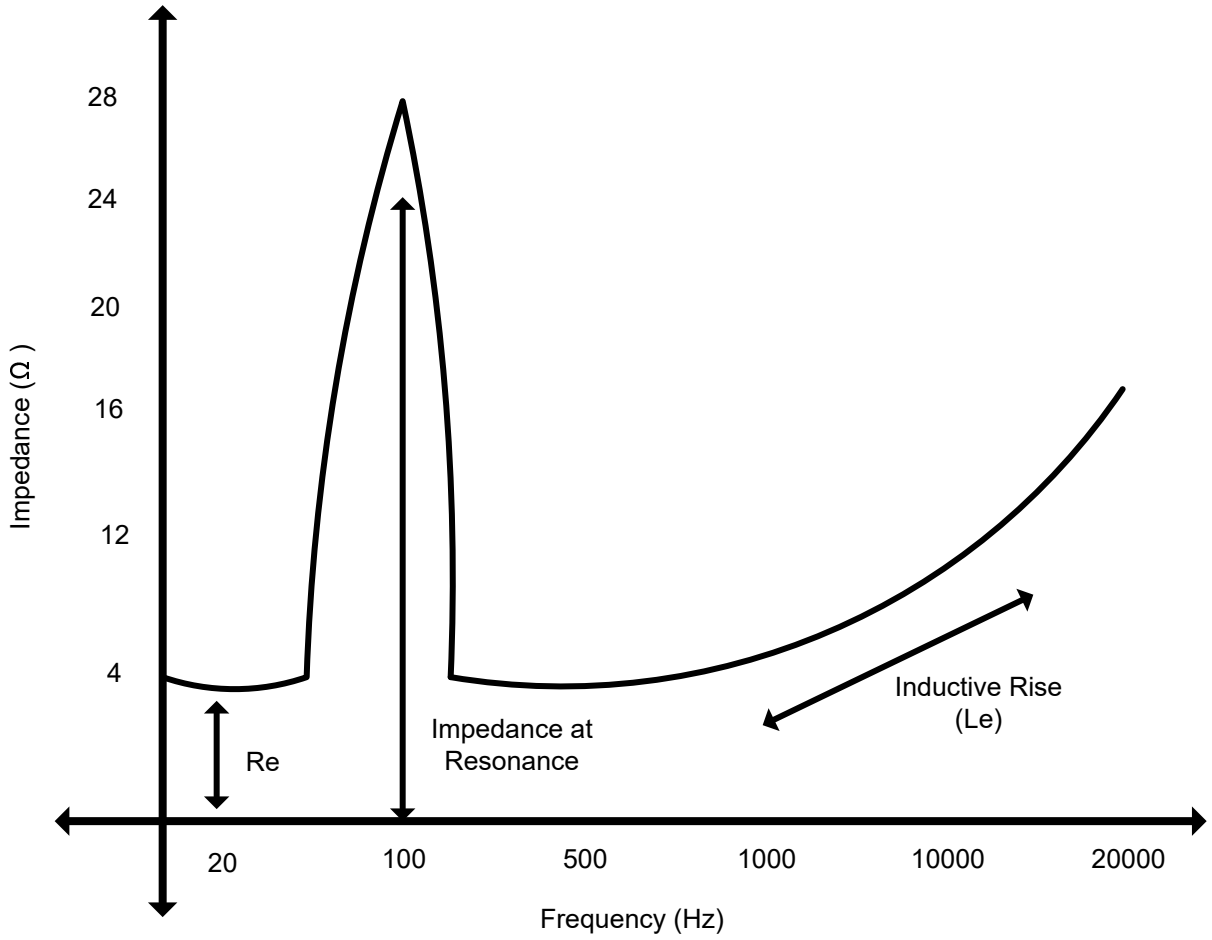


図 7-11. Speaker Impedance Measurement

7.4 Power Supply Recommendations

The INA750x makes accurate measurements beyond the connected power-supply voltage (VS) because the inputs (IN+ and IN–) operate anywhere between –4V and +110V, independent of VS. For example, the VS power supply equals 5V and the common-mode voltage of the measured shunt can be as high as 110V. Although the common-mode voltage of the input can be beyond the supply voltage, the output voltage range of the INA750x is constrained to the supply voltage.

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. If the INA750x output is set to mid-supply, then take extreme care to minimize noise on the power supply.

7.5 Layout

7.5.1 Layout Guidelines

- This device is specified for current handling of up to 25A over the entire –40°C to +125°C temperature range using a 2oz copper pour for the input power plane, as well as no external airflow passing over the device.

- The primary current-handling limitation for this device is how much heat is dissipated inside the package. Efforts to improve heat transfer out of the package and into the surrounding environment improve the ability of the device to handle currents of up to 25A over a wider temperature range.
- Heat transfer improvements primarily involve larger copper power traces and planes with increased copper thickness (2oz.), as well as providing airflow to pass over the device. Thermal vias help spread the current and power dissipated over multiple board layers. The INA750x evaluation module (EVM) features a 2oz copper pour for the planes, and is capable of supporting 25A at temperatures up to 125°C.
- The bypass capacitor must be placed close to device ground and supply pins, but can be moved farther out if needed to avoid cutting thermal planes. The recommended value of this bypass capacitor is 0.1µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

7.5.2 Layout Example

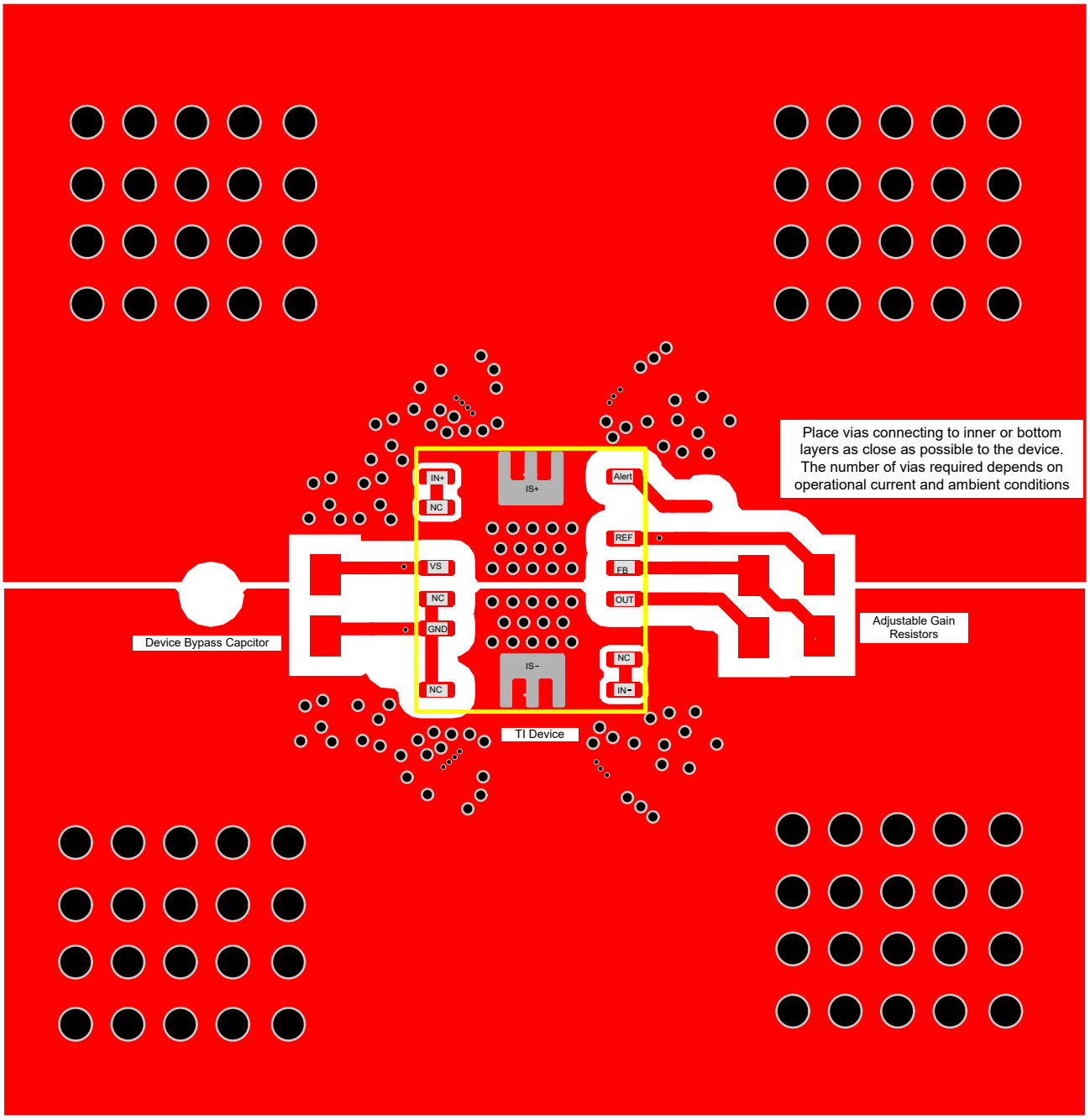


図 7-12. INA750x Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, INA75xEVM, EVM User's Guide

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.4 Trademarks

EZShunt™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

DATE	REVISION	NOTE
December 2024	*	Initial release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA750BIREMR	ACTIVE	VQFN	REM	14	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA 750B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

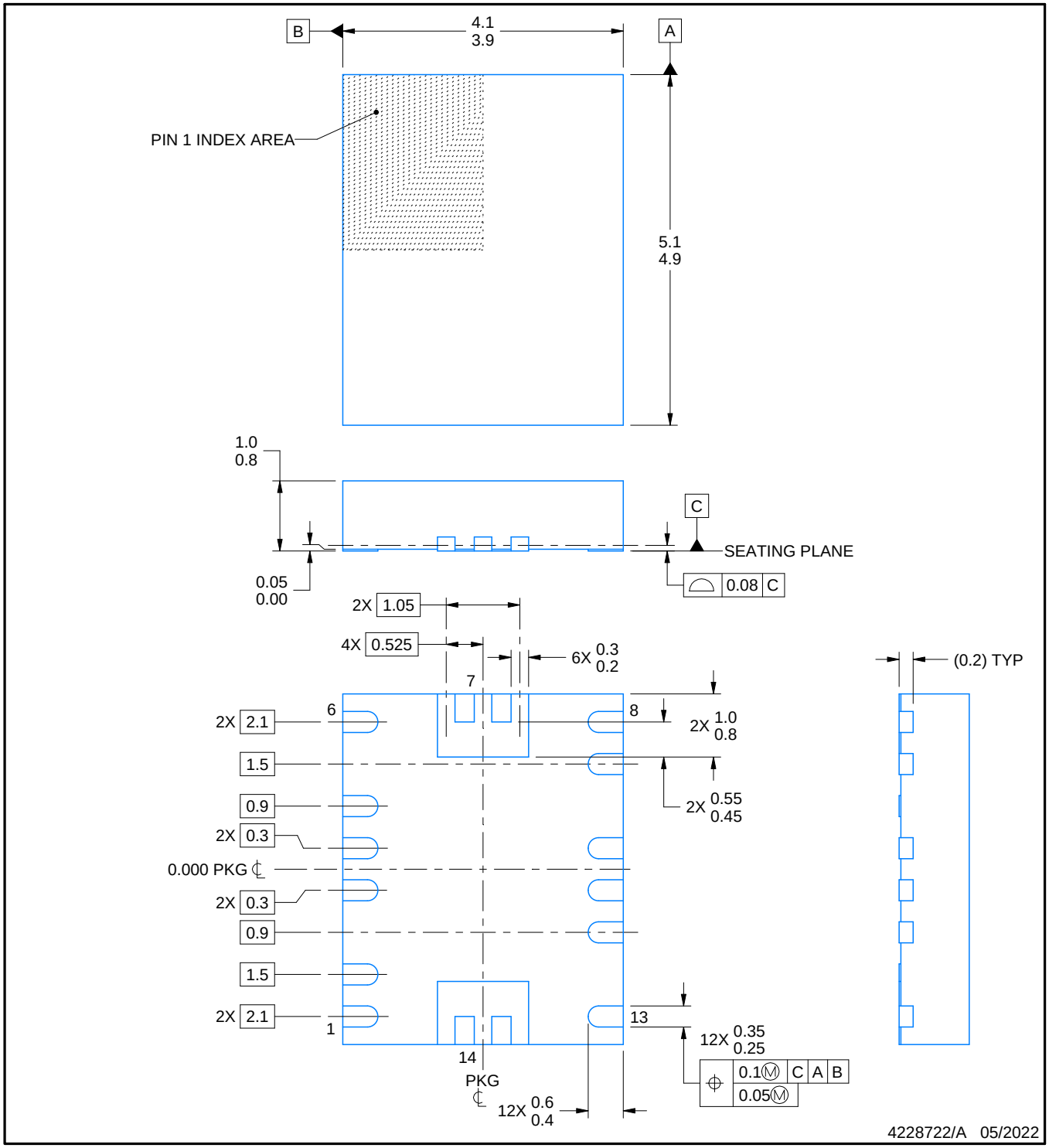
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

REM0014B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

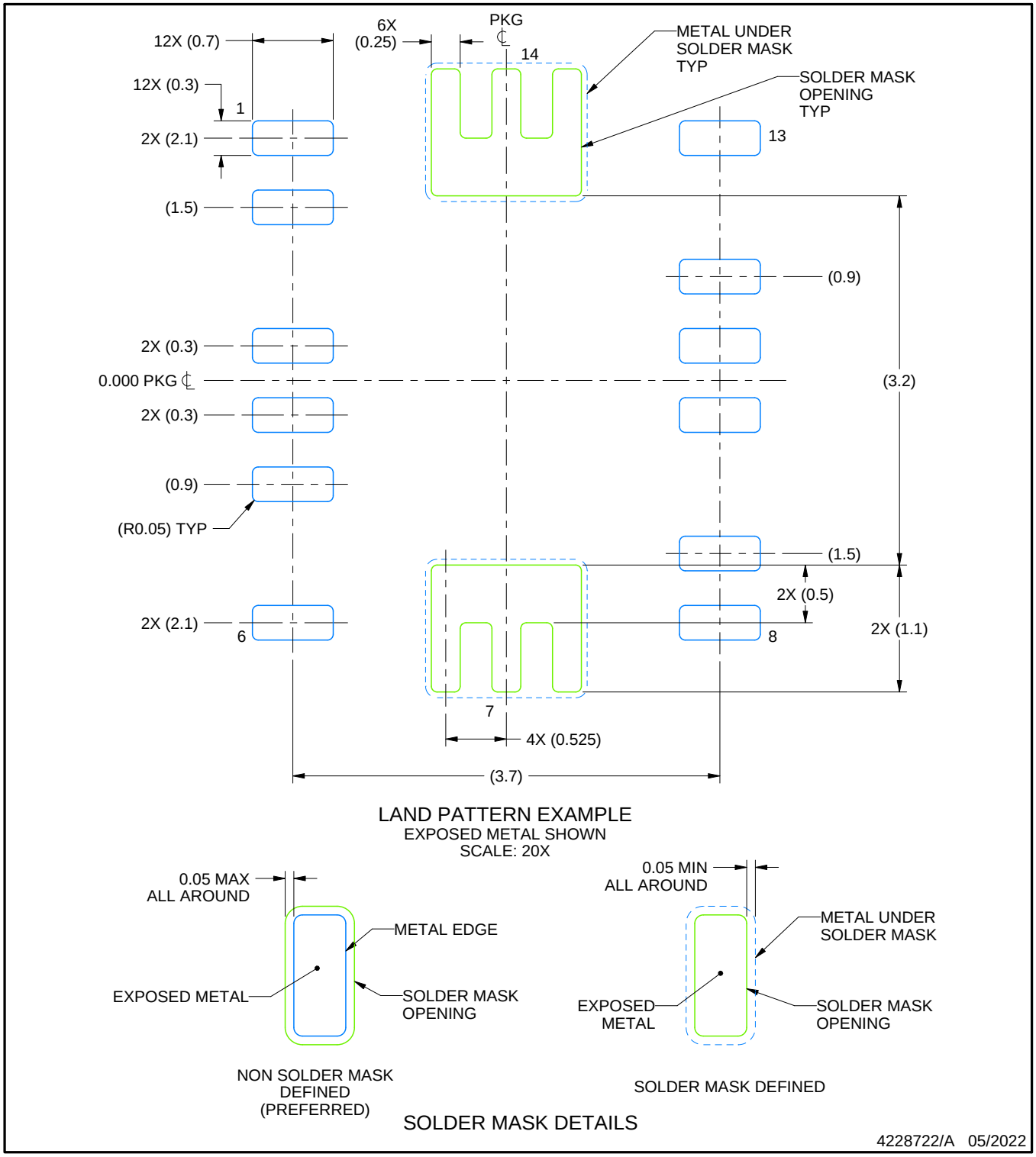
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

REM0014B

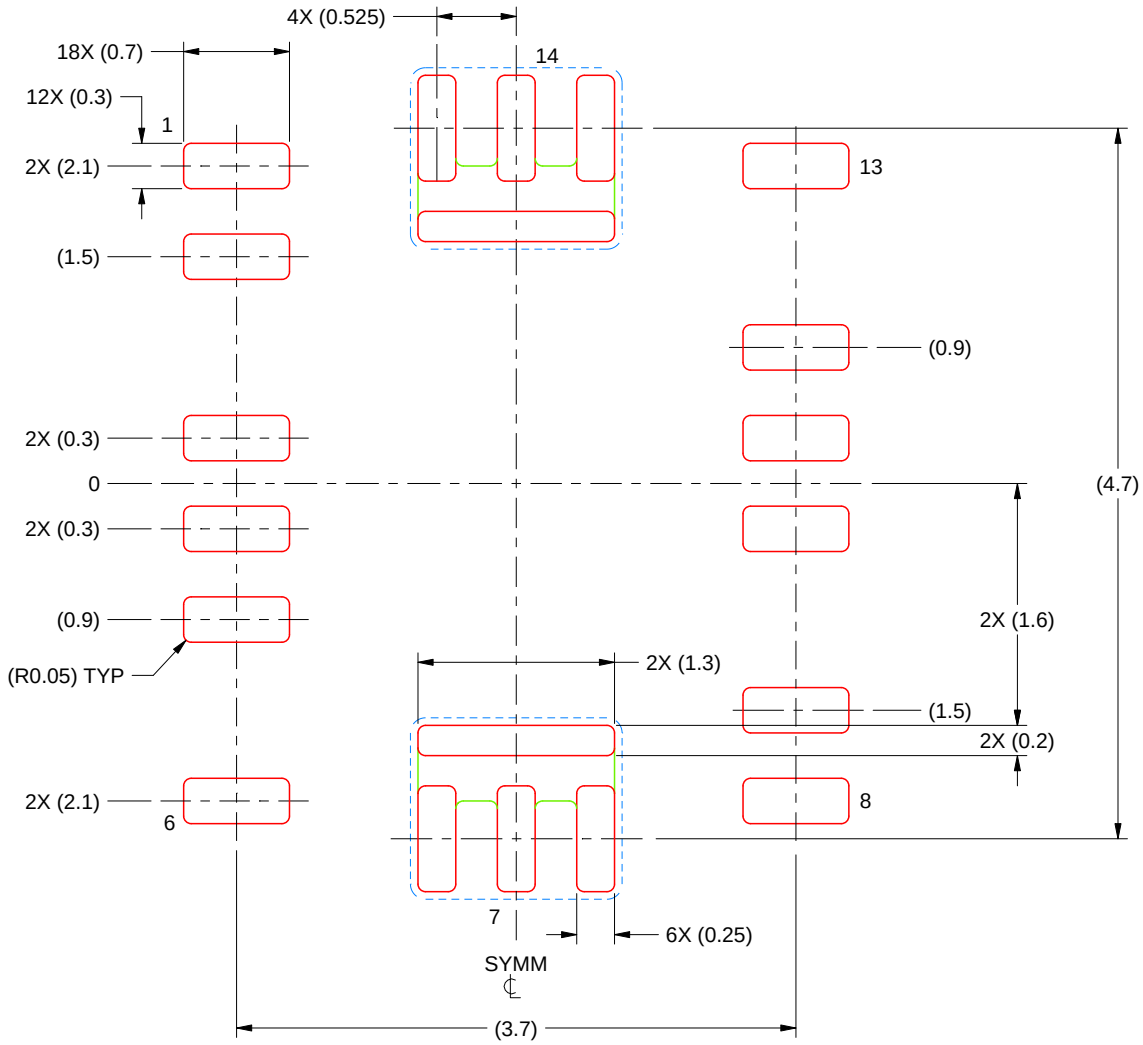
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4228722/A 05/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265