参考資料

Texas Instruments

INA823
JAJSLD8B – JULY 2021 – REVISED NOVEMBER 2021

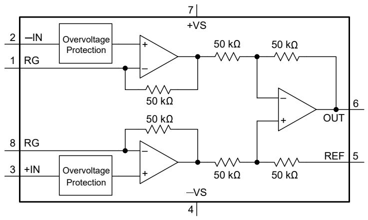
INA823 電源電圧範囲が広い (2.7V～36V) 低消費電力の高精度計装アンプ

1 特長

- 最大 ±60V の入力過電圧保護
- 負電源を 150mV 下回る電圧まで拡張された入力電圧
- 低消費電流：180μA (標準値)
- 高精度
  - 低いオフセット電圧：20μV (標準値)、100μV (最大値)
  - 低い入力バイアス電流：8nA (最大値)
  - 同相除去
    - 84dB、G = 1 (最小値)
    - 104dB、G = 10 (最小値)
    - 120dB、G = 100 (最小値)
  - 電源除去：100dB、G = 1 (最小値)
- 入力電圧ノイズ：21nV/$\sqrt{\text{Hz}}$
- 帯域幅：1.9MHz (G = 1)、60kHz (G = 100)
- 1nF の容量性負荷で安定
- 電源電圧範囲
  - 単一電源：2.7V～36V
  - デュアル電源：±1.35V～±18V
- 仕様温度範囲：–40℃～+125℃
- パッケージ：8 ピン SOIC、8 ピン VSSOP

2 アプリケーション

- 流量トランスミッタ
- ウェアラブル・フィットネスおよびアクティビティ・モニタ
- 点滴用ポンプ
- 血糖値測定器
- 心電図 (ECG)
- 外科用機器
- 重量計
- アナログ入力モジュール
- プロセス分析 (pH、ガス、濃度、力、湿度)
- バッテリ試験装置



INA823 の簡略化された内部回路図

3 概要

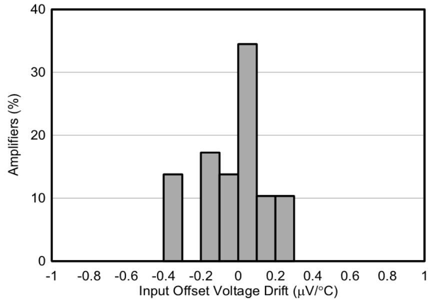
INA823 は、広い電圧範囲の単一電源またはデュアル電源で動作する低消費電力統合型計装アンプです。1 個の外付け抵抗により、1～10,000 の範囲で任意のゲインを設定できます。本デバイスは、低コストを維持しながら小さい入力オフセット電圧、小さいオフセット電圧ドリフト、小さい入力バイアス電流、小さい電流ノイズを実現しています。追加回路により、±60V までの過電圧から入力を保護します。

INA823 は、高い同相除去比を実現するよう最適化されています。G = 1 での同相除去比は、全入力同相範囲を通じて 84dB を上回ります。INA823 は、負電源を 150mV 下回る電圧までの広い同相電圧範囲を実現しています。本デバイスは、2.7V の単一電源による低電圧動作と最大 ±18V のデュアル電源による動作のために設計されています。この低消費電力と単一電源動作はハンドヘルドのバッテリ駆動システムに最適です。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
INA823	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00m × 3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



入力段のオフセット電圧ドリフトの代表的な分布

English Data Sheet: SBOSA75

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4 Revision History

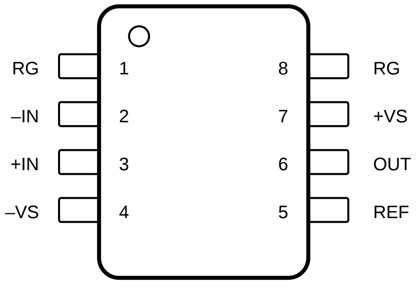
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (April 2019) to Revision B (November 2021)	Page
• デバイスを事前情報 (プレビュー) から量産データ (アクティブ) に変更	1

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG AT PINS
INA849	1-nV/$\sqrt{\text{Hz}}$ Noise, 35-µV Offset, 0.4 µV/°C V_{OS} Drift, 28-MHz Bandwidth, Precision Instrumentation Amplifier	G = 1 + 6 kΩ / RG	2, 3
INA821	35-µV Offset, 0.4 µV/°C V_{OS} Drift, 7-nV/$\sqrt{\text{Hz}}$ Noise, High-Bandwidth, Precision Instrumentation Amplifier	G = 1 + 49.4 kΩ / RG	2, 3
INA819	35-µV Offset, 0.4 µV/°C V_{OS} Drift, 8-nV/$\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	2, 3
INA826	200-µA Supply Current, 3-V to 36-V Supply Instrumentation Amplifier With Rail-to-Rail Output	G = 1 + 49.4 kΩ / RG	2, 3
INA818	35-µV Offset, 0.4 µV/°C V_{OS} Drift, 8-nV/$\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	1, 8
INA828	50-µV Offset, 0.5 µV/°C V_{OS} Drift, 7-nV/$\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	1, 8
INA333	25-µV V_{OS}, 0.1 µV/°C V_{OS} Drift, 1.8-V to 5-V, RRO, 50-µA I_Q, Chopper-Stabilized INA	G = 1 + 100 kΩ / RG	1, 8
PGA280	1/8 V/V to 128 V/V Programmable Gain Instrumentation Amplifier With 3-V or 5-V Differential Output; Analog Supply up to ±18 V	Digital programmable	N/A
INA159	G = 0.2 V Differential Amplifier for ±10-V to 3-V and 5-V Conversion	G = 0.2 V/V	N/A
PGA112	Precision Programmable Gain Op Amp With SPI	Digital programmable	N/A

6 Pin Configuration and Functions



Not to scale

図 6-1. D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN	2	Input	Negative (inverting) input
+IN	3	Input	Positive (noninverting) input
OUT	6	Output	Output
REF	5	Input	Reference input. This pin must be driven by a low impedance source.
RG	1, 8	—	Gain setting pin. Place a gain resistor between pin 1 and pin 8.
–VS	4	Power	Negative supply
+VS	7	Power	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	–VS, +VS pins voltage	Dual supply, $V_S = (+V_S) – (–V_S)$		± 20	V
		Single supply, $V_S = (+V_S)$		40	
	IN pins voltage		$(–V_S) – 60$	$(+V_S) + 60$	V
	RG, REF, OUT pins voltage		$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
	RG pins current		–10	10	mA
	OUT pin current		–50	50	mA
I_{SC}	Output short-circuit current(2)		Continuous		
T_A	Operating temperature		–50	150	°C
T_J	Junction temperature			175	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply, $V_S = (+V_S)$	2.7	36	V
		Dual supply, $V_S = (+V_S) – (–V_S)$	±1.35	±18	
T_A	Specified temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA823		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.7	167.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.0	60.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.1	88.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.6	7.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	69.4	87.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OSI}	Input stage offset voltage(1) (3)				20	100	μV
		T_A = –40°C to +125°C(2)				190	
					0.2	1.2	μV/°C
V_{OSO}	Output stage offset voltage(1) (3)				140	450	μV
		T_A = –40°C to +125°C(2)				850	
					1	5	μV/°C
PSRR	Power-supply rejection ratio	V_S = ±1.35 V to ±18 V	G = 1, RTI	100	130		dB
			G = 10, RTI	115	148		
			G = 100, RTI	120	148		
			G = 1000, RTI	120	148		
Z_{IN}	Input impedance				12 || 8.5		GΩ || pF
	RFI filter, –3-dB frequency				20		MHz
V_{CM}	Operating input voltage(4)	V_S = ±1.35 V to ±18 V		(–V_S) – 0.15		(+V_S) – 1	V
			T_A = –40°C to +125°C		See 図 7-53		
	Input overvoltage	T_A = –40°C to +125°C(2)				±60	V
CMRR	Common-mode rejection ratio	At dc to 60 Hz, RTI, V_{CM} = (V–) –0.15 V to (V+) – 1 V, G = 1		84	110		dB
		At dc to 60 Hz, RTI, V_{CM} = (V–) –0.15 V to (V+) – 1 V, G = 10		104	136		
		At dc to 60 Hz, RTI, V_{CM} = (V–) –0.15 V to (V+) – 1 V, G ≥ 100		120	149		
BIAS CURRENT							
I_B	Input bias current				1.2	8	nA
		T_A = –40°C to +125°C			2.4		
					15		pA/°C
I_{OS}	Input offset current				0.4	4	nA
		T_A = –40°C to +125°C			0.8		
					4		pA/°C
NOISE VOLTAGE							
e_{NI}	Input stage voltage noise density(6)	f = 1 kHz, G = 1000, R_S = 0 Ω			21		nV/√Hz
	Input stage voltage noise(6)	f_B = 0.1 Hz to 10 Hz, G = 1000, R_S = 0 Ω			0.4		μV_{PP}
e_{NO}	Output stage voltage noise density(6)	f = 1 kHz, R_S = 0 Ω			120		nV/√Hz
	Output stage voltage noise(6)	f_B = 0.1 Hz to 10 Hz, R_S = 0 Ω			5		μV_{PP}
i_n	Current noise density	f = 1 kHz			160		fA/√Hz
	Current noise	f_B = 0.1 Hz to 10 Hz, G = 100			5		pA_{PP}

7.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GAIN							
	Gain equation				1 + (100 kΩ / R_G)		V/V
G	Gain			1		10000	V/V
GE	Gain error[5]	V_O = ±10 V	G = 1		±0.01	±0.04	%
			G = 10		±0.025	±0.2	
			G = 100		±0.025	±0.2	
			G = 1000		±0.05	±0.2	
	Gain drift[5]	T_A = –40°C to +125°C	G = 1		±0.2	±5	ppm/°C
			G > 1		±12	±35	
	Gain nonlinearity	G = 1 to 10			2	10	ppm
		G > 10			5		
		G = 1 to 100, R_L = 2 kΩ			15		
OUTPUT							
	Output voltage swing			$(–V_S)$ + 0.15		$(+V_S)$ – 0.15	V
	Load capacitance	Stable operation			1000		pF
Z_{OUT}	Closed-loop output impedance				See 図 7-37		Ω
I_{SC}	Short-circuit current	Continuous to V_S / 2			±20		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 1			1.9		MHz
		G = 10			350		kHz
		G = 100			60		
		G = 1000			6		
SR	Slew rate	G = 1, V_O = ±10 V			0.9		V/μs
t_S	Settling time	To 0.01%	G = 1 to 10, V_{STEP} = 10 V		12		μs
			G = 100, V_{STEP} = 10 V		28		
			G = 1000, V_{STEP} = 10 V		260		
		To 0.001%	G = 1 to 10, V_{STEP} = 10 V		14		
			G = 100, V_{STEP} = 10 V		33		
			G = 1000, V_{STEP} = 10 V		290		
REFERENCE INPUT							
R_{IN}	Input impedance				100		kΩ
	Reference input voltage			$(–V_S)$		$(+V_S)$	V
	Gain to output				1		V/V
	Reference gain error	inside the output voltage swing			0.01	0.05	%
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0 V			180	250	μA
			T_A = –40°C to +125°C			300	

(1) Total offset, referred-to-input (RTI): $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$.
(2) Specified by characterization.
(3) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}{}^2 + (\Delta V_{OSO} / G)^2]}$.
(4) Input voltage range of the instrumentation amplifier input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves for more information.
(5) The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.
(6) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}{}^2 + (e_{NO} / G)^2]}$.

7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)

表 7-1. Table of Graphs

FIGURE TITLE	FIGURE NUMBER
Typical Distribution Graphs	
Typical Distribution of Input Stage Offset Voltage	Figure 7-1
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Typical Distribution of Output Stage Offset Voltage	Figure 7-3
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7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)

表 7-1. Table of Graphs (continued)

FIGURE TITLE	FIGURE NUMBER
Input and Output Voltage Graphs	
Input Current vs Input Overvoltage	Figure 7-38
Gain Nonlinearity, G = 1	Figure 7-39
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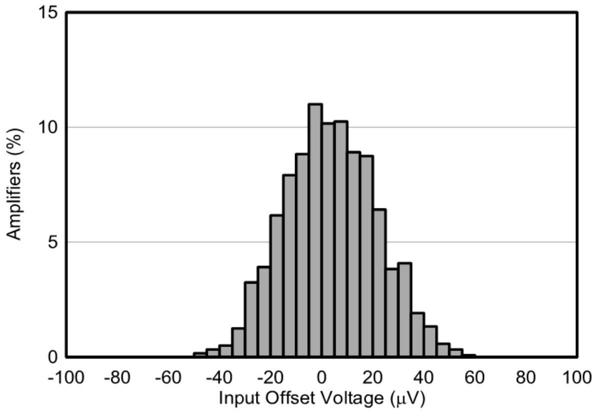
Input Common-Mode Voltage vs Output Voltage, V_S = 5 V, G = 100	Figure 7-56
Input Common-Mode Voltage vs Output Voltage, V_S = 24 V and V_S = 30 V, G = 1	Figure 7-57
Input Common-Mode Voltage vs Output Voltage, V_S = 24 V and V_S = 30 V, G = 10	Figure 7-58

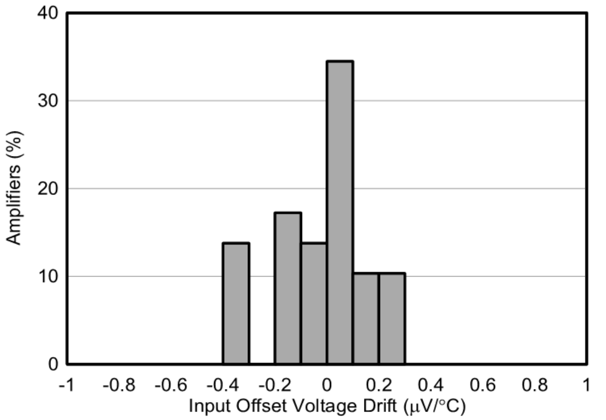
7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)



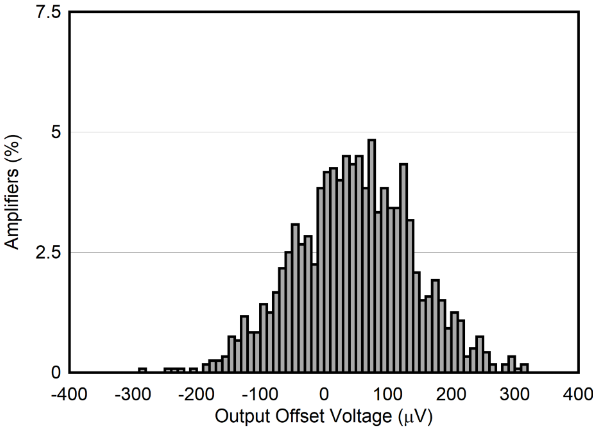
N = 1225 Mean = 3.63 µV Std Dev = 18.0 µV

図 7-1. Typical Distribution of Input Stage Offset Voltage



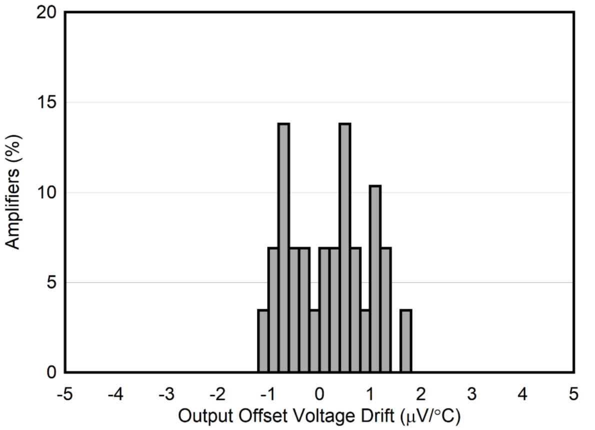
N = 30 Mean = –0.024 µV/ºC Std Dev = 0.177 µV//ºC

図 7-2. Typical Distribution of Input Stage Offset Voltage Drift



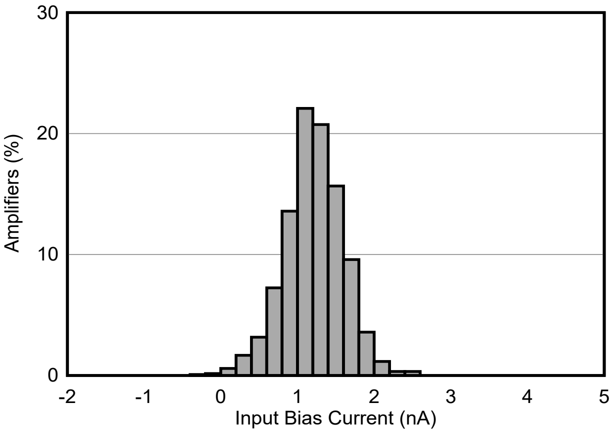
N = 1225 Mean = 48.0 µV Std Dev = 92.4 µV

図 7-3. Typical Distribution of Output Stage Offset Voltage



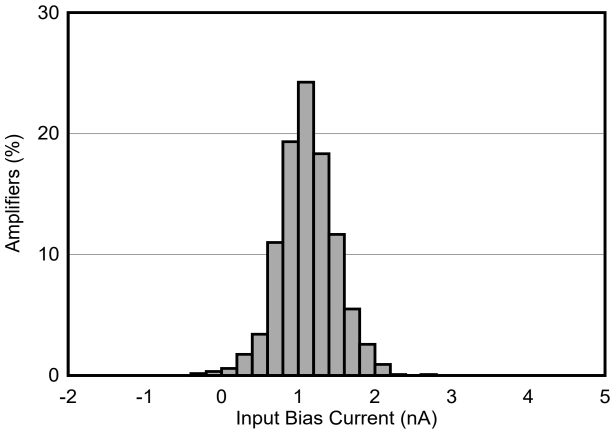
N = 30 Mean = 0.17 µV/ºC Std Dev = 0.795 µV/ºC

図 7-4. Typical Distribution of Output Stage Offset Voltage Drift



N = 1200 Mean = 1.21 nA Std Dev = 0.384 nA

図 7-5. Typical Distribution of Inverting Input Bias Current

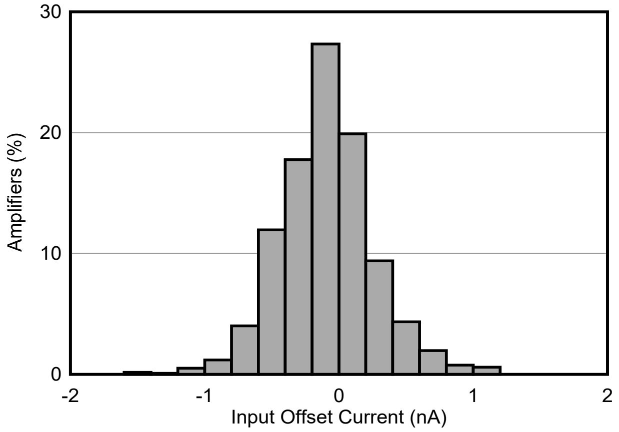


N = 1200 Mean = 1.11 nA Std Dev = 0.368 nA

図 7-6. Typical Distribution of Noninverting Input Bias Current

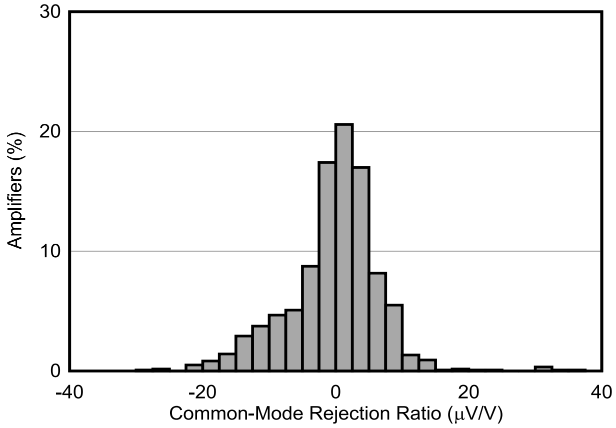
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)



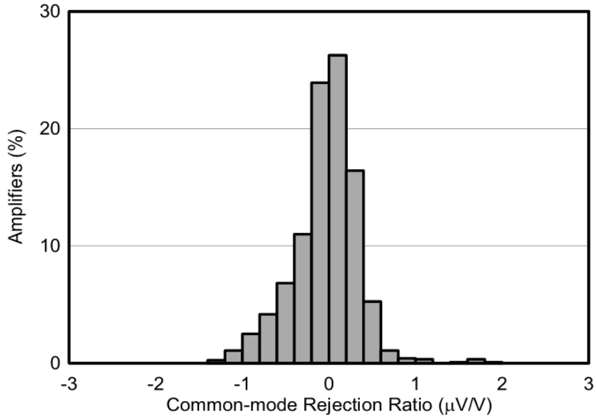
N = 1170 Mean = –0.092 nA Std Dev = 0.35 nA

図 7-7. Typical Distribution of Input Offset Current



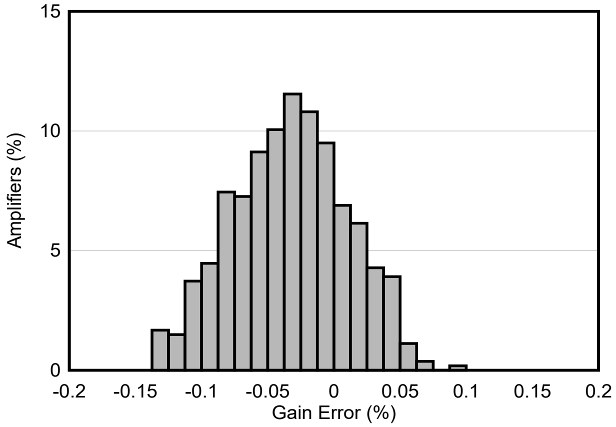
N = 1225 Mean = –0.22 µV/V Std Dev = 6.95 µV/V

図 7-8. Typical CMRR Distribution



N = 1225 Mean = –0.0599 µV/V Std. Dev = 0.710 µV/V
G = 10

図 7-9. Typical CMRR Distribution



N = 550 Mean = –0.0334 % Std. Dev = 0.0433 %
G = 10

図 7-10. Typical Gain Error Distribution

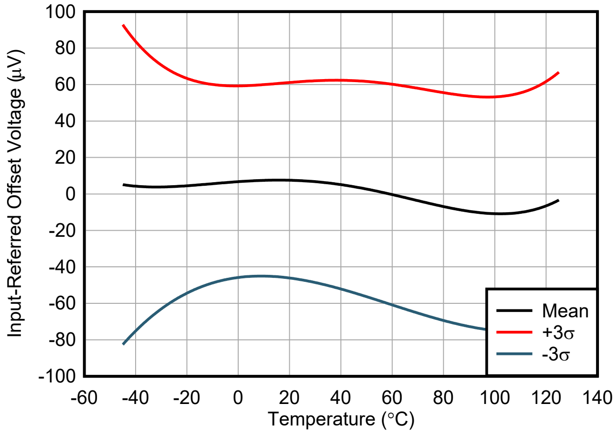


図 7-11. Input Stage Offset Voltage vs Temperature

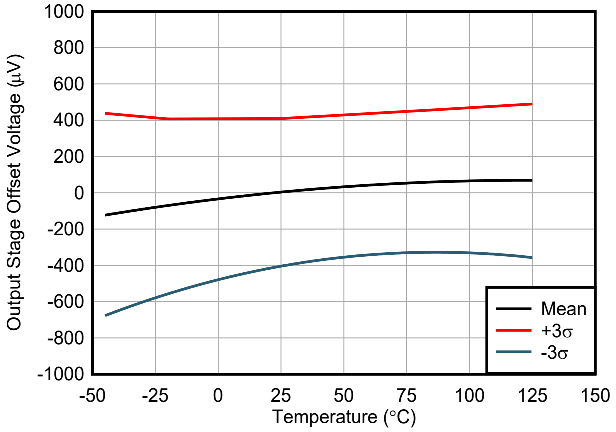


図 7-12. Output Stage Offset Voltage vs Temperature

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)

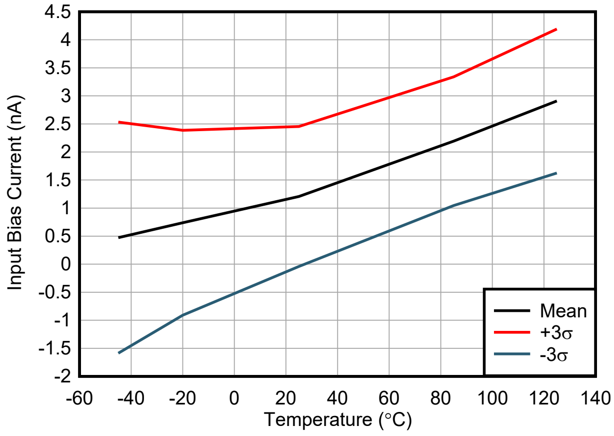


図 7-13. Input Bias Current vs Temperature

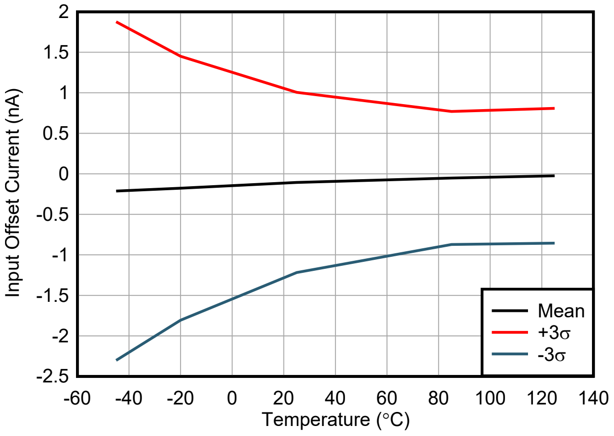
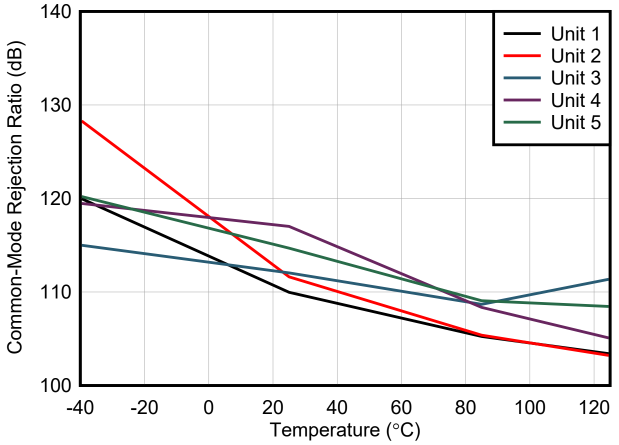
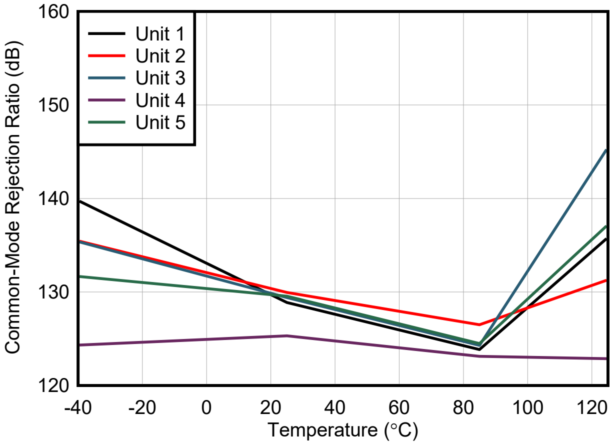


図 7-14. Input Offset Current vs Temperature



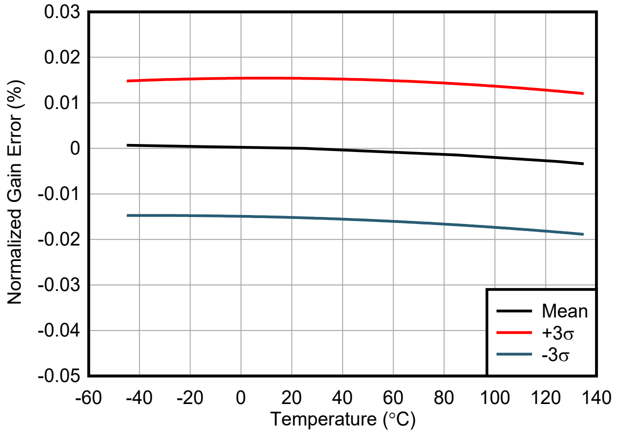
G = 1

図 7-15. CMRR vs Temperature



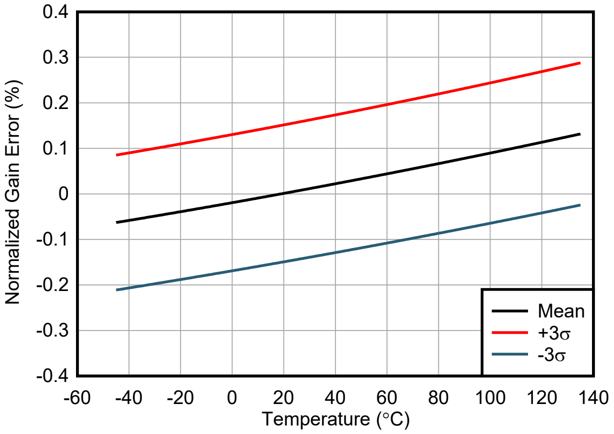
G = 10

図 7-16. CMRR vs Temperature



G = 1 Average of 120 units Normalized at +25°C

図 7-17. Gain Error vs Temperature



G = 100 Average of 120 units Normalized at +25°C

図 7-18. Gain Error vs Temperature

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)

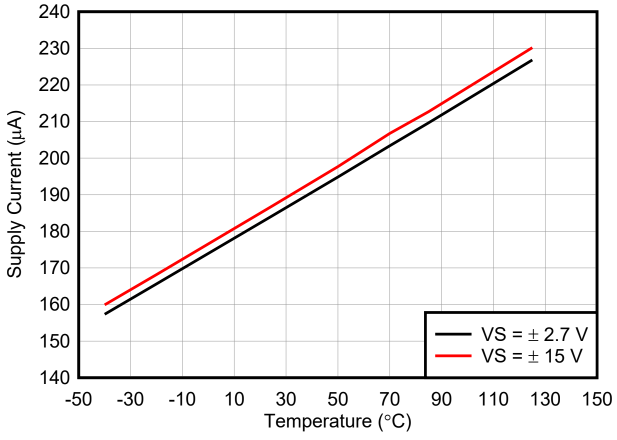


図 7-19. Supply Current vs Temperature

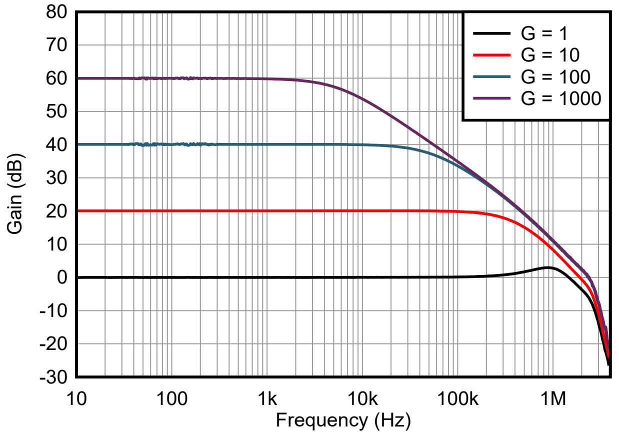


図 7-20. Closed-Loop Gain vs Frequency

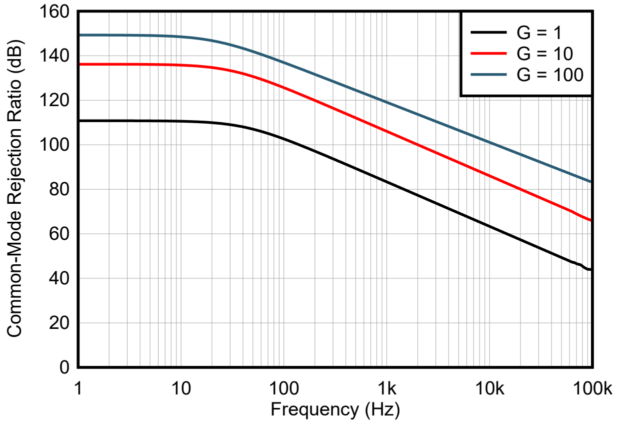


図 7-21. CMRR vs Frequency (RTI)

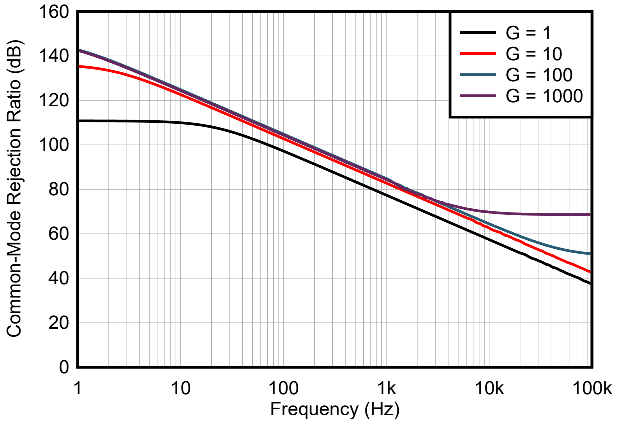


図 7-22. CMRR vs Frequency (RTI, 1-kΩ source imbalance)

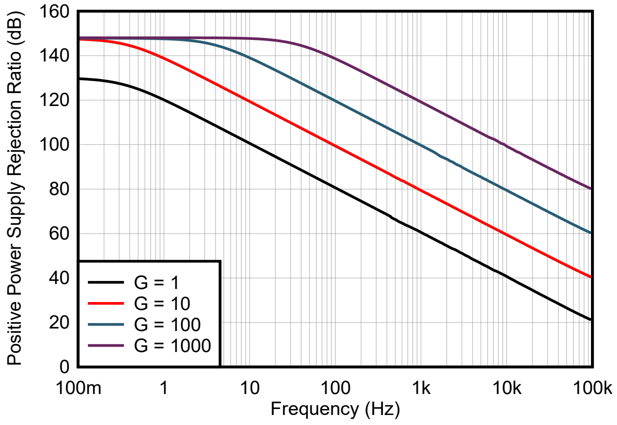


図 7-23. Positive PSRR vs Frequency (RTI)

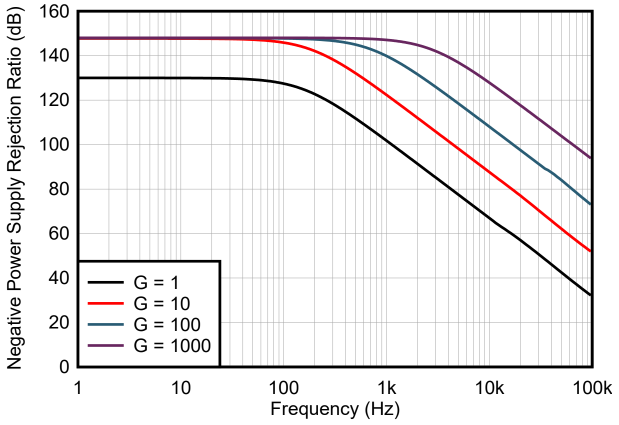


図 7-24. Negative PSRR vs Frequency (RTI)

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)

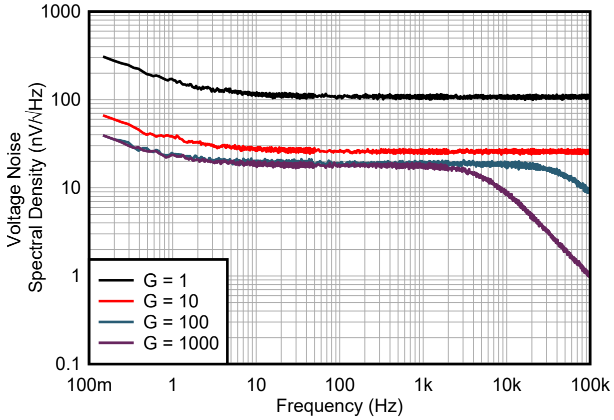


図 7-25. Voltage Noise Spectral Density vs Frequency (RTI)

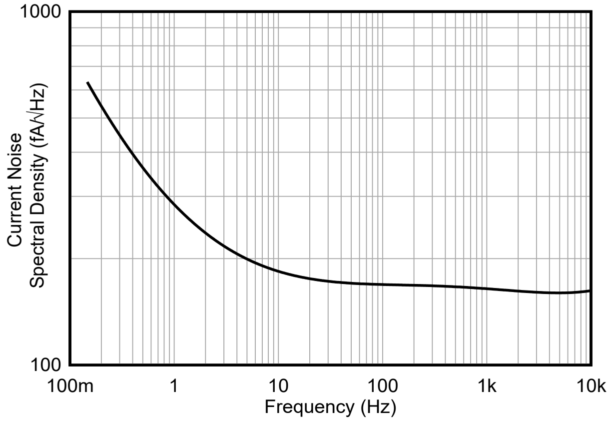


図 7-26. Current Noise Spectral Density vs Frequency (RTI)

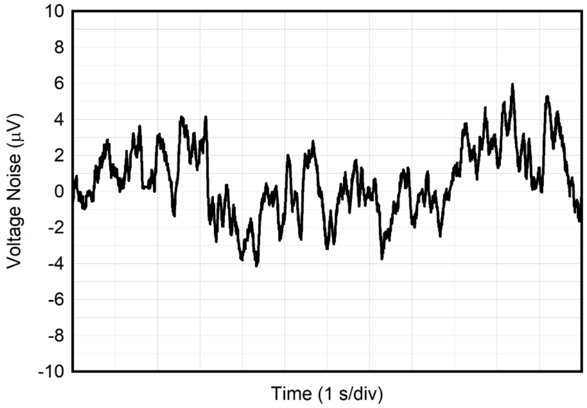


図 7-27. 0.1-Hz to 10-Hz RTI Voltage Noise

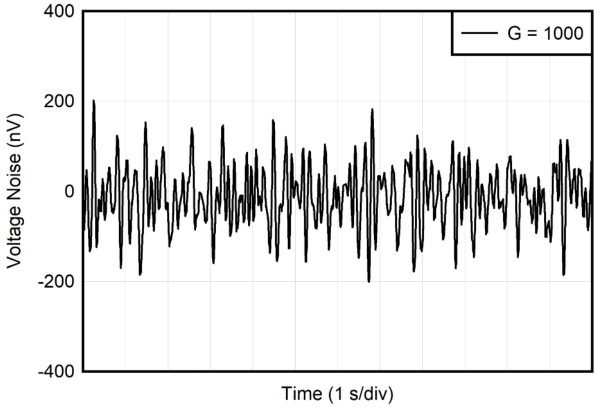
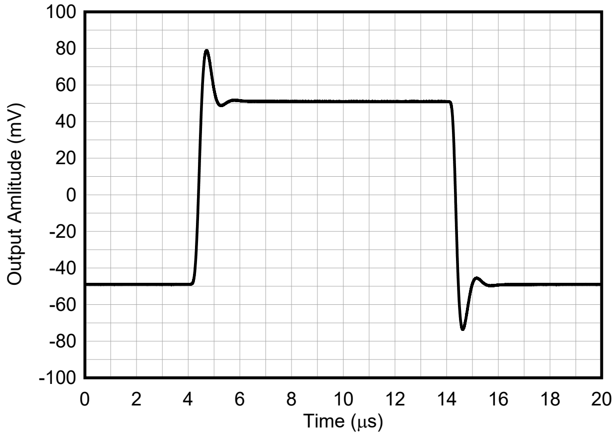
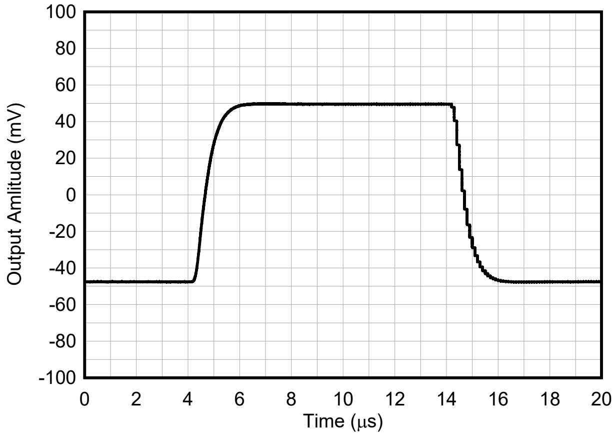


図 7-28. 0.1-Hz to 10-Hz RTI Voltage Noise



G = 1 R_L = 10 kΩ C_L = 100 pF

図 7-29. Small-Signal Response

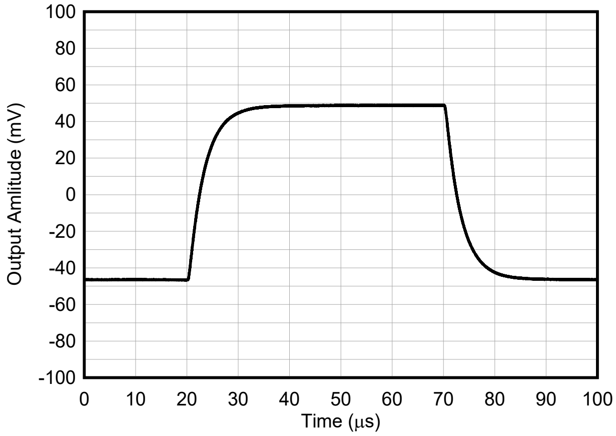


G = 10 R_L = 10 kΩ C_L = 100 pF

図 7-30. Small-Signal Response

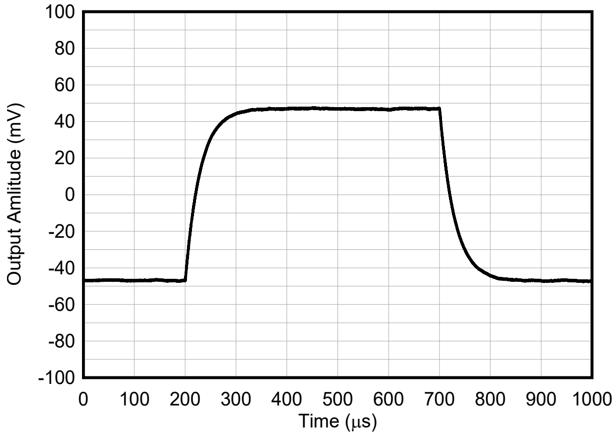
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)



G = 100 R_L = 10 kΩ C_L = 100 pF

図 7-31. Small-Signal Response



G = 1000 R_L = 10 kΩ C_L = 100 pF

図 7-32. Small-Signal Response

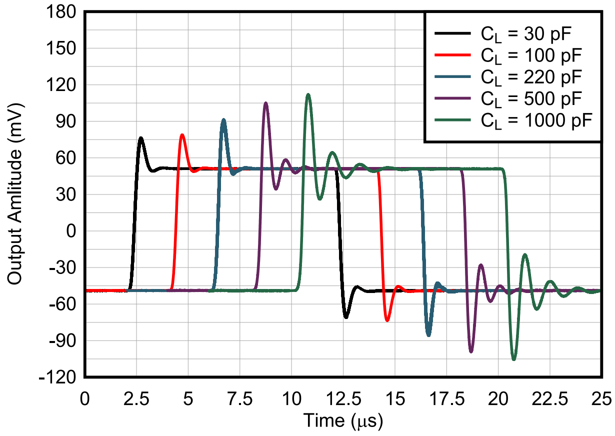


図 7-33. Overshoot vs Capacitive Loads

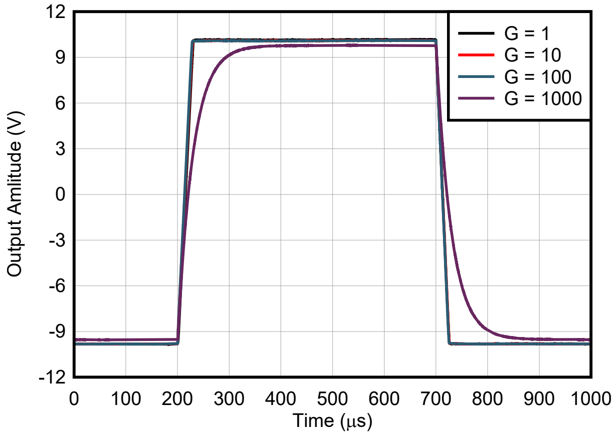


図 7-34. Large-Signal Step Response

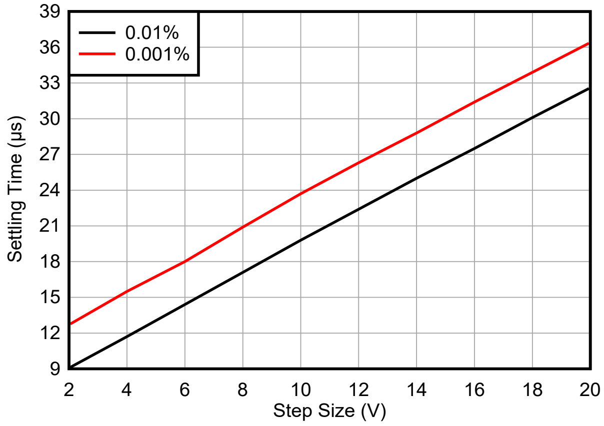


図 7-35. Settling Time vs Step Size

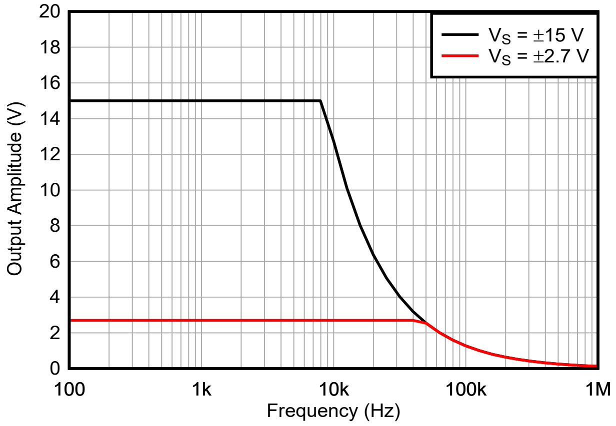


図 7-36. Large-Signal Frequency Response

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)

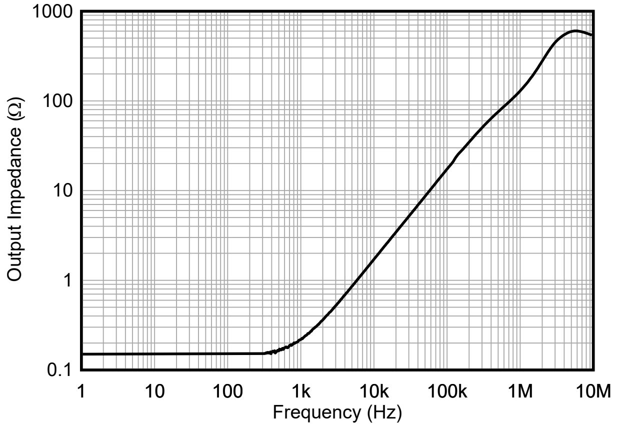
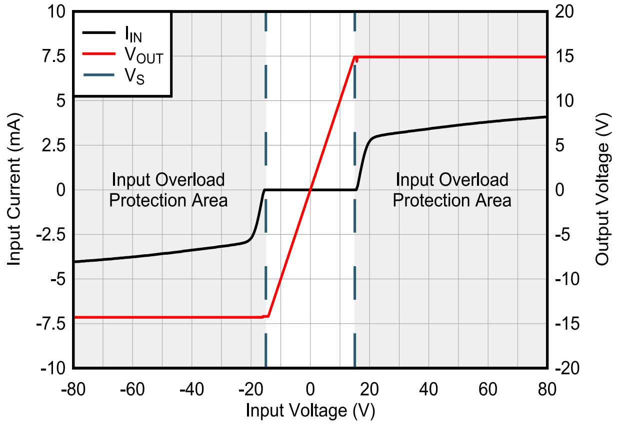


図 7-37. Closed-Loop Output Impedance vs Frequency



V_S = ±15 V

図 7-38. Input Current vs Input Overvoltage

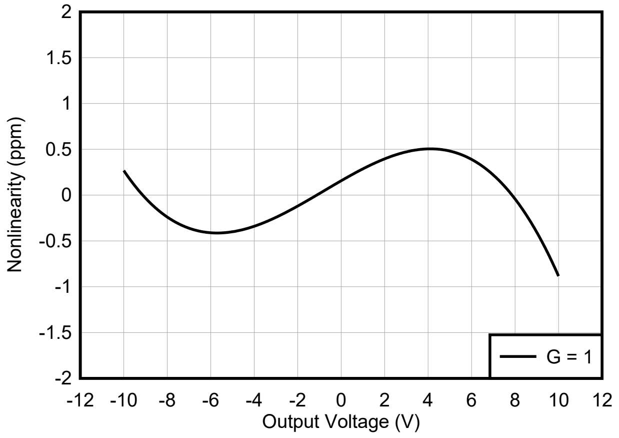


図 7-39. Gain Nonlinearity

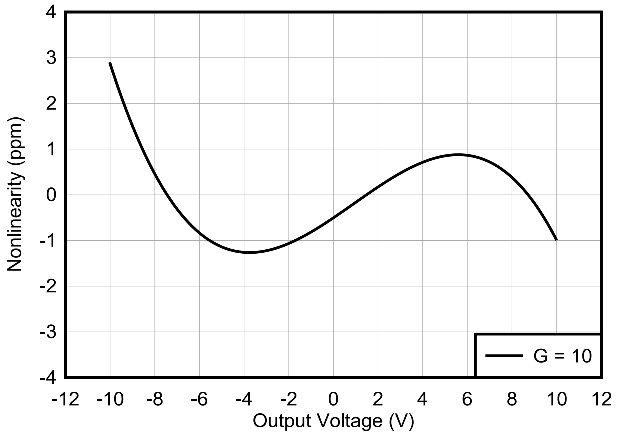


図 7-40. Gain Nonlinearity

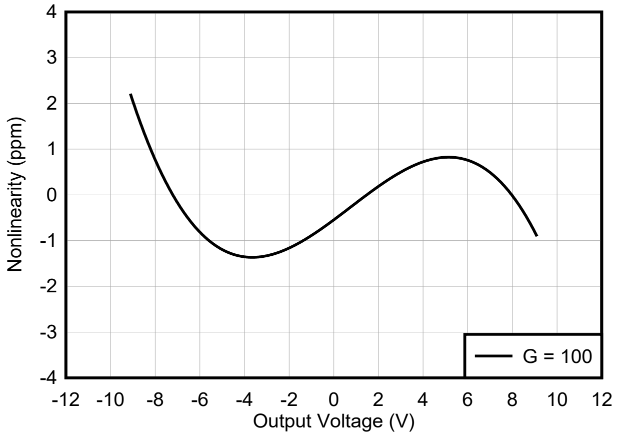


図 7-41. Gain Nonlinearity

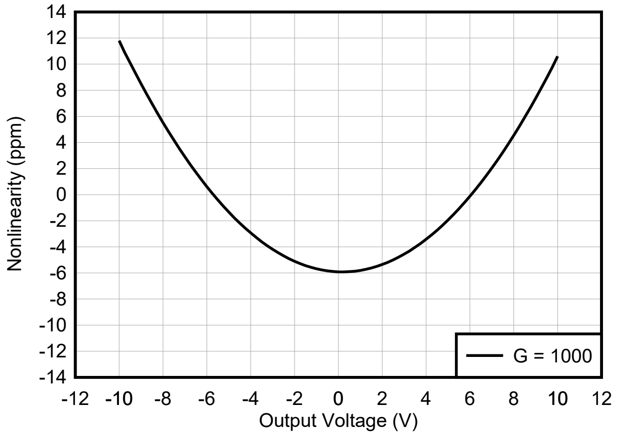


図 7-42. Gain Nonlinearity

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)

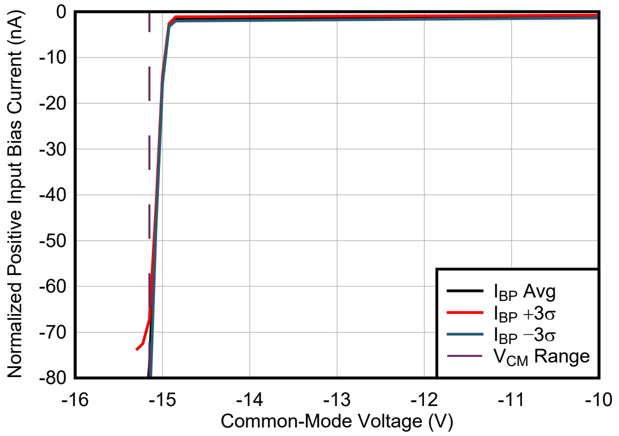


図 7-43. Positive Input Bias Current vs Common-Mode Voltage ($V_{S–}$)

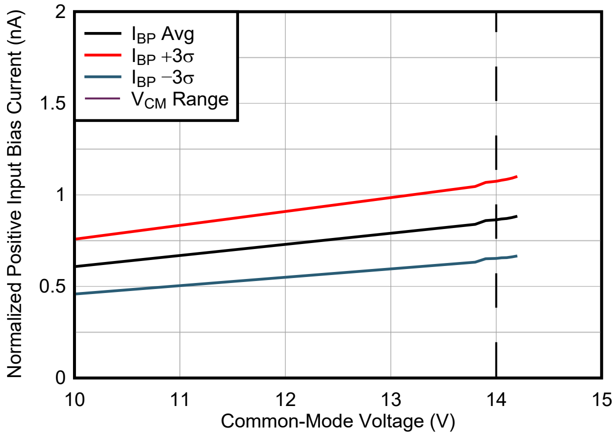


図 7-44. Positive Input Bias Current vs Common-Mode Voltage (V_{S+})

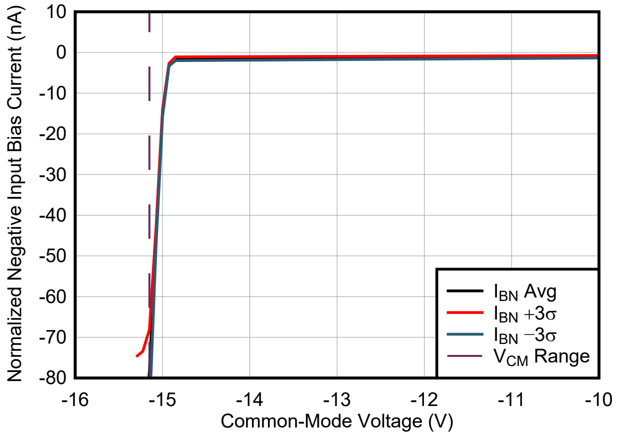


図 7-45. Negative Input Bias Current vs Common-Mode Voltage ($V_{S–}$)

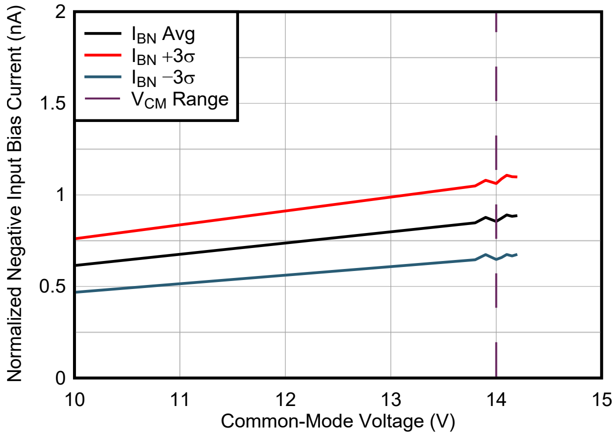
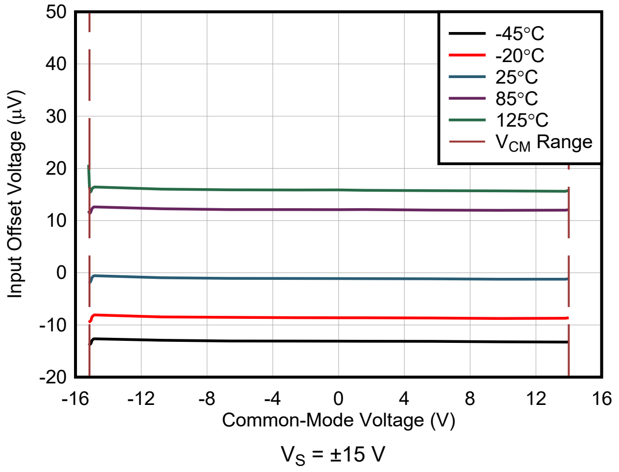
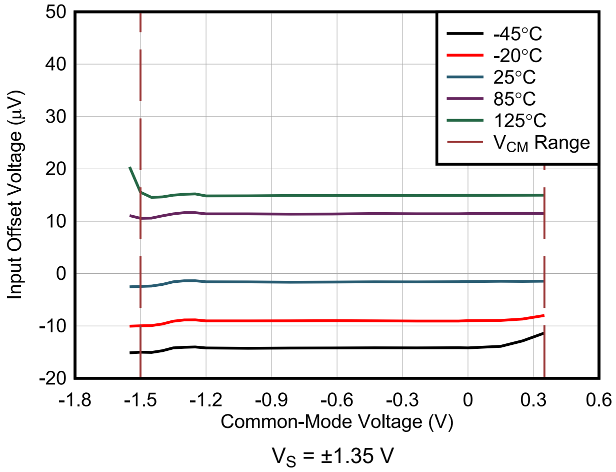


図 7-46. Negative Input Bias Current vs Common-Mode Voltage (V_{S+})



V_S = ±15 V

図 7-47. Offset Voltage vs Common-Mode Voltage

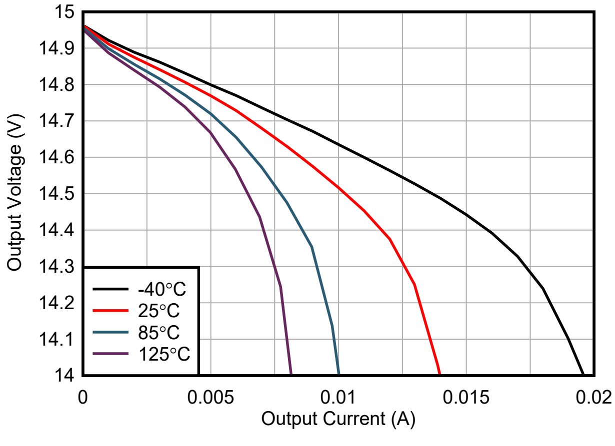


V_S = ±1.35 V

図 7-48. Offset Voltage vs Common-Mode Voltage

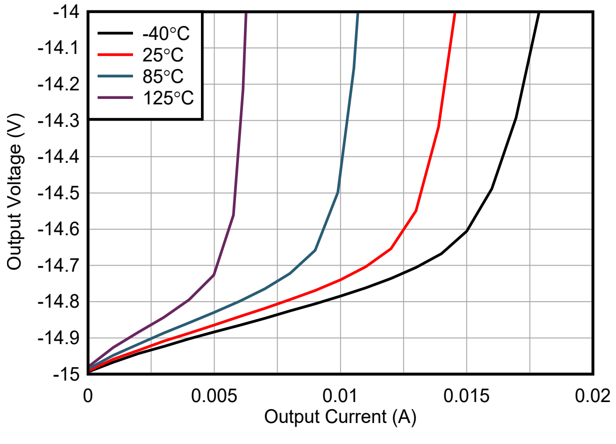
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)



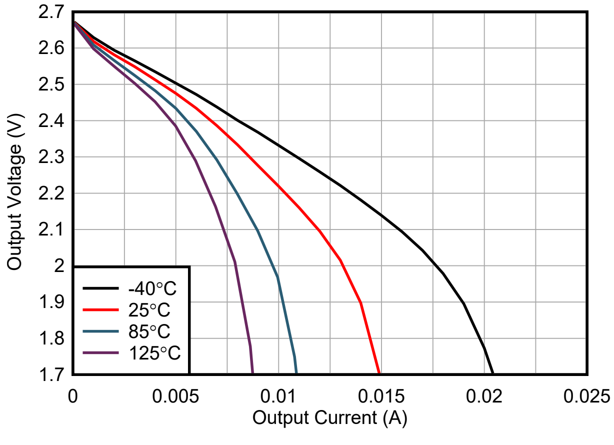
V_S = ±15 V

図 7-49. Positive Output Voltage Swing vs Output Current



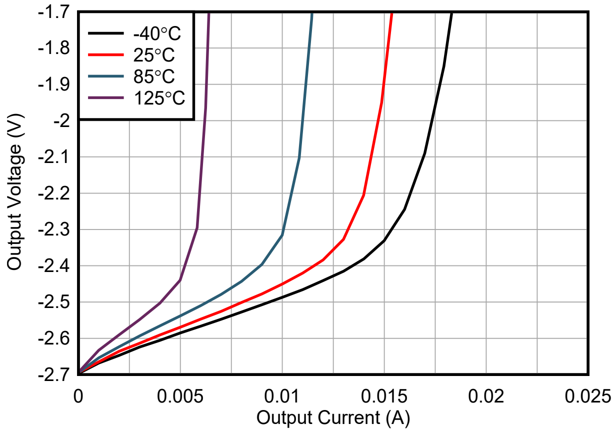
V_S = ±15 V

図 7-50. Negative Output Voltage Swing vs Output Current



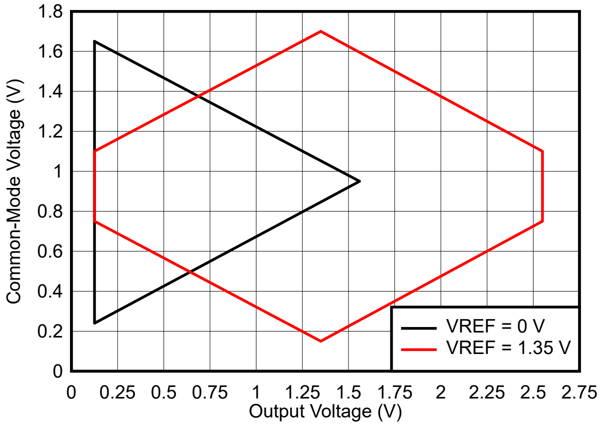
V_S = ±1.35 V

図 7-51. Positive Output Voltage Swing vs Output Current



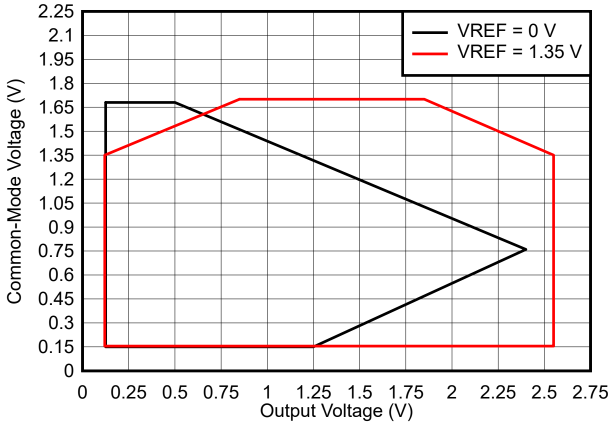
V_S = ±1.35 V

図 7-52. Negative Output Voltage Swing vs Output Current



V_S = 2.7 V G = 1

図 7-53. Input Common-Mode Voltage vs Output Voltage



V_S = 2.7 V G = 100

図 7-54. Input Common-Mode Voltage vs Output Voltage

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, C_L = 0 pF, V_{CM} = V_{REF} = 0 V, and G = 1 (unless otherwise noted)

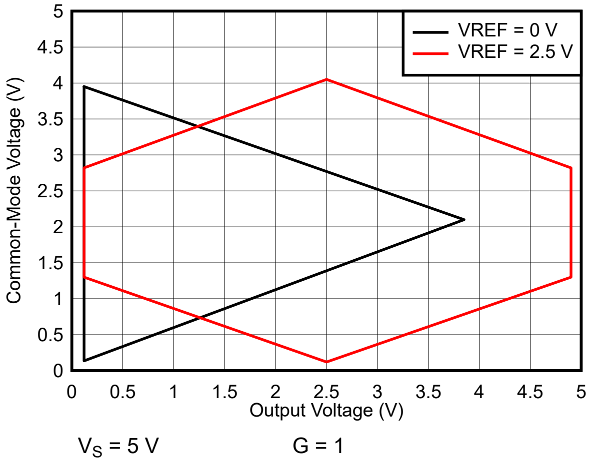


図 7-55. Input Common-Mode Voltage vs Output Voltage

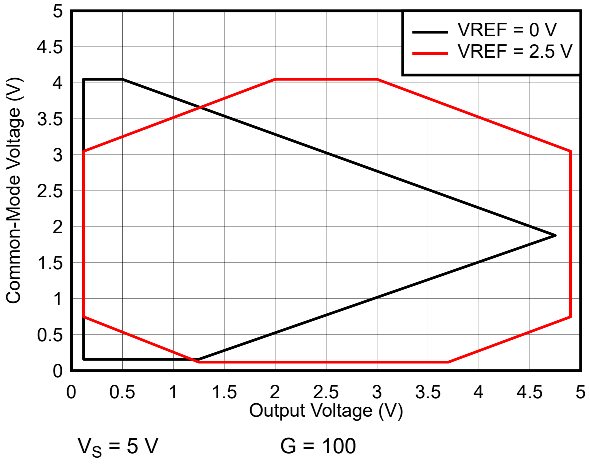


図 7-56. Input Common-Mode Voltage vs Output Voltage

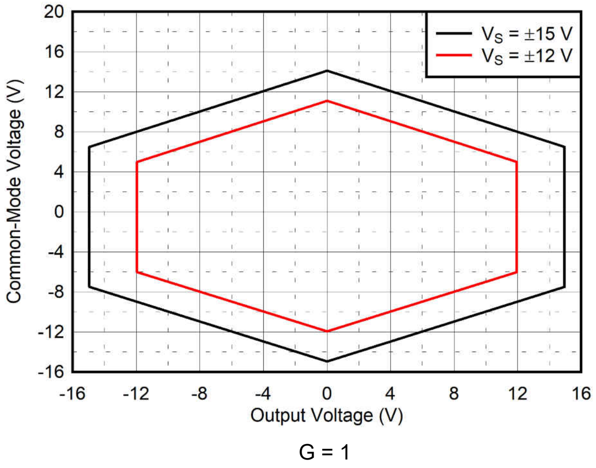


図 7-57. Input Common-Mode Voltage vs Output Voltage

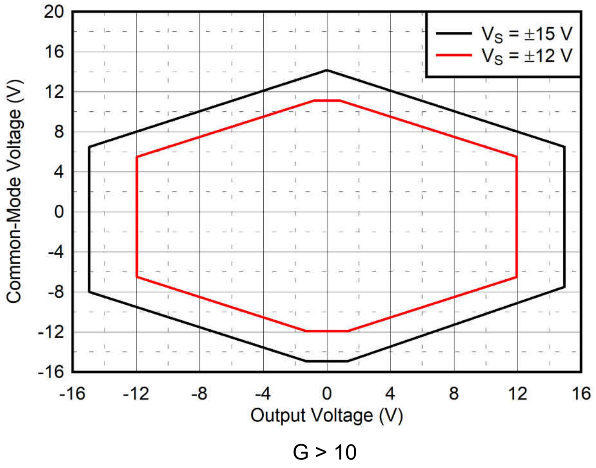


図 7-58. Input Common-Mode Voltage vs Output Voltage

8 Detailed Description

8.1 Overview

The INA823 is a monolithic precision instrumentation amplifier that incorporates a current-feedback input stage and a four-resistor difference-amplifier output stage. One of the features of an instrumentation amplifier (IA) is that the gain is set by placing an external resistor across the RG pins, as described in セクション 8.3.1. The three-op-amp IA topology in the INA823 limits the maximum input voltage applied to the input terminal. The maximum input voltage depends on the common-mode voltage, differential voltage, gain, and the reference voltage; for more information, see セクション 8.3.2. The INA823 also features protection at each input by two junction field-effect transistors (JFETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit the input current, as described in セクション 8.3.3.

The INA823 is developed for medical-sector applications such as infusion pumps (see セクション 9.2.1), and industrial applications such as programmable logic controllers (see セクション 9.2.2)

The schematic in 図 8-1 shows how the INA823 operates. A differential input voltage is buffered by the input transistors, Q_1 and Q_2, and is forced across R_G. This causes a signal current through R_G, R_1, and R_2. The output difference amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the REF pin. The threshold voltage of Q_1 and Q_2 (defined as V_{BE}) along with the voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2, respectively, that are approximately 0.8 V less than the input voltages.

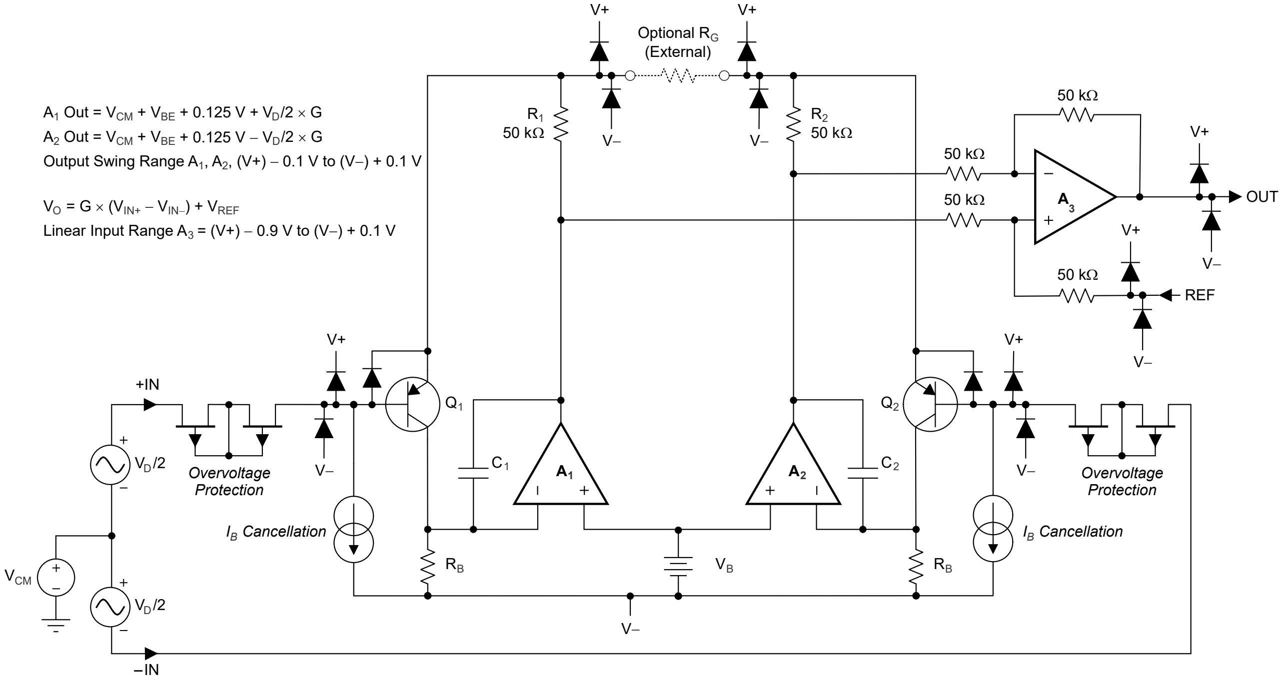
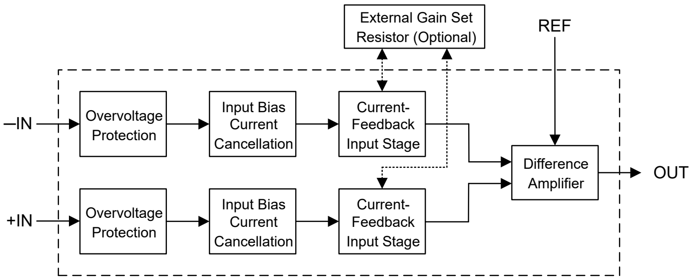


図 8-1. Detailed Schematic

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Gain-Setting Function

図 8-2 shows that the gain of the INA823 is set by a single external resistor (R_G) connected between the RG pins (pins 1 and 8).

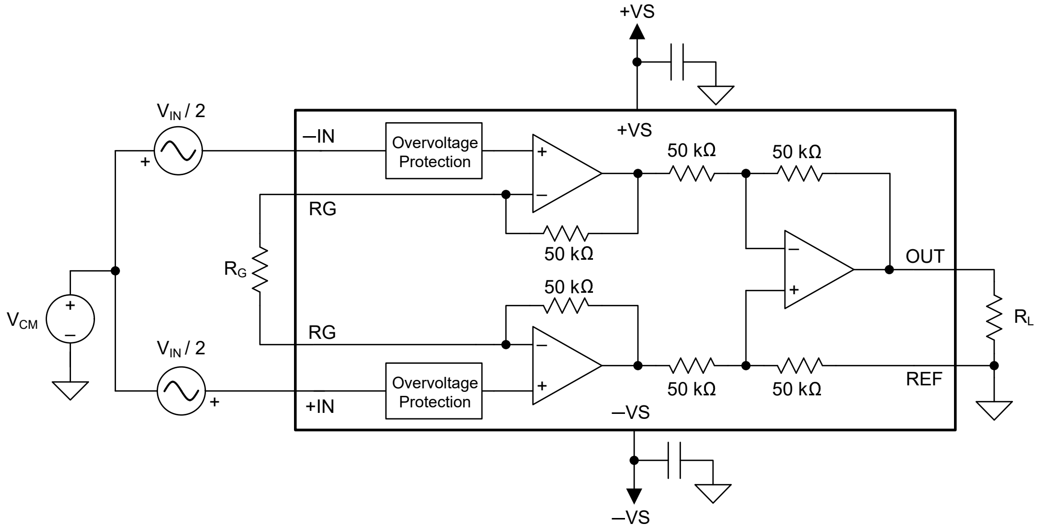


図 8-2. Simplified Schematic of the INA823 With Gain and Output Equations

The gain of the INA823 can be calculated with 式 1:

$$G = 1 + \frac{100\ \text{k}\Omega}{R_G} \tag{1}$$

The value of the external gain resistor R_G is then derived from the gain equation:

$$R_G = \frac{100\ \text{k}\Omega}{G - 1} \tag{2}$$

表 8-1 lists several commonly used gains and resistor values. The 100-kΩ term in 式 1 is a result of the sum of the two internal 50-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the セクション 7.5. As shown in 図 8-2 and explained in more details in *セクション 11*, make sure to connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground that are placed as close to the device as possible.

表 8-1. Commonly Used Gains and Resistor Values

DESIRED GAIN	NEAREST 1% R_G (Ω)	CALCULATED GAIN ERROR (%)
1	Not connected	Not connected
2	100 k	0
5	24.9 k	0.321
10	11 k	0.909
20	5.23 k	0.602
33	3.09 k	1.098
50	2.05 k	0.439
65	1.58 k	1.091
100	1.02 k	0.961
200	499	0.700
500	200	0.200

表 8-1. Commonly Used Gains and Resistor Values (continued)

DESIRED GAIN	NEAREST 1% R_G (Ω)	CALCULATED GAIN ERROR (%)
1000	100	0.100

8.3.1.1 Gain Drift

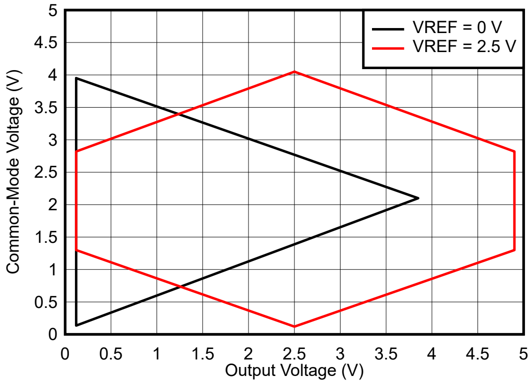
The stability and temperature drift of the external gain setting resistor (R_G) also affects gain. The contribution of R_G to gain accuracy and drift is determined from 式 2.

The best gain drift of 5 ppm/°C (maximum) is achieved when the INA823 uses G = 1 V/V without R_G connected. In this case, gain drift is limited by the slight mismatch of the temperature coefficient of the integrated 50-kΩ resistors in the differential amplifier (A_3).

At gains greater than 1 V/V, gain drift increases as a result of the individual drift of the 50-kΩ resistors in the feedback of A_1 and A_2 relative to the drift of the external gain resistor (R_G.) The low temperature coefficient of the internal feedback resistors significantly improves the overall temperature stability of applications using gains greater than 1 V/V over alternate options.

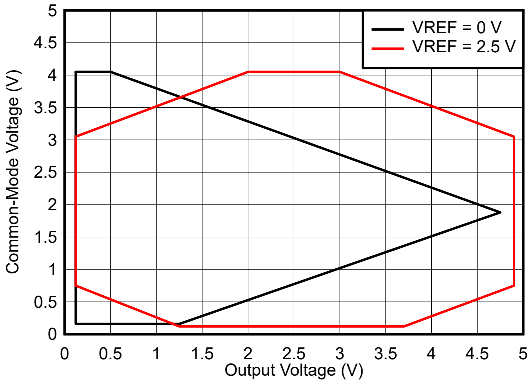
8.3.2 Input Common-Mode Voltage Range

The INA823 linear input voltage range extends from 1 V less than the positive supply to 0.15 V less than the negative supply, and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in 図 8-3. While there are other methods to calculate the common-mode voltage range, the suggested tool is the Analog Engineers Calculator.



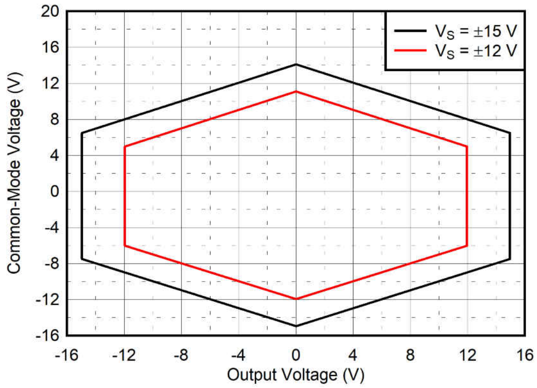
V_S = 5 V, G = 1

図 8-3. Input Common-Mode Voltage vs Output Voltage



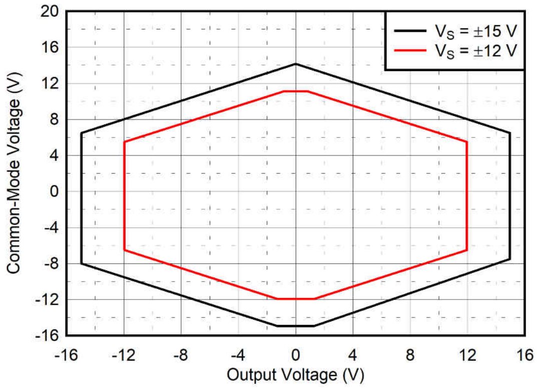
V_S = 5 V, G = 100

図 8-4. Input Common-Mode Voltage vs Output Voltage



G = 1, V_{REF} = 0 V

図 8-5. Input Common-Mode Voltage vs Output Voltage



G > 10, V_{REF} = 0 V

図 8-6. Input Common-Mode Voltage vs Output Voltage

A single-supply instrumentation amplifier has special design considerations. To achieve a common-mode range that extends to single-supply ground, the INA823 employs a current-feedback topology with PNP input transistors. The matched PNP transistors, Q1 and Q2, shift the input voltages of both inputs up by a diode drop, and (through the feedback network) shift the output of A1 and A2 by approximately 0.6 V. The output of A1 and A2 is well within the linear range when the inputs are within the single-supply ground. When inputs are within the supply ground, differential measurements can be made at the ground level. As a result of this input level-shifting, the voltages at pin 1 and pin 8 are not equal to the respective input pin voltages. For most applications, this inequality is not important because only the gain-setting resistor connects to these pins.

8.3.3 Input Protection

The inputs of the INA823 device are individually protected for voltages up to ±60 V and for short transients up to ±80 V. For example, a condition of –60 V on one input and +60 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4 mA.

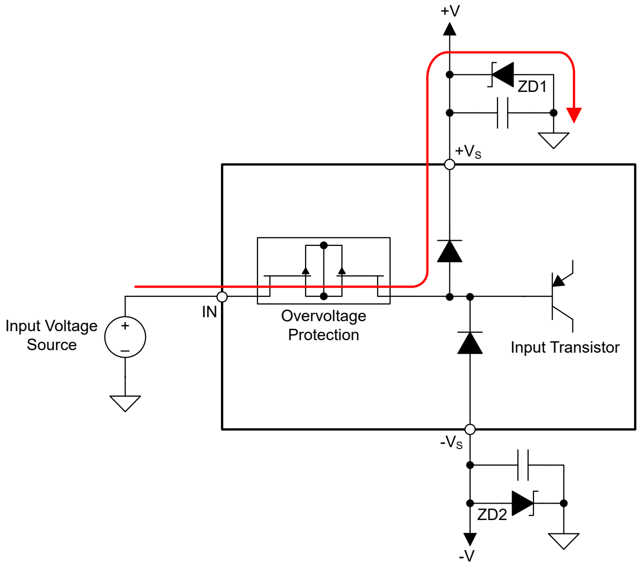


図 8-7. Input Current Path During an Overvoltage Condition

During an input overvoltage condition, current flows through the input protection diodes into the power supplies, as shown in 図 8-7. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in

図 8-7) must be placed on the power supplies to provide a current pathway to ground. 図 8-8 shows the input current for input voltages from –80 V to +80 V when the INA823 is powered by ±15-V supplies.

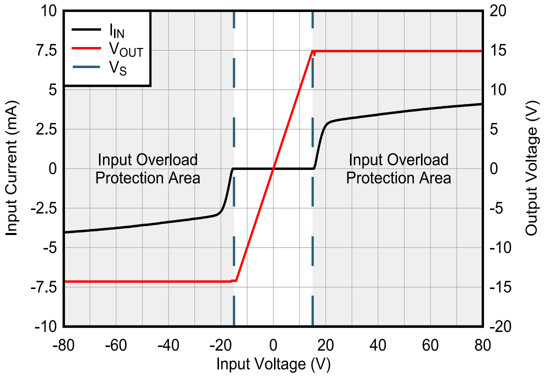


図 8-8. Input Current vs Input Overvoltage

8.4 Device Functional Modes

The INA823 has a single functional mode and is operational when the power supply voltage is greater than 2.7 V (±1.35 V). The maximum power-supply voltage for the INA823 is 36 V (±18 V).

9 Application and Implementation

Note

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9.1 Application Information

9.1.1 Input Bias Current Return Path

The input impedance of the INA823 is extremely high, but a path must be provided for the input bias current of both inputs. This input bias current is typically 1.2 nA. High input impedance means that this input bias current changes little with varying input voltage.

For proper operation, input circuitry must provide a path for this input bias current. 図 9-1 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA823, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (as shown in the thermocouple example in 図 9-1). With a higher source impedance, use two equal resistors to provide a balanced input, with the possible advantages of a lower input offset voltage as a result of bias current, and better high-frequency common-mode rejection. Furthermore, matched input impedances generally minimize the impact to performance in cases where the input common-mode voltage is very low and input bias current can increase as the I_B cancellation circuity runs out of headroom. The input offset current typically remains low; therefore, well-matched input impedances reduce the differential error voltage that would otherwise arise.

For more details about why a valid input bias current return path is necessary, see the *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application note.

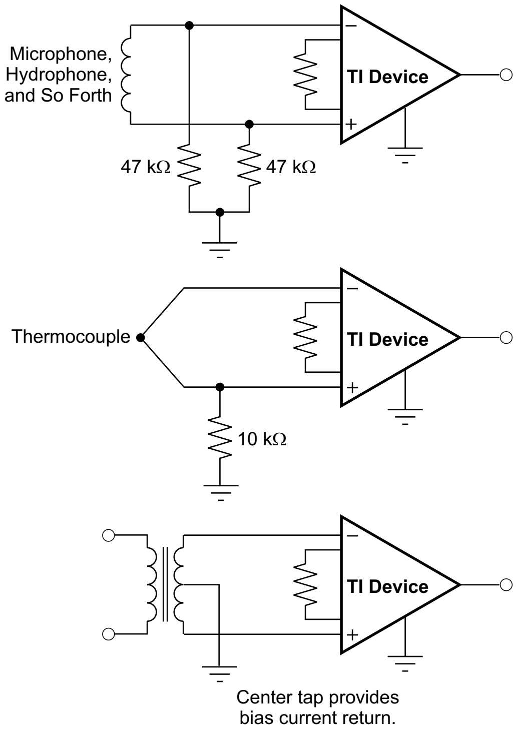

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図 9-1. Providing an Input Common-Mode Current Path

9.2 Typical Applications

9.2.1 Resistive-Bridge Pressure Sensor

The INA823 is an integrated instrumentation amplifier that measures small differential voltages while simultaneously rejecting larger common-mode voltages. The device offers a low power consumption of 250 µA (max) and high precision, thus minimizing errors with voltage offset, offset drift and gain error.

The device is designed for portable applications where sensors measure physical parameters, such as changes in fluid, pressure, temperature, or humidity. An example of a pressure sensor used in the medical sector is in portable infusion pumps or dialysis machines.

The pressure sensor is made of a piezo-resistive element that can be derived as a classical 4-resistor Wheatstone bridge. Occlusion (infusion of fluids, medication, or nutrients) happens only in one direction, and therefore, can only cause the resistive element (R) to expand. This expansion causes a change in voltage on one leg of the Wheatstone bridge, which induces a differential voltage V_{DIFF}.

図 9-2 showcases an exemplary circuit for an occlusion pressure sensor application, as required in infusion pumps. When blockage (occlusion) occurs against a set-point value, the tubing depresses, thus causing the piezo-resistive element to expand (Node AD: R + ΔR). The signal chain connected to the bridge downstream processes the pressure change and can trigger an alarm.

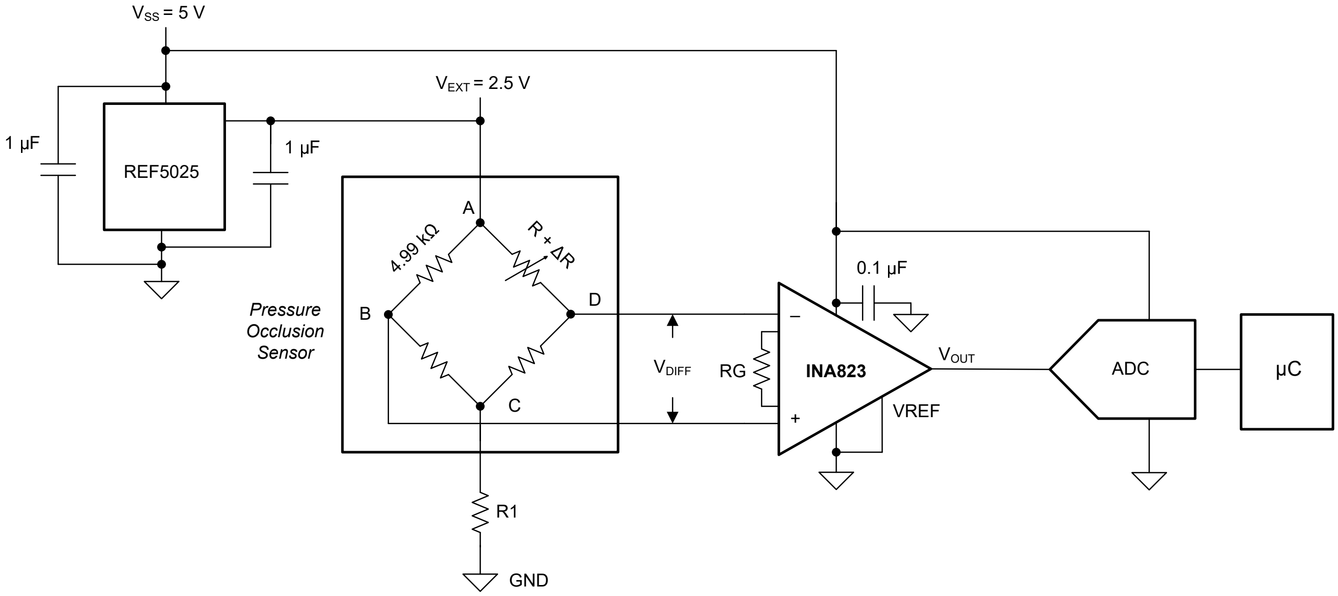


図 9-2. Resistive-Bridge Pressure Sensor

Low-tolerance bridge resistors must be used to minimize the offset and gain errors.

Given that there is only a positive differential voltage applied, this circuit is laid out in single-ended supply mode. The excitation voltage, V_{EXT}, to the bridge must be precise and stable; otherwise, measurement error is introduced.

The REF5025 is a low-noise, low-drift (3 ppm/C), and high-precision (0.05%) voltage reference that is an excellent option to generate the excitation voltage V_{EXT}.

The following subsections give the design requirements and detailed design procedure for an application with a occlusion pressure sensor.

For more information and design tips to consider when using a resistive-bride pressure sensor, see the *Design tips for a resistive-bridge pressure sensor in industrial process-control systems* analog applications journal.

9.2.1.1 Design Requirements

For this application, the design requirements are as shown in 表 9-1.

表 9-1. Design Requirements

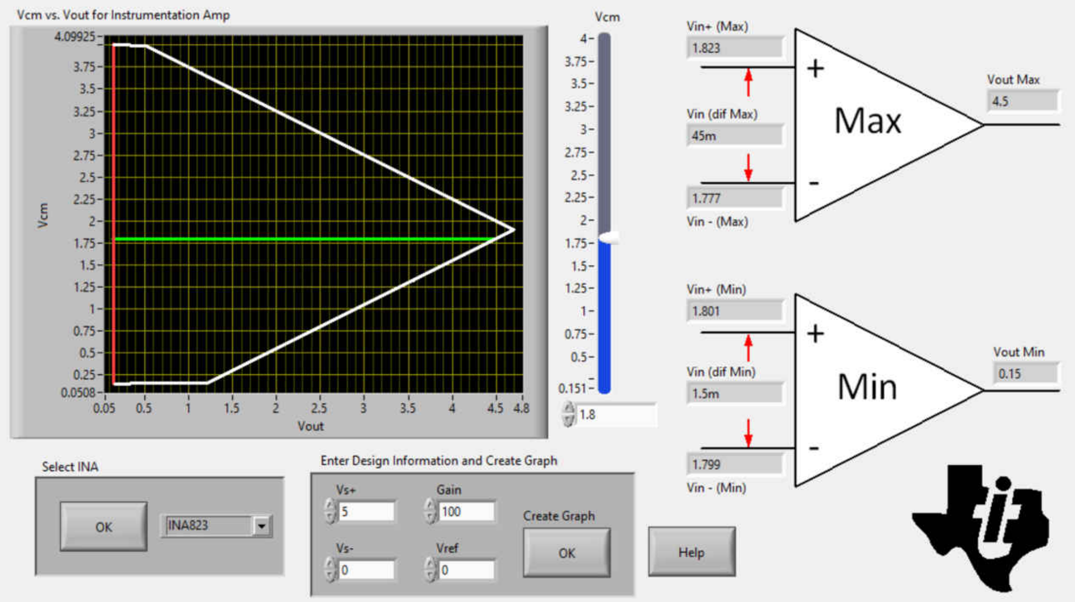
DESCRIPTION	VALUE
Single supply voltage	V_S= 5 V
Excitation voltage	V_{EXT} = 2.5 V
Occlusion pressure range	P = 1...10 psi, increments of p = 0.5 psi
Occlusion pressure sensitivity	S = 2 ± 0.5 (25%) mV/V/psi
Occlusion pressure impedance (R)	R = 4.99 kΩ ± 50 Ω (0.1%)
Total pressure sampling rate	Sr = 20 Hz
Full-scale range of ADC	$V_{ADC(fs)}$ = V_{OUT} = 4.5 V

9.2.1.2 Detailed Design Procedure

This section provides basic calculations to lay out the instrumentation amplifier with respect to the given design requirements.

One of the key considerations in resistive-bridge sensors is the common-mode voltage, V_{CM}. If the bridge is balanced (no pressure, thus no voltage change), $V_{CM(MAX)}$ is half of the bridge excitation (V_{EXT}). As the pressure increases to the maximum value, the common-mode voltage decreases to $V_{CM(MIN)}$.

To achieve the output voltage of V_{OUT} = 4.5 V with the INA823, the limitation for the common-mode voltage is at $V_{CM(INA823max)}$ = 1.8 V, as shown in 図 7-56 and 図 9-3 (where an initial gain value of 100 V/V is used as an approximation). An additional series resistor in the Wheatstone bridge string (R1) is required to shift the common-mode voltage to this value. However, be aware that shifting the common-mode voltage also changes the effective excitation voltage V_{EXT} across the bridge.



Vin+ (Max) 1.823
Vin (dif Max) 45m
Vin - (Max) 1.777
Vout Max 4.5
Vin+ (Min) 1.801
Vin (dif Min) 1.5m
Vin - (Min) 1.799
Vout Min 0.15
Vcm 1.8
Select INA: INA823
Vs+ 5
Gain 100
Vs- 0
Vref 0

図 9-3. Screen Shot From Analog Engineer's Calculator

Calculate the new effective excitation voltage $V_{EXT(NOM)}$ associated with a desired $V_{CM(MIN)}$ value by solving the following:

$$V_{EXT(NOM)} = 2^{*}\left(\frac{V_{EXT} - V_{CM(MIN)}}{1 + S_{MAX}{}^{*}P_{MAX}}\right) = 2^{*}\left(\frac{2.5 - 1.8}{1 + 2.5\ \mathrm{mV}/_{V^{*}psi}{}^{*}10\ psi}\right) = 1.366\ V \tag{3}$$

$V_{EXT(NOM)}$ can in turn be used to calculate the desired value of R1:

$$R_1 = R\left(\frac{V_{EXT}}{V_{EXT(NOM)}} - 1\right) = 4.99\ \text{k}\Omega\left(\frac{2.5\ \text{V}}{1.366\ \text{V}} - 1\right) = 4.144\ \text{k}\Omega \tag{4}$$

Use a standard 0.1% resistor value of 4.12 kΩ.

Calculate the maximum value of V_{DIFF} by solving the following equation for the maximum pressure of 10 psi:

$$V_{DIFF} = (S_{MAX}{*}P_{MAX}){*}V_{EXT(NOM)} = \left(2.5\ {}^{\text{mV}}\!/\!_{\text{V*psi}}{*}10\ \text{psi}\right){*}1.366\ \text{V} = 34.15\ \text{mV} \tag{5}$$

Use the resulting value to verify that the minimum bridge common-mode voltage, $V_{CM(MIN)}$, is within the limits of the INA823 by solving the following:

$$V_{CM(MAX)} = V_{CM(MIN)} + \frac{V_{DIFF}}{2} = 1.8\ \text{V} + \frac{34.15\ \text{mV}}{2} = 1.817\ \text{V} \tag{6}$$

Next, use 式 7 to calculate the required gain for the given maximum sensor output voltage span, V_{DIFF}, with respect to the required V_{OUT}, which is the full-scale range of the ADC.

$$G = \frac{V_{OUT}}{V_{DIFF(MAX)}} = \frac{4.5\ \text{V}}{34.15\ \text{mV}} = 131.77\ \text{V/V} \tag{7}$$

式 8 calculates the gain-setting resistor value using the INA823 gain equation shown in 式 2:

$$R_G = \frac{100\ \text{k}\Omega}{G - 1} = \frac{100\ \text{k}\Omega}{131.77\ {}^{\text{V}}\!/\!_{\text{V}} - 1} = 764.69\ \Omega \tag{8}$$

Use a standard 0.1% resistor value of 768 Ω, so as not to exceed the full-scale range of the ADC.

9.2.1.3 Application Curves

The following typical characteristic curve is for the circuit in 図 9-2.

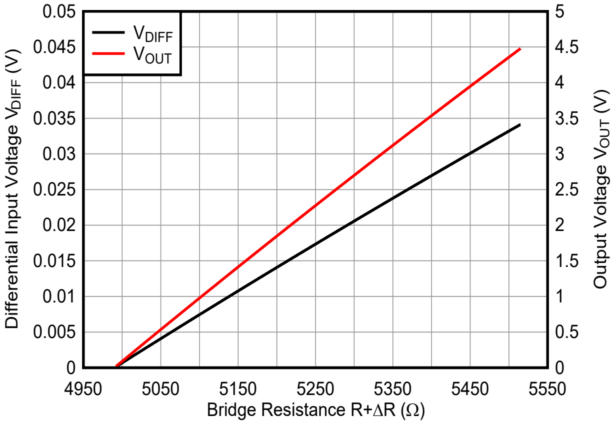


図 9-4. Input Differential Voltage, Output Voltage vs Bridge Resistance

9.2.2 Supporting High Common-Mode Voltage in PLC Input Modules

図 9-5 showcases a high common-mode voltage circuit that is commonly required for programmable logic controller (PLC) analog input modules. This circuit uses a resistive scaling network in front of the IA.

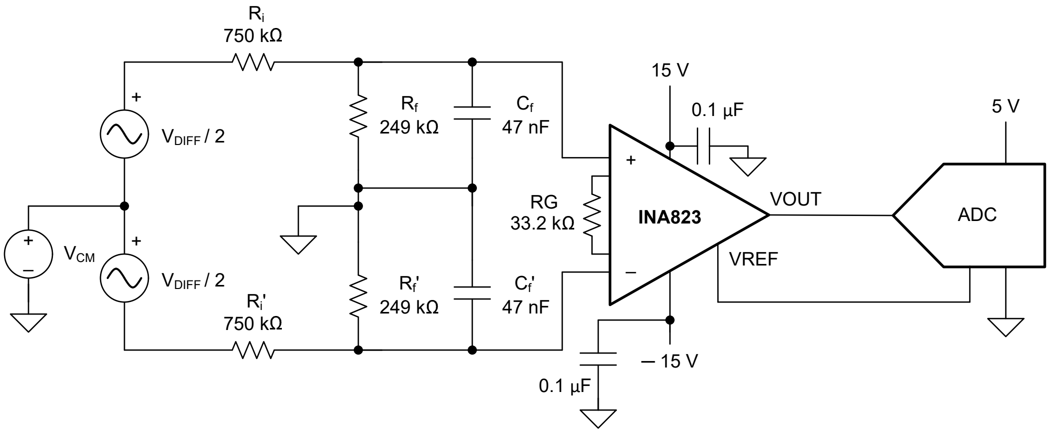


図 9-5. High Common-Mode Voltage PLC Input Module

For a detailed description of the passive scaling approach and more, see the *Supporting High-Voltage Common Mode Using Instrumentation Amplifier* application brief.

9.2.2.1 Design Requirements

表 9-2 lists the requirements for this design example.

表 9-2. Design Parameters

PARAMETER	VALUE
Supply voltage	±15 V
Common-mode voltage	+36 V / –43 V
Input differential signal	1 V
Gain V_{OUT}/V_{DIFF}	1 V/V
Minimum dc CMRR	65 dB

9.2.2.2 Detailed Design Procedure

The gain of the IA is calculated so that the circuit operates at unity gain, where $V_{OUT} = V_{DIFF}$.

The single-ended input impedance, R_{in}(SE), of the circuit is the sum of the scaling resistors (R_f + R_i). To minimize the error that is caused by the tolerance of the scaling resistors, keep R_{in} > 1 MΩ.

Ideally, choose the resistors so that Rf / Ri = Rf' / Ri'. In the real world, designers have to trade off between the mismatch of ratios that degrades the common-mode rejection ratio (CMRR) and the acceptable cost for the design.

The following text describe how to estimate the CMRR performance of the external resistor scaling approach. In the calculation of CMRR, the following factors are considered:

- Take into account the number of resistors, which is estimated by $\sqrt{n}$, where n is the number of resistors applied. In this case, this estimation results in a factor of 2.
- ΔR / R is the resistor matching ratio. The resistor tolerance for all four resistors is 0.1%.
- Take into account that a normal production distribution of the resistor value with a standard deviation of ±3 σ (99.7%). In this case, the assumption results in a factor σ = 1/3 = 0.33 into the equation.

式 9 calculates the common-mode rejection ratio with given factors:

$$\mathrm{CMRR_{dB}} = \frac{\mathrm{G1} + 1}{\alpha \cdot \frac{\Delta R}{R} \cdot \sqrt{n}} \tag{9}$$

$$\mathrm{CMRR_{dB}} = \frac{0.25 + 1}{0.33 \cdot 0.1\% \cdot \sqrt{4}} = 65.5\ \mathrm{dB} \tag{10}$$

The scaling ratio G1 is calculated by:

$$\mathrm{G1} = \frac{R_f}{R_f + R_i} \tag{11}$$

where

- R_f is variable
- R_i is fixed at 750 kΩ.

図 9-6 shows a comparison between the CMRR performance at worst-case (α neglected) and considering normal distribution for different gain settings of G1.

For more details about the calculation of CMRR, see the *Difference amplifier (subtractor) circuit* analog engineer's circuit.

9.2.2.3 Application Curves

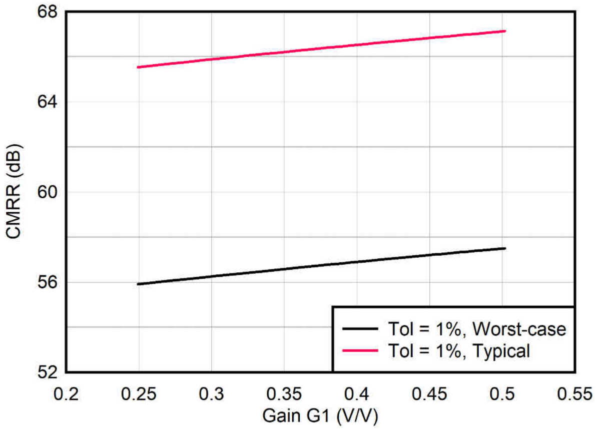


図 9-6. Common-mode Rejection Ratio of External Resistor Network for Different Scaling Ratios

10 Power Supply Recommendations

The nominal performance of the INA823 is specified with a supply voltage of ±15 V and midsupply reference voltage. The device also operates using power supplies from ±1.35 V (2.7 V) to ±18 V (36 V) and non-midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in *セクション 7.6*.

CAUTION

Supply voltages higher than 40 V (±20 V) can permanently damage the device.

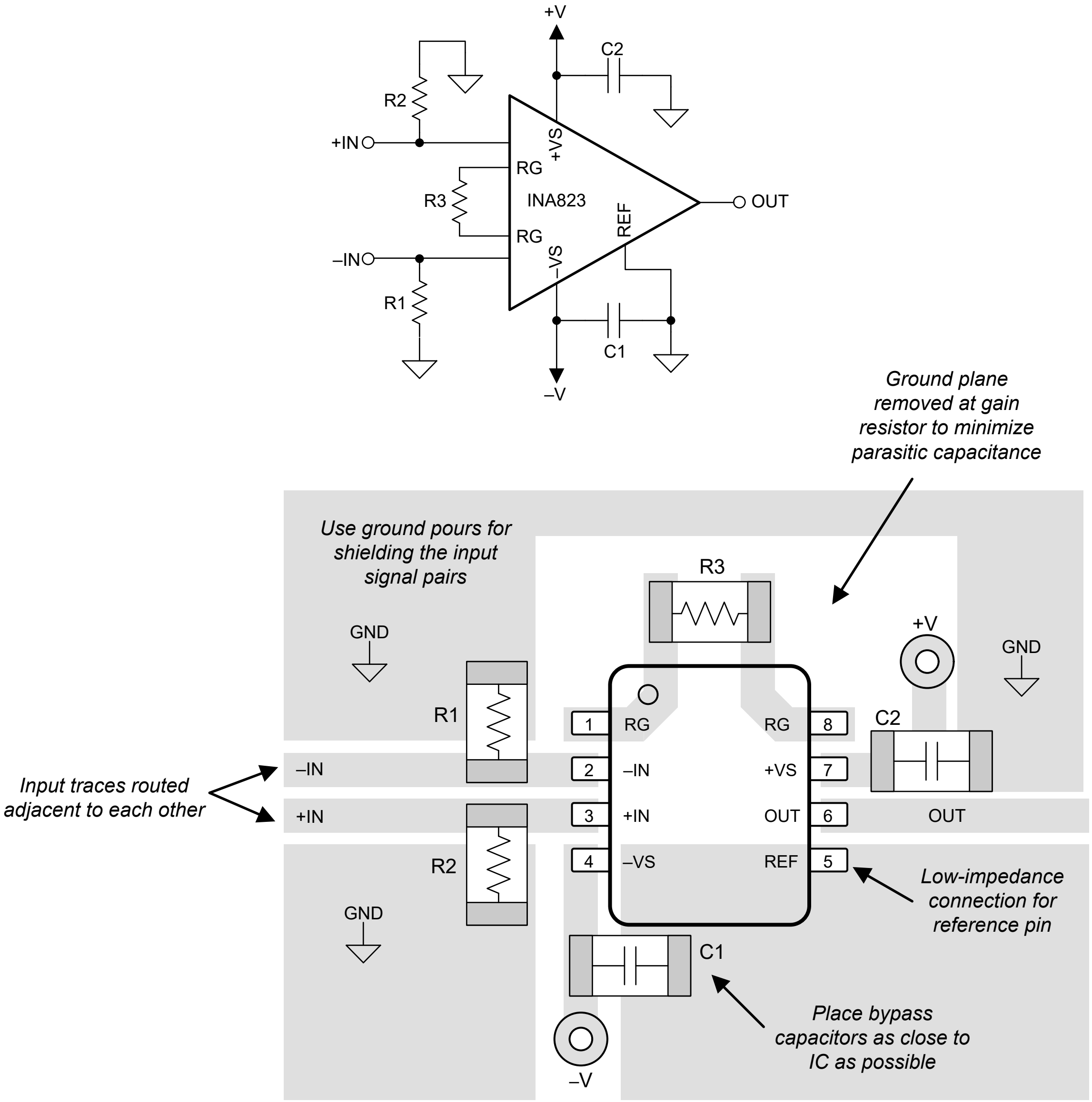
11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use the following PCB layout practices:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Route the input traces as far away from the supply or output traces as possible to reduce parasitic coupling. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Use short, symmetric, and wide traces to connect the external gain resistor to minimize capacitance mismatch between the RG pins.
- Keep the traces as short as possible.

11.2 Layout Example



Ground plane removed at gain resistor to minimize parasitic capacitance

Use ground pours for shielding the input signal pairs

Input traces routed adjacent to each other

Low-impedance connection for reference pin

Place bypass capacitors as close to IC as possible

図 11-1. Example Schematic and Associated PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- *SPICE-based analog simulation program — TINA-TI software folder*
- *Analog Engineer's Calculator*

12.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers* application note
- Texas Instruments, *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application note
- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *OPAx191 36-V, Low Power, Precision, CMOS, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp* data sheet

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 サポート・リソース

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA823DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2IVJ	Samples
INA823DGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2IVJ	Samples
INA823DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA823	Samples
INA823DT	ACTIVE	SOIC	D	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA823	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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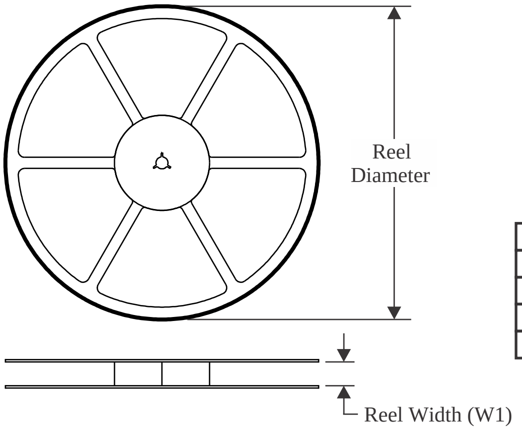
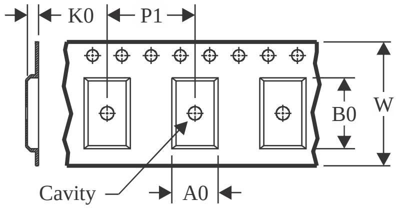
TAPE AND REEL INFORMATION

REEL DIMENSIONS

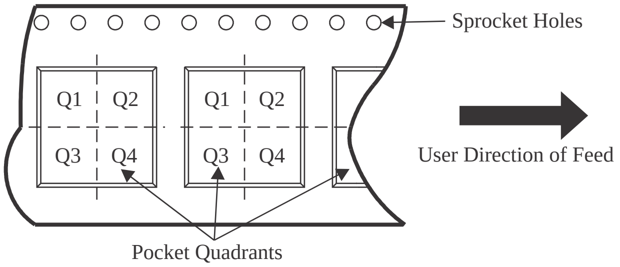


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

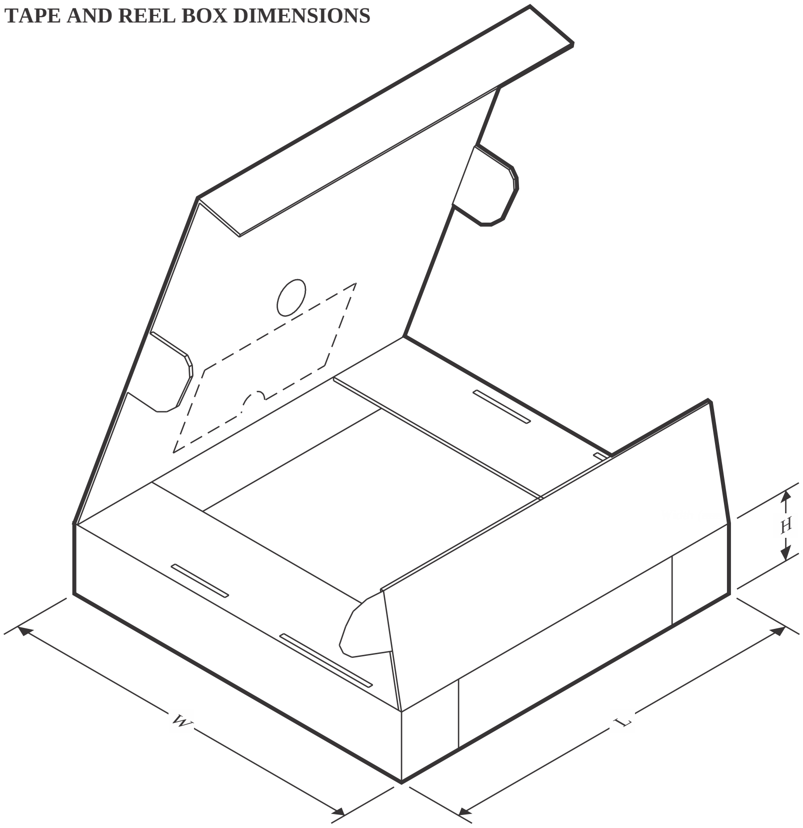
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA823DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA823DGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA823DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA823DT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



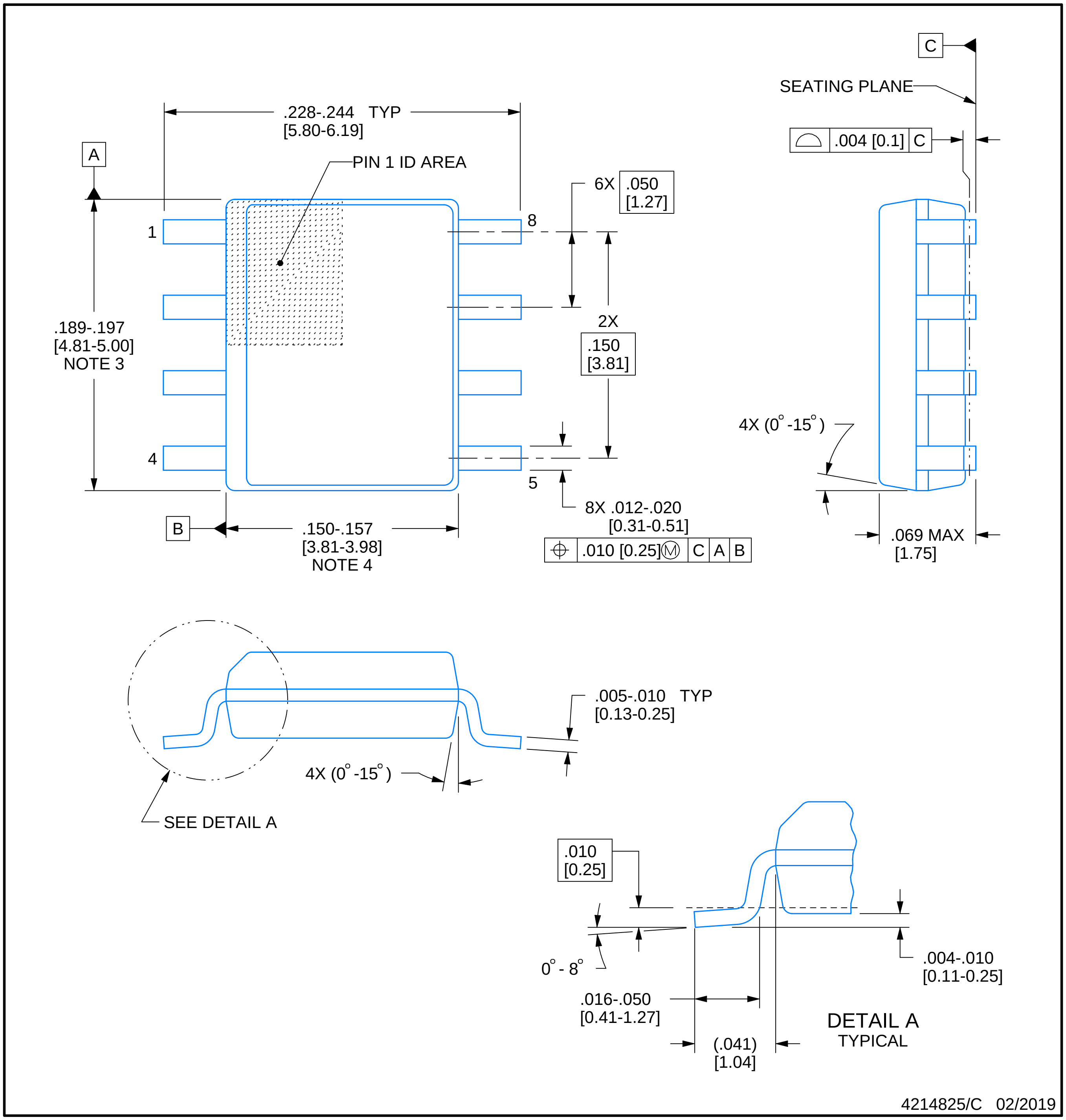
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA823DGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
INA823DGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
INA823DR	SOIC	D	8	3000	356.0	356.0	35.0
INA823DT	SOIC	D	8	250	210.0	185.0	35.0

PACKAGE OUTLINE

SOIC - 1.75 mm max height

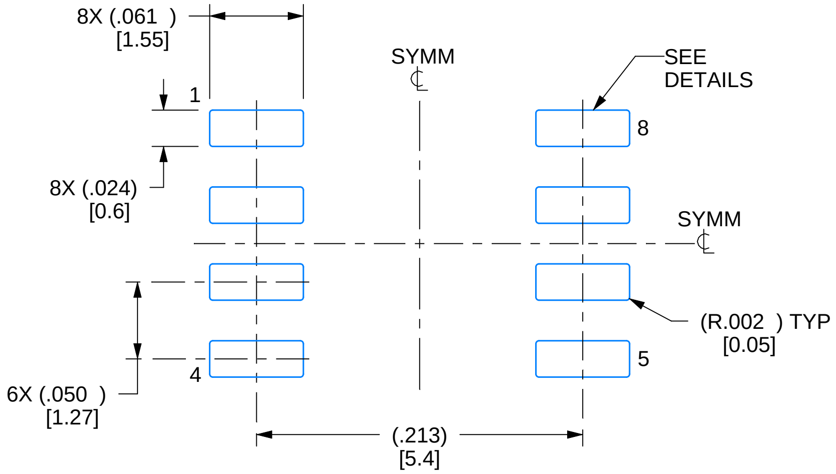
SMALL OUTLINE INTEGRATED CIRCUIT



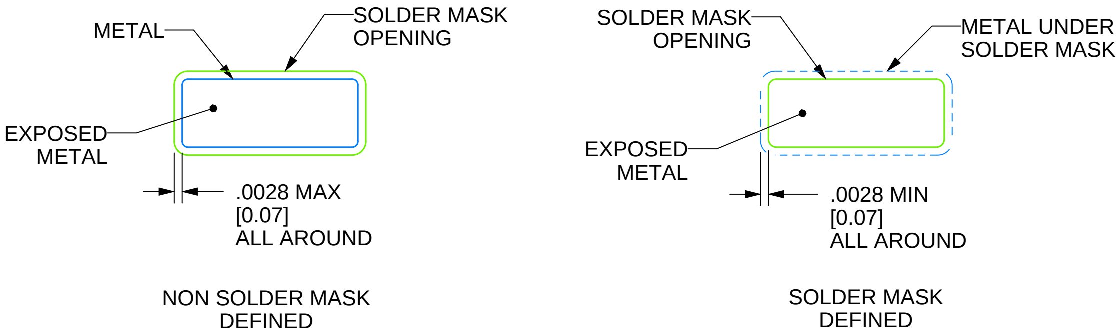
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



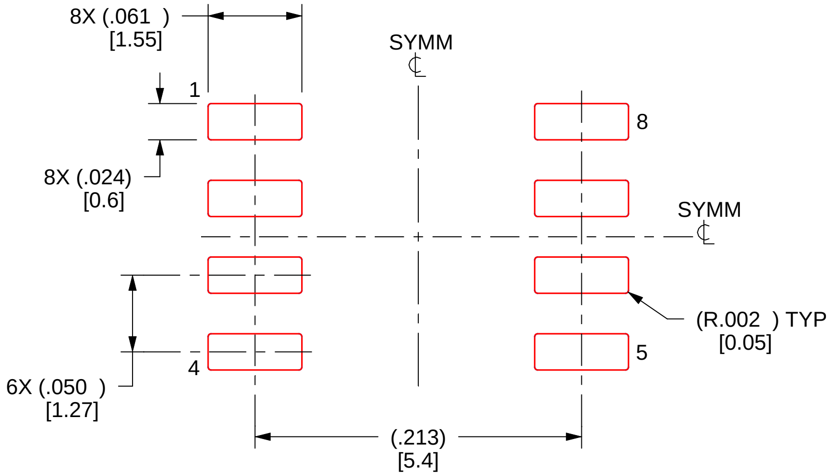
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

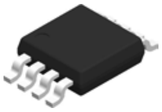


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

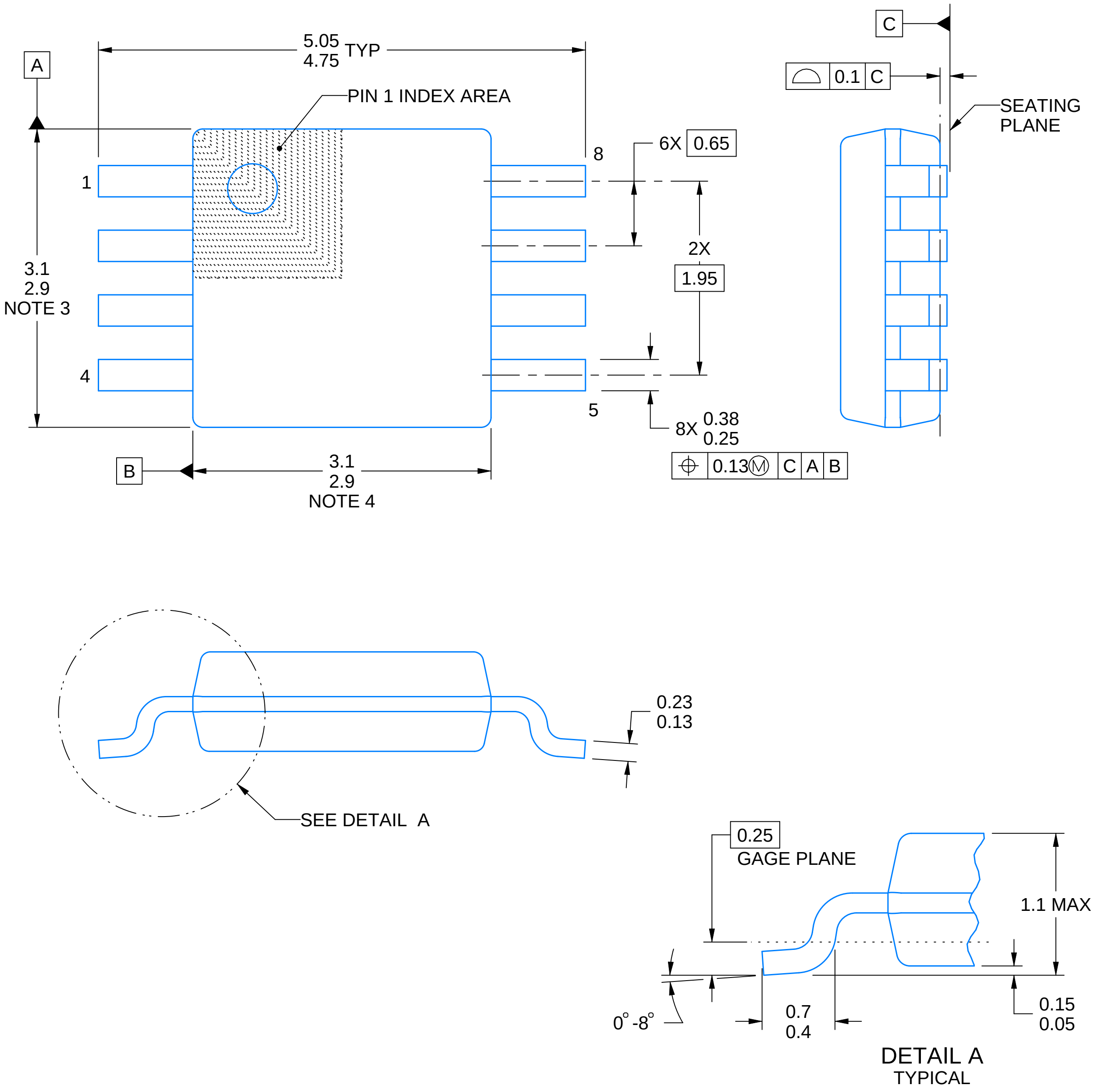
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

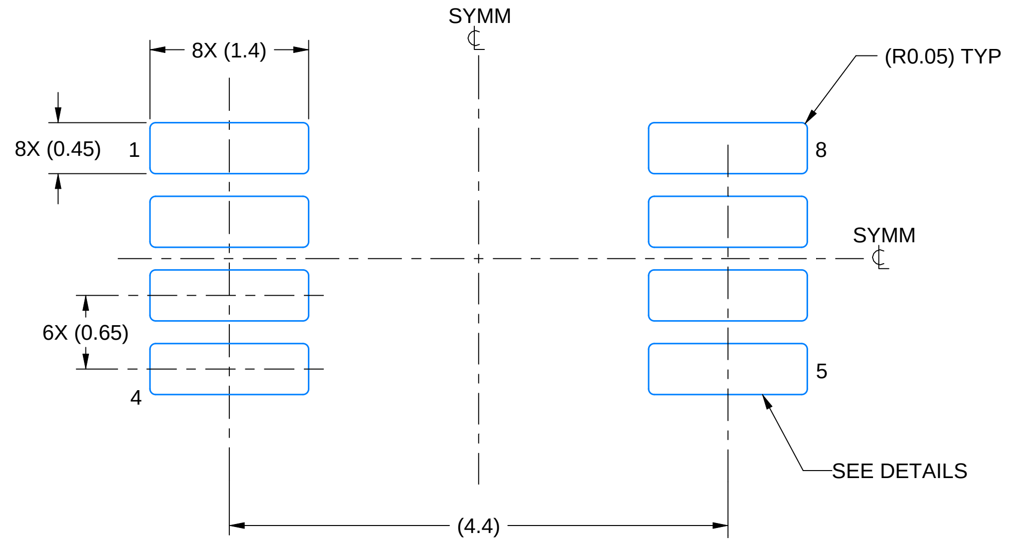


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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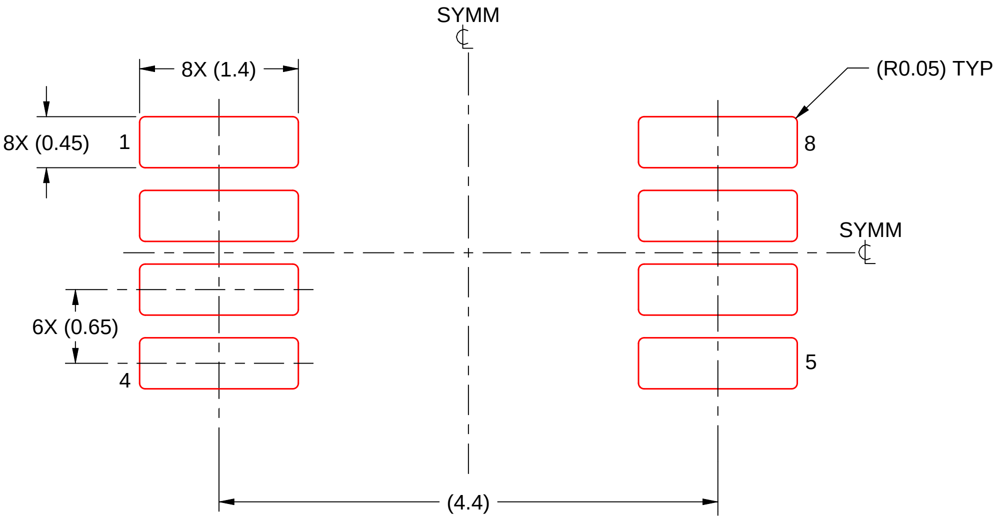
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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