ISO154x-Q1 低消費電力の双方向 I²C アイソレータ

1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 3A
  - デバイス CDM ESD 分類レベル C6
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能 ISO1540-Q1、ISO1541-Q1
- 絶縁型双方向、I²C 互換、通信
- 最高 1MHz での動作に対応
- 電源電圧範囲:3V～5.5V
- オープン・ドレイン出力、サイド 1 で 3.5mA、サイド 2 で 35mA のシンク電流能力
- ±50kV/μs の過渡耐性 (標準値)
- 安全関連の認証:
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した絶縁耐圧:4242V_{PK}
  - UL 1577 に準拠した絶縁耐圧:2500V_{RMS} (1 分間)
  - IEC 62368-1 最終機器標準準拠の CSA 認定
  - GB4943.1-2011 に準拠した CQC 基本絶縁

2 アプリケーション

- 電気自動車、ハイブリッド電気自動車
- 絶縁 I²C バス
- SMBus および PMBus インターフェイス
- オープン・ドレイン・ネットワーク
- モータ制御システム
- バッテリ管理
- I²C のレベル・シフト

3 概要

ISO1540-Q1 および ISO1541-Q1 デバイスは、低消費電力の双方向アイソレータで、I²C インターフェイスと互換性があります。これらのデバイスにはロジック入力および出力バッファがあり、二酸化ケイ素 (SiO_2) バリアを使用したテキサス・インスツルメンツの容量性絶縁テクノロジによって分離されています。これらのデバイスは、絶縁型電源と組み合わせて使用することで、高電圧を遮断し、グランドを絶縁し、ノイズ電流がローカル・グランドに入り込んでノイズに敏感な回路に干渉したり損傷を与えたりすることを防止します。

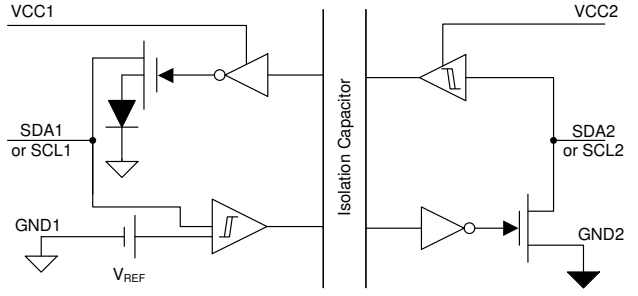
この絶縁テクノロジにより、フォトカプラと比較して機能、性能、サイズ、消費電力が優れています。ISO1540-Q1 および ISO1541-Q1 デバイスにより、小さなフォーム・ファクタ内に、完全に絶縁された I²C インターフェイスを実装できます。

ISO1540-Q1 にはクロックおよびデータ・ライン用の 2 つの絶縁された双方向チャネルがあり、ISO1541-Q1 には双方向のデータ・チャネルと単方向のクロック・チャネルがあります。ISO1541-Q1 は 1 つのコントローラを持つアプリケーションに、ISO1540-Q1 は複数のコントローラを持つアプリケーションに適しています。ターゲットによるクロックのストレッチが可能なアプリケーションでは、ISO1540-Q1 デバイスを使用する必要があります。

絶縁された双方向通信は、これらのデバイス内で、サイド 1 の Low レベル出力電圧を、サイド 1 の High レベル入力電圧より高い値にオフセットすることによって行われるため、標準のデジタル・アイソレータで発生するような内部的なロジック・ラッチを防止できます。

製品情報

部品番号	パッケージ	本体サイズ (公称)
ISO1540-Q1 ISO1541-Q1	SOIC (8)	4.90mm × 3.91mm



概略回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (November 2021) to Revision D (December 2022) — **Page**

- I^2C に言及している場合、すべての旧式の用語をコントローラおよびターゲットに変更 ... 1
- ドキュメント全体を通して編集上および体裁上の変更 ... 1
- Updated electrical and switching parameters ... 5
- Updated 'DIN VDE V 0884-11:2017-01' to 'DIN EN IEC 60747-17 (VDE 0884-17)' and removed references to 'CSA/IEC 60950-1' ... 8

Changes from Revision B (October 2020) to Revision C (November 2021) — **Page**

- Changed scaling on mutiple images ... 23

Changes from Revision A (March 2019) to Revision B (October 2020) — **Page**

- 「セクション 1」に「機能安全情報」の項目を追加 ... 1

Changes from Revision * (November 2016) to Revision A (March 2019) — **Page**

- VDE 標準名を次のように変更:「DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12」から「DIN VDE V 0884-11:2017-01」(「セクション 1」) ... 1
- セクション 1 の項目を次のように変更:「CSA Component Acceptance Notice 5A、IEC 60950-1 および IEC 61010-1 最終機器標準」から「IEC 60950-1 および IEC 62368-1 最終機器標準準拠の CSA 認定」 ... 1
- 「セクション 1」の次の項目を削除:UL 1577 認定は完了、他のすべての認定は計画中 ... 1
- Updated certifications approval status, numbers, standard names, and details according to the latest agency certificates in セクション 6.7 table ... 8
- Changed both bypass capacitors From: 10 µF To: 0.1 µF in . Even though larger capacitors can be used, 0.1 µF is the minimum recommended bypass capacitor size ... 23
- Changed both bypass capacitors From: 10 µF To: 0.1 µF in . Even though larger capacitors can be used, 0.1 µF is the minimum recommended bypass capacitor size ... 23

5 Pin Configuration and Functions

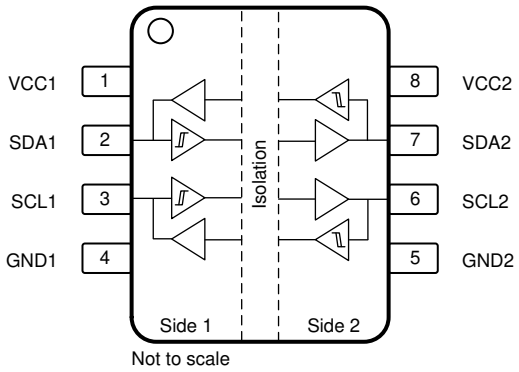


図 5-1. ISO1540-Q1 D Package 8-Pin SOIC Top View

表 5-1. Pin Functions—ISO1540-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	—	Ground, side 1
GND2	5	—	Ground, side 2
SCL1	3	I/O	Serial clock input / output, side 1
SCL2	6	I/O	Serial clock input / output, side 2
SDA1	2	I/O	Serial data input / output, side 1
SDA2	7	I/O	Serial data input / output, side 2
VCC1	1	—	Supply voltage, side 1
VCC2	8	—	Supply voltage, side 2

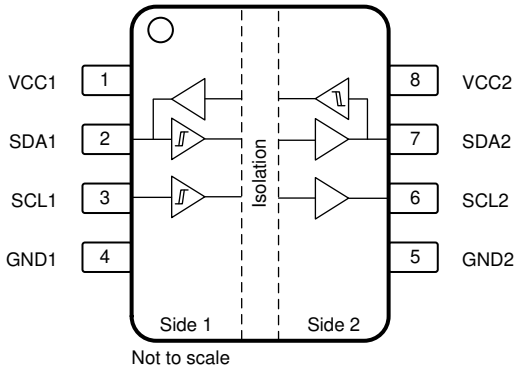


図 5-2. ISO1541-Q1 D Package 8-Pin SOIC Top View

表 5-2. Pin Functions—ISO1541-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	—	Ground, side 1
GND2	5	—	Ground, side 2
SCL1	3	I	Serial clock input, side 1
SCL2	6	O	Serial clock output, side 2
SDA1	2	I/O	Serial data input / output, side 1
SDA2	7	I/O	Serial data input / output, side 2
VCC1	1	—	Supply voltage, side 1
VCC2	8	—	Supply voltage, side 2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Voltage	VCC1, VCC2	–0.5	6	V
		SDA1, SCL1	–0.5	VCC1 + 0.5(3)	
		SDA2, SCL2	–0.5	VCC2 + 0.5(3)	
I_O	Output current	SDA1, SCL1	0	20	mA
		SDA2, SCL2	0	100	
$T_{J(MAX)}$	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values here within are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins except bus pins	±4000	V
			Bus pins	±8000	
		Charged-device model (CDM), per AEC Q100-011		±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
VCC1, VCC2	Supply voltage	3	5.5	V
V_{SDA1}, V_{SCL1}	Input and output signal voltages, side 1	0	VCC1	V
V_{SDA2}, V_{SCL2}	Input and output signal voltages, side 2	0	VCC2	V
V_{IL1}	Low-level input voltage, side 1	0	0.5	V
V_{IH1}	High-level input voltage, side 1	0.7 × VCC1	VCC1	V
V_{IL2}	Low-level input voltage, side 2	0	0.3 × VCC2	V
V_{IH2}	High-level input voltage, side 2	0.7 × VCC2	VCC2	V
I_{OL1}	Output current, side 1	0.5	3.5	mA
I_{OL2}	Output current, side 2	0.5	35	mA
C1	Capacitive load, side 1		40	pF
C2	Capacitive load, side 2		400	pF
f_{MAX}	Operating frequency(1)		1	MHz
T_A	Ambient temperature	–40	125	°C
T_J	Junction temperature	–40	136	°C
T_{SD}	Thermal shutdown	139	197	°C

(1) This represents the maximum frequency with the maximum bus load (C) and the maximum current sink (I_O). If the system has less bus capacitance, then higher frequencies can be achieved.

6.4 Thermal Information

THERMAL METRIC(1)		ISO154x-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VCC1 = VCC2 = 5.5 V, T_J = 150 °C, C1 = 20 pF, C2 = 400 pF; R1 = 1.4 kΩ, R2 = 94 Ω; Input a 1-MHz 50% duty cycle clock signal			105	mW
P_{D1}	Maximum power dissipation (side-1)				37	mW
P_{D2}	Maximum power dissipation (side-2)				68	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.014	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I–IV	
		Rated mains voltage ≤ 300 V_{RMS}	I–III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 s (qualification) t = 1 s (100% production)	4242	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 680\ V_{PK}$, t_m = 10 s	<5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 906\ V_{PK}$, t_m = 10 s	<5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 1062\ V_{PK}$, t_m = 1 s	<5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	~1	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 2500 V_{RMS}, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC
Certified according to DIN EN IEC 60747-17 (VDE 0884-17) and DIN EN 61010-1 (VDE 0411-1)	Certified according to CSA/IEC 62368-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK}; Maximum Repetitive Peak Voltage, 566 V_{PK}	2.5-kV_{RMS} Insulation Rating; 300 V_{RMS} Basic Insulation working voltage per CSA 62368-1-14 and IEC 62368-1:2014	Single protection, 2500 V_{RMS}	Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40047657	Master contract number: 220991	File number: E181974	Certificate number: CQC14001109540

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 114.6°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see 図 6-1			198	mA
		$R_{\theta JA}$ = 114.6°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see 図 6-1			303	
T_S	Safety temperature				150	°C

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *セクション 6.4* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics

over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SIDE 1 (ONLY)						
V_{ILT1}	Voltage input threshold low, SDA1 and SCL1		480	550	660	mV
V_{IHT1}	Voltage input threshold high, SDA1 and SCL1		520	610	700	mV
V_{HYST1}	Voltage input hysteresis	$V_{IHT1} - V_{ILT1}$	40	60		mV
V_{OL1}	Low-level output voltage, SDA1 and SCL1(1)	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA	570		800	mV
ΔV_{OIT1}	Low-level output voltage to high-level input voltage threshold difference, SDA1 and SCL1(1) (2)	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA	50			mV
SIDE 2 (ONLY)						
V_{ILT2}	Voltage input threshold low, SDA2 and SCL2		0.3 × VCC2		0.4 × VCC2	V
V_{IHT2}	Voltage input threshold high, SDA2 and SCL2		0.4 × VCC2		0.5 × VCC2	V
V_{HYST2}	Voltage input hysteresis	$V_{IHT2} - V_{ILT2}$	0.05 × VCC2			V
V_{OL2}	Low-level output voltage, SDA2 and SCL2	0.5 mA ≤ (I_{SDA2} and I_{SCL2}) ≤ 35 mA			0.4	V
BOTH SIDES						
$\lvert I_I \rvert$	Input leakage currents, SDA1, SCL1, SDA2, and SCL2	V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2		0.01	10	µA
C_I	Input capacitance to local ground, SDA1, SCL1, SDA2, and SCL2	V_I = 0.4 × sin(2E6πt) + 2.5 V		7		pF
CMTI	Common-mode transient immunity	See 図 7-3	25	50		kV/µs
V_{CCUV}	VCC undervoltage lockout threshold(3)		1.7	2.5	2.9	V

(1) This parameter does not apply to the ISO1541-Q1 SCL1 line as it is unidirectional.
(2) $\Delta V_{OIT1} = V_{OL1} - V_{IHT1}$. This represents the minimum difference between a Low-Level Output Voltage and a High-Level Input Voltage Threshold to prevent a permanent latch condition that would otherwise exist with bidirectional communication.
(3) Any VCC voltages, on either side, less than the minimum will ensure device lockout. Both VCC voltages greater than the maximum will prevent device lockout.

6.10 Supply Current Characteristics

over recommended operating conditions, unless otherwise noted. For more information, see 図 7-1.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3 V ≤ VCC1, VCC2 ≤ 3.6 V						
I_{CC1} Supply current, side 1	ISO1540-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1, R2 = Open; C1, C2 = Open		2.4	7.1	mA
		V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		2.5	4	
	ISO1541-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1, R2 = Open; C1, C2 = Open		2.1	6.1	
		V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		2.3	3.6	
I_{CC2} Supply current, side 2	ISO1540-Q1 and ISO1541-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1, R2 = Open; C1, C2 = Open		1.7	6.7	mA
		V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		1.9	3.5	
4.5 V ≤ VCC1, VCC2 ≤ 5.5 V						
I_{CC1} Supply current, side 1	ISO1540-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1,R2 = Open; C1,C2 = Open		3.1	7.2	mA
		V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		3.1	4.7	
	ISO1541-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1, R2 = Open; C1, C2 = Open		2.8	6.2	
		V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		2.9	4.5	
I_{CC2} Supply current, side 2	ISO1540-Q1 and ISO1541-Q1	V_{SDA1}, V_{SCL1} = GND1; V_{SDA2}, V_{SCL2} = GND2; R1, R2 = Open; C1, C2 = Open		2.3	6.8	mA
		V_{SDA1}, V_{SCL1} = VCC1; V_{SDA2}, V_{SCL2} = VCC2; R1, R2 = Open; C1, C2 = Open		2.5	4	

6.11 Timing Requirements

			MIN	NOM	MAX	UNIT
t_{UVLO}	Time to recover from UVLO	2.7 V to 0.9 V; See 図 7-4	30	50	151	µs

6.12 Switching Characteristics

over recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
3 V ≤ VCC1, VCC2 ≤ 3.6 V							
t_{f1}	Output Signal Fall Time (SDA1, SCL1)	See 図 7-1 R1 = 953 Ω, C1 = 40 pF	0.7 × VCC1 to 0.3 × VCC1	8	17	29	ns
			0.9 × VCC1 to 900 mV	16	29	48	
t_{f2}	Output Signal Fall Time (SDA2, SCL2)	See 図 7-1 R2 = 95.3 Ω, C2 = 400 pF	0.7 × VCC2 to 0.3 × VCC2	14	23	47	ns
			0.9 × VCC2 to 400 mV	35	50	100	
t_{pLH1-2}	Low-to-High Propagation Delay, Side 1 to Side 2	See 図 7-1 R1 = 953 Ω, R2 = 95.3 Ω, C1, C2 = 10 pF	0.55 V to 0.7 × VCC2		33	65	ns
t_{PHL1-2}	High-to-Low Propagation Delay, Side 1 to Side 2		0.7 V to 0.4 V		90	181	ns
PWD_{1-2}	Pulse Width Distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$				55	123	ns
t_{PLH2-1} (1)	Low-to-High Propagation Delay, Side 2 to Side 1		0.4 × VCC2 to 0.7 × VCC1		47	68	ns
t_{PHL2-1} (1)	High-to-Low Propagation Delay, Side 2 to Side 1		0.4 × VCC2 to 0.9 V		67	109	ns
PWD_{2-1} (1)	Pulse Width Distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$				20	49	ns
t_{LOOP1} (1)	Round-trip propagation delay on Side 1	See 図 7-2; R1 = 953 Ω, C1 = 40 pF R2 = 95.3 Ω, C2 = 400 pF	0.4 V to 0.3 × VCC1		100	165	ns
4.5 V ≤ VCC1, VCC2 ≤ 5.5 V							
t_{f1}	Output Signal Fall Time (SDA1, SCL1)	See 図 7-1 R1 = 1430 Ω, C1 = 40 pF	0.7 × VCC1 to 0.3 × VCC1	6	11	22	ns
			0.9 × VCC1 to 900 mV	13	21	48	
t_{f2}	Output Signal Fall Time (SDA2, SCL2)	See 図 7-1 R2 = 143 Ω, C2 = 400 pF	0.7 × VCC2 to 0.3 × VCC2	10	18	35	ns
			0.9 × VCC2 to 400 mV	28	41	76	
t_{pLH1-2}	Low-to-High Propagation Delay, Side 1 to Side 2	See 図 7-1 R1 = 1430 Ω, R2 = 143 Ω, C1,2 = 10 pF	0.55 V to 0.7 × VCC2		31	62	ns
t_{PHL1-2}	High-to-Low Propagation Delay, Side 1 to Side 2		0.7 V to 0.4 V		70	139	ns
PWD_{1-2}	Pulse Width Distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$				38	80	ns
t_{PLH2-1} (1)	Low-to-high propagation delay, side 2 to side 1		0.4 × VCC2 to 0.7 × VCC1		55	80	ns
t_{PHL2-1} (1)	High-to-low propagation delay, Side 2 to side 1		0.4 × VCC2 to 0.9 V		47	85	ns
PWD_{2-1} (1)	Pulse Width Distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$				8	34	ns
t_{LOOP1} (1)	Round-trip propagation delay on side 1	See 図 7-2; R1 = 1430 Ω, C1 = 40 pF R2 = 143 Ω, C2 = 400 pF	0.4 V to 0.3 × VCC1		110	180	ns

(1) This parameter does not apply to the ISO1541-Q1 SCL1 line as it is unidirectional.

6.13 Insulation Characteristics Curves

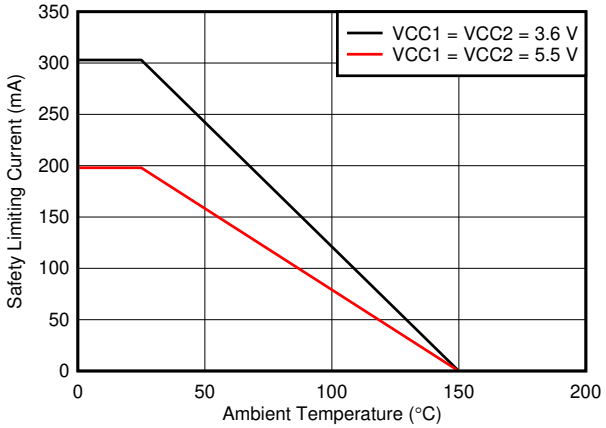


図 6-1. Thermal Derating Curve for Limiting Current per VDE

6.14 Typical Characteristics

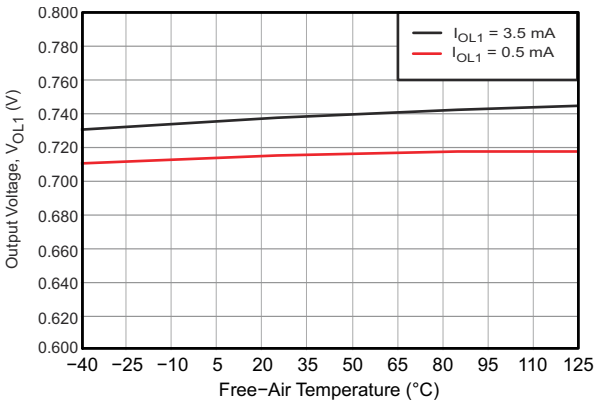
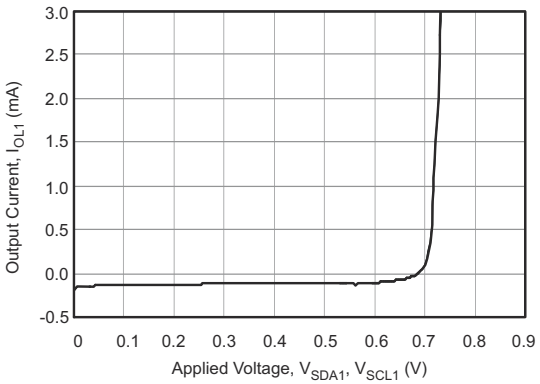
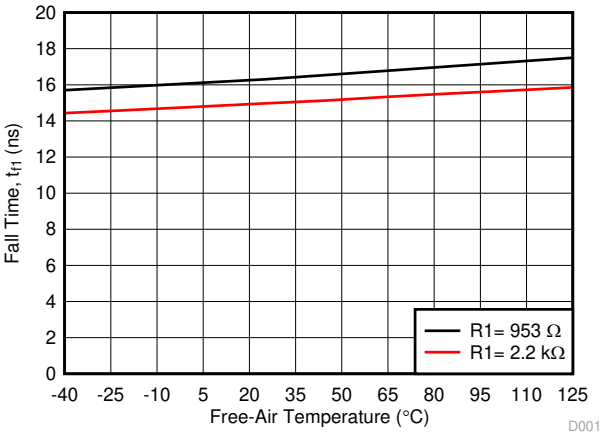


図 6-2. Side 1: Output Low Voltage vs Free-Air Temperature



T_A = 25°C

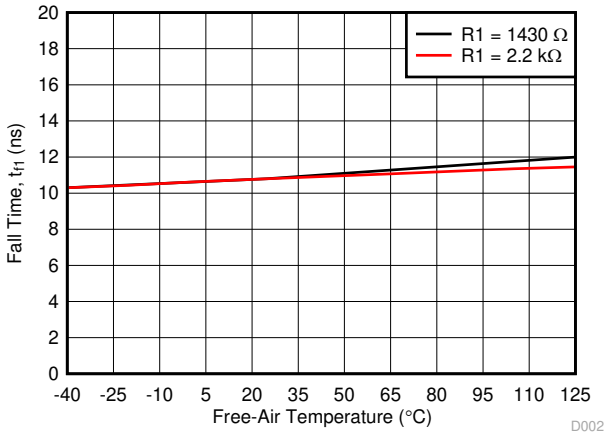
図 6-3. Side 1: Output Low Current vs S_{DA1} or S_{CL1} Applied Voltage



VCC1 = 3.3 V C1 = 40 pF

Fall time measured from 70% to 30% VCC1

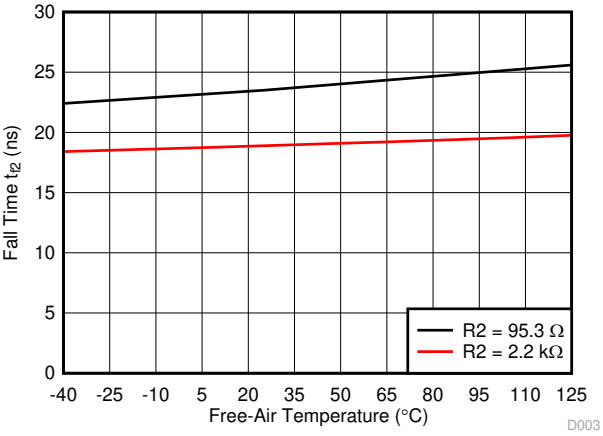
図 6-4. Side 1: Output Fall Time vs Free-Air Temperature



VCC1 = 5 V C1 = 40 pF

Fall time measured from 70% to 30% VCC1

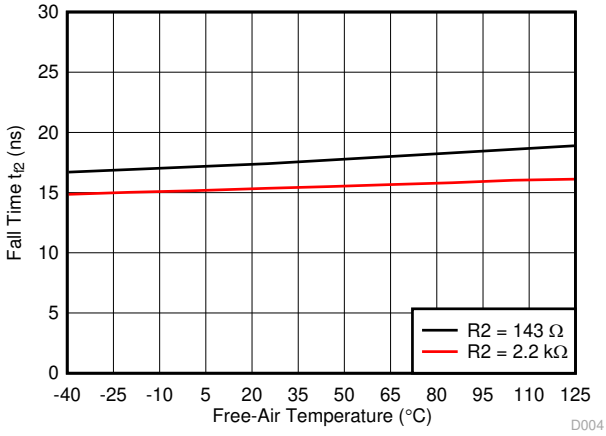
図 6-5. Side 1: Output Fall Time vs Free-air Temperature



VCC2 = 3.3 V C2 = 400 pF

Fall time measured from 70% to 30% VCC2

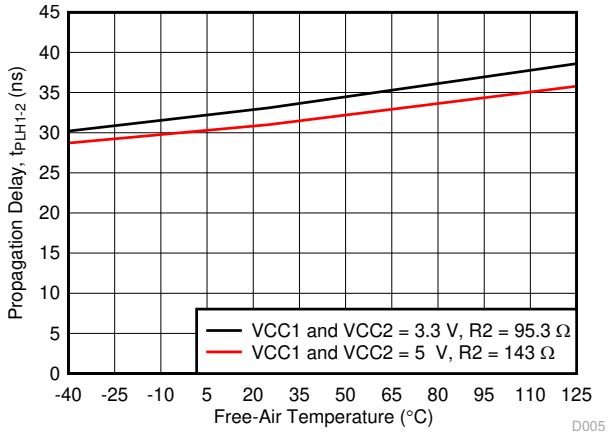
図 6-6. Side 2: Output Fall Time vs Free-Air Temperature



VCC2 = 5 V C2 = 400 pF

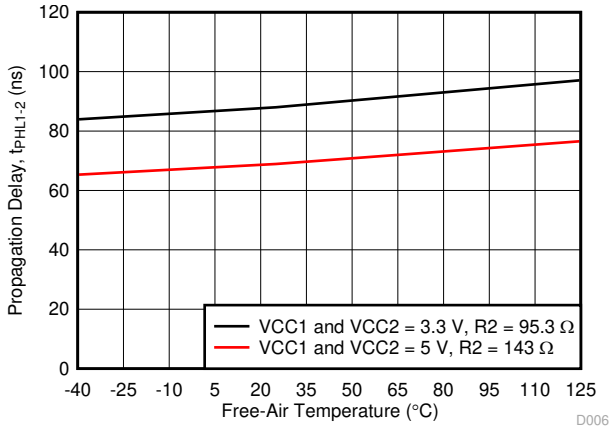
Fall time measured from 70% to 30% VCC2

図 6-7. Side 2: Output Fall Time vs Free-Air Temperature



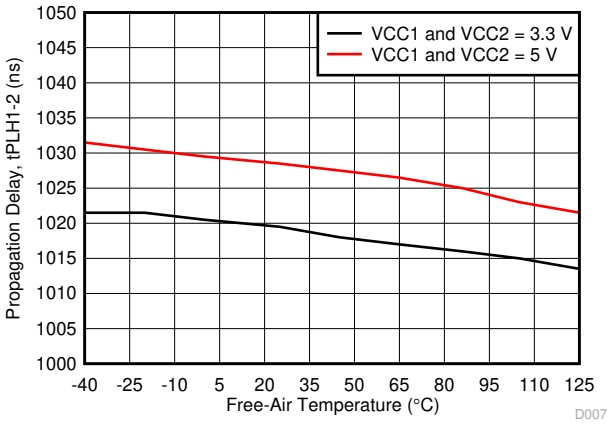
C2 = 10 pF

図 6-8. t_{PLH1-2} Propagation Delay vs Free-Air Temperature



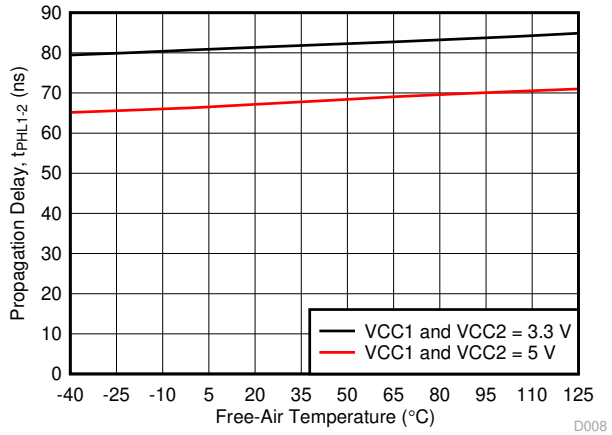
C2 = 10 pF

図 6-9. t_{PHL1-2} Propagation Delay vs Free-Air Temperature



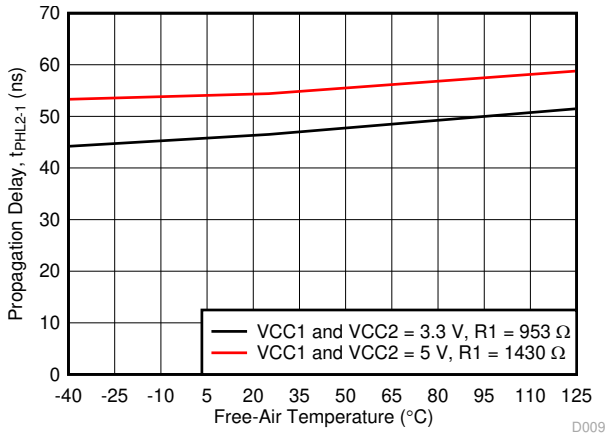
R2 = 2.2 kΩ C2 = 400 pF

図 6-10. t_{PLH1-2} Propagation Delay vs Free-Air Temperature



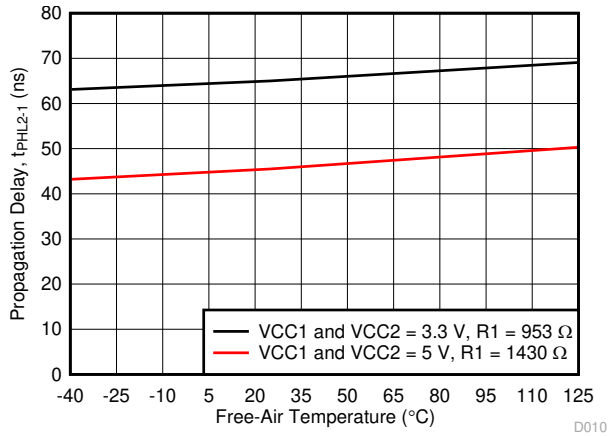
R2 = 2.2 kΩ C2 = 400 pF

図 6-11. t_{PHL1-2} Propagation Delay vs Free-Air Temperature



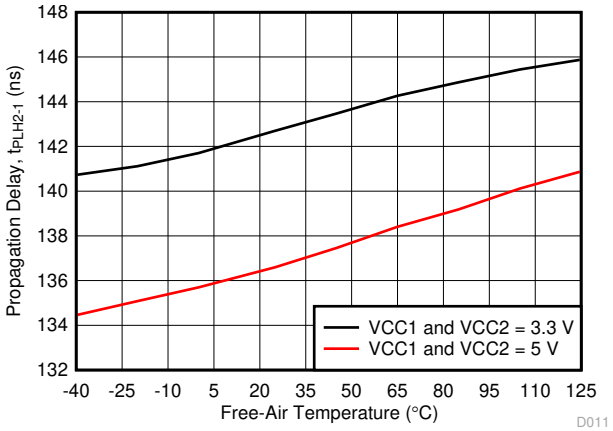
C1 = 10 pF

図 6-12. t_{PLH2-1} Propagation Delay vs Free-Air Temperature



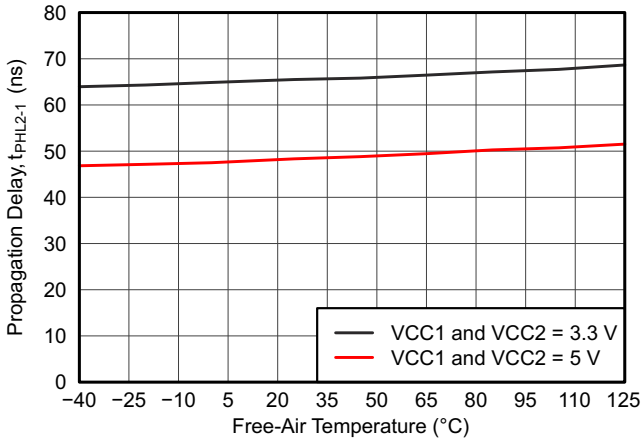
C1 = 10 pF

図 6-13. t_{PHL2-1} Propagation Delay vs Free-Air Temperature



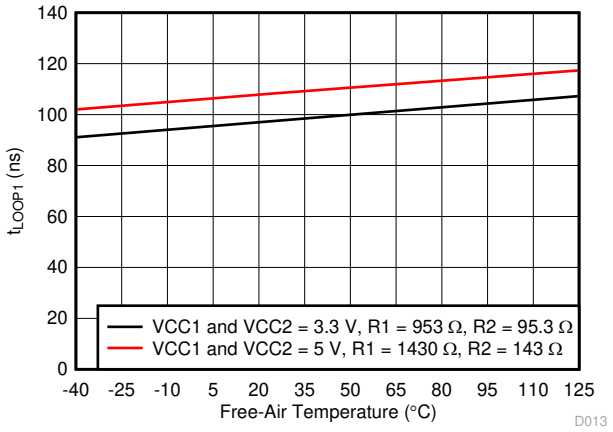
R1 = 2.2 kΩ C1 = 40 pF

図 6-14. t_{PLH2-1} Propagation Delay vs Free-Air Temperature



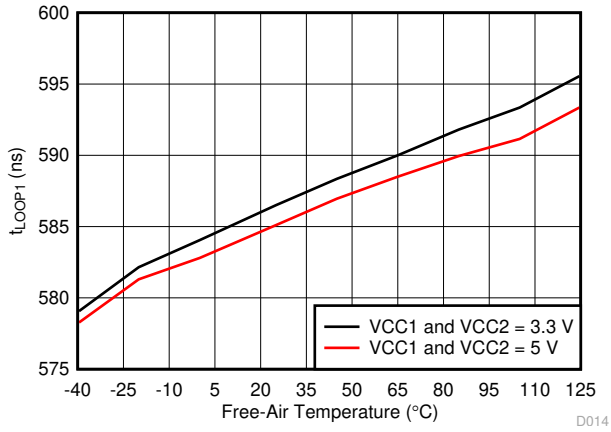
R1 = 2.2 kΩ C1 = 40 pF

図 6-15. t_{PHL2-1} Propagation Delay vs Free-Air Temperature



C1 = 40 pF C2 = 400 pF

図 6-16. t_{LOOP1} vs Free-Air Temperature



C1 = 40 pF C2 = 400 pF
R1 = 2.2 kΩ R2 = 2.2 kΩ

図 6-17. t_{LOOP1} vs Free-Air Temperature

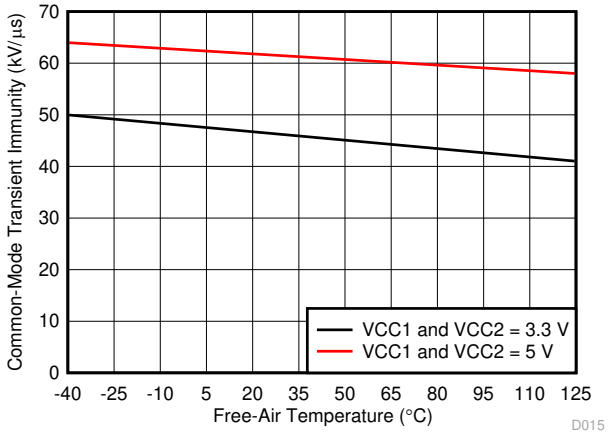


図 6-18. CMTI vs Free-Air Temperature

Parameter Measurement Information

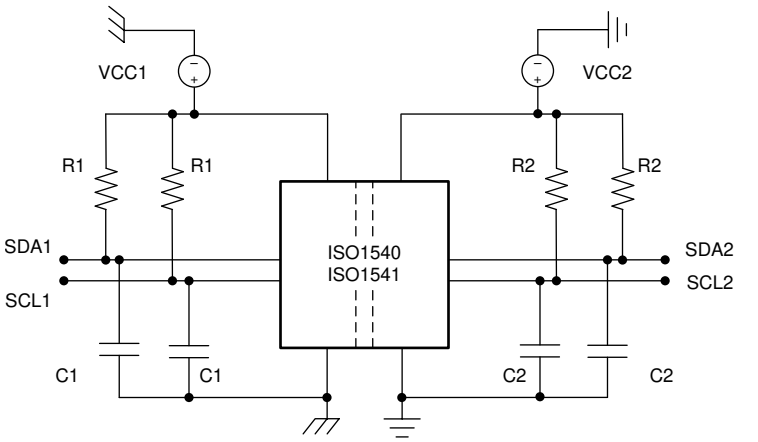


図 7-1. Test Diagram

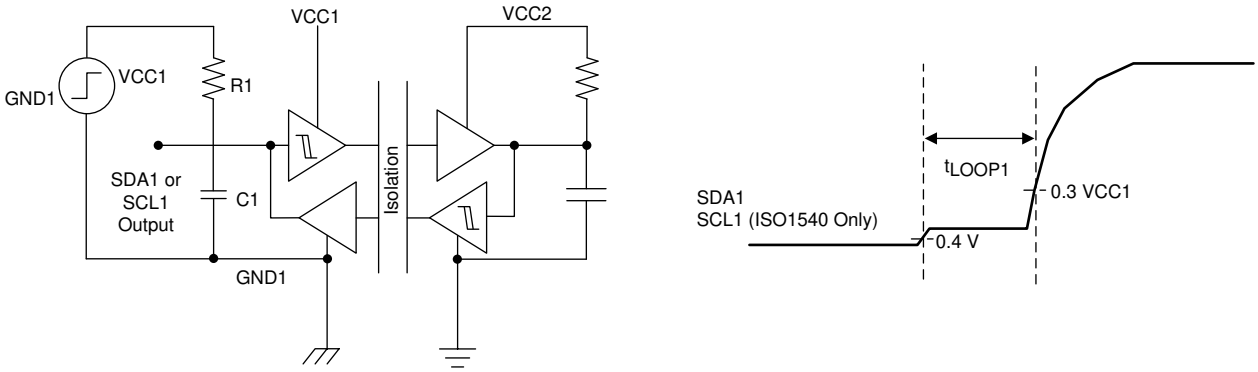


図 7-2. t_{Loop1} Setup and Timing Diagram

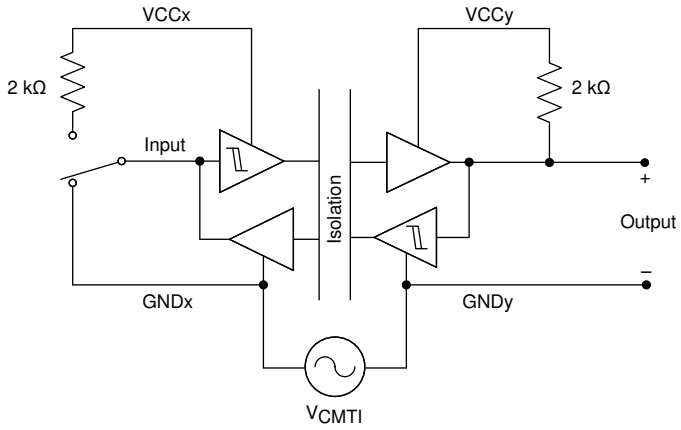
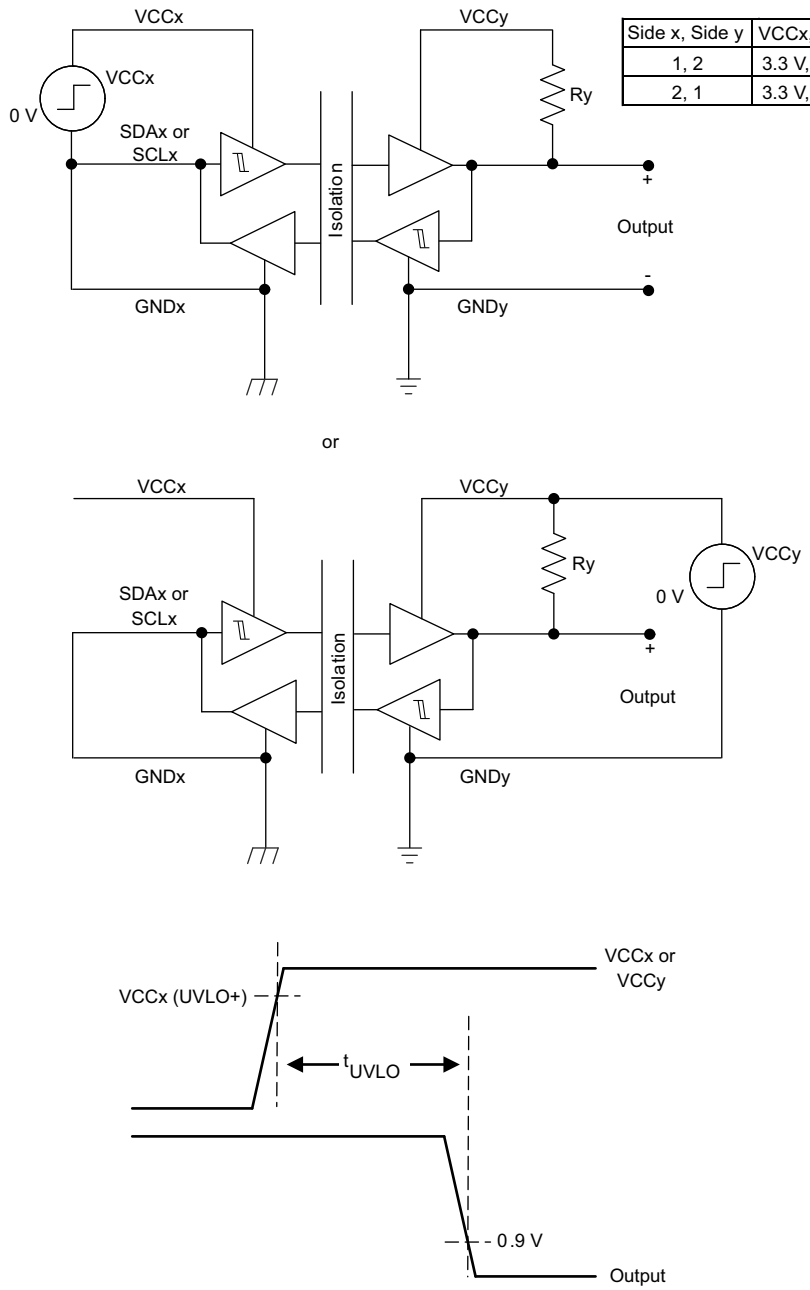


図 7-3. Common-Mode Transient Immunity Test Circuit



Side x, Side y	VCCx,VCCy	Ry
1, 2	3.3 V, 3.3 V	95.3 Ω
2, 1	3.3 V, 3.3 V	953 Ω

図 7-4. t_{UVLO} Test Circuit and Timing Diagrams

7 Detailed Description

7.1 Overview

The I^2C bus is used in a wide range of applications because it is simple to use. The bus consists of a two-wire communication bus that supports bidirectional data transfer between a controller device and several target devices. The controller, or processor, controls the bus, specifically the serial clock (SCL) line. Data is transferred between the controller and target through a serial data (SDA) line. This data can be transferred in four speeds: standard mode (0 to 100 kbps), fast mode (0 to 400 kbps), fast-mode plus (0 to 1 Mbps), and high-speed mode (0 to 3.4 Mbps). The most common speeds are the standard and fast modes.

The I^2C bus operates in bidirectional, half-duplex mode, while standard digital isolators are unidirectional devices. To make efficient use of one technology supporting the other, external circuitry is required that separates the bidirectional bus into two unidirectional signal paths without introducing significant propagation delay. These devices have their logic input and output buffers separated by TI's capacitive isolation technology using a silicon dioxide (SiO_2) barrier. When used in conjunction with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

7.2 Functional Block Diagrams

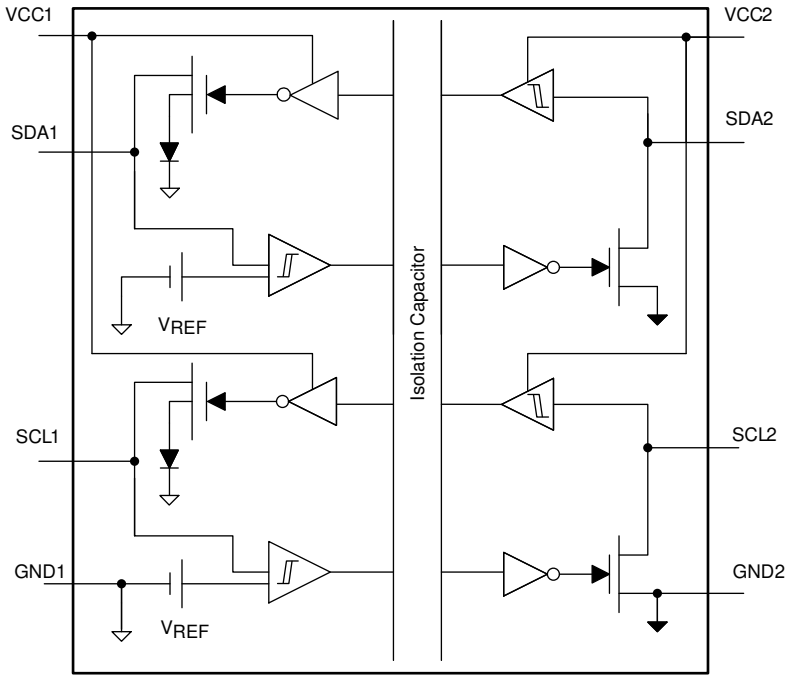


図 7-1. ISO1540-Q1 Block Diagram

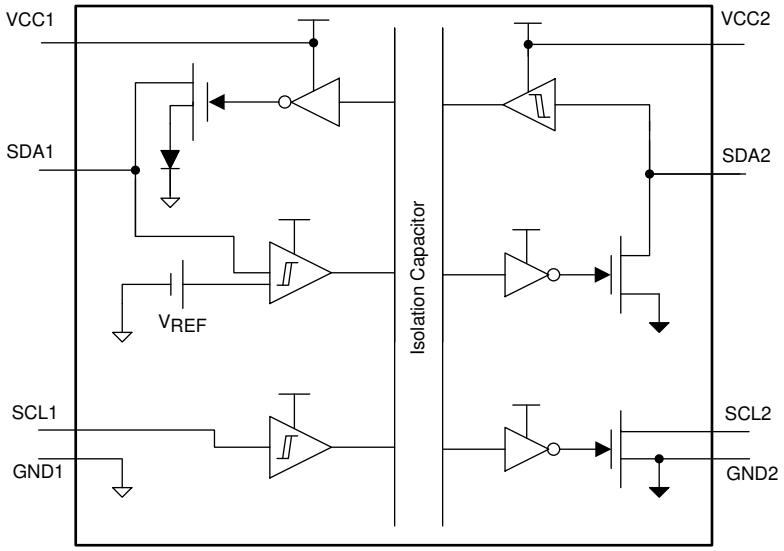


図 7-2. ISO1541-Q1 Block Diagram

7.3 Feature Description

The device enables a complete isolated I^2C interface to be implemented within a small form factor having the features listed in 表 7-1.

表 7-1. Features List

PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION(1)	MAXIMUM FREQUENCY
ISO1540-Q1	Bidirectional (SCL) Bidirectional (SDA)	2500 V_{RMS} 4242 V_{PK}	1 MHz
ISO1541-Q1	Unidirectional (SCL) Bidirectional (SDA)		

(1) See *セクション 6.7* for detailed Isolation specifications.

7.4 Isolator Functional Principle

To isolate a bidirectional signal path (SDA or SCL), the ISO1540-Q1 internally splits a bidirectional line into two unidirectional signal lines, each of which is isolated through a single-channel digital isolator. Each channel output is made open-drain to comply with the open-drain technology of I^2C. Side 1 of the ISO1540-Q1 connects to a low-capacitance I^2C node, while side 2 is designed for connecting to a fully loaded I^2C bus with up to 400 pF of capacitance.

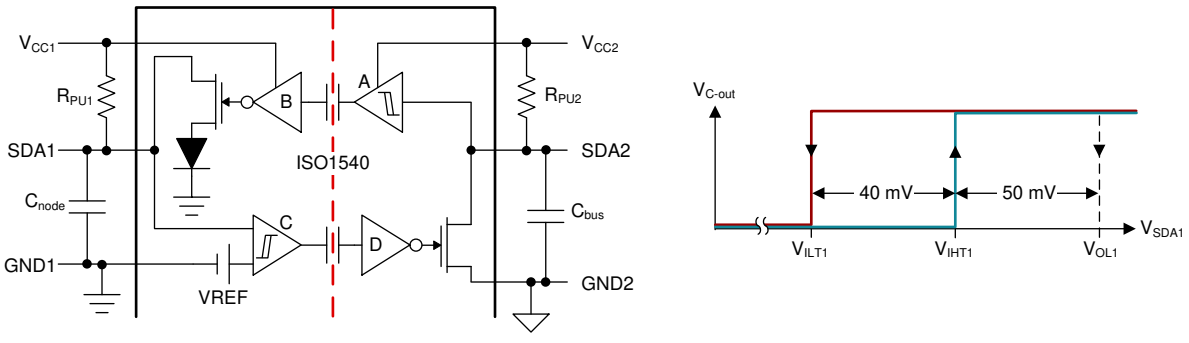


図 7-3. SDA Channel Design and Voltage Levels at SDA1

At first sight, the arrangement of the internal buffers suggests a closed signal loop that is prone to latch-up. However, this loop is broken by implementing an output buffer (B) whose output low-level is raised by a diode drop to approximately 0.75 V, and the input buffer (C) that consists of a comparator with defined hysteresis. The

comparator's upper and lower input thresholds then distinguish between the proper low-potential of 0.4 V (maximum) driven directly by SDA1 and the buffered output low-level of B.

図 7-4 demonstrate the switching behavior of the I²C isolator, ISO1540-Q1, between a controller node at SDA1 and a heavy loaded bus at SDA2.

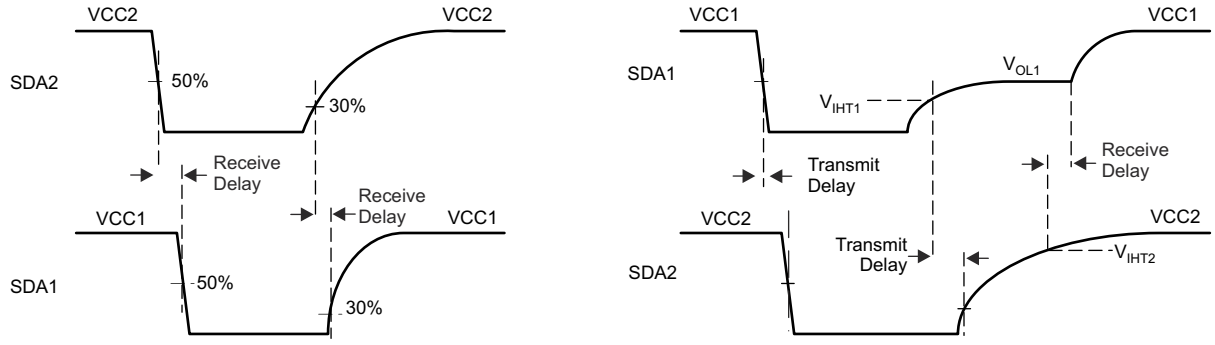


図 7-4. SDA Channel Timing in Receive and Transmit Directions

7.4.1 Receive Direction (Left Diagram of)

When the I²C bus drives SDA2 low, SDA1 follows after a certain delay in the receive path. The output low is the buffered output of V_{OL1} = 0.75 V, which is sufficiently low to be detected by Schmitt-trigger inputs with a minimum input-low voltage of V_{IL} = 0.9 V at 3 V supply levels.

When SDA2 is released, its voltage potential increases towards VCC2 following the time-constant formed by R_{PU2} and C_{bus}. After the receive delay, SDA1 is released and also rises towards VCC1, following the time-constant R_{PU1} × C_{node}. Because of the significant lower time-constant, SDA1 may reach VCC1 before SDA2 reaches VCC2 potential.

7.4.2 Transmit Direction (Right Diagram of)

When a controller drives SDA1 low, SDA2 follows after a certain delay in the transmit direction. When SDA2 turns low it also causes the output of buffer B to turn low but at a higher 0.75 V level. This level cannot be observed immediately as it is overwritten by the lower low-level of the controller.

However, when the controller releases SDA1, the voltage potential increases and first must pass the upper input threshold of the comparator, V_{IHT1}, to release SDA2. SDA1 then increases further until it reaches the buffered output level of V_{OL1} = 0.75 V, maintained by the receive path. When comparator C turns high, SDA2 is released after the delay in transmit direction. It takes another receive delay until B's output turns high and fully releases SDA1 to move toward VCC1 potential.

7.5 Device Functional Modes

表 7-2 lists the ISO154x-Q1 functional modes.

表 7-2. Function Table

POWER STATE	INPUT	OUTPUT
VCC1 or VCC2 < 2.1 V	X	Z
VCC1 and VCC2 > 2.8 V	L	L
VCC1 and VCC2 > 2.8 V	H	Z
VCC1 and VCC2 > 2.8 V	Z(1)	?

(1) Invalid input condition as an I²C system requires that a pullup resistor to VCC is connected.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 I²C Bus Overview

The inter-integrated circuit (I^2C) bus is a single-ended, multi-controller, 2-wire bus for efficient inter-IC communication in half-duplex mode.

I^2C uses open-drain technology, requiring two lines, serial data (SDA) and serial clock (SCL), to be connected to VDD by resistors (see 図 8-1). Pulling the line to ground is considered a logic zero while letting the line float is a logic one. This logic is used as a channel access method. Transitions of logic states must occur while the SCL pin is low. Transitions while the SCL pin is high indicate START and STOP conditions. Typical supply voltages are 3.3 V and 5 V, although systems with higher or lower voltages are allowed.

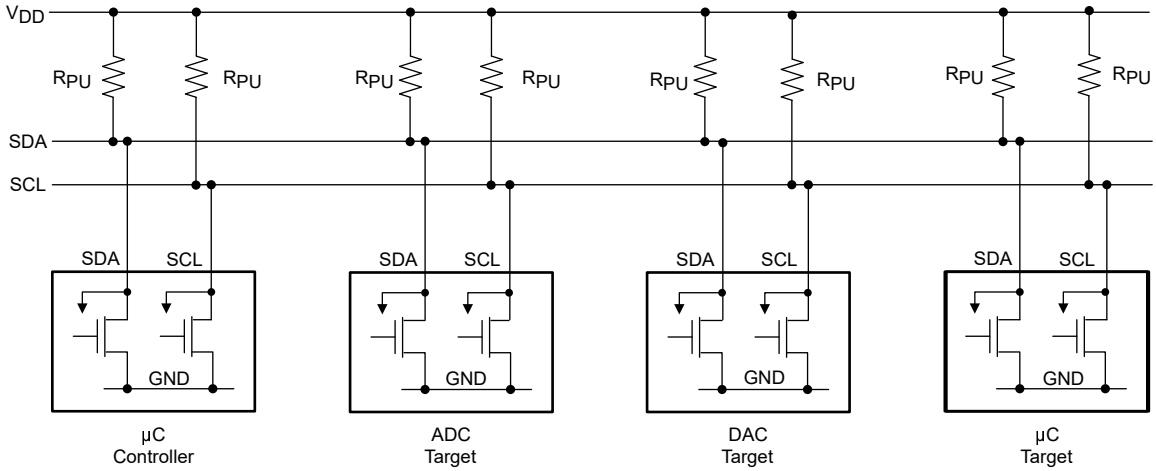


図 8-1. I^2C Bus

I^2C communication uses a 7-bit address space with 16 reserved addresses, so a theoretical maximum of 112 nodes can communicate on the same bus. In praxis, however, the number of nodes is limited by the specified, total bus capacitance of 400 pF, which restricts communication distances to a few meters.

The specified signaling rates for the ISO1540-Q1 and ISO1541-Q1 devices are 100 kbps (standard mode), 400 kbps (fast mode), 1 Mbps (fast mode plus).

The bus has two roles for nodes: controller and target. A controller node issues the clock and target addresses, and also initiates and ends data transactions. A target node receives the clock and addresses and responds to requests from the controller. 図 8-2 shows a typical data transfer between controller and target.

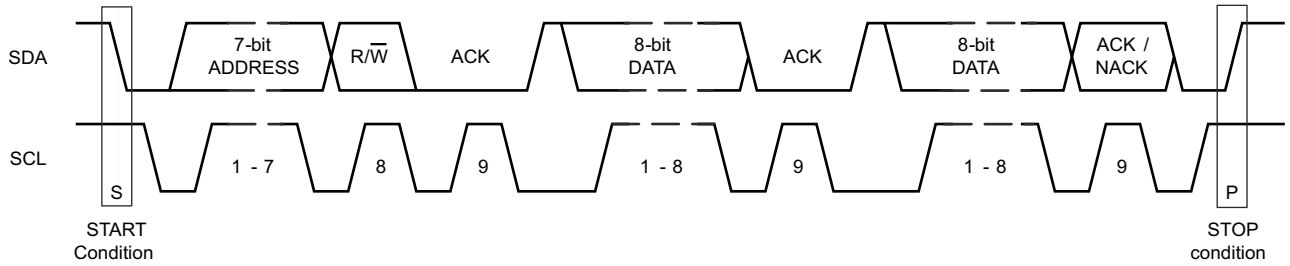


図 8-2. Timing Diagram of a Complete Data Transfer

The controller initiates a transaction by creating a START condition, following by the 7-bit address of the target it wishes to communicate with. This is followed by a single read and write (R/W) bit, representing whether the controller wishes to write to 0, or to read from 1 the target. The controller then releases the SDA line to allow the target to acknowledge the receipt of data.

The target responds with an acknowledge bit (ACK) by pulling the SDA pin low during the entire high time of the 9th clock pulse on the SCL signal, after which the controller continues in either transmit or receive mode (according to the R/W bit sent), while the target continues in the complementary mode (receive or transmit, respectively).

The address and the 8-bit data bytes are sent most significant bit (MSB) first. The START bit is indicated by a high-to-low transition of SDA while SCL is high. The STOP condition is created by a low-to-high transition of SDA while SCL is high.

If the controller writes to a target, it repeatedly sends a byte with the target sending an ACK bit. In this case, the controller is in controller-transmit mode and the target is in target-receive mode.

If the controller reads from a target, it repeatedly receives a byte from the target, while acknowledging (ACK) the receipt of every byte but the last one (see 図 8-3). In this situation, the controller is in controller-receive mode and the target is in target-transmit mode.

The controller ends the transmission with a STOP bit, or may send another START bit to maintain bus control for further transfers.

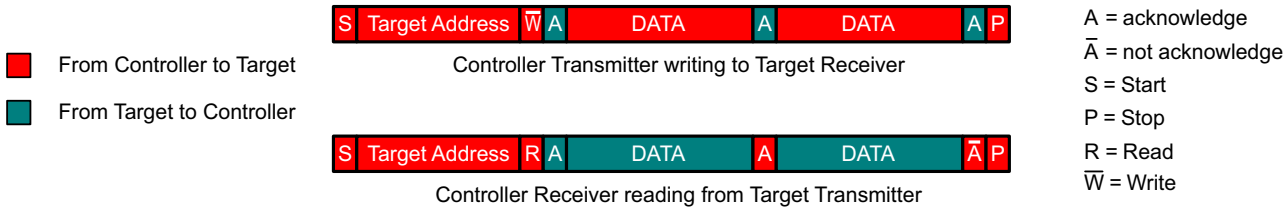


図 8-3. Transmit or Receive Mode Changes During a Data Transfer

When writing to a target, a controller mainly operates in transmit-mode and only changes to receive-mode when receiving acknowledgment from the target.

When reading from a target, the controller starts in transmit-mode and then changes to receive-mode after sending a READ request (R/W bit = 1) to the target. The target continues in the complementary mode until the end of a transaction.

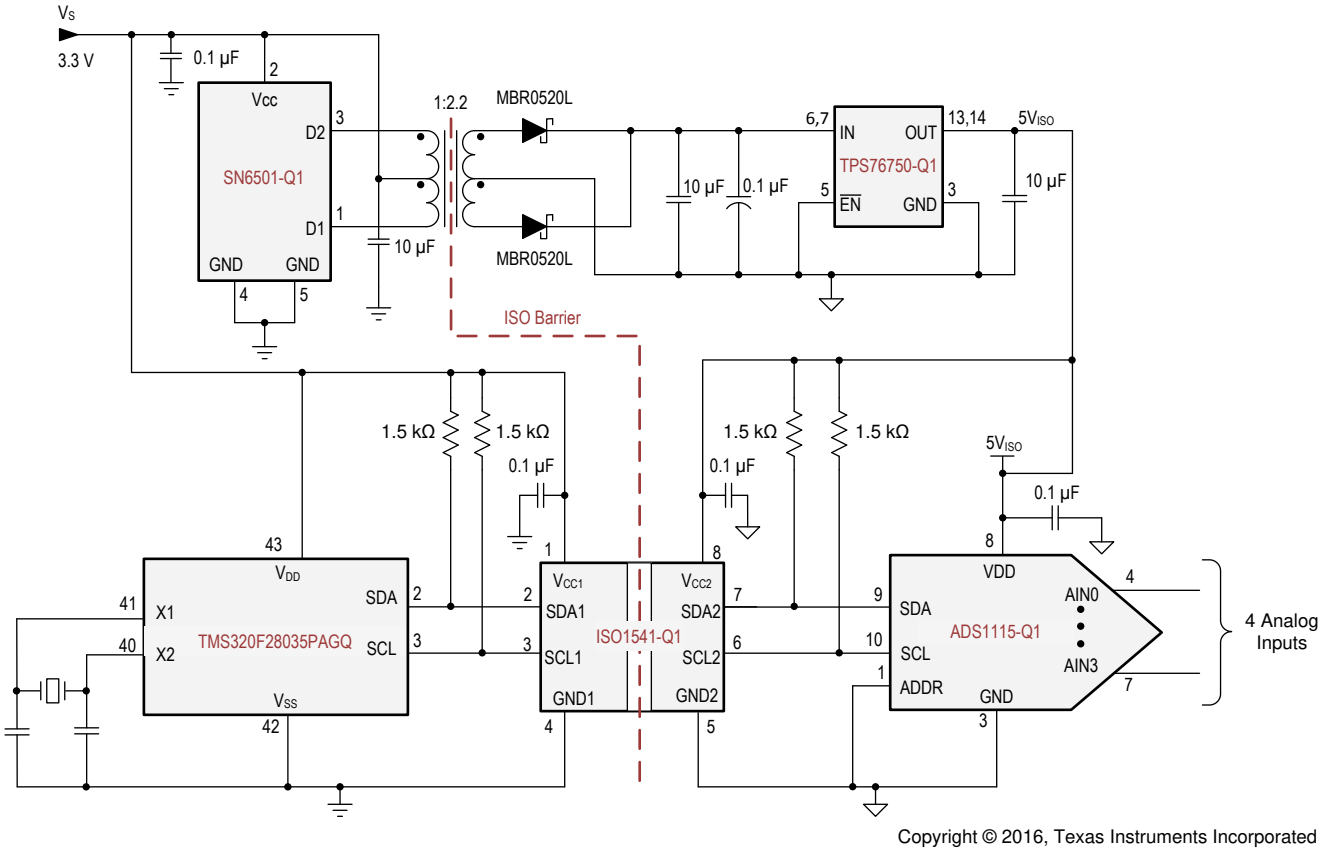
注

The controller ends a reading sequence by not acknowledging (NACK) the last byte received. This procedure resets the target state machine and allows the controller to send the STOP command.

8.2 Typical Application

図 8-4 shows isolated I²C data acquisition system built with TI microcontroller, analog-to-digital converter, and I²C isolator, ISO1541-Q1.

The entire circuit operates from a single 3.3-V supply. A low-power push-pull converter, SN6501-Q1, drives a center-tapped transformer with an output that is rectified and linearly regulated to provide a stable 5-V supply for the data converter.



Copyright © 2016, Texas Instruments Incorporated

図 8-4. Isolated I²C Data Acquisition System

8.2.1 Design Requirements

The recommended power supply voltages (VCC1 and VCC2) must be from 3 V to 5.5 V. A recommended decoupling capacitor with a value of 0.1 µF is required between both the VCC1 and GND1 pins, and the VCC2 and GND2 pins to support of power supply voltages transient and to ensure reliable operation at all data rates.

8.2.2 Detailed Design Procedure

The power-supply capacitor with a value of 0.1-µF must be placed as close to the power supply pins as possible. The recommended placement of the capacitors must be 2-mm maximum from input and output power supply pins (VCC1 and VCC2).

The maximum load permissible on the input lines, SDA1 and SCL1, is ≤ 40 pF and on the output lines, SDA2 and SCL2, is ≤ 400 pF.

The minimum pullup resistors on the input lines, SDA1 and SCL1 to VCC1 must be selected in such a way that input current drawn is ≤ 3.5 mA. The minimum pullup resistors on the input lines, SDA2 and SCL2, to VCC2 must be selected in such a way that output current drawn is ≤ 35 mA. The maximum pullup resistors on the input

lines (SDA1 and SCL1) to VCC1 and on output lines (SDA1 and SCL1) to VCC2, depends on the load and rise time requirements on the respective lines.

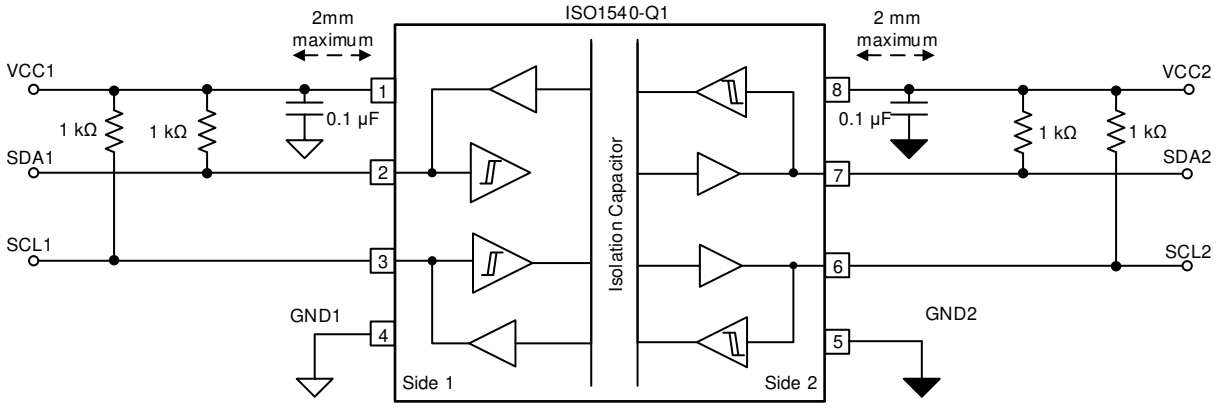


図 8-5. Typical ISO1540-Q1 Circuit Hookup

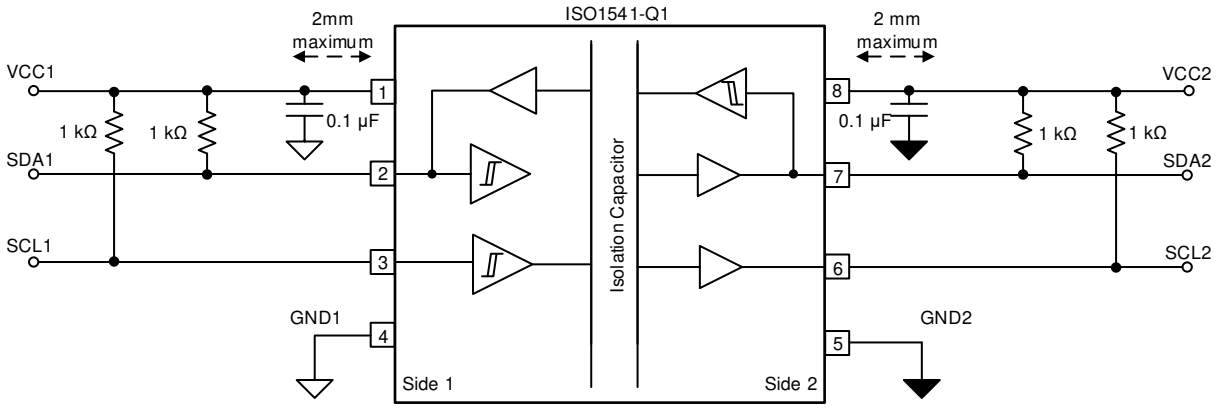


図 8-6. Typical ISO1541-Q1 Circuit Hookup

8.2.3 Application Curve

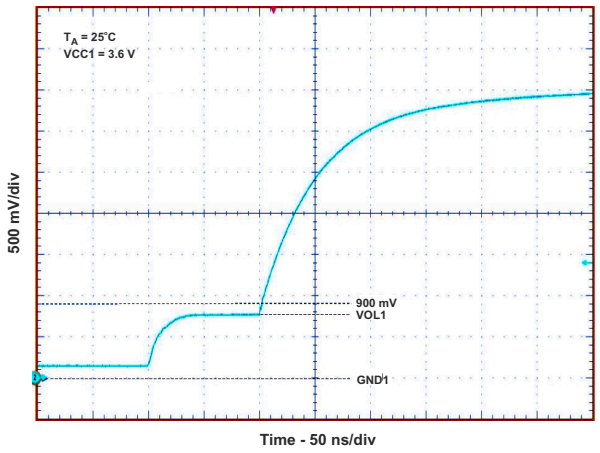


図 8-7. Side 1: Low-to-High Transition

9 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, TI recommends connecting a 0.1-µF bypass capacitor at the input and output supply pins (VCC1 and VCC2). The capacitors should be placed as close to the supply pins as possible. If only a single, primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's SN6501-Q1 device. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies* (SLLSEF3).

10 Layout

10.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 10-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the *Digital Isolator Design Guide* (SLLA284)

10.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

10.2 Layout Example

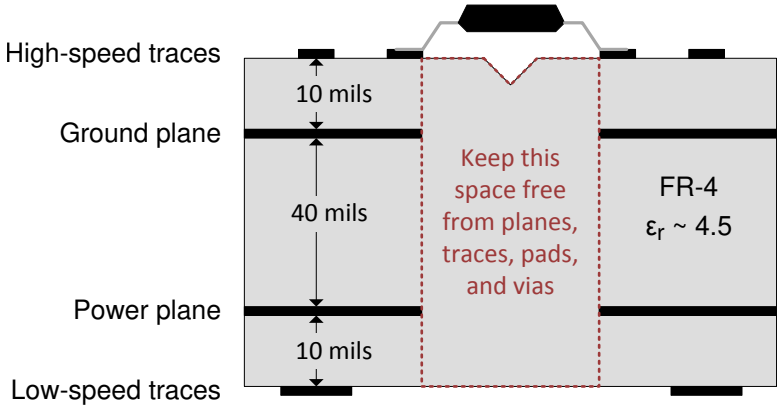


図 10-1. Recommended Layer Stack

11 Device and Documentation Support

11.1 Documentation Support

注

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

11.1.1 Related Documentation

For related documentation see the following:

- *Digital Isolator Design Guide* (SLLA284)
- *TI Isolation Glossary* (SLLA353)
- *SN6501-Q1 Transformer Driver for Isolated Power Supplies.* (SLLSEF3)
- TPS767xx-Q1 *Fast-Transient-Response 1-A Low-Dropout Voltage Regulators* (SGLS009)
- *ADS1115-Q1 Low-Power, 16-Bit Analog-to-Digital Converter With Internal Reference* (SBAS563)
- *TMS320F2803x Piccolo™ Microcontrollers* (TMS320F2803x Piccolo™ Microcontrollers)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO1540-Q1	Click here	Click here	Click here	Click here	Click here
ISO1541-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

11.5 Trademarks

Piccolo™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO1540QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I1540Q
ISO1540QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I1540Q
ISO1541QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I1541Q
ISO1541QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I1541Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF ISO1540-Q1, ISO1541-Q1 :

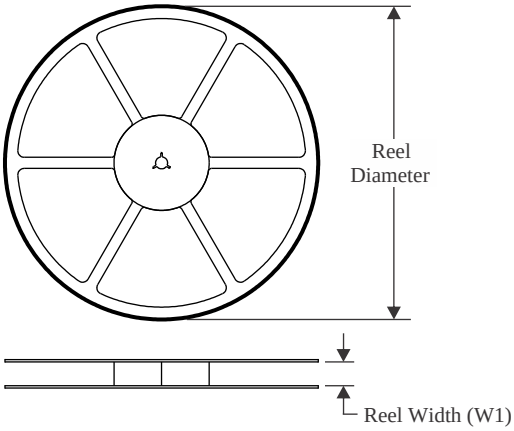
- Catalog : ISO1540, ISO1541

NOTE: Qualified Version Definitions:

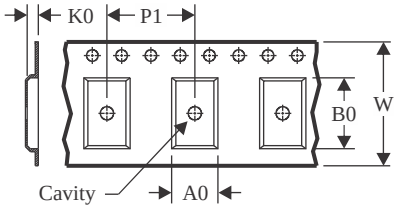
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

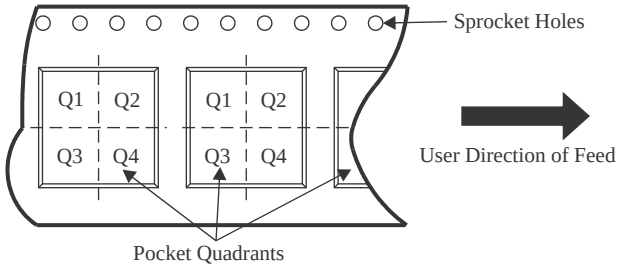


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

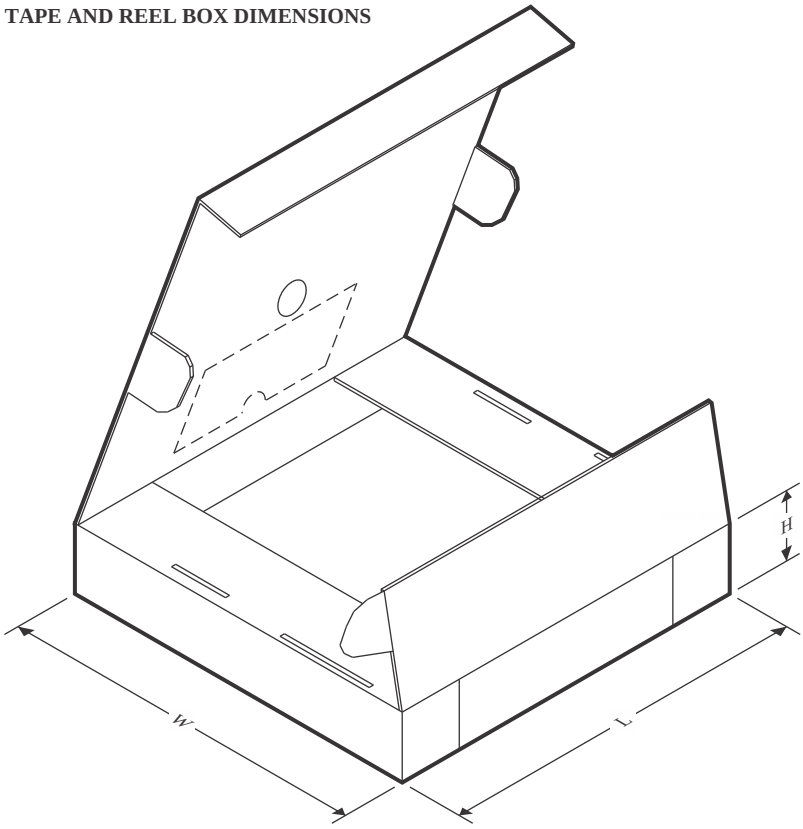
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

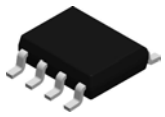
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1540QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO1540QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO1541QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1540QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO1540QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
ISO1541QDRQ1	SOIC	D	8	2500	350.0	350.0	43.0

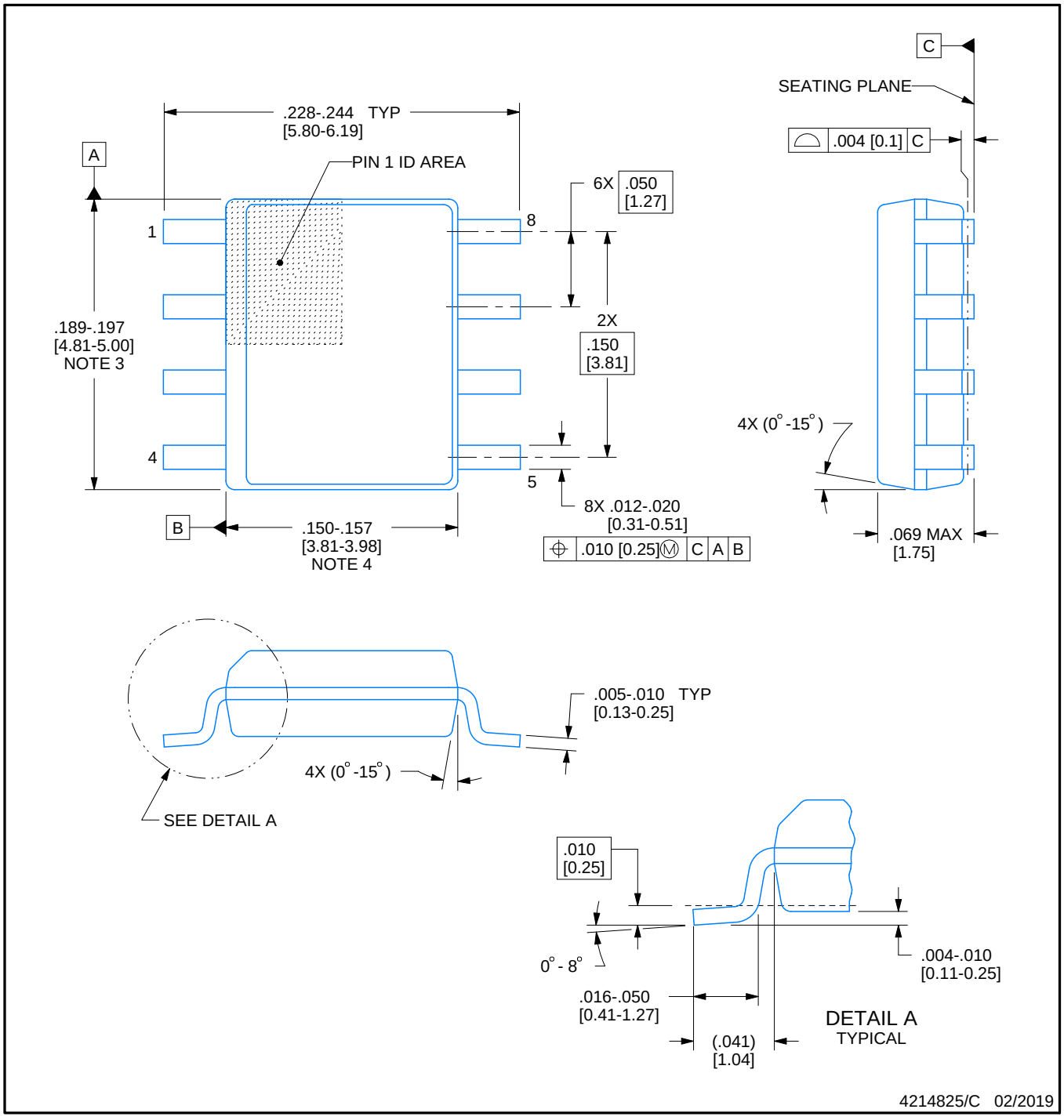


PACKAGE OUTLINE

D0008A

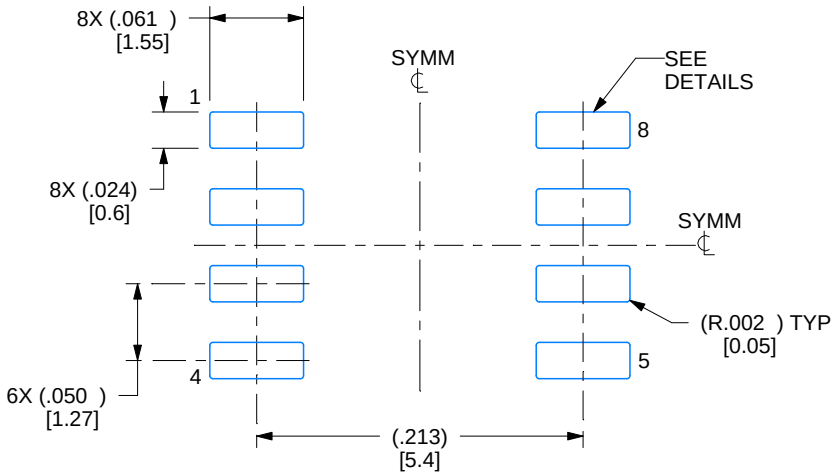
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

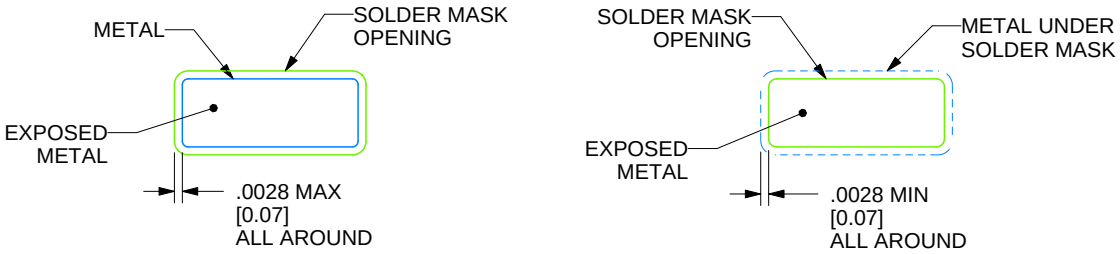


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

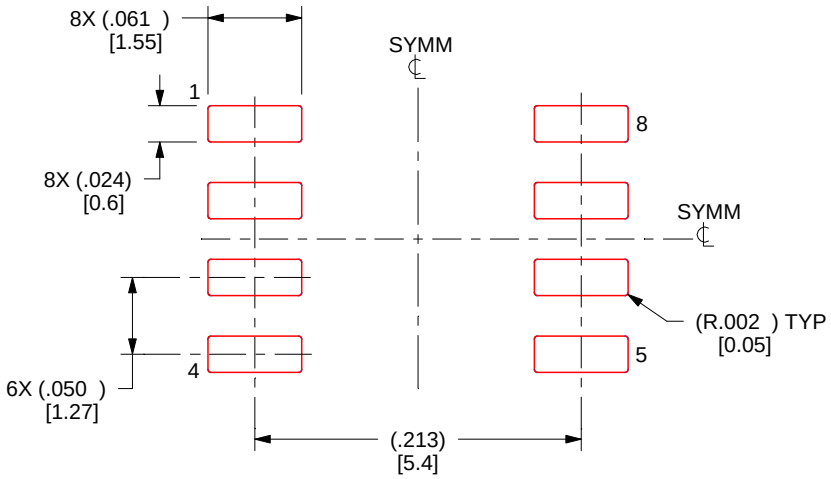
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月