

JFE150 超低ノイズ、低ゲート電流、オーディオ、N チャネル JFET



1 特長

- 超低ノイズ:
 - 電圧ノイズ:
 - 1kHz, $I_{DS} = 5\text{mA}$ で $0.8\text{nV}/\sqrt{\text{Hz}}$
 - 1kHz, $I_{DS} = 2\text{mA}$ で $0.9\text{nV}/\sqrt{\text{Hz}}$
 - 電流ノイズ: 1kHz で $1.8\text{fA}/\sqrt{\text{Hz}}$
- 低ゲート電流: 10pA (最大値)
- 低入力容量: $V_{DS} = 5\text{V}$ で 24pF
- ゲート・ドレイン間およびゲート・ソース間の高ブレイクダウン電圧: -40V
- 高相互コンダクタンス: 68mS
- パッケージ: 小型 SC70 および SOT-23

2 アプリケーション

- マイクロフォン入力
- ハイドロフォンと海洋機器
- DJ コントローラ、ミキサ、その他の DJ 機器
- 業務用オーディオ・ミキサ / 制御卓
- ギターアンプ / その他楽器用アンプ
- 状況監視センサ

3 概要

JFE150 は、テキサス・インスツルメンツの最新の高性能アナログ・バイポーラ・プロセスで構築された Burr-Brown™ ディスクリート JFET です。JFE150 は、従来のディスクリート JFET テクノロジでは利用できなかった性能を備えています。JFE150 は、ノイズから電力までの効率と柔軟性

を最大化します。この場合、静止電流をユーザーが設定し、 $50\mu\text{A} \sim 20\text{mA}$ の電流で優れたノイズ性能を発揮できます。 5mA でバイアスすると、入力換算ノイズ $0.8\text{nV}/\sqrt{\text{Hz}}$ が得られ、超高入力インピーダンス ($1\text{T}\Omega$ 超) で超低ノイズ性能を実現します。JFE150 は、個別のクランプ・ノードに接続されたダイオードも内蔵しており、高リークの非線形外部ダイオードを追加せずに保護機能を提供します。

JFE150 は、高ドレイン・ソース間で 40V、ゲート・ソース間、ゲート・ドレイン間で -40V の電圧です。温度範囲は $-40^\circ\text{C} \sim +125^\circ\text{C}$ で規定され、5 ピンの SOT-23 および SC-70 パッケージで供給されます。

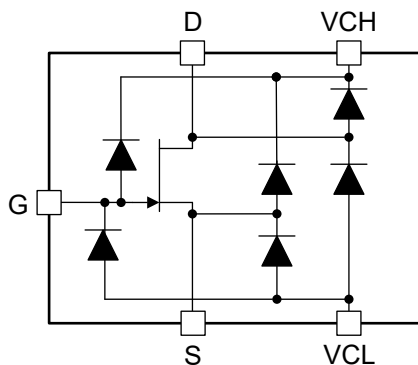
パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
JFE150	DBV (SOT-23, 5)	2.90mm × 1.60mm
	DCK (SC70, 5)	2.00mm × 1.25mm

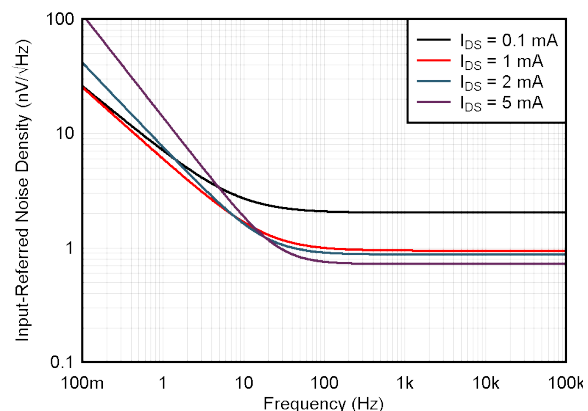
(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

デバイスの概要

パラメータ	値
V_{GSS}	ゲート・ソース間ブレイクダウン電圧 -40V
V_{DSS}	ドレイン・ソース間ブレイクダウン電圧 $\pm 40\text{V}$
C_{ISS}	入力容量 24pF
T_J	接合部温度 $-40^\circ\text{C} \sim +125^\circ\text{C}$
I_{DSS}	ドレイン・ソース間飽和電流 35mA



機能ブロック図



超低入力電圧ノイズ



Table of Contents

1 特長.....	1	8.3 Feature Description.....	9
2 アプリケーション.....	1	8.4 Device Functional Modes.....	10
3 概要.....	1	9 Application and Implementation.....	11
4 Revision History.....	2	9.1 Application Information.....	11
5 Pin Configuration and Functions.....	3	9.2 Typical Application.....	14
6 Specifications.....	4	9.3 Power Supply Recommendations.....	16
6.1 Absolute Maximum Ratings.....	4	9.4 Layout.....	16
6.2 ESD Ratings.....	4	10 Device and Documentation Support.....	17
6.3 Recommended Operating Conditions.....	4	10.1 Device Support.....	17
6.4 Thermal Information.....	4	10.2 Documentation Support.....	18
6.5 Electrical Characteristics.....	5	10.3 ドキュメントの更新通知を受け取る方法.....	18
6.6 Typical Characteristics.....	6	10.4 サポート・リソース.....	18
7 Parameter Measurement Information.....	8	10.5 Trademarks.....	18
7.1 AC Measurement Configurations.....	8	10.6 静電気放電に関する注意事項.....	18
8 Detailed Description.....	9	10.7 用語集.....	18
8.1 Overview.....	9	11 Mechanical, Packaging, and Orderable Information.....	18
8.2 Functional Block Diagram.....	9		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2021) to Revision B (April 2023)	Page
• DBV パッケージ (SOT-23、5) をプレビューから量産データ (アクティブ) に変更し、関連コンテンツを追加.....	1
• 「電気的特性」と一致するように「デバイスの概要」表のパラメータの説明を「ゲート・ソース間電圧」から「ゲート・ソース間ブレークダウン電圧」に、「ドレイン・ソース間電圧」から「ドレイン・ソース間ブレークダウン電圧」に変更.....	1
• 「電気的特性」と一致するように「デバイスの概要」表の「ドレイン・ソース間飽和電流」の値を 36mA から 35mA に変更.....	1
• Changed VCH and VCL pin type and description in <i>Pin Functions</i> to reflect optional nature of diode clamps....	3
• Changed Figure 6-2, <i>Drain-to-Source Current vs Drain-to-Source Voltage</i> , to show correct V_{GS} values.....	6
• Changed Figure 8-1, V_{DS} vs I_{DS} , to show correct V_{GS} values and improve image resolution.....	10
• Added JFE150EVM user's guide and JFE150 Ultra-Low-Noise Pre-Amp application note to <i>Related Documentation</i>	18

Changes from Revision * (June 2021) to Revision A (November 2021)	Page
• Changed V_{GS} minimum from -1.1 V to -1.3 V (100 μA), -0.9 V to -1.1 V (2 mA)	5
• Changed Figure 6-3, <i>Drain-to-Source Current vs Drain-to-Source Voltage</i> , to show correct V_{GS} values.....	6

5 Pin Configuration and Functions

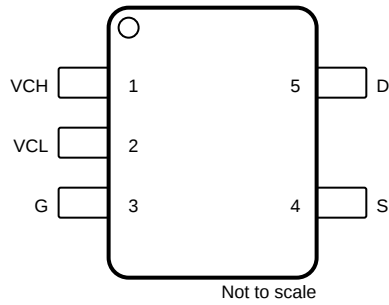


图 5-1. DBV, 5-Pin SOT-23 and DCK, 5-Pin SC70 Packages (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D	5	Output	Drain
G	3	Input	Gate
S	4	Output	Source
VCH	1	—	Positive diode clamp voltage. Float this pin if clamp diodes are not used.
VCL	2	—	Negative diode clamp voltage. Float this pin if clamp diodes are not used.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{DS}	Drain-to-source voltage	-40	40	V
V _{GS} , V _{GD}	Gate-to-source, gate-to-drain voltage	-40	0.9	V
V _{VCH}	Voltage between VCH to D, G, or S		40	V
V _{VCL}	Voltage between VCL to D, G, or S	-40		
I _{VCL} , I _{VCH}	Clamp diode current	DC	20	mA
		50-ms pulse ⁽²⁾	200	
I _{DS}	Drain-to-source current	-50	50	mA
I _{GS} , I _{GD}	Gate-to-source, gate-to-drain current	-20	20	mA
T _A	Ambient temperature	-55	150	°C
T _J	Junction temperature	-55	150	°C
T _{stg}	Storage temperature	-55	175	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Maximum diode current pulse specified for 50 ms at 1% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I _{DS}	Drain-to-source current	0.02		I _{DSS}	mA
V _{GS}	Gate-to-source voltage	0		-1.2	V
T _A	Specified temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		JFE150		UNIT
		DCK (SC70)	DBV (SOT-23)	
		5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	197.1	183.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	93.7	83.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	44.8	51.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	16.7	24.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	44.6	51.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

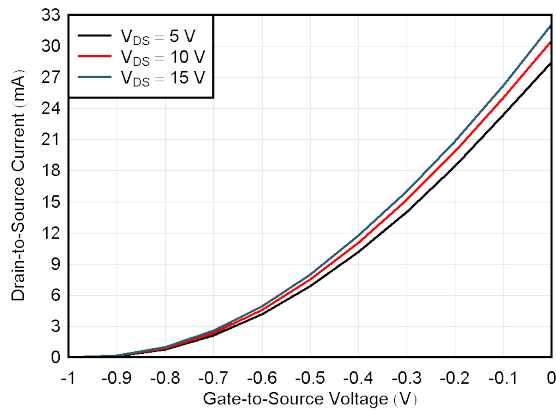
6.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $I_{DS} = 2\text{ mA}$, and $V_{DS} = 10\text{ V}$ (unless otherwise noted)

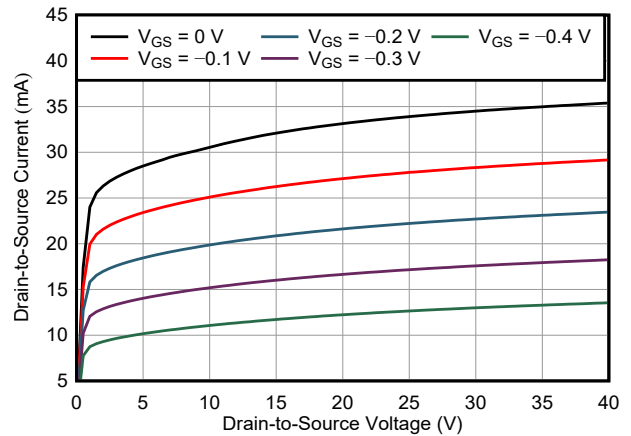
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE							
e_n	Input-referred voltage noise density	$I_{DS} = 100\ \mu\text{A}$, $V_{DS} = 5\text{ V}$	$f = 10\text{ Hz}$		3		nV/ $\sqrt{\text{Hz}}$
			$f = 1\text{ kHz}$		2		
		$I_{DS} = 2\text{ mA}$, $V_{DS} = 5\text{ V}$	$f = 10\text{ Hz}$		1.6		
			$f = 1\text{ kHz}$		0.9		
		$I_{DS} = 5\text{ mA}$, $V_{DS} = 5\text{ V}$	$f = 10\text{ Hz}$		1.8		
			$f = 1\text{ kHz}$		0.8		
Input-referred voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$, $V_{DS} = 5\text{ V}$	$I_{DS} = 100\ \mu\text{A}$		0.19		μV_{PP}	
		$I_{DS} = 2\text{ mA}$		0.09			
		$I_{DS} = 5\text{ mA}$		0.13			
e_i	Input current noise	$f = 1\text{ kHz}$, $V_{DS} = 5\text{ V}$			1.8		fA/ $\sqrt{\text{Hz}}$
INPUT CURRENT							
I_G	Input gate current	$V_{DS} = 2\text{ V}$, $V_{GS} = -0.7\text{ V}$, $V_{VCH} = 5\text{ V}$, $V_{VCL} = -5\text{ V}$		0.2	± 10	pA	
				0.2			
		$V_{DS} = 0\text{ V}$, $V_{GS} = -30\text{ V}$	$T_A = -40^\circ\text{C to }+85^\circ\text{C}$		± 2000		
			$T_A = -40^\circ\text{C to }+125^\circ\text{C}$		± 10000		
INPUT VOLTAGE							
V_{GSS}	Gate-to-source breakdown voltage	$V_{DS} = 0\text{ V}$, $ I_G < 100\ \mu\text{A}$			-40		V
V_{GSC}	Gate-to-source cutoff voltage	$V_{DS} = 10\text{ V}$, $I_{DS} = 0.1\ \mu\text{A}$		-1.5	-1.2	-0.9	V
V_{GS}	Gate-to-source voltage	$I_{DS} = 100\ \mu\text{A}$		-1.3		-0.7	V
		$I_{DS} = 2\text{ mA}$		-1.1		-0.5	
INPUT IMPEDANCE							
R_{IN}	Gate input resistance	$V_{GS} = -5\text{ V to }0\text{ V}$, $V_{DS} = 0\text{ V}$			1		T Ω
C_{ISS}	Input capacitance	$V_{DS} = 0\text{ V}$			30		pF
		$V_{DS} = 5\text{ V}$			24		
C_{RSS}	Reverse transfer capacitance	$V_{DS} = 0\text{ V}$			7		
OUTPUT							
I_{DSS}	Drain-to-source saturation current	$V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$		24	35	46	mA
			$T_A = -40^\circ\text{C to }+125^\circ\text{C}$	22		57	
g_m	Transconductance	$I_{DS} = 100\ \mu\text{A}$			3		mS
		$I_{DS} = 2\text{ mA}$			18		
G_{FS}	Full conduction transconductance	$V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$		55	68	80	mS
V_{DSS}	Drain-to-source breakdown voltage	$ I_{DS} < 100\ \mu\text{A}$, $V_{GS} = -2\text{ V}$		40			V
C_{OSS}	Output capacitance	$V_{DS} = 5\text{ V}$			8		pF

6.6 Typical Characteristics

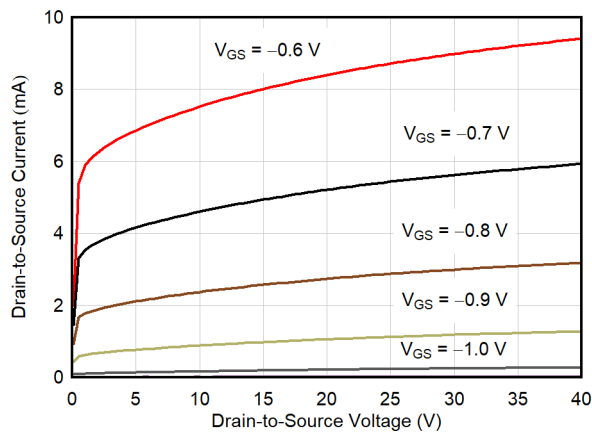
at $T_A = 25^\circ\text{C}$, $I_{DS} = 2\text{ mA}$, common-source configuration, and $V_{DS} = 5\text{ V}$ (unless otherwise noted)



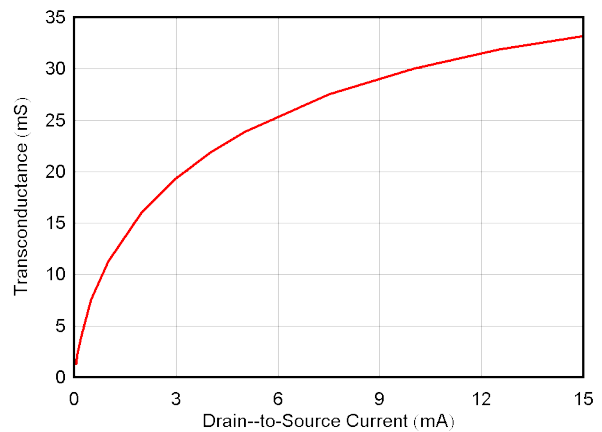
6-1. Drain-to-Source Current vs Gate-to-Source Voltage



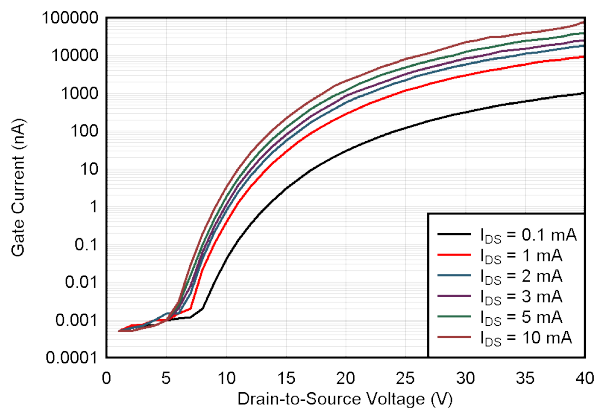
6-2. Drain-to-Source Current vs Drain-to-Source Voltage



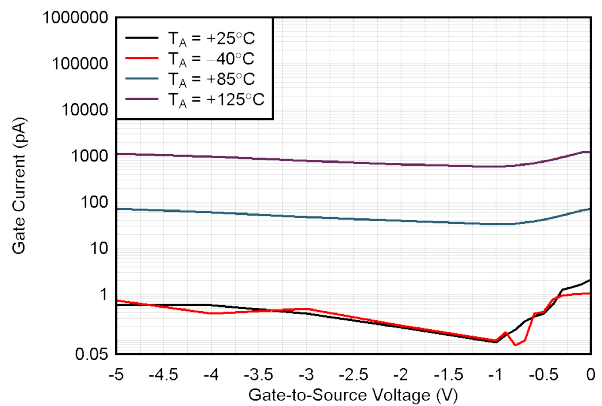
6-3. Drain-to-Source Current vs Drain-to-Source Voltage



6-4. Common Source Transconductance vs Drain-to-Source Current



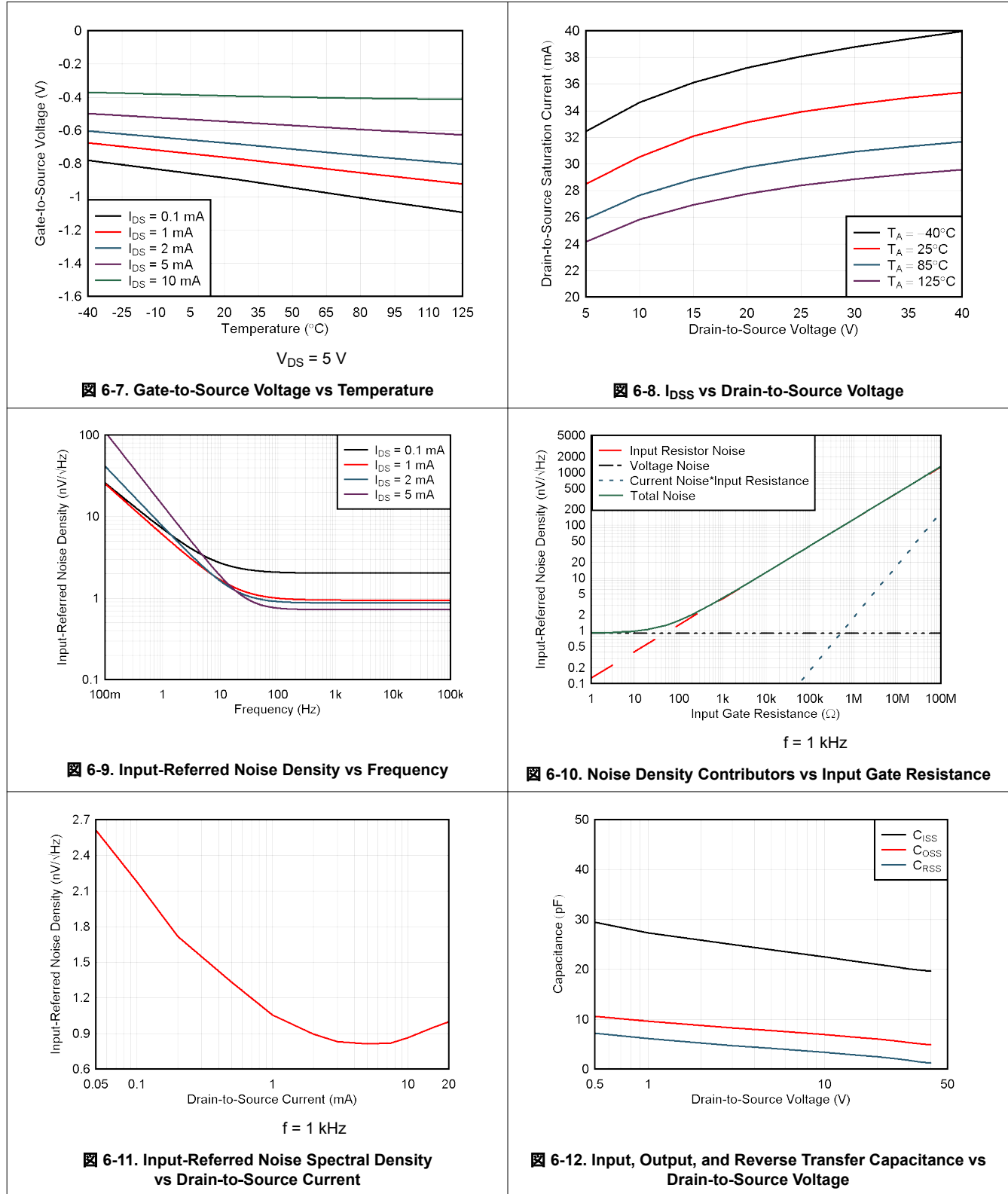
6-5. Gate Current vs Drain-to-Source Voltage



6-6. Gate Current vs Gate-to-Source Voltage

6.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_{DS} = 2\text{ mA}$, common-source configuration, and $V_{DS} = 5\text{ V}$ (unless otherwise noted)



7 Parameter Measurement Information

7.1 AC Measurement Configurations

The circuit configuration used for noise measurements is seen in [Figure 7-1](#). The nominal I_{DS} current is configured in the schematic by calibrating V_- . After I_{DS} is fixed, the V_{DS} voltage is set by calibrating V_+ . For input-referred noise data, the gain of the circuit is calibrated from V_{IN} to V_{OUT} and used for the input-referred gain calculation.

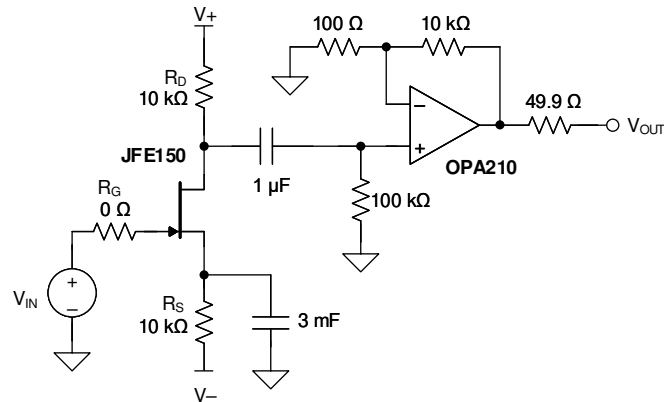


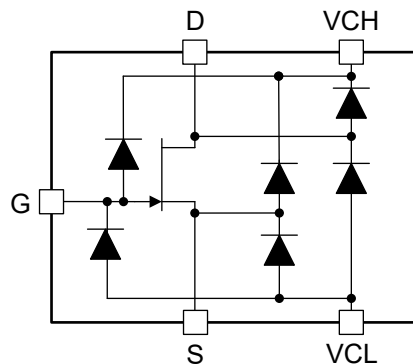
Figure 7-1. AC Measurement Reference Schematic

8 Detailed Description

8.1 Overview

The JFE150 is an ultra-low noise JFET designed to create low-noise gain stages for very high output impedance sensors or microphones. Advanced processing technology gives the JFE150 extremely low-noise performance, a high g_m/C_{ISS} ratio, and ultra-low gate-current performance. Input protection diodes are integrated to clamp high-voltage spurious input signals without the need for additional input diodes that can add leakage current or distortion-creating non-linear capacitance. The JFE150 provides a next-generation device to implement low-noise amplifiers for piezoelectric sensors, transducers, large-area condenser microphones, and hydrophones in small-package options.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Ultra-Low Noise

Junction-gate field-effect transistors (JFETs) are commonly used as an input stage in high-input-impedance, low-noise designs in audio, SONAR, vibration analysis, and other technologies. The JFE150 is a new generation JFET device that offers very low noise performance at the lowest possible current consumption in high-input-impedance amplifier designs. The JFE150 is manufactured on a high-performance analog process technology, giving tighter process parameter control than a standard JFET.

Designs that feature operational amplifiers (op amps) as the primary gain stage are common, but these designs are not able to achieve the lowest possible noise as a result of the inherent challenges and tradeoffs required from a full operational amplifier design. Noise in JFET designs can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or $1/f$ noise, is extremely important for systems that require signal gain at frequencies less than 100 Hz. The JFE150 achieves extremely low $1/f$ noise in this range. Thermal noise is noise in the region greater than 1 kHz and depends on the gain, or g_m , of the circuit. The g_m is a function of the drain-to-source bias current; therefore, thermal noise is also a function of drain-to-source bias current. [Figure 6-9](#) shows both $1/f$ and thermal noise with multiple bias conditions measured using the circuit shown in [Figure 7-1](#).

Noise is typically modeled as a voltage source (voltage noise) and current source (current noise) on the input. The $1/f$ and thermal noise can be represented as voltage noise. Current noise is dominated by current flow into the gate, and is called *shot noise*. The JFE150 features extremely low gate current, and therefore, extremely low current noise. [Figure 6-10](#) shows how source impedance on the input is the dominant noise source. In nearly all cases, noise created as a result of current noise is negligible.

8.3.2 Low Gate Current

The JFE150 features a maximum gate current of 10 pA at room temperature, making the device an excellent choice for maximizing the gain and dynamic range from extremely high impedance sensors. Additionally, any noise contributions as a result of gate current are minimized because of the negligible shot noise at low current levels. As with all JFET devices, when the drain-to-source voltage increases, the gate current also increases. Keep the drain-to-source voltage to less than 5 V for the lowest gate input current operation.

8.3.3 Input Protection

The JFE150 features input protection diodes that are used for surge clamping and ESD events. The diodes are rated to withstand high current surges for short times, steering current from the gate (G) pin to the VCH and VCL pins. The diodes also feature very low leakage, removing the need for external protection devices that can have high leakage currents or nonlinear capacitance that degrade the distortion performance.

8.4 Device Functional Modes

The JFE150 functionality is identical to standard N-channel depletion JFET devices. The gate-to-source (V_{GS}) voltage, drain-to-source voltage (V_{DS}) and drain-to-source current (I_{DS}) determine the region of operation.

- For $V_{GS} < V_{GSC}$: JFE150 conduction channel is closed; I_{DS} is only determined by junction leakage current.
- For $V_{GS} > V_{GSC}$: Two modes of operation can exist depending on V_{DS} . When V_{DS} is less than the linear (saturation) region threshold (see [Figure 8-1](#)), the device operates in the linear region, meaning that the device behaves as a resistor connected from drain-to-source with minimal variation from any changes in V_{GS} . When V_{DS} is greater than the linear (saturation) region threshold, I_{DS} has a strong dependence on V_{GS} , where the relationship is described by the parameter g_m .

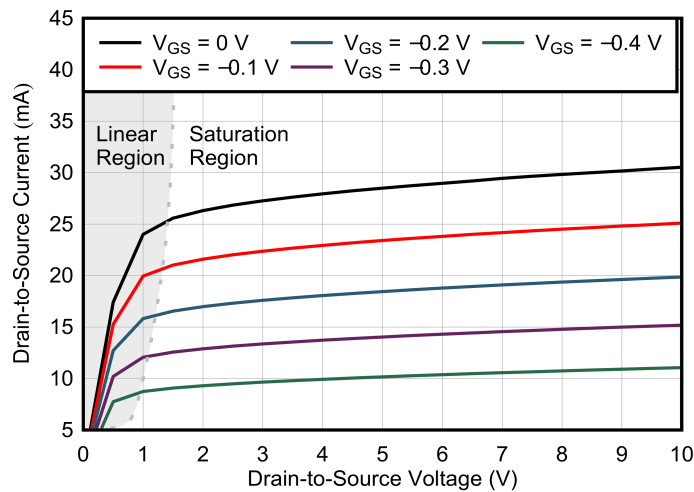


Figure 8-1. V_{DS} vs I_{DS}

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

9.1.1 Input Protection Diodes

The JFE150 features diodes that are used to help clamp voltage surges that can occur on the input sensor to the gate. The diodes are connected between the gate and two separate pins, VCL and VCH. The clamping mechanism works by *steering* current from the gate into the VCL or VCH nodes when the voltage at the gate is less than VCL or greater than VCH. [図 9-1](#) shows an example of a microphone input circuit where a dc blocking capacitor operates with a large dc voltage. When the microphone input is dropped or shorted, the dc blocking capacitor discharges into the VCL or VCH nodes, thus helping eliminate large signal transient voltages on the gate. There are also clamping diodes from the drain and source to VCL and VCH, respectively. The clamping diodes can withstand high surge currents up to 200 mA for 50 ms; however, limit dc current to less than 20 mA.

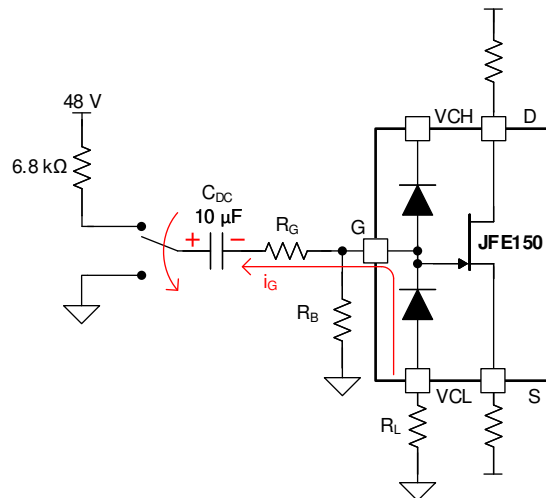


図 9-1. JFE150 Clamping Diode Example

[図 9-1](#) shows an example of configuring the diode clamp to protect the JFET against overvoltage in a phantom-powered microphone circuit. Phantom power typically delivers 48 V through a 6.8-k Ω pullup resistor to a microphone or dynamic load. If the microphone is disconnected, dc blocking capacitor C_{DC} can be biased up to 48 V. If the input to the capacitor is then shorted to ground (shown by the switch in [図 9-1](#)), the gate voltage can exceed the absolute maximum rating for V_{GS} . In this case, the blocking diode is used, along with current limiting resistors R_G and R_L , to clamp the gate voltage to a safe level. Be aware that the thermal noise of R_G couples directly into the gate input; therefore, make sure to minimize the resistance of R_G .

The clamping diodes are not required for operation. The V_{GS} voltage can withstand -40 V, so clamping is not required if the V_{GS} voltage is kept greater than this limit. If the diodes are not needed, leave the VCL and VCH nodes floating.

Most previous-generation JFET devices featured only three pins (gate, source, and drain). For these devices, the gate pin is in the same physical location as the VCL pin on the JFE150. To test the JFE150 in a three-pin socket, short pin 2 of the JFE150 (VCL) to pin 3 (G). When the devices are connected with pin 2 shorted to pin 3, the diode from VCL is shorted out and cannot provide any clamping protection. The input capacitance (C_{ISS}) also increases by 1 pF; see [図 6-12](#).

9.1.2 Capacitive Transducer Input Stage

Piezoelectric transducers are used for many different applications that require low-noise, high-gain performance. These transducers exhibit high output impedance ($> 10 \text{ M}\Omega$), and therefore require very high impedance loading for subsequent input stages. The JFE150 has ultra-low input gate current (maximum $I_G = \pm 10 \text{ pA}$) and low input capacitance ($C_{ISS} = 24 \text{ pF}$), which makes the device an excellent choice for transducers with an effective capacitance of greater than 240 pF . For smaller, lower-capacitance transducers, the C_{ISS} can impact the gain of the front end by attenuating the input signal, thereby reducing the noise performance.

9.1.3 Common-Source Amplifier

The common-source amplifier is a commonly used open-loop gain stage for JFET amplifiers. [Figure 9-2](#) shows the basic circuit.

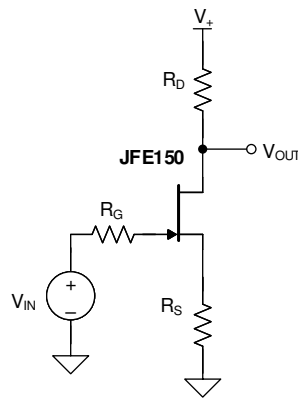


Figure 9-2. Common-Source Amplifier

[Equation 1](#) shows the equation for gain of the circuit in [Figure 9-2](#).

$$\frac{V_{OUT}}{V_{IN}} = - \frac{g_m * R_D}{1 + g_m * R_S} \quad (1)$$

Generally, higher gain results in improved noise performance. Gain increases as the bias current is increased as a result of increasing g_m (see [Figure 6-4](#)). As a result, the input-referred noise decreases as bias current is increased (see [Figure 6-9](#)). Any JFET design must make a tradeoff between current consumption and noise performance. The JFE150, however, delivers significantly lower noise performance than most operational amplifiers at the same current consumption. The bias current (I_{DS}) is set by the value of the source resistor, R_S , and the threshold voltage, V_T , of the JFE150. [Figure 9-3](#) is a graph showing nominal I_{DS} vs R_S .

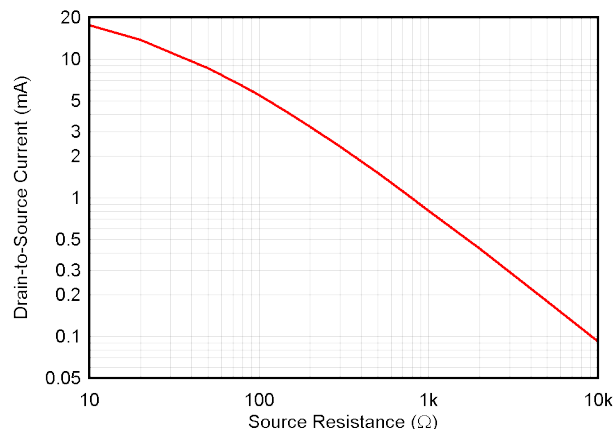


Figure 9-3. Drain-to-Source Current vs R_S , $V_{DS} = 5 \text{ V}$

The bias current varies according to the resistor and threshold voltage tolerances. Additionally, thermal noise associated with R_S couples directly into the gain of the circuit, degrading the overall noise performance. To improve the circuit in [Figure 9-4](#), use a current-source biasing scheme. Current-source biasing removes the JFET threshold variation from the biasing scheme, and allows for lower-value filtering capacitance (C_S) for equivalent filtering due to the high output impedance of current sources.

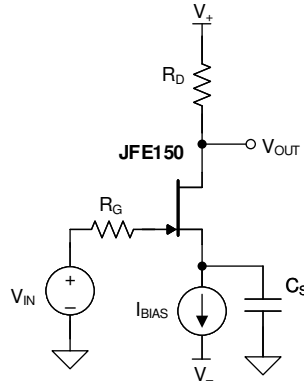


Figure 9-4. Common-Source Amplifier With Current-Source Biasing

9.1.4 Composite Amplifiers

The JFE150 can be configured to provide a low-noise, high-input impedance front-end stage for a typical op amp. Open-loop transistor gain stages shown previously suffer from wide gain variations that are dependent on the forward transconductance of the JFE150. When precision gain is required, the composite amplifier (JFET front-end + operational amplifier) achieves excellent results by allowing for a fixed gain determined by external resistors, and improving the noise and bandwidth of the operational amplifier. The JFE150 gain stage provides a boost to the open-loop performance of the system, extending the bandwidth beyond what the operational amplifier alone can provide, and gives a high-input impedance, ultra-low noise input stage to interface with high source impedance microphones.

[Figure 9-5](#) shows a generic schematic representation of a current-feedback composite amplifier. The component requirements and tradeoffs are listed in [Table 9-1](#).

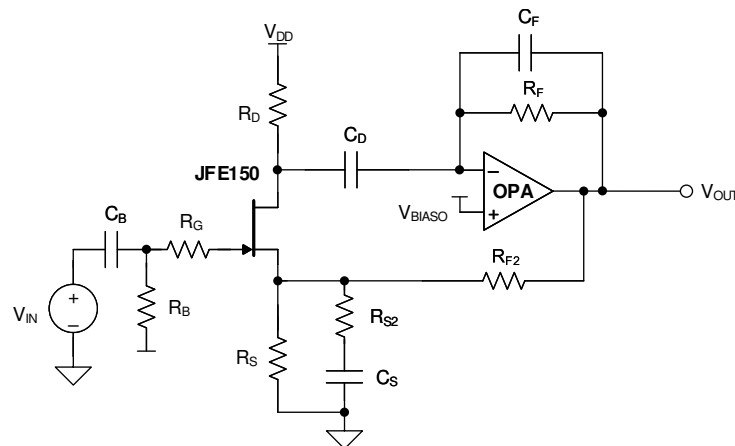


Figure 9-5. Low Noise, High Input Impedance Composite Amplifier

表 9-1. Composite Amplifier Component List and Function

COMPONENT	DESCRIPTION	RELATED EQUATION
C _B	DC blocking capacitor for input source. Use a dc blocking capacitor if the dc voltage of the input source is not the same as the gate bias voltage.	$f_{-3dBDC} = \frac{1}{2 * \pi * R_{B1} R_{B2} * C_{B1}}$ (2)
R _B	Bias resistor. Use biasing resistors to set the dc voltage at the gate. High-value resistors can be used without an impact to noise if the source impedance and bypass capacitor have sufficiently low impedance.	See 式 2
R _G	Gate resistor. Can be used to help limit current flow into gate in overvoltage cases.	
R _D	Drain resistor. Sets gain of JFET stage in common source biasing, along with gm and R _S .	
R _S	Source resistor. Used to set bias of JFET; see 图 9-3. Resistor thermal noise directly impacts noise performance.	
C _D	DC blocking capacitor. Blocks nominal drain voltage so the amplifier operates at a midsupply bias point.	
C _F	Feedback capacitor. Along with R _F , this capacitor sets the –3-dB high-pass cutoff frequency when the amplifier gain-bandwidth product (GBW) is sufficiently high enough to support the –3-dB frequency. If the GBW is not high enough, then the GBW sets the –3-dB frequency.	$f_{-3dBHP} = \frac{1}{2 * \pi * R_F * C_F}$ (3)
R _F	Feedback resistor. Along with C _F , this resistor sets the –3-dB high-pass cutoff frequency when the amplifier gain-bandwidth product (GBW) is sufficiently high enough to support the –3-dB frequency. If the GBW is not high enough, then the GBW sets the –3-dB frequency.	See 式 3
R _{F2}	Current feedback gain-setting resistor 1. Along with R _{S2} , sets gain closed-loop.	$\frac{V_{OUT}}{V_{IN}} = \frac{R_{F2}}{R_{S2}}$ (4)
R _{S2}	Current feedback gain-setting resistor 2. Along with R _{S2} , sets gain closed-loop. Resistor thermal noise directly impacts noise performance.	See 式 4
C _S	Current feedback ac-coupling capacitor. This capacitor, along with R ₂ , sets the low-pass –3-dB frequency.	$f_{-3dBLP} = \frac{1}{2 * \pi * R_{S2} * C_S}$ (5)

9.2 Typical Application

The JFE150 can be configured to provide a low-noise, high-input-impedance front-end stage for a typical op amp. Single-transistor gain stages shown previously suffer from wide gain variations dependent on the forward transconductance of the JFE150. When precision gain is required, the composite amplifier (JFET front-end + operational amplifier) achieves excellent results.

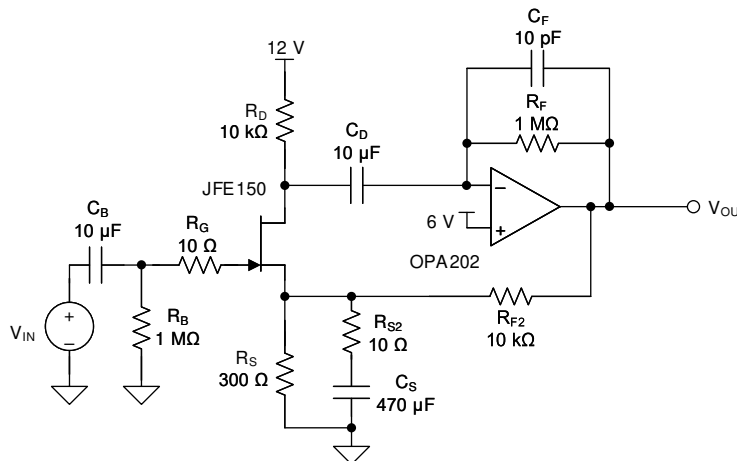


图 9-6. Low-Noise, High-Input-Impedance Composite Amplifier

9.2.1 Design Requirements

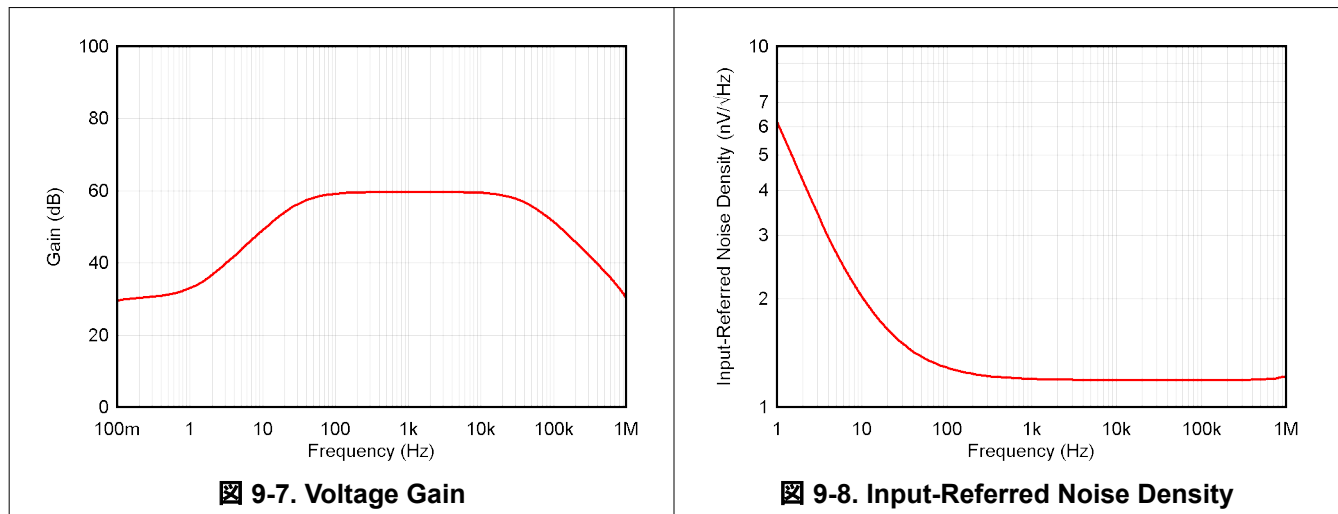
PARAMETER	DESIGN GOAL
Gain	60 dB
Frequency response	60 Hz to 20 kHz
Noise	< 1.5 nV/ $\sqrt{\text{Hz}}$
Input current	< 100 pA
Output swing	± 5 V

9.2.2 Detailed Design Procedure

This design provides 60 dB of gain with extremely high input impedance at a very low frequency response. The order of design priorities are as follows:

- The JFE150 bias current is set by selecting the desired bias current and noise tradeoff (see [Figure 6-11](#)). The input-referred noise is dominated by the JFE150 bias current and gain. To set the bias current point, adjust the source resistance according to [Figure 9-3](#).
- After the bias current is selected, set the JFET stage gain as high as possible without pushing the device into the linear region of operation. This is achieved by using the largest drain resistor (R_D) possible while maintaining a minimum of 2 V across the drain to source nodes. Be aware that the amplifier forces the drain node to match the noninverting amplifier input in normal closed-loop operation. Both ac and dc voltages must be considered, but generally, only the dc operating point on the drain is considered because the ac voltage swing is minimal.
- Set the closed gain according to R_{F2} and R_{S2} , as seen in [Equation 4](#). Thermal noise from R_{S2} directly couples into the circuit; therefore, small values for this resistor are required.
- C_S is required to block dc voltages from altering the bias point set by source resistor R_S . C_S also forms the low-frequency response as described in [Equation 5](#).

9.2.3 Application Curves



9.3 Power Supply Recommendations

The JFE150 is a JFET transistor with clamping diodes. There are no specific power-supply connections; however, take care not to exceed any absolute maximum voltages on any of the pins if system supply voltages greater than or equal to 40 V are used.

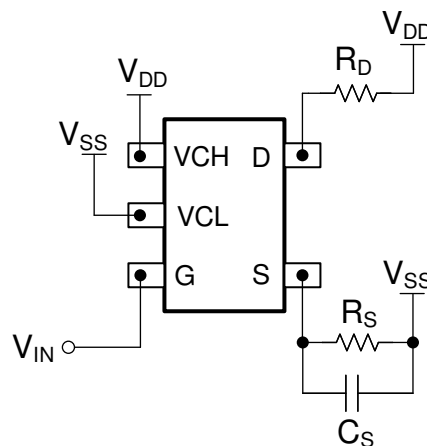
9.4 Layout

9.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Keep high impedance input signals away from noisy traces.
- Make sure supply voltages are adequately filtered.
- Minimize distance between source-connected and drain-connected components to the JFE150.
- Consider a driven, low-impedance guard ring around the critical gate traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

9.4.2 Layout Example



✎ 9-9. JFE150 Layout Example, Common Source Configuration

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 PSpice® for TI

PSpice® for TI は、アナログ回路の性能評価に役立つ設計およびシミュレーション環境です。レイアウトと製造に移る前に、サブシステムの設計とプロトタイプ・ソリューションを作成することで、開発コストを削減し、市場投入までの期間を短縮できます。

10.1.1.2 TINA-TI™ シミュレーション・ソフトウェア (無償ダウンロード)

TINA-TI™ シミュレーション・ソフトウェアは、SPICE エンジンに基づいた単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TI シミュレーション・ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション・ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TI シミュレーション・ソフトウェアは設計ツールとシミュレーション Web ページから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

これらのファイルを使用するには、TINA ソフトウェアまたは TINA-TI ソフトウェアがインストールされている必要があります。TINA-TI™ ソフトウェア・フォルダから、無償の TINA-TI シミュレーション・ソフトウェアをダウンロードしてください。

10.1.1.3 TI のリファレンス・デザイン

TI のリファレンス・デザインは、TI の高精度アナログ・アプリケーション専門家により作成されたアナログ・ソリューションです。TI のリファレンス・デザインは、動作原理、部品の選択、シミュレーション、完全な PCB 回路図およびレイアウト、部品表、測定済みの性能を提供します。TI のリファレンス・デザインは、<http://www.ti.com/ww/en/analog/precision-designs/> からオンラインで入手できます。

10.1.1.4 フィルタ設計ツール

フィルタ設計ツールは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。フィルタ設計ツールを使用すると、TI のベンダ・パートナーからの TI 製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

フィルタ設計ツールは、設計ツールとシミュレーション Web ページから Web 対応ツールとして利用でき、包括的な複数段アクティブ・フィルタ・ソリューションをわずか数分で設計、最適化、シミュレーションできます。

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [JFE150 Ultra-Low-Noise Pre-Amp application note](#)
- Texas Instruments, [JFE150 Evaluation Module user's guide](#)
- Texas Instruments, [OPAx202 Precision, Low-Noise, Heavy Capacitive Drive, 36-V Operational Amplifiers data sheet](#)
- Texas Instruments, [OPAx210 2.2-nV/√Hz Precision, Low-Power, 36-V Operational Amplifiers data sheet](#)

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

10.5 Trademarks

Burr-Brown™, TINA-TI™, and TI E2E™ are trademarks of Texas Instruments.

TINA™ is a trademark of DesignSoft, Inc.

PSpice® is a registered trademark of Cadence Design Systems, Inc.

すべての商標は、それぞれの所有者に帰属します。

10.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JFE150DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2GLW
JFE150DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2GLW
JFE150DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2GLW
JFE150DBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2GLW
JFE150DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IF
JFE150DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IF
JFE150DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IF
JFE150DCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IF

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
JFE150DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
JFE150DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
JFE150DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
JFE150DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
JFE150DCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
JFE150DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
JFE150DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
JFE150DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
JFE150DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
JFE150DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
JFE150DCKT	SC70	DCK	5	250	210.0	185.0	35.0
JFE150DCKT	SC70	DCK	5	250	180.0	180.0	18.0

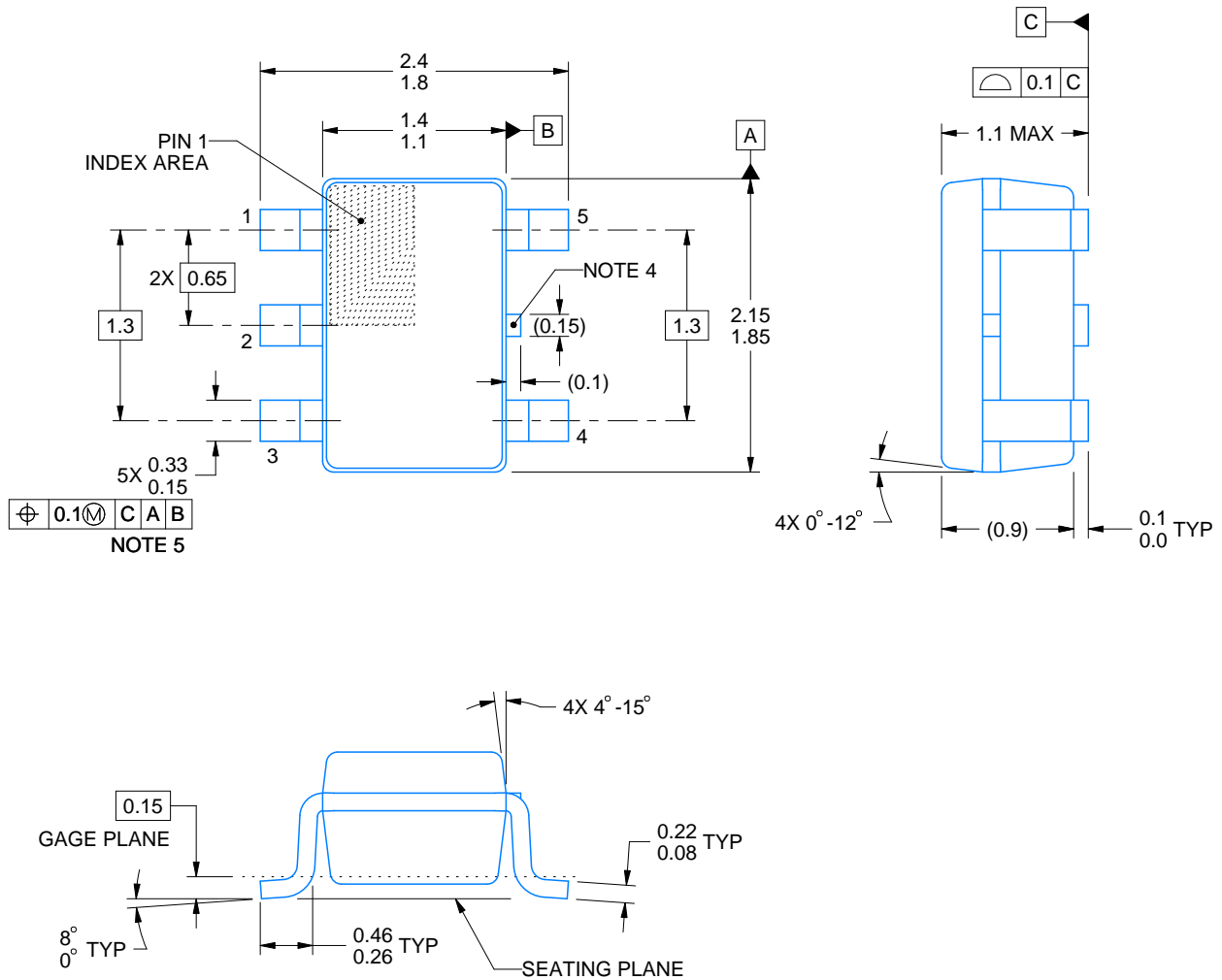
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

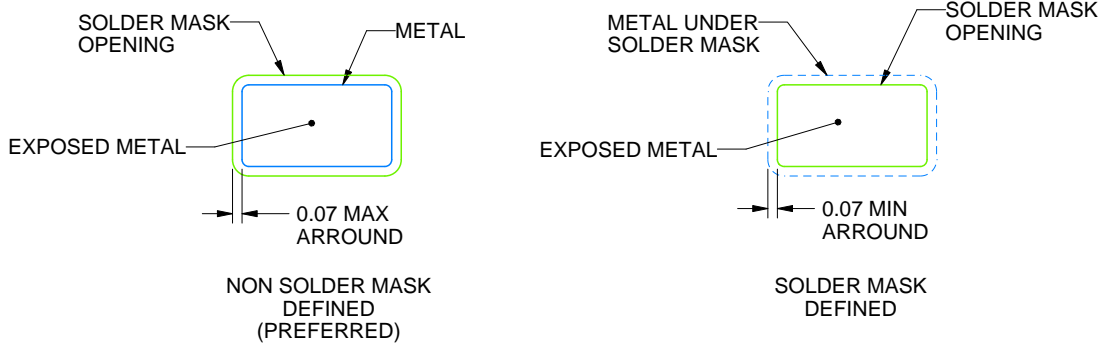
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

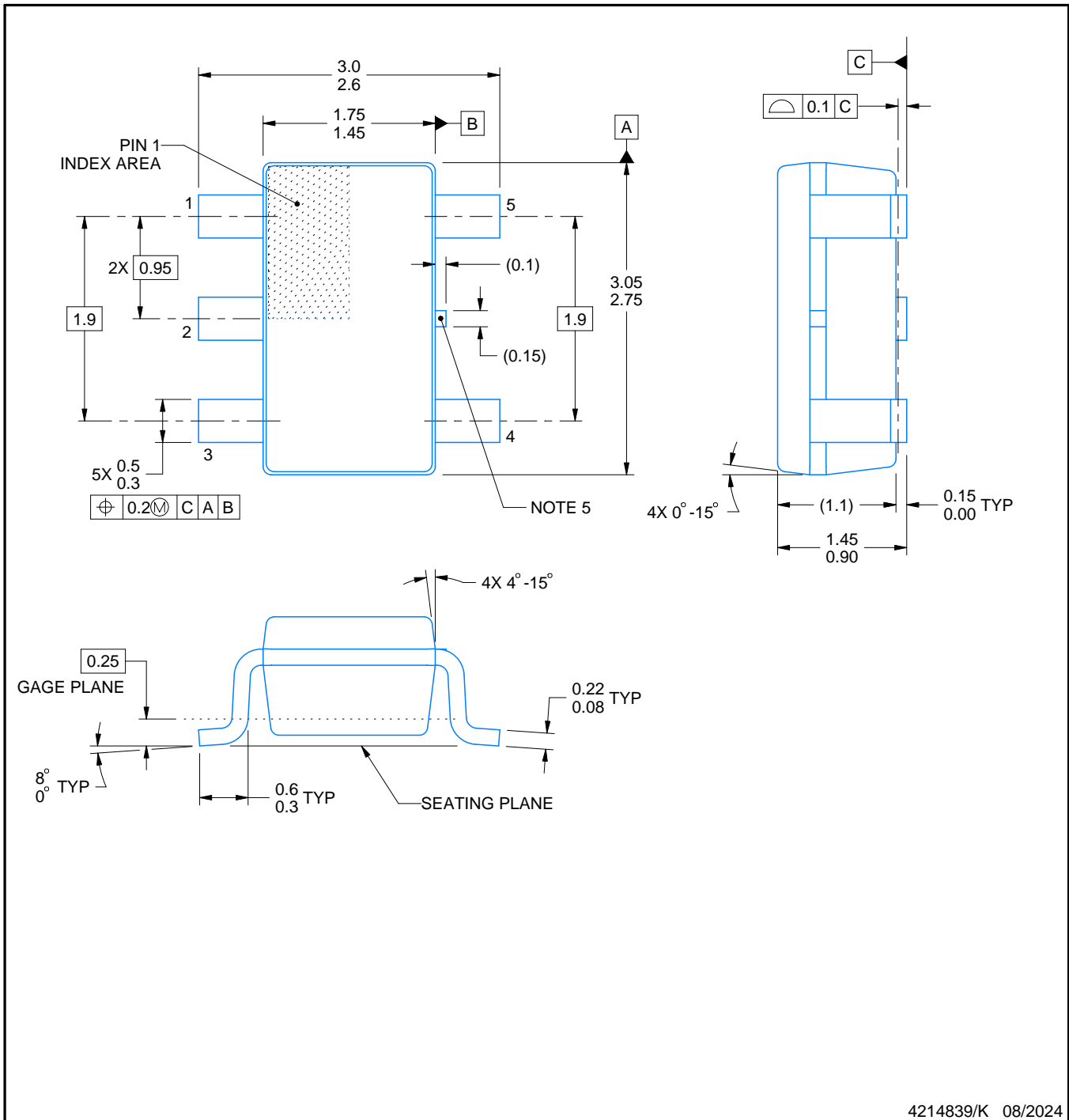


PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日 : 2025 年 10 月