TEXAS INSTRUMENTS

LM22679, LM22679-Q1
JAJSAZ1M – FEBRUARY 2013 – REVISED OCTOBER 2020

LM22679/-Q1 使用しやすいパッケージの 42V、5A SIMPLE SWITCHER® 降圧レギュレータ

1 特長

- 新製品のご案内：LM61460 3V～36V、6A、低 EMI 同期整流式降圧コンバータ
- 広い入力電圧レンジ：4.5V～42V
- 内部補償電圧モード制御
- 低 ESR のセラミック・コンデンサで安定動作
- 100mΩ の N チャネル MOSFET
- 出力電圧オプション：
  -ADJ (最小 1.285V の出力)
  -5.0 (5V 固定の出力)
- ±1.5% のフィードバック・リファレンス精度
- 500kHz のスイッチング周波数
- 動作時の接合部温度範囲：–40℃～125℃
- 調整可能なソフト・スタート
- 調節可能な電流制限
- ブートストラップ・ダイオードを内蔵
- WEBENCH® 完全対応
- AEC-Q100 認定済みの LM22679-Q1 は車載グレードのフローで製造
- PFM (露出パッド) パッケージ

2 アプリケーション

- 産業用分散電源アプリケーション
- 試験 / 測定機器
- 家電製品
- 広い V_{IN} の汎用アプリケーション

3 概要

LM22679 スイッチング・レギュレータは、最小限の外付け部品を使用して高効率高電圧の降圧レギュレータを実装するために必要なすべての機能を備えています。この使用しやすいレギュレータは、最大 5A の負荷電流を供給できる 42V の N チャネル MOSFET スイッチを内蔵して

います。優れたラインおよび負荷レギュレーションと高効率 (90% 超) が特長です。電圧モード制御は最小オン時間が短いため、入力電圧と出力電圧の比率を最も大きくできます。内部ループ補償により、ユーザーはループ補償部品を計算する煩雑な作業から解放されます。固定 5V 出力品と可変出力電圧品を提供しています。500kHz のスイッチング周波数を使用するため、小型の外付け部品を使用でき、良好な過渡応答を実現できます。1 つの外付けコンデンサを選択することで調整できるソフトスタート機能を備えています。また、スイッチ電流制限機能を 1 つの外付け抵抗でプログラムできるため、ソリューションを最適化できます。LM22679 デバイスはサーマル・シャットダウン機能と、偶発的な過負荷に対して保護する電流制限機能も内蔵しています。
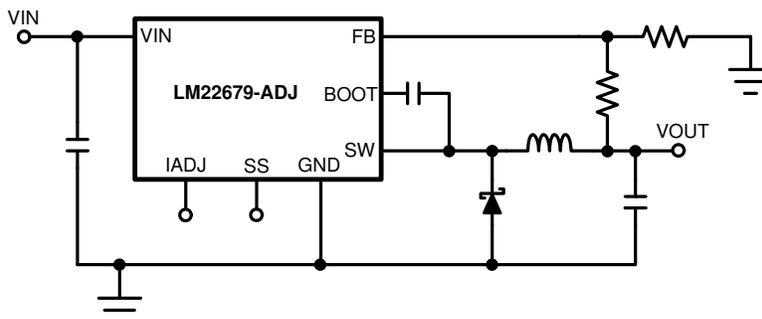
新製品の LM61460 は高効率、スタンバイ時の低静止電流、優れた EMI 性能を実現しています。比較するには、デバイス比較表を参照してください。WEBENCH により、LM61460 を使用する設計を開始できます。

LM22679 デバイスは、テキサス・インスツルメンツの SIMPLE SWITCHER® ファミリの製品です。SIMPLE SWITCHER のコンセプトにより、最小限の外付け部品数で、TI の WEBENCH 設計ツールを使用して、使いやすい完全な設計が可能になります。TI の WEBENCH ツールには、外付け部品の計算、電気的シミュレーション、熱シミュレーション、デザインインを容易にする Build-It ボードなどの機能が含まれています。

製品情報

型番	パッケージ[(1)]	本体サイズ (公称)
LM22679	TO-263 (7)	10.16mm × 9.85mm
LM22679-Q1		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

アプリケーション概略回路図

English Data Sheet: SNVS581

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• 「ピン構成および機能」、「取り扱い定格」の表、「機能説明」、「デバイスの機能モード」、「アプリケーションと実装」、「電源に関する推奨事項」、「レイアウト」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」を追加..1
• Deleted *Inverting Regulator Application* 14

5 Pin Configuration and Functions
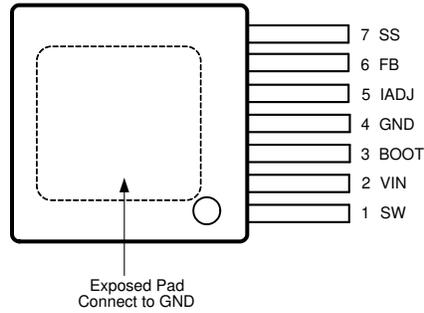
図 5-1. 7-Pin NDR Package Top View

Pin Functions

PIN		TYPE	DESCRIPTION	APPLICATION INFORMATION
NAME	NO.			
SW	1	O	Switch Output	Switching output of regulator
VIN	2	I	Input Voltage	Supply input to regulator
BOOT	3	I	Bootstrap input	Provides the gate voltage for the high side NFET
GND	4	—	Ground input to regulator; system common	System ground pin
IADJ	5	I	Current limit adjust input pin	A resistor attached between this pin and GND can be used to set the current limit threshold. Pin can be left floating and internal setting will be default.
FB	6	I	Feedback Input	Feedback input to regulator
SS	7	O	Soft-start pin	Used to increase soft-start time. See セクション 7.3.2.
EP	EP	—	Exposed Pad	Connect to ground. Provides thermal connection to PCB. See セクション 8.

Product Folder Links: *LM22679 LM22679-Q1*

6 Specifications

6.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
VIN to GND		43	V
SS, IADJ Pin Voltage	−0.5	7	V
SW to GND[1]	−5	V_{IN}	V
Boot Pin Voltage		V_{SW} + 7	V
FB Pin Voltage	−0.5	7	V
Power Dissipation	Internally Limited		
Junction Temperature[2]		150	°C

(1) The absolute-maximum specification of the 'SW to GND' applies to dc voltage. An extended negative voltage limit of −10 V applies to a pulse of up to 50 ns.
(2) For soldering specifications, refer to refer to application report *Absolute Maximum Ratings for Soldering* (SNOA549).

6.2 Handling Ratings: LM22679

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	−2	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Handling Ratings: LM22679-Q1

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	−2	2	kV

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply Voltage	4.5	42	V
	Junction Temperature Range	−40	125	°C

6.5 Thermal Information

	THERMAL METRIC[1] [2]	LM22679	UNIT
		NDR	
		7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22	°C/W

(1) For more information about traditional and new thermal metrics, see the application report *IC Package Thermal Metrics* (SPRA953).
(2) The value of $R_{\theta JA}$ for the PFM (TJ) package of 22°C/W is valid if package is mounted to 1 square inch of copper. The $R_{\theta JA}$ value can range from 20 to 30°C/W depending on the amount of PCB copper dedicated to heat transfer. See application note *AN-1797 TO-263 THIN Package* (SNVA328) for more information.

6.6 Electrical Characteristics

Typical values represent the most likely parametric norm at $T_A = T_J = 25°C$, and are provided for reference purposes only. Unless otherwise specified: $V_{IN} = 12$ V.

| PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
LM22679-5.0						
V_{FB}	Feedback Voltage	$V_{IN} = 8$ V to 42 V	4.925	5.0	5.075	V
		$V_{IN} = 8$ V to 42 V, $-40°C ≤ T_J ≤ 125°C$	4.9		5.1	
LM22679-ADJ						
V_{FB}	Feedback Voltage	$V_{IN} = 4.7$ V to 42 V	1.266	1.285	1.304	V
		$V_{IN} = 4.7$ V to 42 V, $-40°C ≤ T_J ≤ 125°C$	1.259		1.311	
ALL OUTPUT VOLTAGE VERSIONS						
I_Q	Quiescent Current	$V_{FB} = 5$ V		3.4		mA
		$V_{FB} = 5$ V, $-40°C ≤ T_J ≤ 125°C$			6	
V_{ADJ}	Current Limit Adjust Voltage			0.8		V
			0.65		0.9	
		$-40°C ≤ T_J ≤ 125°C$				
I_{CL}	Current Limit		6.0	7.1	8.4	A
		$-40°C ≤ T_J ≤ 125°C$	5.75		8.75	
I_L	Output Leakage Current	$V_{IN} = 42$ V, SS Pin = 0 V, $V_{SW} = 0$ V		32	60	µA
		$V_{SW} = -1$ V		31	75	µA
$R_{DS(ON)}$	Switch On-Resistance			0.10	0.14	Ω
					0.2	
f_O	Oscillator Frequency			500		kHz
		$-40°C ≤ T_J ≤ 125°C$	400		600	
T_{OFFMIN}	Minimum Off-time			200		ns
		$-40°C ≤ T_J ≤ 125°C$	100		300	
T_{ONMIN}	Minimum On-time			100		ns
I_{BIAS}	Feedback Bias Current	$V_{FB} = 1.3$ V (ADJ Version Only)		230		nA
I_{SS}	Soft-start Current			50		µA
		$-40°C ≤ T_J ≤ 125°C$	30		70	
T_{SD}	Thermal Shutdown Threshold			150		°C

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Typical values represent most likely parametric norms at the conditions specified and are not ensured.
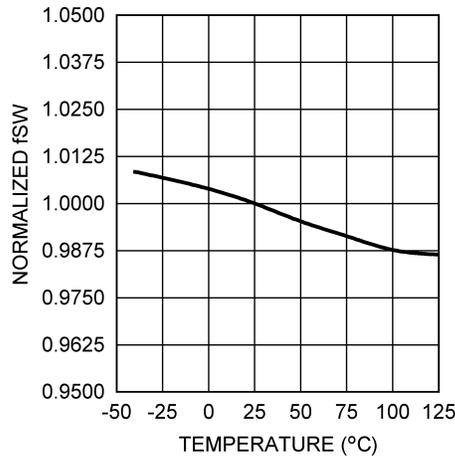
6.7 Typical Characteristics

V_{in} = 12 V, T_J = 25°C (unless otherwise specified)
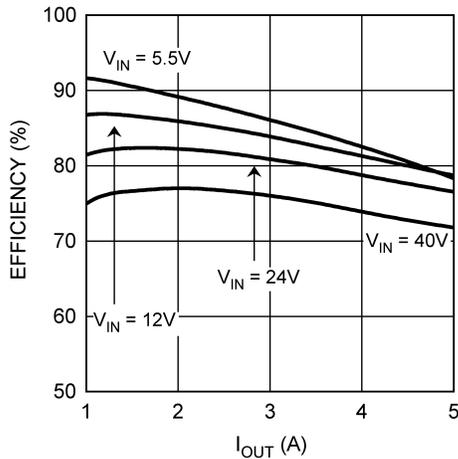
図 6-1. Efficiency vs I_{OUT} and V_{IN} (V_{OUT} = 3.3 V)
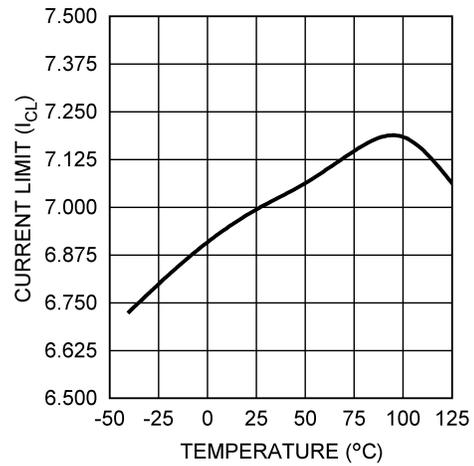
図 6-2. Current Limit vs Temperature

図 6-3. Normalized Switching Frequency vs Temperature
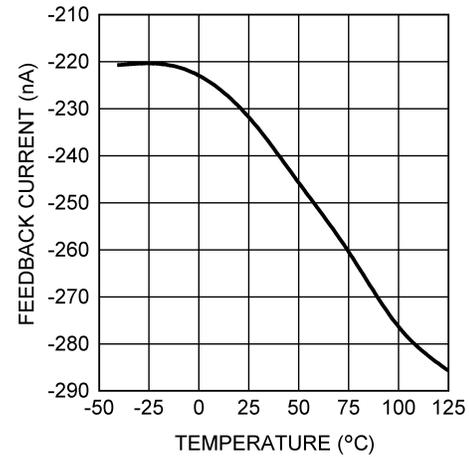
図 6-4. Feedback Bias Current vs Temperature
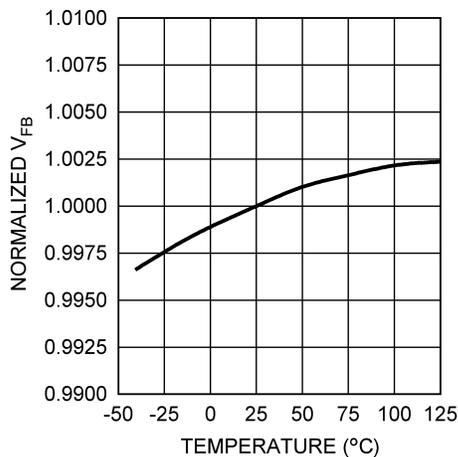
図 6-5. Normalized Feedback Voltage vs Temperature

図 6-6. Normalized $R_{DS(ON)}$ vs Temperature

Product Folder Links: *LM22679 LM22679-Q1*

図 6-7. Normalized Feedback Voltage vs Input Voltage
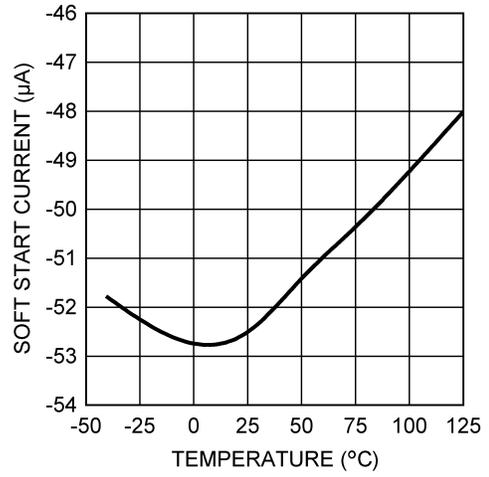
図 6-8. Soft-Start Current vs Temperature
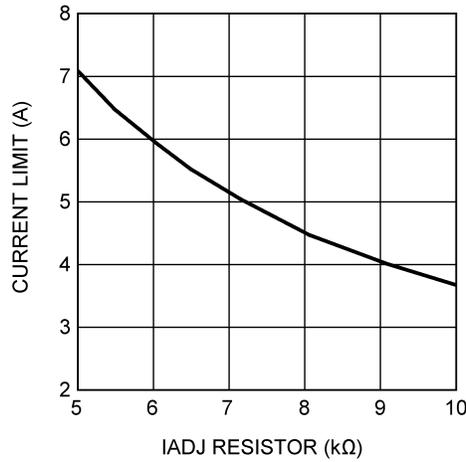
図 6-9. Current Limit vs IADJ Resistor

7 Detailed Description

7.1 Overview

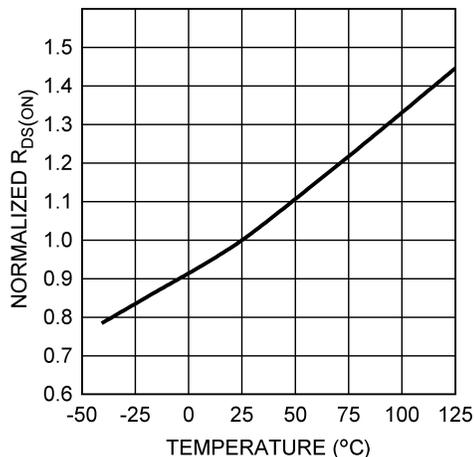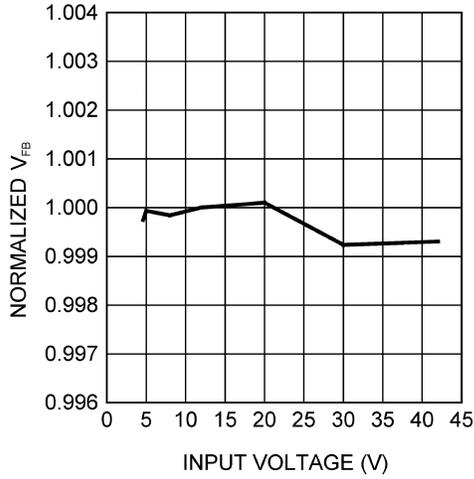The LM22679 incorporates a voltage mode constant frequency PWM architecture. In addition, input voltage feedforward is used to stabilize the loop gain against variations in input voltage. This allows the loop compensation to be optimized for transient performance. The power MOSFET, in conjunction with the diode, produces a rectangular waveform at the switch pin, that swings from about zero volts to VIN. The inductor and output capacitor average this waveform to become the regulator output voltage. By adjusting the duty cycle of this waveform, the output voltage can be controlled. The error amplifier compares the output voltage with the internal reference and adjusts the duty cycle to regulate the output at the desired value.

The internal loop compensation of the -ADJ option is optimized for outputs of 5 V and below. If an output voltage of 5 V or greater is required, the -5.0 option can be used with an external voltage divider. The minimum output voltage is equal to the reference voltage, that is, 1.285 V (typ).

7.2 Functional Block Diagram
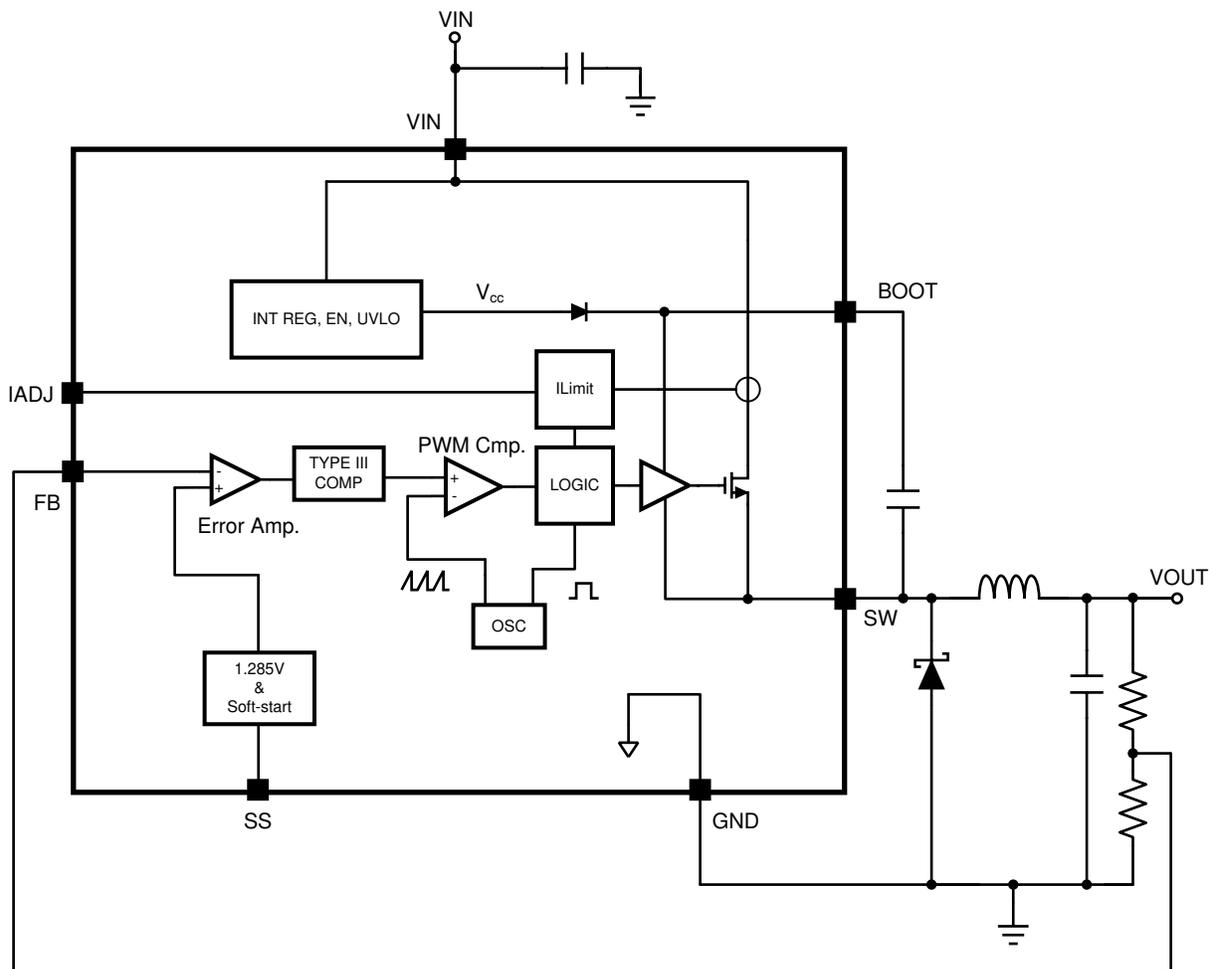
7.3 Feature Description

7.3.1 UVLO

The LM22679 also incorporates an input undervoltage lock-out (UVLO) feature. This prevents the regulator from turning on when the input voltage is not great enough to properly bias the internal circuitry. The rising threshold is 4.3 V (typ) while the falling threshold is 3.9 V (typ).

7.3.2 Soft-Start

The soft-start feature allows the regulator to gradually reach steady-state operation, thus reducing start-up stresses. The internal soft-start feature brings the output voltage up in about 500 µs. This time can be extended by using an external capacitor connected to the SS pin. Values in the range of 100 nF to 1 µF are recommended. The approximate soft-start time can be estimated from 式 1.

$$T_{SS} \approx 26 \times 10^3 \times C_{SS} \tag{1}$$

Soft-start is reset any time the part is shut down or a thermal overload event occurs.

7.3.3 Bootstrap Supply

The LM22679 device incorporates a floating high-side gate driver to control the power MOSFET. The supply for this driver is the external boot-strap capacitor connected between the BOOT pin and SW. A good quality 10-nF ceramic capacitor must be connected to these pins with short, wide PCB traces. One reason the regulator imposes a minimum off-time is to ensure that this capacitor recharges every switching cycle. A minimum load of about 5 mA is required to fully recharge the bootstrap capacitor in the minimum off-time. Some of this load can be provided by the output voltage divider, if used.

7.3.4 Internal Compensation

The LM22679 device has internal loop compensation designed to provide a stable regulator over a wide range of external power stage components. The internal compensation of the -ADJ option is optimized for output voltages below 5 V. If an output voltage of 5 V or greater is needed, the -5.0 option with an external resistor divider can be used.

Ensuring stability of a design with a specific power stage (inductor and output capacitor) can be tricky. The LM22679 stability can be verified using the WEBENCH Designer online circuit simulation tool. A quick start spreadsheet can also be downloaded from the online product folder.

The complete transfer function for the regulator loop is found by combining the compensation and power stage transfer functions. The LM22679 has internal type III loop compensation, as detailed in Internal Loop Compensation section. This is the approximate "straight line" function from the FB pin to the input of the PWM modulator. The power stage transfer function consists of a dc gain and a second order pole created by the inductor and output capacitor or capacitors. Due to the input voltage feedforward employed in the LM22679, the power stage dc gain is fixed at 20 dB. The second order pole is characterized by its resonant frequency and its quality factor (Q). For a first pass design, the product of inductance and output capacitance should conform to 式 2.

$$L \cdot C_{out} \approx 1.1 \times 10^{-9} \tag{2}$$

Alternatively, this pole should be placed between 1.5 kHz and 15 kHz and is given by 式 3.

$$F_o = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{out}}} \tag{3}$$

The Q factor depends on the parasitic resistance of the power stage components and is not typically in the control of the designer. Of course, loop compensation is only one consideration when selecting power stage components (see セクション 8 for more details).
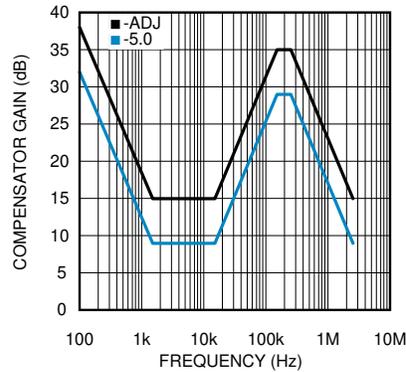
図 7-1. Compensator Gain

In general, hand calculations or simulations can only aid in selecting good power stage components. Good design practice dictates that load and line transient testing should be done to verify the stability of the application. Also, Bode plot measurements should be made to determine stability margins. The *AN-1889 How to Measure the Loop Transfer Function of Power Supplies* application report (SNVA364) shows how to perform a loop transfer function measurement with only an oscilloscope and function generator.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The LM22679 device incorporates an input undervoltage lock-out (UVLO) feature. This prevents the regulator from turning on when the input voltage is not great enough to properly bias the internal circuitry. The rising threshold is 4.3 V (typ) while the falling threshold is 3.9 V (typ).

7.4.2 Active Mode

The LM22679 is in Active Mode when VIN is above its UVLO level. See セクション 7.3.1 for more information on the UVLO level.

7.4.3 Current Limit

The LM22679 device has current limiting to prevent the switch current from exceeding safe values during an accidental overload on the output. This peak current limit is found in セクション 6.6 under the heading of I_{CL}. The maximum load current that can be provided, before current limit is reached, is determined from 式 4.

$$I_{out}\big|_{max} \approx I_{CL} - \frac{(V_{in} - V_{out})}{2 \cdot L \cdot F_{sw}} \cdot \frac{V_{out}}{V_{in}}$$

(4)

where

• L is the value of the power inductor

When the LM22679 enters current limit, the output voltage will drop and the peak inductor current will be fixed at I_{CL} at the end of each cycle. The switching frequency will remain constant while the duty cycle drops. The load current will not remain constant, but will depend on the severity of the overload and the output voltage.

For very severe overloads ("short-circuit"), the regulator changes to a low frequency current foldback mode of operation. The frequency foldback is about 1/5 of the nominal switching frequency. This will occur when the current limit trips before the minimum on-time has elapsed. This mode of operation is used to prevent inductor current "run-away", and is associated with very low output voltages when in overload. 式 5 can be used to determine what level of output voltage will cause the part to change to low frequency current foldback.

Product Folder Links: *LM22679 LM22679-Q1*

$$V_x \leq V_{in} \cdot F_{sw} \cdot T_{on} \cdot 1.8 \tag{5}$$

where

- F_{sw} is the normal switching frequency
- V_{in} is the maximum for the application

If the overload drives the output voltage to less than or equal to V_x, the part will enter current foldback mode. If a given application can drive the output voltage to $\leq V_x$, during an overload, then a second criterion must be checked. 式 6 gives the maximum input voltage, when in this mode, before damage occurs.

$$V_{in} \leq \frac{V_{sc} + 0.4}{T_{on} \cdot F_{sw} \cdot 0.36} \tag{6}$$

where

- V_{sc} is the value of output voltage during the overload
- f_{sw} is the normal switching frequency

Note

If the input voltage should exceed this value, while in foldback mode, the regulator, the diode can be damaged, or both.

It is important to note that the voltages in these equations are measured at the inductor. Normal trace and wiring resistance will cause the voltage at the inductor to be higher than that at a remote load. Therefore, even if the load is shorted with zero volts across its terminals, the inductor will still see a finite voltage. It is this value that should be used for V_x and V_{sc} in the calculations. In order to return from foldback mode, the load must be reduced to a value much lower than that required to initiate foldback. This load "hysteresis" is a normal aspect of any type of current limit foldback associated with voltage regulators.

The safe operating area, when in short circuit mode, is shown in 図 7-2. Operating points below and to the right of the curve represent safe operation.
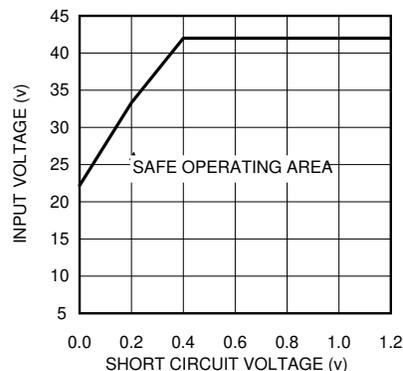

図 7-2. SOA

7.4.4 Current Limit Adjustment

A key feature of the LM22679 device is the ability to adjust the peak switch current limit. This can be useful when the full current capability of the regulator is not required for a given application. A smaller current limit may allow the use of power components with lower current ratings, thus saving space and reducing cost. A single resistor between the IADJ pin and ground controls the current limit in accordance with 図 7-3. The current limit mode is set during start-up of the regulator. When V_{IN} is applied, a weak pullup is connected to the IADJ pin and, after approximately 100 μs, the voltage on the pin is checked against a threshold of about 0.8 V. With the IADJ pin open, the voltage floats above this threshold, and the current limit is set to the default value of 7.1 A (typ). With a resistor present, an internal reference holds the pin voltage at 0.8 V; thus, the resulting current sets the current limit. The accuracy of the adjusted current limit will be slightly worse than that of the default value; +35% / –25% is to be expected. Resistor values should not exceed the limits shown in 図 7-3.
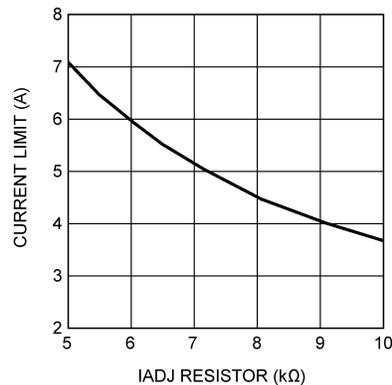
図 7-3. Current Limit vs IADJ Resistor

7.4.5 Thermal Protection

Internal thermal shutdown circuitry protects the LM22679 device, should the maximum junction temperature be exceeded. This protection is activated at about 150°C, with the result that the regulator will shut down until the temperature drops below about 135°C.

7.4.6 Duty-Cycle Limits

Ideally the regulator would control the duty cycle over the full range of zero to one. However due to inherent delays in the circuitry, there are limits on both the maximum and minimum duty cycles that can be reliably controlled. This in turn places limits on the maximum and minimum input and output voltages that can be converted by the LM22679. A minimum on-time is imposed by the regulator in order to correctly measure the switch current during a current limit event. A minimum off-time is imposed in order the re-charge the bootstrap capacitor. 式 7 can be used to determine the approximate maximum input voltage for a given output voltage.

$$ V_{in}\big|_{max} \approx \frac{V_{out} + 0.4}{T_{on} \cdot F_{sw} \cdot 1.8} $$

(7)

where

- F_{sw} is the switching frequency
- T_{ON} is the minimum on-time

Both parameters are found in セクション 6.6.

Nominal values should be used. The worst case is lowest output voltage. If this input voltage is exceeded, the regulator will skip cycles, effectively lowering the switching frequency. The consequences of this are higher output voltage ripple and a degradation of the output voltage accuracy.

Product Folder Links: *LM22679 LM22679-Q1*

The second limitation is the maximum duty cycle before the output voltage will "dropout" of regulation. 式 8 can be used to approximate the minimum input voltage before dropout occurs:

where

$$V_{in}\big|_{min} \approx \frac{V_{out} + 0.4 + I_{out} \cdot R_L}{1 - T_{off} \cdot F_{sw} \cdot 1.8} + I_{out} \cdot R_{dson}$$

(8)

- The values of T_{OFF} and $R_{DS(ON)}$ are found in *セクション 6.6*.

The worst case here is largest load. In this equation, R_L is the dc inductor resistance. Of course, the lowest input voltage to the regulator must not be less than 4.5 V (typ).

8 Application and Implementation

> **Note**
>
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8.1 Application Information

The LM22679 device is a step down dc-to-dc regulator. It is typically used to convert a higher dc voltage to a lower dc voltage with a maximum output current of 5 A. The following design procedure can be used to select components for the LM22679. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH software utilizes iterative design procedure and accesses comprehensive databases of components. Go to WEBENCH Designer for more details. This section presents a simplified discussion of the design process.

8.1.1 Output Voltage Divider Selection

For output voltages between about 1.285 V and 5 V, the -ADJ option should be used, with an appropriate voltage divider as shown in 図 8-1. 式 9 can be used to calculate the resistor values of this divider.

$$R_{FBT} = \left[\frac{V_{out}}{1.285} - 1 \right] \cdot R_{FBB}$$

(9)

A good value for R_{FBB} is 1 kΩ. This will help to provide some of the minimum load current requirement and reduce susceptibility to noise pick-up. The top of R_{FBT} should be connected directly to the output capacitor or to the load for remote sensing. If the divider is connected to the load, a local high-frequency bypass should be provided at that location.

For output voltages of 5 V, the -5.0 option should be used. In this case no external divider is needed and the FB pin is connected to the output. The approximate values of the internal voltage divider are as follows: 7.38 kΩ from the FB pin to the input of the error amplifier and 2.55 kΩ from there to ground.

Both the -ADJ and -5.0 options can be used for output voltages greater than 5 V, by using the correct output divider. As mentioned in セクション 7.3.4, the -5.0 option is optimized for output voltages of 5V. However, for output voltages greater than 5 V, this option may provide better loop bandwidth than the -ADJ option, in some applications. If the -5.0 option is to be used at output voltages greater than 5 V, 式 10 should be used to determine the resistor values in the output divider:

$$R_{FBT} = \frac{R_{FBB} \cdot (V_{out} - 5)}{5 + R_{FBB} \cdot 5 \times 10^{-4}}$$

(10)

A value of R_{FBB} of about 1 kΩ is a good first choice.
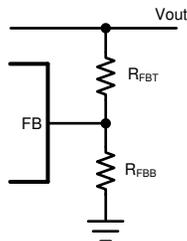

図 8-1. Resistive Feedback Divider

A maximum value of 10 kΩ is recommended for the sum of R_{FBB} and R_{FBT} to maintain good output voltage accuracy for the -ADJ option. A maximum of 2 kΩ is recommended for the -5.0 option. For the -5.0 option, the total internal divider resistance is typically 9.93 kΩ.

In all cases, the output voltage divider should be placed as close as possible to the FB pin of the LM22679, because this is a high impedance input and is susceptible to noise pick-up.

8.1.2 Power Diode

A Schottky-type power diode is required for all LM22679 applications. Ultra-fast diodes are not recommended and may result in damage to the IC due to reverse recovery current transients. The near ideal reverse recovery characteristics and low forward voltage drop of Schottky diodes are particularly important for high input voltage and low output voltage applications common to the LM22679 device. The reverse breakdown rating of the diode should be selected for the maximum V_{IN}, plus some safety margin. A good rule of thumb is to select a diode with a reverse voltage rating of 1.3 times the maximum input voltage.

Select a diode with an average current rating at least equal to the maximum load current that will be seen in the application.

8.2 Typical Application

8.2.1 Typical Buck Regulator Application

図 8-2 shows an example of converting an input voltage range of 5.5 V to 42 V, to an output of 3.3 V at 5 A.
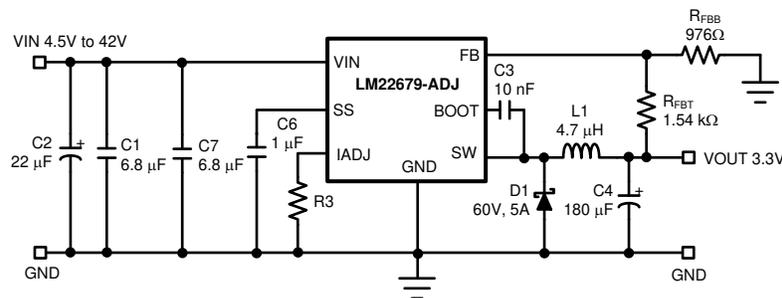
図 8-2. Typical Buck Regulator Application

8.2.1.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (VIN)	5.5 to 42 V
Output Voltage (VOUT)	3.3 V
R_{FBT}	Calculated based on R_{FBB} and V_{REF} of 1.285 V.
R_{FBB}	1 kΩ to 10 kΩ
I_{OUT}	5 A

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 External Components

The following guidelines should be used when designing a step-down (buck) converter with the LM22679.

8.2.1.2.2 Inductor

The inductor value is determined based on the load current, ripple current, and the minimum and maximum input voltages. To keep the application in continuous conduction mode (CCM), the maximum ripple current, I_{RIPPLE}, should be less than twice the minimum load current.

The general rule of keeping the inductor current peak-to-peak ripple around 30% of the nominal output current is a good compromise between excessive output voltage ripple and excessive component size and cost. Using this value of ripple current, the value of inductor, L, is calculated using 式 11.

$$L = \frac{(V_{in} - V_{out}) \cdot V_{out}}{0.3 \cdot I_{out} \cdot F_{sw} \cdot V_{in}}$$

(11)

where

- F_{sw} is the switching frequency
- V_{in} should be taken at its maximum value, for the given application

The formula in 式 11 provides a guide to select the value of the inductor L; the nearest standard value will then be used in the circuit.

Once the inductor is selected, the actual ripple current can be found from 式 12.

$$\Delta I = \frac{(V_{in} - V_{out}) \cdot V_{out}}{L \cdot F_{sw} \cdot V_{in}}$$

(12)

Increasing the inductance will generally slow down the transient response but reduce the output voltage ripple. Reducing the inductance will generally improve the transient response but increase the output voltage ripple.

The inductor must be rated for the peak current, I_{PK}, in a given application, to prevent saturation. During normal loading conditions, the peak current is equal to the load current plus 1/2 of the inductor ripple current.

During an overload condition, as well as during certain load transients, the controller may trip current limit. In this case the peak inductor current is given by I_{CL}, found in セクション 6.6. Good design practice requires that the inductor rating be adequate for this overload condition.

Note

If the inductor is not rated for the maximum expected current, it can saturate resulting in damage to the LM22679, the power diode, or both. This consideration highlights the value of the current limit adjust feature of the LM22679.

8.2.1.2.3 Input Capacitor

The input capacitor selection is based on both input voltage ripple and RMS current. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the regulator current during switch on-time. Low-ESR ceramic capacitors are preferred. Larger values of input capacitance are desirable to reduce voltage ripple and noise on the input supply. This noise may find its way into other circuitry, sharing the same input supply, unless adequate bypassing is provided. A very approximate formula for determining the input voltage ripple is shown in 式 13.

$$V_{ri} \approx \frac{I_{out}}{4 \cdot F_{sw} \cdot C_{in}}$$

(13)

where

- V_{ri} is the peak-to-peak ripple voltage at the switching frequency

Another concern is the RMS current passing through this capacitor. 式 14 determines an approximation to this current.

$$I_{rms} \approx \frac{I_{out}}{2}$$

(14)

The capacitor must be rated for at least this level of RMS current at the switching frequency.

All ceramic capacitors have large voltage coefficients, in addition to normal tolerances and temperature coefficients. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum capacitance up to the desired value. This may also help with RMS current constraints by sharing the current among several capacitors. Many times it is desirable to use an electrolytic capacitor on the input, in parallel with the ceramics. The moderate ESR of this capacitor can help to damp any ringing on the input supply caused by long power leads. This method can also help to reduce voltage spikes that can exceed the maximum input voltage rating of the LM22679.

It is good practice to include a high frequency bypass capacitor as close as possible to the LM22679. This small case size, low ESR, ceramic capacitor should be connected directly to the VIN and GND pins with the shortest possible PCB traces. Values in the range of 0.47 µF to 1 µF are appropriate. This capacitor helps to provide a low impedance supply to sensitive internal circuitry. It also helps to suppress any fast noise spikes on the input supply that can lead to increased EMI.

8.2.1.2.4 Output Capacitor

The output capacitor is responsible for filtering the output voltage and supplying load current during transients. Capacitor selection depends on application conditions as well as ripple and transient requirements. Best performance is achieved with a parallel combination of ceramic capacitors and a low ESR SP™ or POSCAP™ types. Very low ESR capacitors such as ceramics reduce the output ripple and noise spikes, while higher value electrolytics or polymers provide large bulk capacitance to supply transients. Assuming very low ESR, 式 15 gives an approximation to the output voltage ripple:

$$V_{ro} \approx \frac{(V_{in}-V_{out}) \cdot V_{out}}{8 \cdot V_{in}} \cdot \frac{1}{F_{sw}^2 \cdot L \cdot C_{out}}$$

(15)

Typically, a total value of 100 µF or greater is recommended for output capacitance.

In applications with V_{out} less than 3.3 V, it is critical that low ESR output capacitors are selected. This will limit potential output voltage overshoots as the input voltage falls below the device normal operating range.

8.2.1.2.5 Bootstrap Capacitor

The bootstrap capacitor between the BOOT pin and the SW pin supplies the gate current to turn on the N-channel MOSFET. The recommended value of this capacitor is 10 nF and should be a good quality, low-ESR ceramic capacitor. In some cases, it can be desirable to slow down the turn-on of the internal power MOSFET to reduce EMI. This can be done by placing a small resistor in series with the C_{boot} capacitor. Resistors in the range of 10 Ω to 50 Ω can be used. This technique should only be used when absolutely necessary, because it will increase switching losses and thereby reduce efficiency.

8.2.1.3 Application Curve

図 8-3. Efficiency vs I_{OUT} and V_{IN} (V_{OUT} = 3.3 V)

Product Folder Links: LM22679 LM22679-Q1
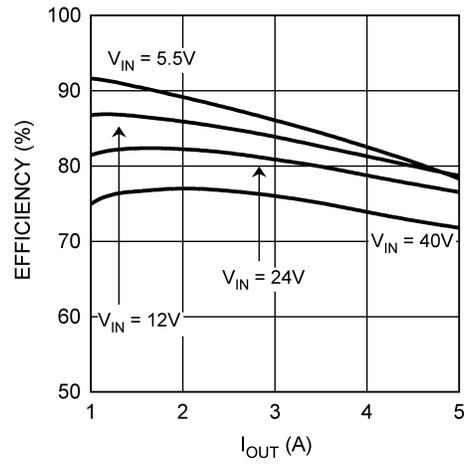
9 Power Supply Recommendations

The LM22679 device is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LM22679 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LM22679 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

Board layout is critical for the proper operation of switching power supplies. First, the ground plane area must be sufficient for thermal dissipation purposes. Second, appropriate guidelines must be followed to reduce the effects of switching noise. Switch mode converters are very fast switching devices. In such cases, the rapid increase of input current combined with the parasitic trace inductance generates unwanted L di/dt noise spikes. The magnitude of this noise tends to increase as the output current increases. This noise may turn into electromagnetic interference (EMI) and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise.

The most important layout rule is to keep the ac current loops as small as possible. 図 10-1 shows the current flow in a buck converter. The top schematic shows a dotted line which represents the current flow during the FET switch on-state. The middle schematic shows the current flow during the FET switch off-state.

The bottom schematic shows the currents referred to as ac currents. These ac currents are the most critical because they are changing in a very short time period. The dotted lines of the bottom schematic are the traces to keep as short and wide as possible. This will also yield a small loop area reducing the loop inductance. To avoid functional problems due to layout, review the PCB layout example. Best results are achieved if the placement of the LM22679, the bypass capacitor, the Schottky diode, R_{FBB}, R_{FBT}, and the inductor are placed as shown in 図 10-2. In the layout shown, R1 = R_{FBB} and R2 = R_{FBT}. It is also recommended to use 2 oz copper boards or heavier to help thermal dissipation and to reduce the parasitic inductances of board traces. See *AN-1229 SIMPLE SWITCHER ® PCB Layout Guidelines* (SNVA054) for more information.
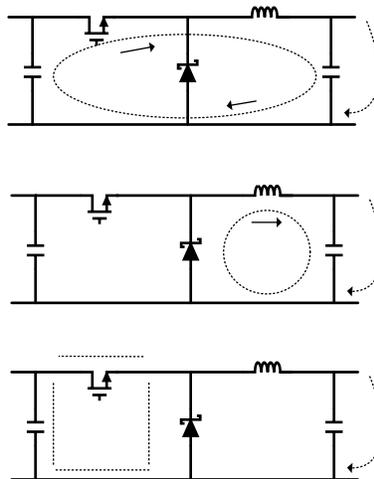

図 10-1. Current Flow in a Buck Application

10.2 Layout Example

図 10-2. LM22679 Layout Example

10.3 Thermal Considerations

The components with the highest power dissipation are the power diode and the power MOSFET internal to the LM22679 regulator. The easiest method to determine the power dissipation within the LM22679 is to measure the total conversion losses then subtract the power losses in the diode and inductor. The total conversion loss is the difference between the input power and the output power. An approximation for the power diode loss is shown in 式 16.

$$P_D = I_{out} \cdot V_D \cdot \left[1 - \frac{V_{out}}{V_{in}} \right]$$

(16)

where

- V_D is the diode voltage drop

An approximation for the inductor power is shown in 式 17.

$$P_L = I_{out}^2 \cdot R_L \cdot 1.1$$

(17)

where

- R_L is the dc resistance of the inductor
- The 1.1 factor is an approximation for the ac losses

The regulator has an exposed thermal pad to aid power dissipation. Adding multiple vias under the device to the ground plane will greatly reduce the regulator junction temperature. Selecting a diode with an exposed pad will also aid the power dissipation of the diode. The most significant variables that affect the power dissipation of the regulator are output current, input voltage and operating frequency. The power dissipated while operating near the maximum output current and maximum input voltage can be appreciable. The junction-to-ambient thermal resistance of the LM22679 will vary with the application. The most significant variables are the area of copper in the PC board, the number of vias under the IC exposed pad and the amount of forced air cooling provided. A large continuos ground plane on the top or bottom PCB layer will provide the most effective heat dissipation. The integrity of the solder connection from the IC exposed pad to the PC board is critical. Excessive voids will greatly diminish the thermal dissipation capacity. The junction-to-ambient thermal resistance of the LM22679 PFM package is specified in セクション 6.6. See *AN-2020 Thermal Design By Insight, Not Hindsight* (SNVA419) for more information.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *AN-2020 Thermal Design By Insight, Not Hindsight* (SNVA419)
- *AN-1229 SIMPLE SWITCHER ® PCB Layout Guidelines* (SNVA054)
- *AN-1891 LM22679 Evaluation Board* (SNVA365)
- *AN-1889 How to Measure the Loop Transfer Function of Power Supplies* (SNVA364)

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Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM22679QTJ-5.0/NO.A	Active	Production	TO-263 (NDR) | 7	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 QTJ-5.0
LM22679QTJ-5.0/NOPB	Active	Production	TO-263 (NDR) | 7	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 QTJ-5.0
LM22679QTJ-ADJ/NO.A	Active	Production	TO-263 (NDR) | 7	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 QTJ-ADJ
LM22679QTJ-ADJ/NOPB	Active	Production	TO-263 (NDR) | 7	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 QTJ-ADJ
LM22679QTJE-5.0/NO.A	Active	Production	TO-263 (NDR) | 7	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 QTJ-5.0
LM22679QTJE-5.0/NOPB	Active	Production	TO-263 (NDR) | 7	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 QTJ-5.0
LM22679QTJE-ADJ/NO.A	Active	Production	TO-263 (NDR) | 7	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 QTJ-ADJ
LM22679QTJE-ADJ/NOPB	Active	Production	TO-263 (NDR) | 7	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 QTJ-ADJ
LM22679TJ-5.0/NOPB	Active	Production	TO-263 (NDR) | 7	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 TJ-5.0
LM22679TJ-5.0/NOPB.A	Active	Production	TO-263 (NDR) | 7	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 TJ-5.0
LM22679TJ-ADJ/NOPB	Active	Production	TO-263 (NDR) | 7	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 TJ-ADJ
LM22679TJ-ADJ/NOPB.A	Active	Production	TO-263 (NDR) | 7	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 TJ-ADJ
LM22679TJE-5.0/NO.A	Active	Production	TO-263 (NDR) | 7	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 TJ-5.0
LM22679TJE-5.0/NOPB	Active	Production	TO-263 (NDR) | 7	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 TJ-5.0
LM22679TJE-ADJ/NO.A	Active	Production	TO-263 (NDR) | 7	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 TJ-ADJ
LM22679TJE-ADJ/NOPB	Active	Production	TO-263 (NDR) | 7	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM22679 TJ-ADJ

(1) Status: For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF LM22679, LM22679-Q1 :

- Catalog : LM22679

- Automotive : LM22679-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
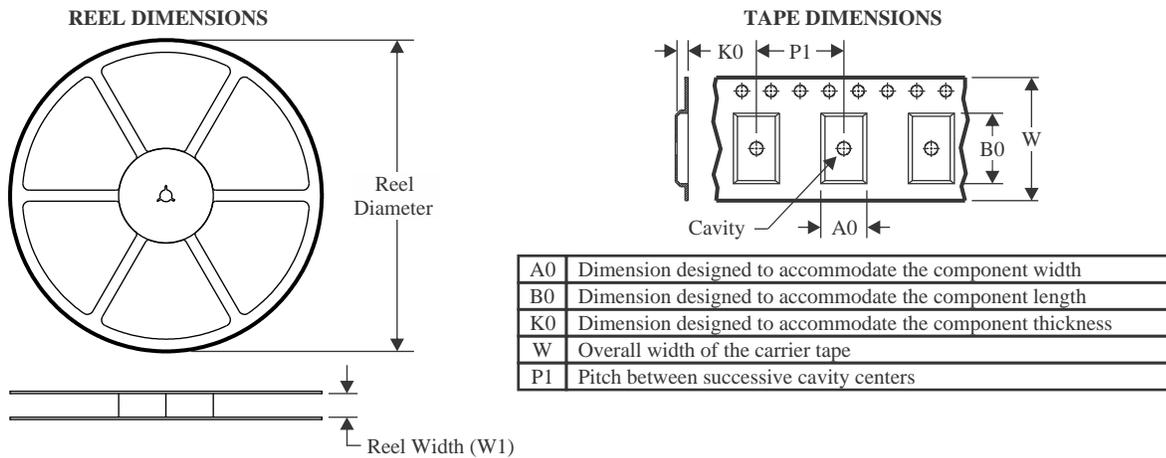
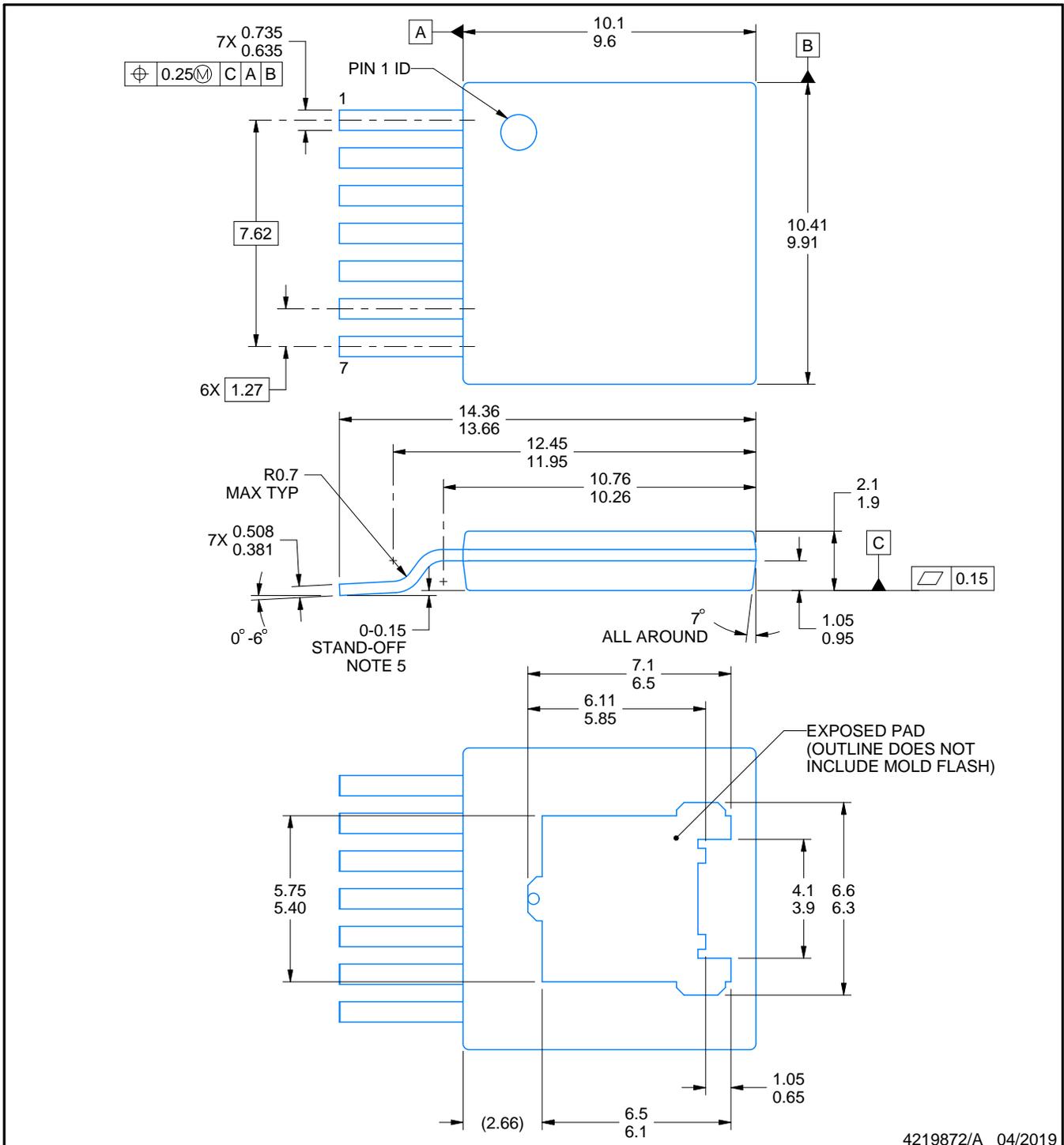**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM22679QTJ-5.0/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22679QTJ-ADJ/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22679QTJE-5.0/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22679QTJE-ADJ/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22679TJ-5.0/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22679TJ-ADJ/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22679TJE-5.0/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22679TJE-ADJ/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM22679QTJ-5.0/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22679QTJ-ADJ/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22679QTJE-5.0/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0
LM22679QTJE-ADJ/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0
LM22679TJ-5.0/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22679TJ-ADJ/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22679TJE-5.0/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0
LM22679TJE-ADJ/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0

7X $\frac{0.735}{0.635}$

⊕ | 0.25 Ⓜ | C | A | B

PIN 1 ID

A

$\frac{10.1}{9.6}$

B

1

$\frac{10.41}{9.91}$

7.62

7

6X 1.27

$\frac{14.36}{13.66}$

$\frac{12.45}{11.95}$

$\frac{10.76}{10.26}$

R0.7
MAX TYP

7X $\frac{0.508}{0.381}$

$\frac{2.1}{1.9}$

C

□ 0.15

0°-6°

0-0.15
STAND-OFF
NOTE 5

7°
ALL AROUND

$\frac{1.05}{0.95}$

$\frac{7.1}{6.5}$

$\frac{6.11}{5.85}$

EXPOSED PAD
(OUTLINE DOES NOT
INCLUDE MOLD FLASH)

$\frac{5.75}{5.40}$

4.1   6.6
3.9   6.3

$\frac{1.05}{0.65}$

(2.66)

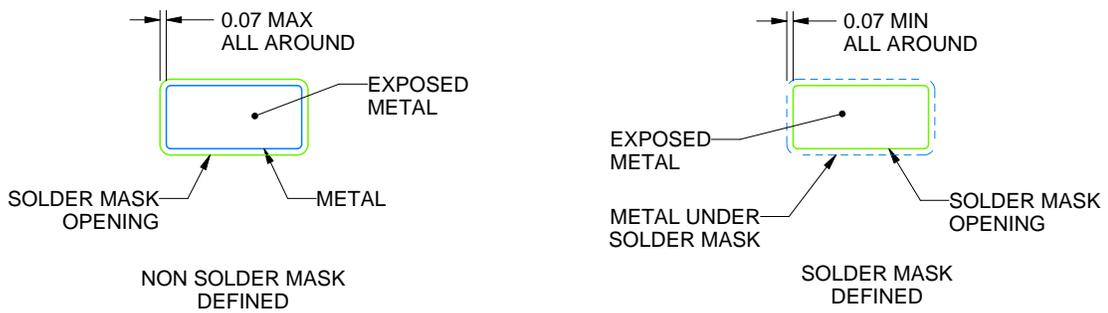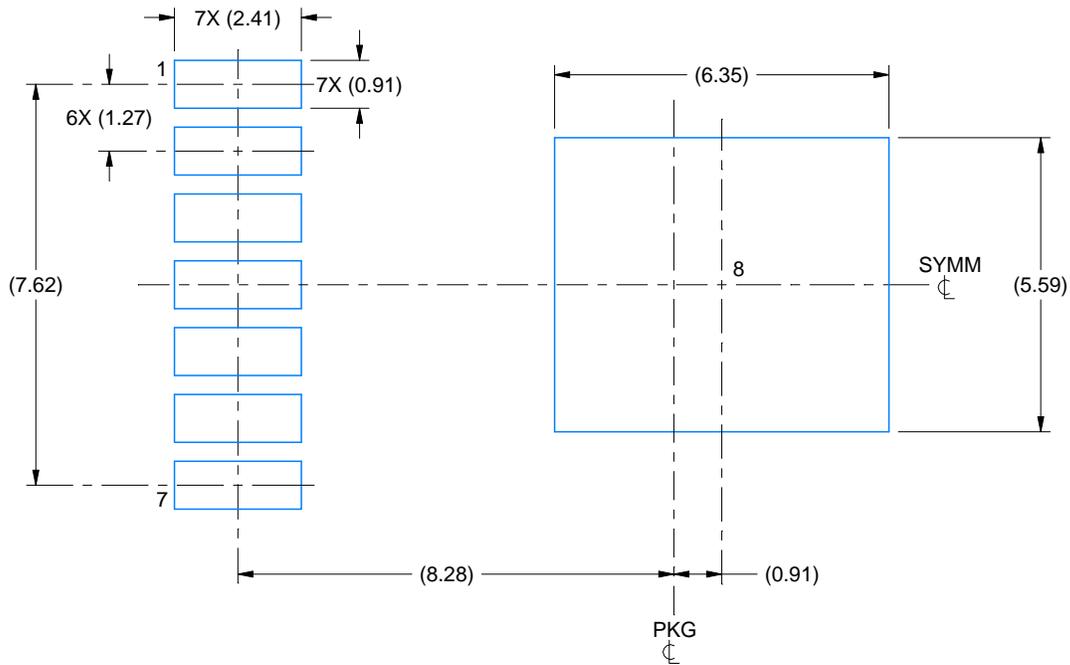$\frac{6.5}{6.1}$

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-279B.
5. Under all conditions, leads must not be above Datum C

7X (2.41)

1

7X (0.91)

6X (1.27)

(6.35)

(7.62)

8

SYMM

(5.59)

7

(8.28)

(0.91)

PKG

0.07 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED

0.07 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

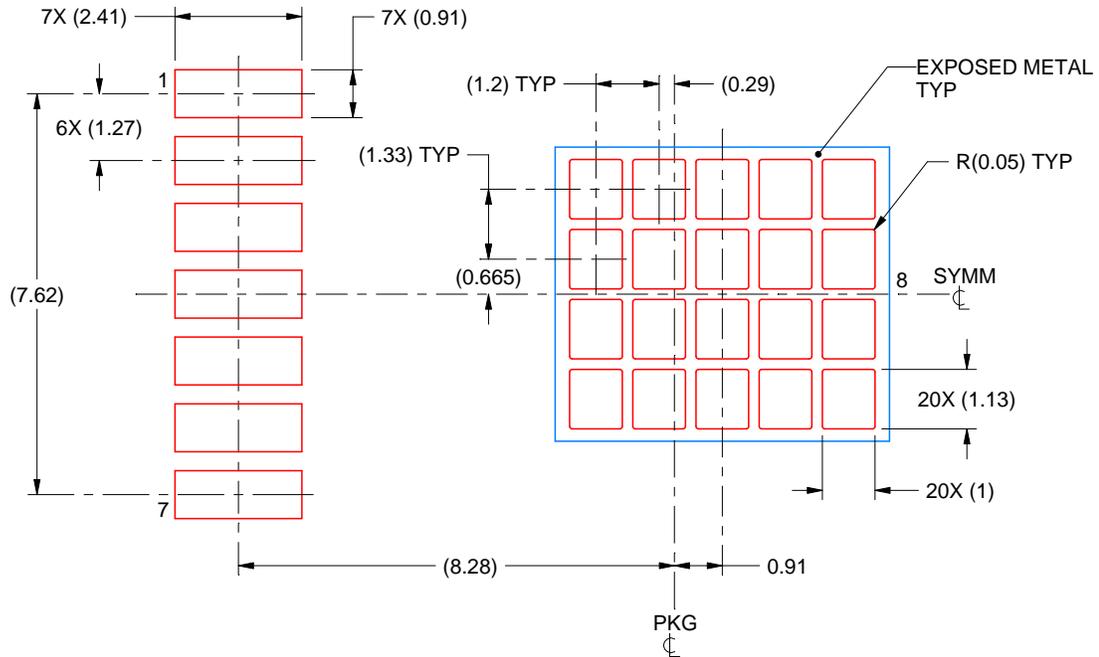SOLDER MASK DETAILS

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NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers
SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

7X (2.41)
7X (0.91)

1

6X (1.27)

(1.2) TYP
(0.29)

EXPOSED METAL
TYP

(1.33) TYP

R(0.05) TYP

(7.62)

(0.665)

8 SYMM

20X (1.13)

7

20X (1)

(8.28)
0.91

PKG

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
64% PRINTED SOLDER COVERAGE BY AREA
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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