# LM3100 1MHz 1.5A同期整流降圧型レギュレータ

## 1 特長

- 入力電圧範囲: 4.5V～36V
- 出力電流: 1.5A
- 0.8V、±1.5%リファレンス
- 耐圧40VのデュアルNチャネル同期整流降圧型スイッチ内蔵
- 外付け部品点数が少なく、小型
- ループ補償が不要
- 超高速の過渡応答
- セラミック・コンデンサなどの低ESRコンデンサ接続により安定動作
- 最大1MHzまでスイッチング周波数を設定可能
- スタートアップ時に最大デューティ・サイクルを制限
- バレー型の電流制限
- 最小0.8Vまでの可変出力に対応する高精度の内部リファレンス
- サーマル・シャットダウン
- 放熱特性の優れたHTSSOP-20パッケージ

## 2 アプリケーション

- 5VDC、12VDC、24VDC、12VAC、24VACの各システム
- 組み込みシステム
- 産業用制御
- 車載用テレマティクス/ボディ・エレクトロニクス
- POL (Point of Load)型レギュレータ
- ストレージ・システム
- ブロードバンド・インフラストラクチャ
- 2/3/4セルのリチウム電池システムからの直接変換

## 3 概要

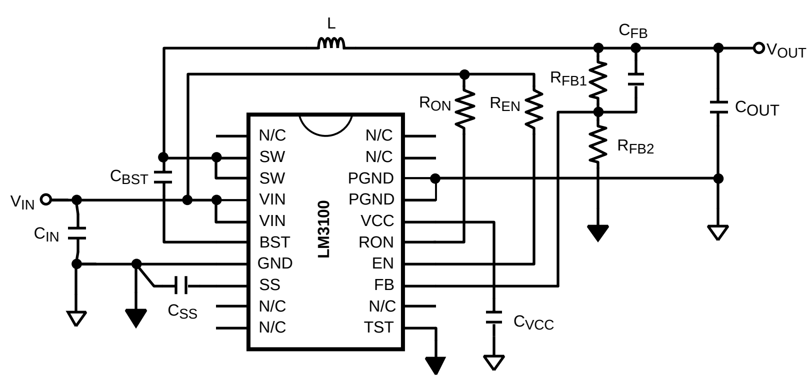
LM3100同期整流降圧型コンバータは、最小0.8Vの出力電圧で1.5Aの負荷電流を供給できる、低コストで高効率の降圧型レギュレータを実現するために必要なすべての機能を備えています。耐圧40VのNチャネル同期整流型デュアルMOSFETスイッチにより、外付け部品点数を削減できるため、設計を簡素化し、基板スペースを最小限に抑えることができます。LM3100は、セラミック・コンデンサなど、ESRの非常に小さい出力コンデンサを接続した場合に極めて良好に動作するよう設計されています。コンスタント・オンタイム(COT)制御方式によりループ補償回路が不要となるため、負荷過渡応答が高速になり、単純な回路構成を実現できます。独自の設計回路を採用することにより、COT制御方式のその他のレギュレータとは異なり、出力コンデンサのESRに依存せずに安定性を確保することが可能です。入力電圧とオン時間は反比例の関係にあるため、入力電圧や負荷の変動に対して動作周波数はほぼ一定に維持されます。動作周波数は外付け部品による設定が可能で、最大1MHzです。$V_{CC}$低電圧誤動作防止、サーマル・シャットダウン、ゲート駆動低電圧誤動作防止の各保護回路を内蔵しています。本製品は、放熱特性の優れたHTSSOP-20パッケージで供給されます。

**製品情報**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| LM3100 | HTSSOP (20) | 6.50mm×4.40mm |

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

**代表的なアプリケーション**






English Data Sheet: SNVS421

# 目次



## 4 改訂履歴

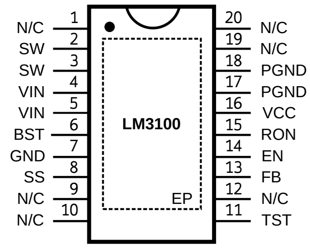
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| **Revision F (December 2009)** から **Revision G** に変更 | **Page** |
|---|---|
| • Changed layout of National Semiconductor Data Sheet to TI format | 16 |

| **Revision G (April 2013)** から **Revision H** に変更 | **Page** |
|---|---|
| • 「*アプリケーションと実装*」セクション、「*製品情報*」表、「*ピン構成および機能*」セクション、「*ESD定格*」表、「*熱に関する情報*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 | 1 |
| • タイトルからSimple Switcher 削除 | 1 |

# 5 Pin Configuration and Functions

**PWP Package**
**20-Pin HTSSOP**
**Top View**




**Pin Functions**

| PIN | | DESCRIPTION |
|---|---|---|
| NO. | NAME | |
| 1,9,10,12,19,20 | N/C | No Connection<br>These pins must be left unconnected. |
| 2, 3 | SW | Switching Node<br>Internally connected to the buck switch source. Connect to output inductor. |
| 4, 5 | VIN | Input supply voltage<br>Supply pin to the device. Nominal input range is 4.5 V to 36 V. |
| 6 | BST | Connection for bootstrap capacitor<br>Connect a 0.033 µF capacitor from SW pin to this pin. An internal diode charges the capacitor during the high-side switch off-time. |
| 7 | GND | Analog Ground<br>Ground for all internal circuitry other than the synchronous switches. |
| 8 | SS | Soft-start<br>An internal 8 µA current source charges an external capacitor to provide the soft- start function. |
| 11 | TST | Test mode enable pin<br>Force the device into test mode. Must be connected to ground for normal operation. |
| 13 | FB | Feedback<br>Internally connected to the regulation and over-voltage comparators. The regulation setting is 0.8 V at this pin. Connect to feedback divider. |
| 14 | EN | Enable pin<br>Connect a voltage higher than 1.26 V to enable the regulator. |
| 15 | RON | On-time Control<br>An external resistor from VIN to this pin sets the high-side switch on-time. |
| 16 | VCC | Start-up regulator Output<br>Nominally regulated to 6 V. Connect a capacitor of not less than 680 nF between VCC and GND for stable operation. |
| 17, 18 | PGND | Power Ground<br>Synchronous rectifier MOSFET source connection. Tie to power ground plane. |
| DAP | EP | Exposed Pad<br>Thermal connection pad, connect to GND. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

| | MIN | MAX | UNIT |
|---|---|---|---|
| VIN, RON to GND | –0.3 | 40 | V |
| SW to GND | –0.3 | 40 | V |
| SW to GND (Transient) | –2 | (< 100 ns) | V |
| VIN to SW | –0.3 | 40 | V |
| BST to SW | –0.3 | 7 | V |
| All Other Inputs to GND | –0.3 | 7 | V |
| Junction Temperature, $T_J$ | –65 | 150 | °C |
| Storage temperature, $T_{stg}$ | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2) | ±2 | kV |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply Voltage Range $V_{IN}$ | 4.5 | 36 | V |
| Junction Temperature Range $T_J$ | –40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | LM3100<br>PWP (HTSSOP)<br>20 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-case thermal resistance | 6.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

at $T_J$ = 25°C, and $V_{IN}$ = 18 V, $V_{OUT}$ = 3.3 V (unless otherwise noted).(1)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **START-UP REGULATOR, $V_{CC}$** | | | | | | | |
| $V_{CC}$ | Output voltage | $C_{CC}$ = 680 nF, no load | $T_J$ = –40°C to 125°C | 5.0 | 6.0 | 7.2 | V |
| $V_{IN}$ - $V_{CC}$ | Dropout voltage | $I_{CC}$ = 2 mA | $T_J$ = –40°C to 125°C | | 50 | 140 | mV |
| | | $I_{CC}$ = 20 mA | $T_J$ = –40°C to 125°C | | 350 | 570 | |
| $I_{VCCL}$ | Current limit(1) | $V_{CC}$ = 0 V | $T_J$ = –40°C to 125°C | 40 | 65 | | mA |
| $V_{CC-UVLO}$ | Under-voltage lockout threshold | $V_{IN}$ increasing | $T_J$ = –40°C to 125°C | 3.6 | 3.75 | 3.85 | V |
| $V_{CC-UVLO-HYS}$ | UVLO hysteresis | $V_{IN}$ decreasing | | | 130 | | mV |
| $t_{VCC-UVLO-D}$ | UVLO filter delay | | | | 3 | | µs |
| $I_{IN}$ | Operating current | No switching, $V_{FB}$ = 1 V | $T_J$ = –40°C to 125°C | | 0.7 | 1 | mA |
| $I_{IN-SD}$ | Operating current, Device shutdown | $V_{EN}$ = 0 V | $T_J$ = –40°C to 125°C | | 17 | 30 | µA |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| $R_{DS-UP-ON}$ | Main MOSFET Rds(on) | | $T_J$ = –40°C to 125°C | | 0.18 | 0.35 | Ω |
| $R_{DS-DN-ON}$ | Syn. MOSFET Rds(on) | | $T_J$ = –40°C to 125°C | | 0.11 | 0.2 | Ω |
| $V_{G-UVLO}$ | Gate drive voltage UVLO | $V_{BST}$ - $V_{SW}$ increasing | $T_J$ = –40°C to 125°C | | 3.3 | 4 | V |
| **SOFT-START** | | | | | | | |
| $I_{SS}$ | SS pin source current | $V_{SS}$ = 0.5 V | $T_J$ = –40°C to 125°C | 6 | 8 | 9.8 | µA |
| **CURRENT LIMIT** | | | | | | | |
| $I_{CL}$ | Syn. MOSFET current limit threshold | | | | 1.9 | | A |
| **ON/OFF TIMER** | | | | | | | |
| $t_{ON}$ | ON timer pulse width | $V_{IN}$ = 10 V, $R_{ON}$ = 100 kΩ | | | 1.38 | | µs |
| | | $V_{IN}$ = 30 V, $R_{ON}$ = 100 kΩ | | | 0.47 | | |
| $t_{ON-MIN}$ | ON timer minimum pulse width | | | | 200 | | ns |
| $t_{OFF}$ | OFF timer pulse width | | | | 260 | | ns |
| **ENABLE INPUT** | | | | | | | |
| $V_{EN}$ | EN Pin input threshold | $V_{EN}$ rising | $T_J$ = –40°C to 125°C | 1.236 | 1.26 | 1.285 | V |
| $V_{EN-HYS}$ | Enable threshold hysteresis | $V_{EN}$ falling | | | 90 | | mV |
| **REGULATION and OVER-VOLTAGE COMPARATOR** | | | | | | | |
| $V_{FB}$ | In-regulation feedback voltage | $V_{SS}$ ≥ 0.8 V | $T_J$ = –40°C to 125°C | 0.784 | 0.8 | 0.816 | V |
| | | $V_{SS}$ ≥ 0.8 V | $T_J$ = –40°C to 125°C | 0.788 | | 0.812 | |
| $V_{FB-OV}$ | Feedback over-voltage threshold | | $T_J$ = –40°C to 125°C | 0.894 | 0.920 | 0.940 | V |
| $I_{FB}$ | | | $T_J$ = –40°C to 125°C | | 5 | 100 | nA |
| **THERMAL SHUTDOWN** | | | | | | | |
| $T_{SD}$ | Thermal shutdown temperature | $T_J$ rising | | | 165 | | °C |
| $T_{SD-HYS}$ | Thermal shutdown temperature hysteresis | $T_J$ falling | | | 20 | | °C |

(1) $V_{CC}$ provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

## 6.6 Typical Characteristics

All curves taken at $V_{IN}$ = 18 V with configuration in typical application circuit for $V_{OUT}$ = 3.3 V shown in this datasheet. $T_A$ = 25°C, unless otherwise specified.

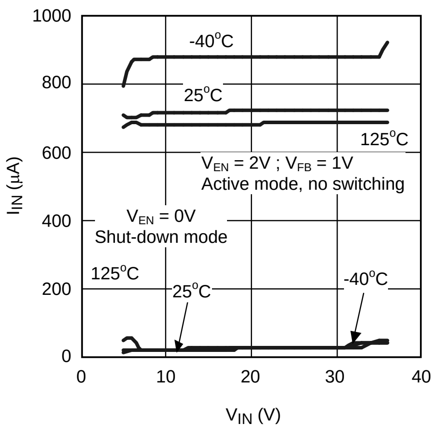



**Figure 1. Quiescent Current, $I_{IN}$ vs $V_{IN}$**

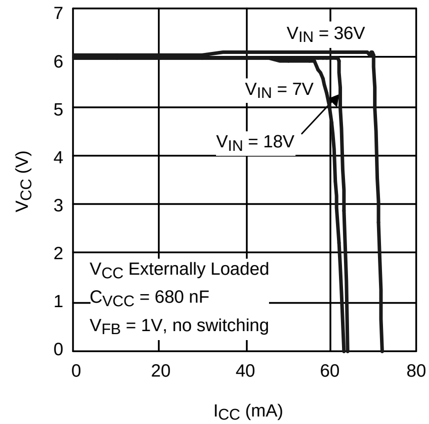



**Figure 2. $V_{CC}$ vs $I_{CC}$**

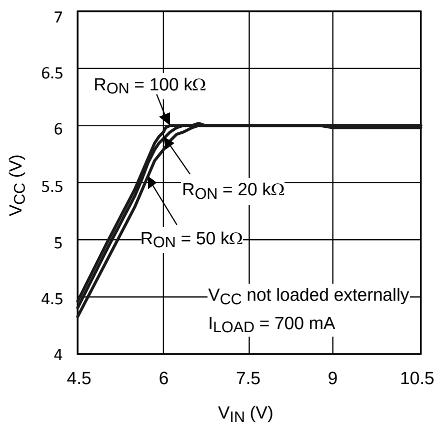



**Figure 3. $V_{CC}$ vs $V_{IN}$**

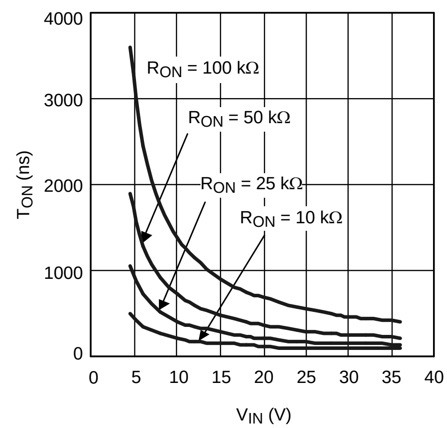



**Figure 4. $T_{ON}$ vs $V_{IN}$**

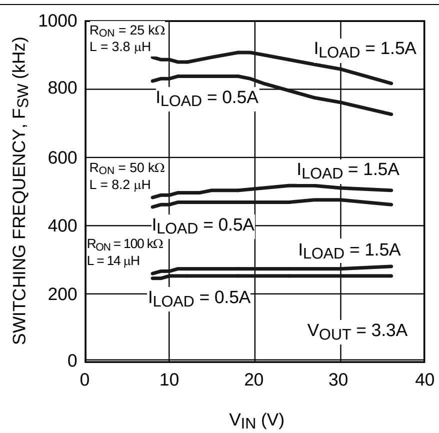



**Figure 5. Switching Frequency, $F_{SW}$ vs $V_{IN}$**

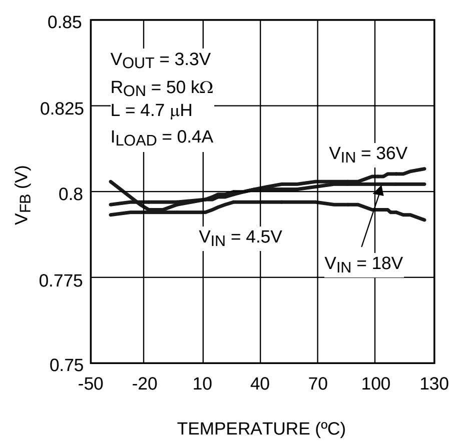



**Figure 6. $V_{FB}$ vs Temperature**

## Typical Characteristics (continued)

All curves taken at $V_{IN}$ = 18 V with configuration in typical application circuit for $V_{OUT}$ = 3.3 V shown in this datasheet. $T_A$ = 25°C, unless otherwise specified.

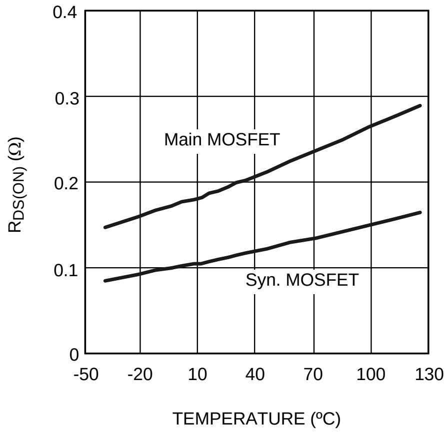
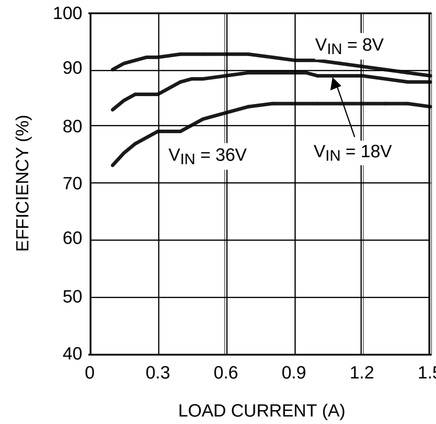
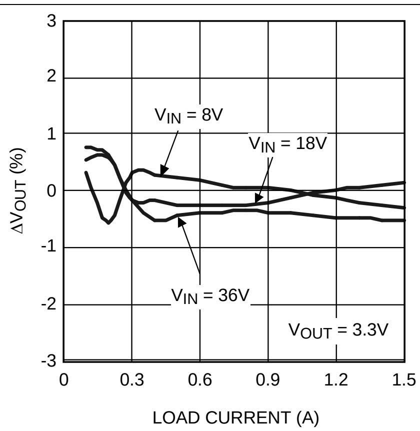



**Figure 7. $R_{DS(ON)}$ vs Temperature**



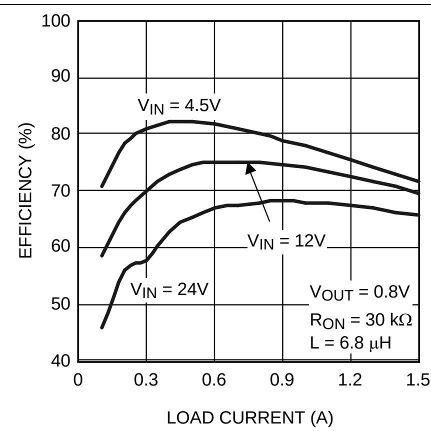

$V_{OUT}$ = 3.3 V

**Figure 8. Efficiency vs Load Current**



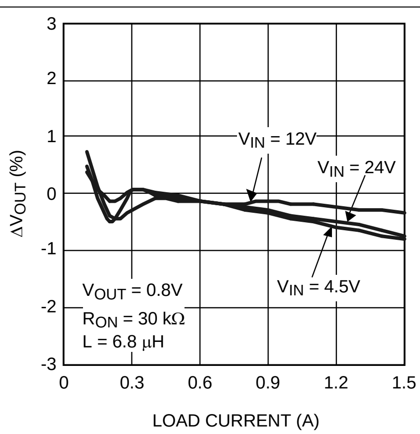

$V_{OUT}$ = 3.3 V

**Figure 9. $V_{OUT}$ Regulation vs Load Current**



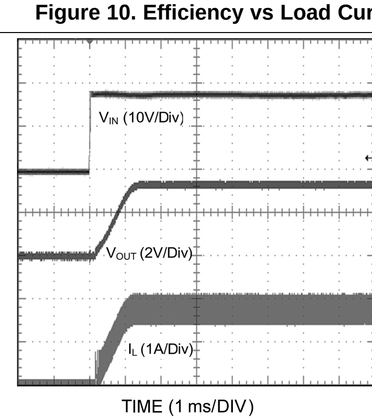

$V_{OUT}$ = 0.8 V

**Figure 10. Efficiency vs Load Current**




$V_{OUT}$ = 0.8 V

**Figure 11. $V_{OUT}$ Regulation vs Load Current**

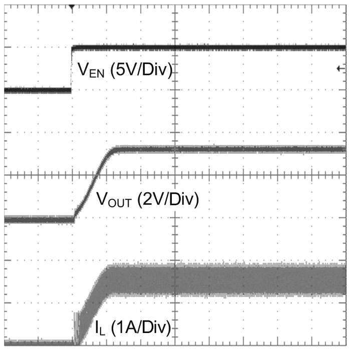



$V_{OUT}$ = 3.3 V, 1.5 A Loaded

**Figure 12. Power Up**

## Typical Characteristics (continued)

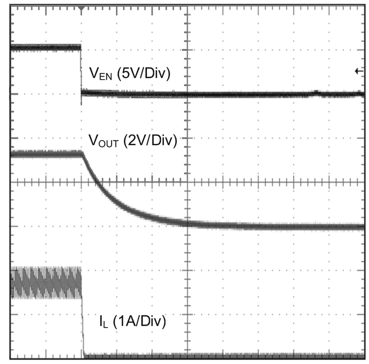
All curves taken at $V_{IN}$ = 18 V with configuration in typical application circuit for $V_{OUT}$ = 3.3 V shown in this datasheet. $T_A$ = 25°C, unless otherwise specified.




TIME (1ms/DIV)

$V_{OUT}$ = 3.3 V, 1.5 A Loaded

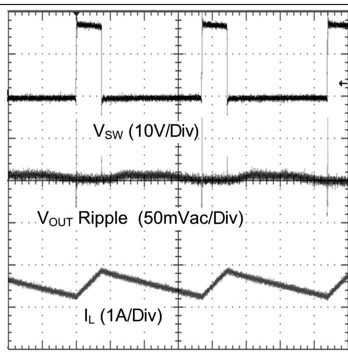
**Figure 13. Enable Transient**




TIME (1ms/DIV)

$V_{OUT}$ = 3.3 V, 1.5 A Loaded

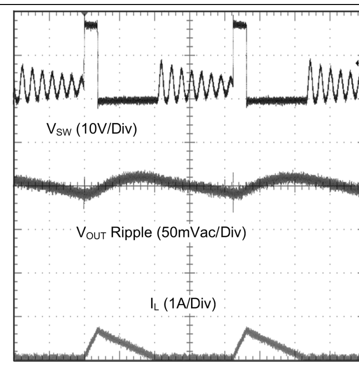
**Figure 14. Shutdown Transient**




TIME (1 µs/DIV)

$V_{OUT}$ = 3.3 V, 1.5 A Loaded

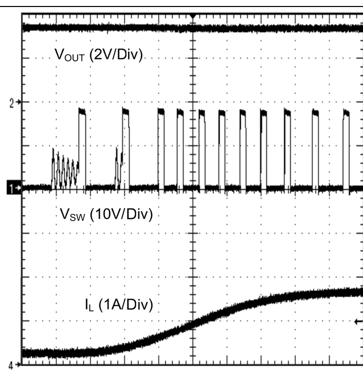
**Figure 15. Continuous Mode Operation**




TIME (1 µs/DIV)

$V_{OUT}$ = 3.3 V, 0.15 A Loaded

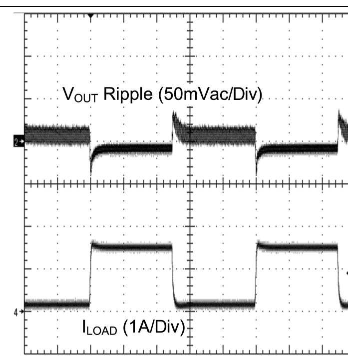
**Figure 16. Discontinuous Mode Operation**




TIME (4 µs/DIV)

$V_{OUT}$ = 3.3 V, 0.15 A - 1.5 A Load

**Figure 17. CCM to DCM Transition**




TIME (400 µs/DIV)

$V_{OUT}$ = 3.3 V, 0.15 A - 1.5 A Load Current slew-rate: 2.5 A/µs

**Figure 18. Load Transient**

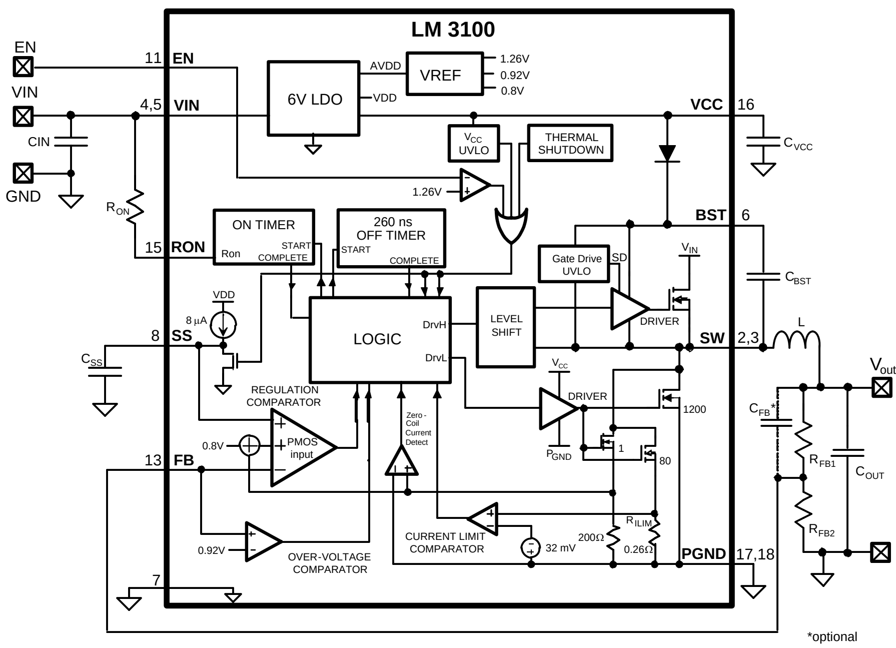
# 7 Detailed Description

## 7.1 Overview

The LM3100 Step Down Switching Regulator features all functions needed to implement a cost effective, efficient buck power converter capable of supplying 1.5 A to a load. This voltage regulator contains Dual 40-V N-Channel buck synchronous switches and is available in a thermally enhanced HTSSOP-20 package. The Constant ON-Time (COT) regulation scheme requires no loop compensation, results in fast load transient response, and simplifies circuit implementation. It will work correctly even with an all ceramic output capacitor network and does not rely on the output capacitor's ESR for stability. The operating frequency remains constant with line and load variations due to the inverse relationship between the input voltage and the on-time. The valley current limit detection circuit, internally set at 1.9 A, inhibits the high-side switch until the inductor current level subsides. Please refer to the functional block diagram with a typical application circuit.

The LM3100 can be applied in numerous applications and can operate efficiently from inputs as high as 36 V. Protection features include: Thermal shutdown, $V_{CC}$ under-voltage lockout, gate drive under-voltage lockout.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Hysteretic Control Circuit Overview

The LM3100 buck DC-DC regulator employs a control scheme in which the high-side switch on-time varies inversely with the line voltage ($V_{IN}$). Control is based on a comparator and the one-shot on-timer, with the output voltage feedback (FB) compared with an internal reference of 0.8 V. If the FB level is below the reference the buck switch is turned on for a fixed time determined by the input voltage and a programming resistor ($R_{ON}$). Following the on-time, the switch remains off for a minimum of 260 ns. If FB is below the reference at that time the switch turns on again for another on-time period. The switching will continue until regulation is achieved.

The regulator will operate in discontinuous conduction mode at light load currents, and continuous conduction mode with heavy load current. In discontinuous conduction mode (DCM), current through the output inductor starts at zero and ramps up to a peak during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below the internal reference. Until then the inductor current remains zero and the load is supplied entirely by the output capacitor. In this mode the operating frequency is lower than in continuous conduction mode, and varies with load current. Conversion efficiency is maintained since the switching losses are reduced with the reduction in load and switching frequency. The discontinuous operating frequency can be calculated approximately as follows:

## Feature Description (continued)

$$F_{SW} = \frac{V_{OUT}\ (V_{IN} - 1) \times L \times 1.18 \times 10^{20} \times I_{OUT}}{(V_{IN} - V_{OUT}) \times R_{ON}^{2}} \quad (1)$$

In continuous conduction mode (CCM), current always flows through the inductor and never reaches zero during the off-time. In this mode, the operating frequency remains relatively constant with load and line variations. The CCM operating frequency can be calculated approximately as follows:

$$F_{SW} = \frac{V_{OUT}}{1.3 \times 10^{-10} \times R_{ON}} \quad (2)$$

The output voltage is set by two external resistors ($R_{FB1}$, $R_{FB2}$). The regulated output voltage is calculated as follows:

$$V_{OUT} = 0.8\ V \times (R_{FB1} + R_{FB2})/R_{FB2} \quad (3)$$

## 7.4 Device Functional Modes

### 7.4.1 Start-up Regulator ($V_{CC}$)

The start-up regulator is integrated within LM3100. The input pin (VIN) can be connected directly to line voltage up to 36 V, with transient capability of 40 V. The $V_{CC}$ output regulates at 6 V, and is current limited to 65 mA. Upon power up, the regulator sources current into the external capacitor at $V_{CC}$ ($C_{VCC}$). $C_{VCC}$ must be at least 680 nF for stability. When the voltage on the VCC pin reaches the under-voltage lockout threshold of 3.75 V, the buck switch is enabled and the Soft-start pin is released to allow the soft-start capacitor ($C_{SS}$) to charge.

The minimum input voltage is determined by the dropout voltage of $V_{CC}$ regulator, and the $V_{CC}$ UVLO falling threshold (≅3.7 V). If VIN is less than ≅4.0 V, the $V_{CC}$ UVLO activates to shut off the output.

### 7.4.2 Regulation Comparator

The feedback voltage at FB pin is compared to the internal reference voltage of 0.8 V. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at FB falls below 0.8 V. The buck switch stays on for the on-time, causing the FB voltage to rise above 0.8 V. After the on-time period, the buck switch stays off until the FB voltage falls below 0.8 V again. Bias current at the FB pin is nominally 100 nA.

### 7.4.3 Over-Voltage Comparator

The voltage at FB pin is compared to an internal 0.92 V reference. If the feedback voltage rises above 0.92 V the on-time pulse is immediately terminated. This condition can occur if the input voltage, or the output load, changes suddenly. Once the OVP is activated, the buck switch remains off until the voltage at FB pin falls below 0.92 V. The low side switch will stay on to discharge the inductor energy until the inductor current decays to zero. The low side switch will be turned off.

### 7.4.4 ON-Time Timer, Shutdown

The ON-Time of LM3100 main switch is determined by the $R_{ON}$ resistor and the input voltage ($V_{IN}$), and is calculated from:

$$t_{ON} = \frac{1.3 \times 10^{-10} \times R_{ON}}{V_{IN}} \quad (4)$$

The inverse relationship of $t_{ON}$ and $V_{IN}$ results in a nearly constant switching frequency as $V_{IN}$ is varied. $R_{ON}$ should be selected for a minimum on-time (at maximum $V_{IN}$) greater than 200 ns for proper current limit operation. This requirement limits the maximum frequency for each application, depending on $V_{IN}$ and $V_{OUT}$, calculated from Equation 5:

$$F_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \times 200\ ns} \quad (5)$$

The LM3100 can be remotely shut down by taking the EN pin below 1.1 V. Refer to Figure 19. In this mode the SS pin is internally grounded, the on-timer is disabled, and bias currents are reduced. Releasing the EN pin allows normal operation to resume.

## Device Functional Modes (continued)

For normal operation, the voltage at the EN pin is set between 1.5 V and 3.0 V, depending on $V_{IN}$ and the external pull-up resistor. For all cases, this voltage must be limited not to exceed 7 V.

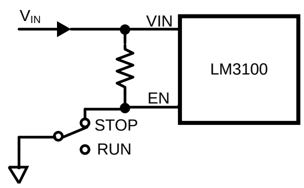



**Figure 19. Shutdown Implementation**

### 7.4.5 Current Limit

Current limit detection occurs during the off-time by monitoring the re-circulating current through the low-side synchronous switch. Referring to Functional Block Diagram, when the buck switch is turned off, inductor current flows through the load, into PGND, and through the internal low-side synchronous switch. If that current exceeds 1.9 A the current limit comparator toggles, forcing a delay to the start of the next on-time period. The next cycle starts when the re-circulating current falls back below 1.9 A and the voltage at FB is below 0.8 V. The inductor current is monitored during the low-side switch on-time. As long as the overload condition persists and the inductor current exceeds 1.9 A, the high-side switch will remain inhibited. The operating frequency is lower during an over-current due to longer than normal off-times.

Figure 20 illustrates an inductor current waveform, the average inductor current is equal to the output current, $I_{OUT}$ in steady state. When an overload occurs, the inductor current will increase until it exceeds the current limit threshold, 1.9 A. Then the control keeps the high-side switch off until the inductor current ramps down below 1.9 A. Within each on-time period, the current ramps up an amount equal to:

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L} \quad (6)$$

During this time the LM3100 is in a constant current mode, with an average load current ($I_{OCL}$) equal to 1.9 A $+\Delta I/2$.

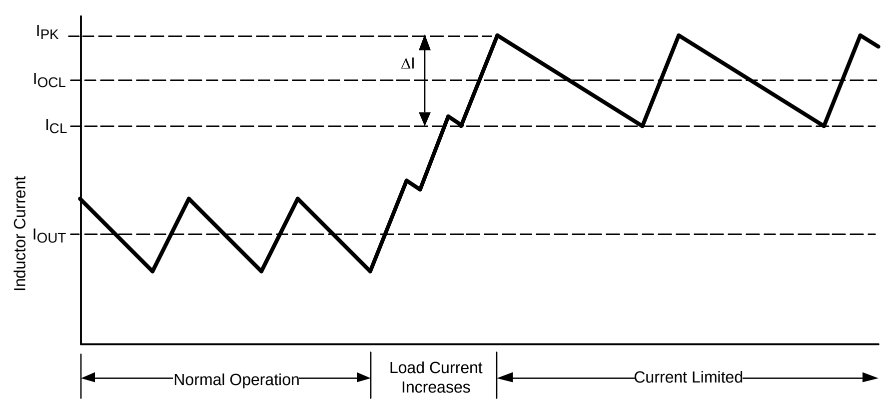



**Figure 20. Inductor Current - Current Limit Operation**

### 7.4.6 N-Channel Buck Switch and Driver

The LM3100 integrates an N-Channel buck (high-side) switch and associated floating high voltage gate driver. The gate drive circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 33 nF capacitor ($C_{BST}$) connected between BST and SW pins provides voltage to the high-side driver during the buck switch on-time. During each off-time, the SW pin falls to approximately –1 V and $C_{BST}$ charges from the $V_{CC}$ supply through the internal diode. The minimum off-time of 260 ns ensures adequate time each cycle to recharge the bootstrap capacitor.

## Device Functional Modes (continued)

### 7.4.7 Soft-Start

The soft-start feature allows the converter to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. Upon turn-on, after $V_{CC}$ reaches the under-voltage threshold, an internal 8 µA current source charges up the external capacitor at the SS pin. The ramping voltage at SS (and the non-inverting input of the regulation comparator) ramps up the output voltage in a controlled manner.

An internal switch grounds the SS pin if any of the following cases happen: (i) VCC falls below the under-voltage lock-out threshold; (ii) a thermal shutdown occurs; or (iii) the EN pin is grounded. Alternatively, the converter can be disabled by connecting the SS pin to ground using an external switch. Releasing the switch allows the SS pin return to pull high and the output voltage returns to normal. The shut-down configuration is shown in Figure 21 .

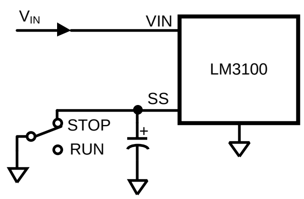



**Figure 21. Alternate Shutdown Implementation**

### 7.4.8 Thermal Protection

The LM3100 should be operated so the junction temperature does not exceed the maximum limit. An internal Thermal Shutdown circuit, which activates (typically) at 165°C, takes the controller to a low power reset state by disabling the buck switch and the on-timer, and grounding the SS pin. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature falls back below 145°C (typical hysteresis = 20°C), the SS pin is released and normal operation resumes.

# 8 Applications and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Applications Information

### 8.1.1 External Components

The following guidelines can be used to select the external components.

#### *8.1.1.1 $R_{FB1}$ and $R_{FB2}$*

The ratio of these resistors is calculated from:

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT}}{0.8V} - 1 \tag{7}$$

$R_{FB1}$ and $R_{FB2}$ should be chosen from standard value resistors in the range of 1.0 kΩ - 10 kΩ which satisfy the above ratio.

For $V_{OUT}$ = 0.8 V, the FB pin can be connected to the output directly. However, the converter operation needs a minimum inductor current ripple to maintain good regulation when no load is connected. This minimum load is about 10 µA and can be implemented by adding a pre-load resistor to the output.

#### *8.1.1.2 $R_{ON}$*

The minimum value for $R_{ON}$ is calculated from:

$$R_{ON} \geq \frac{200\text{ ns} \times V_{IN(MAX)}}{1.3 \times 10^{-10}} \tag{8}$$

Equation 2 in Hysteretic Control Circuit Overview section can be used to select $R_{ON}$ if a specific frequency is desired as long as the above limitation is met.

#### *8.1.1.3 L*

The main parameter affected by the inductor is the output current ripple amplitude ($I_{OR}$). The maximum allowable ($I_{OR}$) must be determined at both the minimum and maximum nominal load currents. At minimum load current, the lower peak must not reach 0 A. At maximum load current, the upper peak must not exceed the current limit threshold (1.9 A). The allowable ripple current is calculated from the following equations:

$$I_{OR(MAX1)} = 2 \times I_{O(min)} \tag{9}$$

or

$$I_{OR(MAX2)} = 2 \times (1.9\text{ A} - I_{O(max)}) \tag{10}$$

The lesser of the two ripple amplitudes calculated above is then used in the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{OR} \times F_S \times V_{IN}} \tag{11}$$

where $V_{IN}$ is the maximum input voltage and Fs is determined from Equation 1. This provides a value for L. The next larger standard value should be used. L should be rated for the $I_{PK}$ current level shown in Figure 20.

## Applications Information (continued)

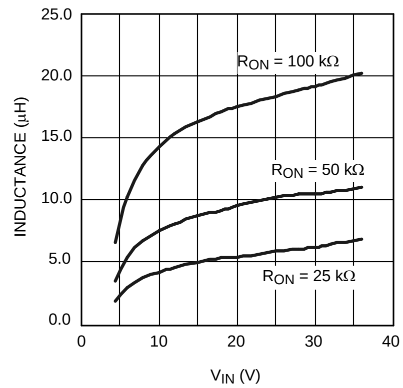



**Figure 22. Inductor Selector for $V_{OUT}$ = 3.3 V**

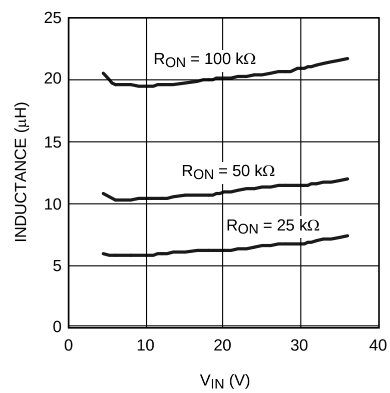



**Figure 23. Inductor Selector for $V_{OUT}$ = 0.8 V**

#### *8.1.1.4 $C_{VCC}$*

The capacitor on the $V_{CC}$ output provides not only noise filtering and stability, but also prevents false triggering of the $V_{CC}$ UVLO at the buck switch on/off transitions. For this reason, $C_{VCC}$ should be no smaller than 680 nF for stability, and should be a good quality, low ESR, ceramic capacitor.

#### *8.1.1.5 $C_O$ and $C_{O3}$*

$C_O$ should generally be no smaller than 10 µF. Experimentation is usually necessary to determine the minimum value for $C_O$, as the nature of the load may require a larger value. A load which creates significant transients requires a larger value for $C_O$ than a fixed load.

$C_{O3}$ is a small value ceramic capacitor to further suppress high frequency noise at $V_{OUT}$. A 47 nF is recommended, located close to the LM3100.

#### *8.1.1.6 $C_{IN}$ and $C_{IN3}$*

$C_{IN}$'s purpose is to supply most of the switch current during the on-time, and limit the voltage ripple at $V_{IN}$, assume the voltage source feeding $V_{IN}$ has an output impedance greater than zero. If the source's dynamic impedance is high (effectively a current source), $C_{IN}$ supplies the average input current, but not the ripple current.

At maximum load current, when the buck switch turns on, the current into $V_{IN}$ suddenly increases to the lower peak of the inductor's ripple current, ramps up to the peak value, then drop to zero at turn-off. The average current during the on-time is the load current. For a worst case calculation, $C_{IN}$ must supply this average load current during the maximum on-time. $C_{IN}$ is calculated from:

## Applications Information (continued)

$$C_{IN} = \frac{I_{OUT} \times t_{ON}}{\Delta V} \quad (12)$$

where $I_{OUT}$ is the load current, $t_{ON}$ is the maximum on-time, and ΔV is the allowable ripple voltage at $V_{IN}$.

$C_{IN3}$'s purpose is to help avoid transients and ringing due to long lead inductance at $V_{IN}$. A low ESR, 0.1 µF ceramic chip capacitor is recommended, located close to the LM3100.

#### *8.1.1.7 $C_{BST}$*

The recommended value for $C_{BST}$ is 33 nF. A high quality ceramic capacitor with low ESR is recommended as $C_{BST}$ supplies a surge current to charge the buck switch gate at turn-on. A low ESR also helps ensure a complete recharge during each off-time.

#### *8.1.1.8 $C_{SS}$*

The capacitor at the SS pin determines the soft-start time, i.e. the time for the reference voltage at the regulation comparator, and the output voltage, to reach their final value. The time is determined from the following:

$$t_{SS} = \frac{C_{SS} \times 0.8V}{8\ \mu A} \quad (13)$$

#### *8.1.1.9 $C_{FB}$*

If output voltage is higher than 1.6 V, this feedback capacitor is needed for Discontinuous Conduction Mode to improve the output ripple performance, the recommended value for $C_{FB}$ is 10 nF.

## 8.2 Typical Application

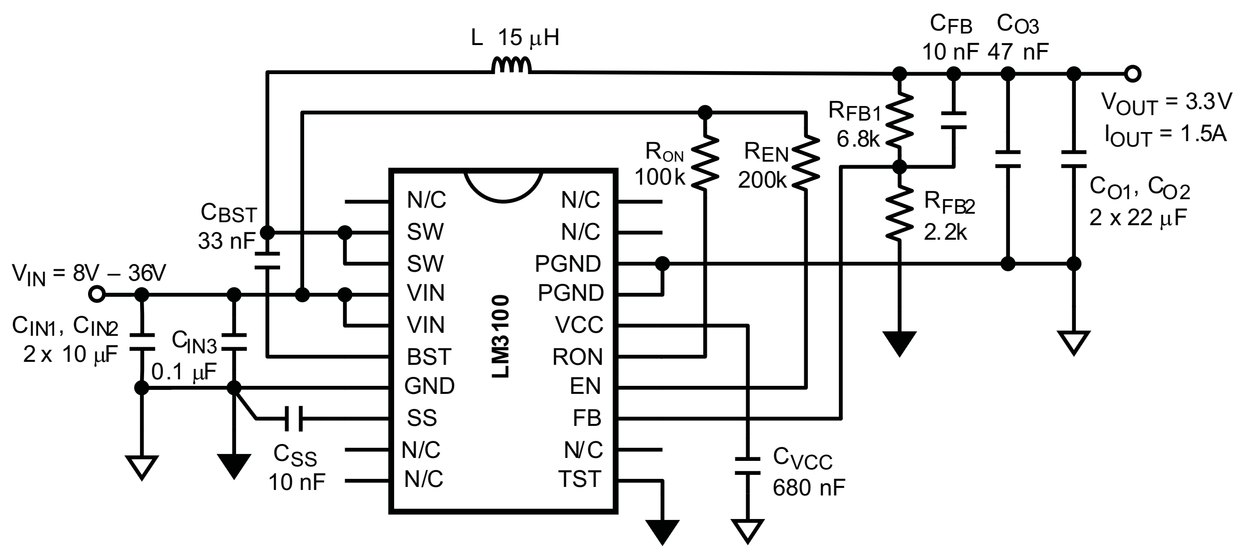



**Figure 24. Typical Application Schematic for $V_{OUT}$ = 3.3 V**

## Typical Application (continued)

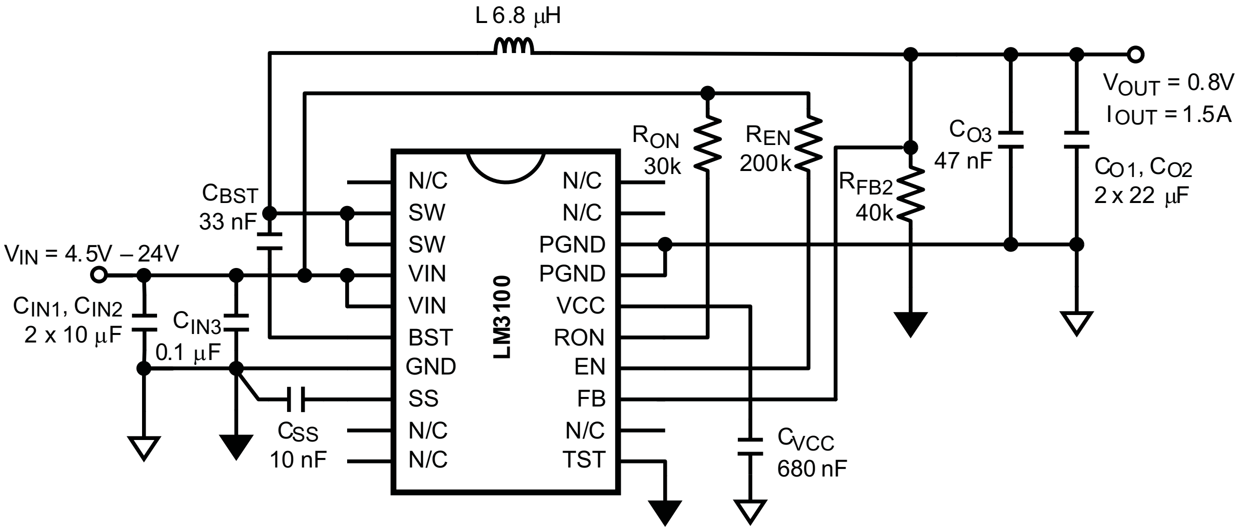



**Figure 25. Typical Application Schematic for $V_{OUT}$ = 0.8 V**

# 9 Layout

## 9.1 Layout Guidelines

### 9.1.1 PC Board Layout

The LM3100 regulation, over-voltage, and current limit comparators are very fast, and will respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible, and all external components must be as close as possible to their associated pins. Refer to the functional block diagram, the loop formed by $C_{IN}$, the high and low-side switches internal to the IC, and the PGND pin should be as small as possible. The PGND connection to Cin should be as short and direct as possible. There should be several vias connecting the Cin ground terminal to the ground plane placed as close to the capacitor as possible. The boost capacitor should be connected as close to the SW and BST pins as possible. The feedback divider resistors and the $C_{FB}$ capacitor should be located close to the FB pin. A long trace run from the top of the divider to the output is generally acceptable since this is a low impedance node. Ground the bottom of the divider directly to the GND (pin 7). The output capacitor, $C_{OUT}$, should be connected close to the load and tied directly into the ground plane. The inductor should connect close to the SW pin with as short a trace as possible to help reduce the potential for EMI (electro-magnetic interference) generation.

If it is expected that the internal dissipation of the LM3100 will produce excessive junction temperatures during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the IC package can be soldered to a ground plane and that plane should extend out from beneath the IC to help dissipate the heat. The exposed pad is internally connected to the IC substrate. Additionally the use of thick copper traces, where possible, can help conduct heat away from the IC. Using numerous vias to connect the die attach pad to an internal ground plane is a good practice. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

# 10 デバイスおよびドキュメントのサポート

## 10.1 ドキュメントの更新通知を受け取る方法

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## 10.2 コミュニティ・リソース

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## 10.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

# 11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3100MH/NOPB | ACTIVE | HTSSOP | PWP | 20 | 73 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LM3100<br>MH | Samples |
| LM3100MHX/NOPB | ACTIVE | HTSSOP | PWP | 20 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LM3100<br>MH | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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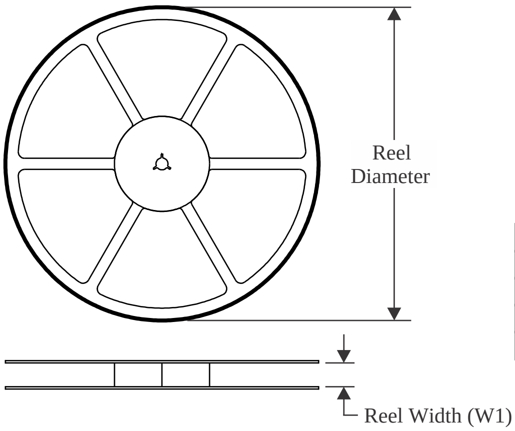
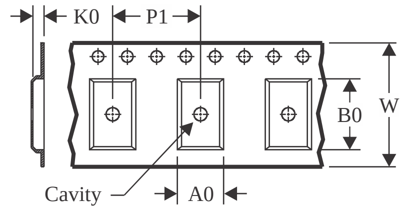
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

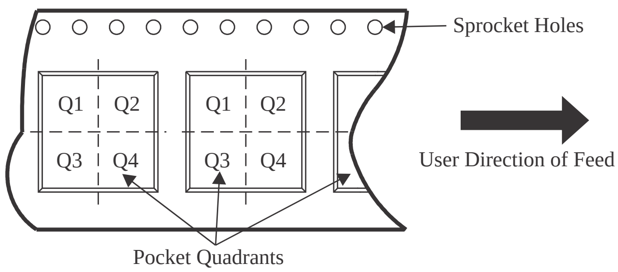



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

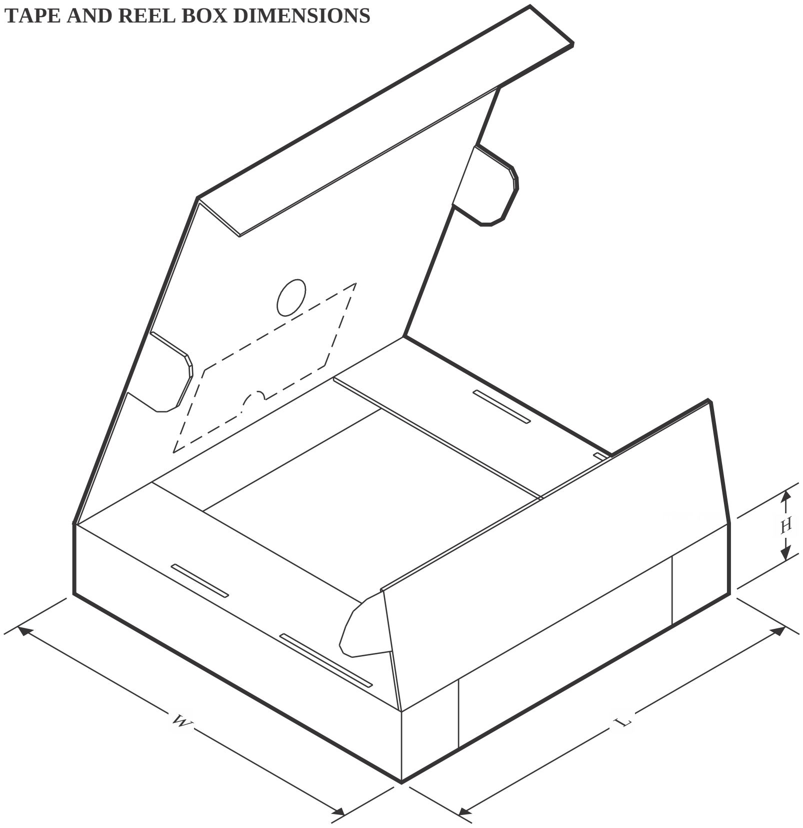
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3100MHX/NOPB | HTSSOP | PWP | 20 | 2500 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

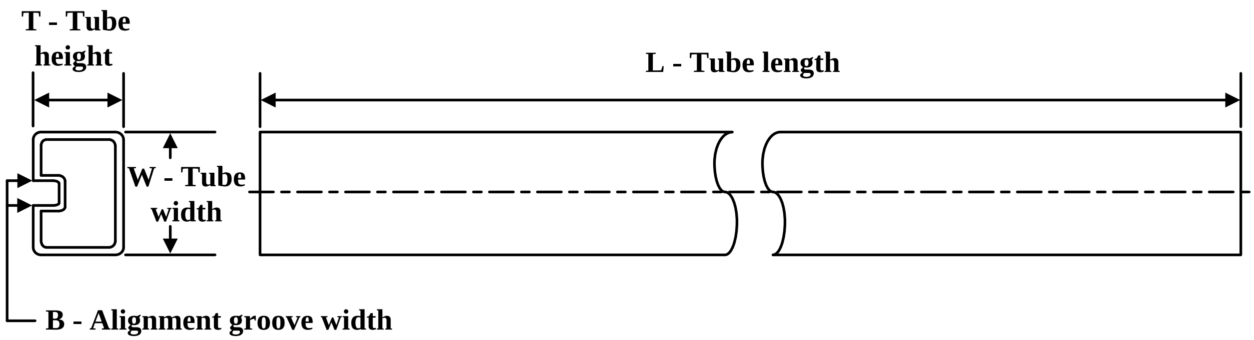
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM3100MHX/NOPB | HTSSOP | PWP | 20 | 2500 | 367.0 | 367.0 | 35.0 |

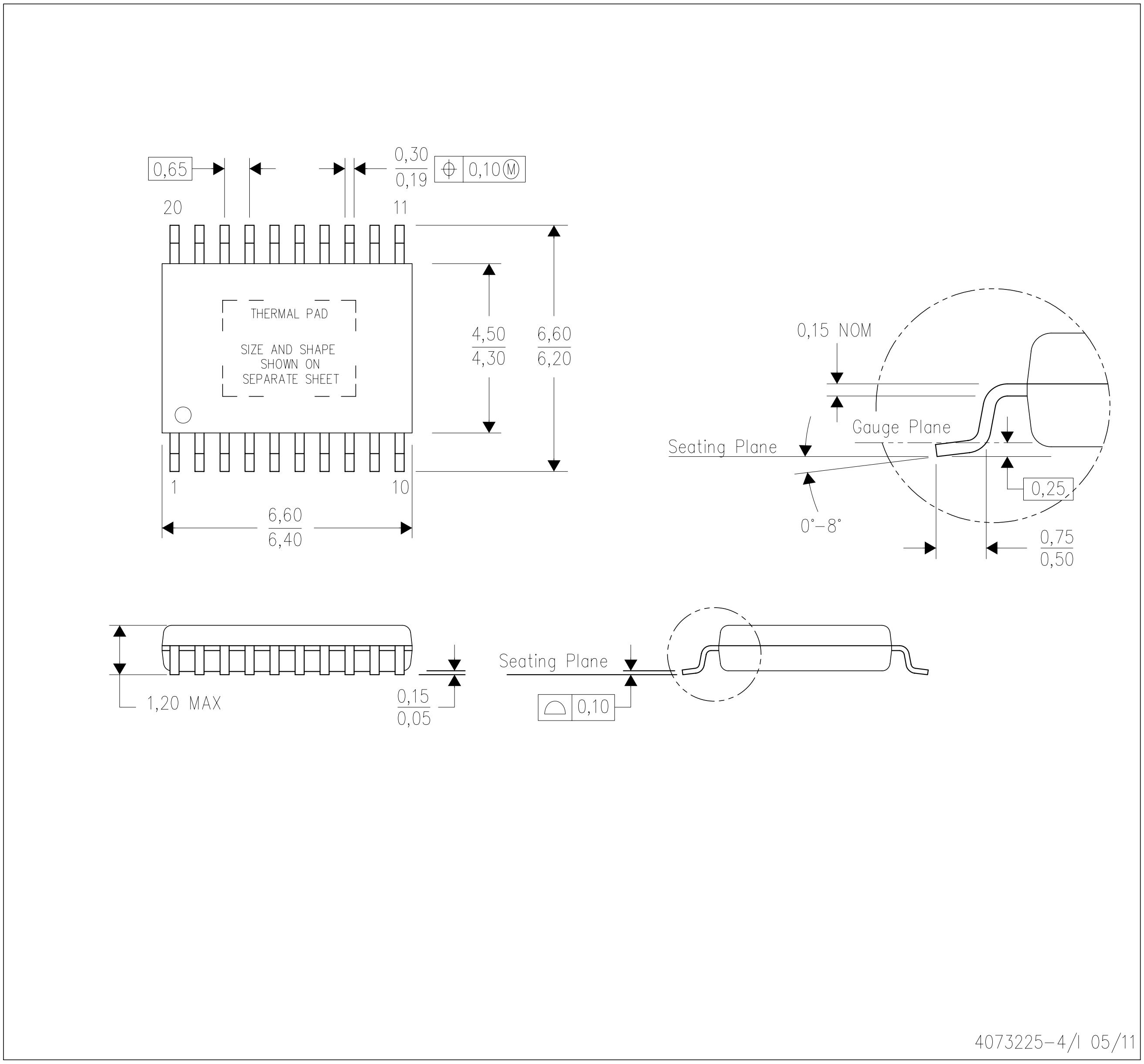
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM3100MH/NOPB | PWP | HTSSOP | 20 | 73 | 495 | 8 | 2514.6 | 4.06 |

PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

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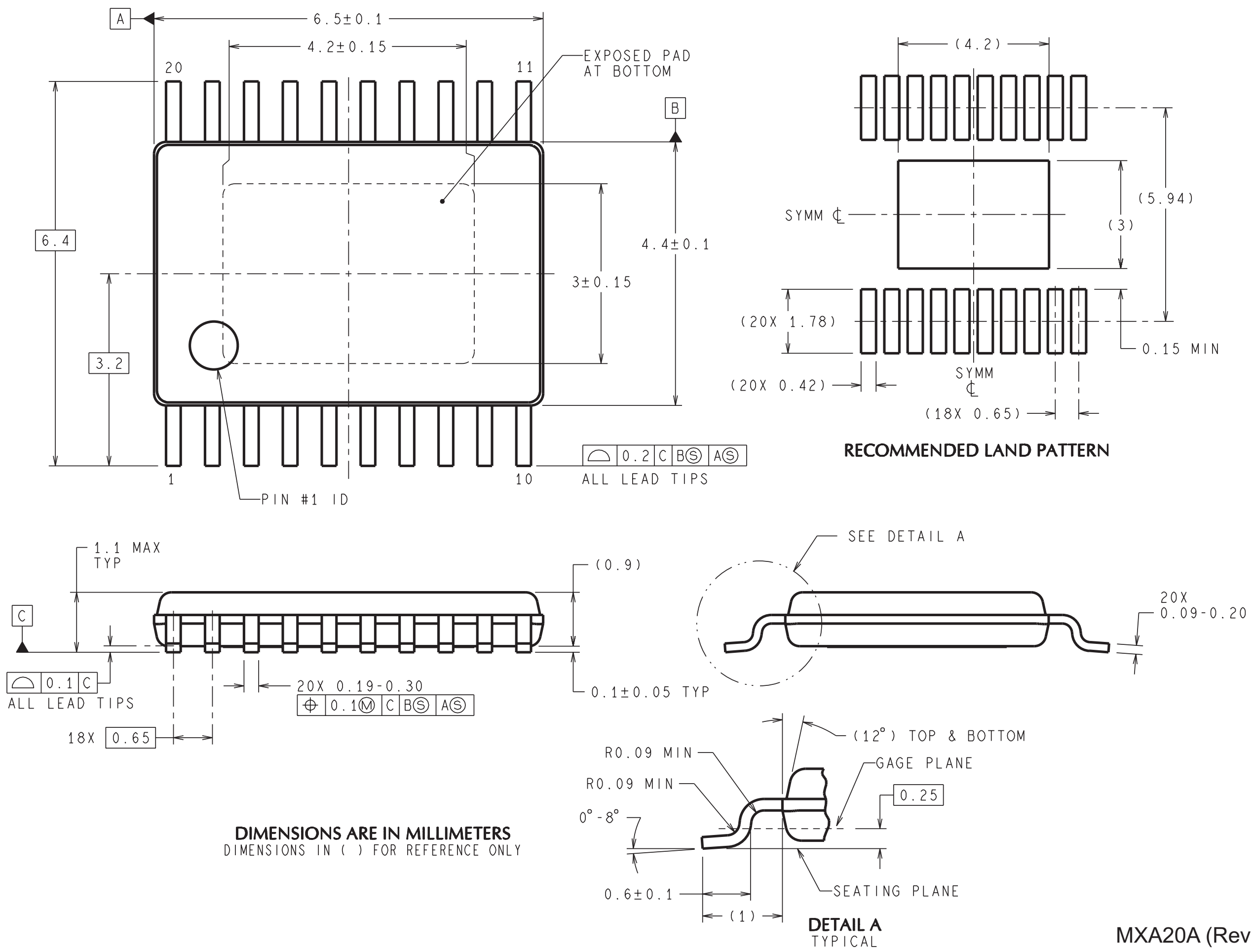
# PWP0020A




MXA20A (Rev C)

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265