LM5102、高電圧ハーフブリッジ・ゲート・ドライバ、プログラマブル遅延付き

1 特長

- ハイサイドとローサイド両方のNチャネルMOSFETを駆動
- ハイサイドとローサイドの立ち上がりエッジ遅延時間を独立してプログラミング可能
- ブートストラップ電源電圧範囲：最大118V DC
- 高速ターンオフ伝搬遅延（標準25ns）
- 15nsの立ち上がり/立ち下がり時間で1000pFの負荷を駆動
- 電源レールの低電圧誤動作防止
- 低消費電力
- シーケンスの途中でタイマを終了可能

2 アプリケーション

- 電流供給プッシュプル・パワー・コンバータ
- ハーフ/フルブリッジのパワー・コンバータ
- 同期降圧コンバータ
- 2スイッチのフォワード・パワー・コンバータ
- アクティブ・クランプ型フォワード・コンバータ

3 概要

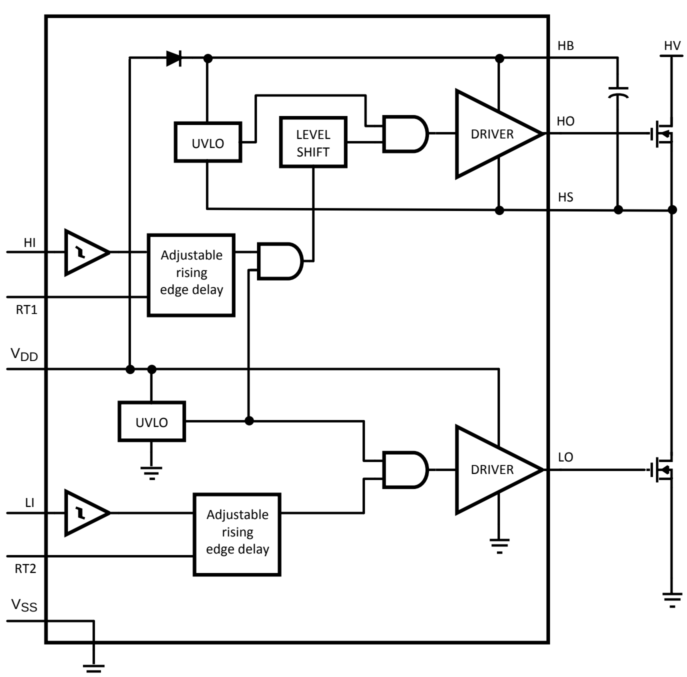
LM5102は、同期降圧型またはハーフブリッジの構成においてハイサイドとローサイド両方のNチャネルMOSFETを駆動するよう設計された、高電圧ゲート・ドライバです。フローティング・ハイサイド・ドライバは、最大100Vの電源電圧で動作できます。各出力は、それぞれ独立に制御されます。プログラミング抵抗を使用して、各出力の立ち上がりエッジを独立して遅延させることができます。ハイサイド・ゲート・ドライバのブートストラップ・コンデンサの充電用に高電圧ダイオードを内蔵しています。堅牢なレベル・シフタにより、消費電力を抑えながら高速で動作し、制御ロジックからハイサイド・ゲート・ドライバへのクリーンなレベル遷移を実現します。ローサイドとハイサイド両方の電源レールに低電圧誤動作防止機能が搭載されています。デバイスは標準のVSSOP 10ピンおよびWSON 10ピン・パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM5102	VSSOP (10)	3.00mm×3.00mm
	WSON (10)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

ブロック概略図



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4 改訂履歴

Revision から変更 A (March 2013) to Revision B — **Page**

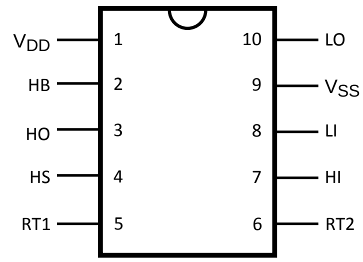
- 「取り扱い定格」の表、「機能説明」、「デバイスの機能モード」、「アプリケーションと実装」、「電源に関する推奨事項」、「レイアウト」、「デバイスとドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」を追加 ... 1

2013年3月発行のものから更新 — **Page**

- Changed layout of National Data Sheet to TI format ... 11

5 Pin Configuration and Functions

**10 Pin
VSSOP (DGS), WSON (DPR)
Top View**



Pin Functions

PIN		TYPE(1)	DESCRIPTION	APPLICATION INFORMATION
NAME	WSON(2), VSSOP			
HB	2	P	High-side gate driver bootstrap rail	Connect the positive terminal of bootstrap capacitor to the HB pin and connect negative terminal of bootstrap capacitor to HS. The Bootstrap capacitor should be placed as close to IC as possible.
HI	7	I	High-side driver control input	TTL compatible thresholds. Unused inputs should be tied to ground and not left open.
HO	3	O	High-side gate driver output	Connect to gate of high-side MOSFET with short low-inductance path.
HS	4	P	High-side MOSFET source connection	Connect bootstrap capacitor negative terminal and source of high side MOSFET.
LI	8	I	Low-side driver control input	TTL compatible thresholds. Unused inputs should be tied to ground and not left open.
LO	10	O	Low-side gate driver output	Connect to the gate of the low side MOSFET with a short low inductance path.
RT1	5	A	High-side output edge delay programming	Resistor from RT1 to ground programs the leading edge delay of the high side gate driver. The resistor should be placed close to the IC to minimize noise coupling from adjacent traces.
RT2	6	A	Low-side output edge delay programming	Resistor from RT2 to ground programs the leading edge delay of the low side gate driver. The resistor should be placed close to the IC to minimize noise coupling from adjacent traces.
V_{DD}	1	P	Positive gate drive supply	Locally decouple to VSS using low ESR/ESL capacitor, located as close to IC as possible.
V_{SS}	9	G	Ground return	All signals are referenced to this ground.

(1) P = Power, G = Ground, I = Input, O = Output, A = Analog
(2) For the WSON package, it is recommended that the exposed pad on the bottom of the LM5100 and LM5101 be soldered to ground plane on the PC board, and the ground plane should extend out from beneath the IC to help dissipate the heat.

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

	MIN	MAX	UNIT
V_{DD} to V_{SS}	–0.3	18	V
V_{HB} to V_{HS}	–0.3	18	V
LI or HI Inputs to V_{SS}	–0.3	V_{DD} + 0.3	V
LO Output	–0.3	V_{DD} + 0.3	V
HO Output	V_{HS} – 0.3	V_{HB} + 0.3	V
V_{HS} to V_{SS}	–1	100	V
V_{HB} to V_{SS}		118	V
RT1 and RT2 to V_{SS}	–0.3	5	V
Junction Temperature		150	°C
Storage Temperature Range	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V_{DD}	9	14	V
HS	–1	100	V
HB	V_{HS} + 8	V_{HS} + 14	V
HS Slew Rate		< 50	V/ns
Junction Temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM5102 DGS	LM5102 DPR[2]	UNIT
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.3	37.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.9	38.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.4	14.9	
Ψ_{JT}	Junction-to-top characterization parameter	6.2	0.4	
Ψ_{JB}	Junction-to-board characterization parameter	83.6	15.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	4.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).
(2) 4 layer board with Cu finished thickness 1.5 oz, 1 oz, 1 oz, 1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50 mm ground and power planes embedded in PCB. See Application Note *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

6.5 Electrical Characteristics

Specifications in standard typeface are for T_J = +25°C. Unless otherwise specified, V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0V, RT1 = RT2 = 100 kΩ. No load on LO or HO.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
SUPPLY CURRENTS						
I_{DD}	V_{DD} Quiescent Current	LI = HI = 0 V		0.4		mA
		LI = HI = 0 V, –40°C to +125°C			0.6	
I_{DDO}	V_{DD} Operating Current	f = 500 kHz		1.5		mA
		f = 500 kHz, –40°C to +125°C			3	
I_{HB}	Total HB Quiescent Current	LI = HI = 0 V		0.06		mA
		LI = HI = 0 V, –40°C to +125°C			0.2	
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.3		mA
		f = 500 kHz, –40°C to +125°C			3	
I_{HBS}	HB to V_{SS} Current, Quiescent	V_{HS} = V_{HB} = 100 V		0.05		µA
		V_{HS} = V_{HB} = 100 V, –40°C to +125°C			10	
I_{HBSO}	HB to V_{SS} Current, Operating	f = 500 kHz		0.08		mA
INPUT PINS						
V_{IL}	Low Level Input Voltage Threshold			1.8		V
		–40°C to +125°C	0.8			
V_{IH}	High Level Input Voltage Threshold			1.8		V
		–40°C to +125°C			2.2	
R_I	Input Pulldown Resistance			200		kΩ
		–40°C to +125°C	100		500	
TIME DELAY CONTROLS						
V_{RT}	Nominal Voltage at RT1, RT2			3		V
		–40°C to +125°C	2.7		3.3	
I_{RT}	RT Pin Current Limit	RT1 = RT2 = 0 V		1.5		mA
		RT1 = RT2 = 0 V, –40°C to +125°C	0.75		2.25	
V_{th}	Timer Termination Threshold			1.8		V
T_{DL1}, T_{DH1}	Rising edge turn-on delay, RT = 10 kΩ			105		ns
		–40°C to +125°C	75		150	
T_{DL2}, T_{DH2}	Rising edge turn-on delay, RT = 100 kΩ			630		ns
		–40°C to +125°C	530		750	
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} Rising Threshold			6.9		V
		–40°C to +125°C	6.0		7.4	
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold			6.6		V
		–40°C to +125°C	5.7		7.1	
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOTSTRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.60		V
		I_{VDD-HB} = 100 µA, –40°C to +125°C			0.9	
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.85		V
		I_{VDD-HB} = 100 mA, –40°C to +125°C			1.1	
R_D	Dynamic Resistance	I_{VDD-HB} = 100 mA		0.8		Ω
		I_{VDD-HB} = 100 mA, –40°C to +125°C			1.5	

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Specifications in standard typeface are for T_J = +25°C. Unless otherwise specified, V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0V, RT1 = RT2 = 100 kΩ. No load on LO or HO.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
LO GATE DRIVER						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 100 mA		0.25		V
		I_{LO} = 100 mA, –40°C to +125°C			0.4	
V_{OHL}	High-Level Output Voltage	I_{LO} = –100 mA, V_{OHL} = V_{DD} – V_{LO}		0.35		V
		I_{LO} = –100 mA, V_{OHL} = V_{DD} – V_{LO}, –40°C to +125°C			0.55	
I_{OHL}	Peak Pullup Current	V_{LO} = 0 V		1.6		A
I_{OLL}	Peak Pulldown Current	V_{LO} = 12 V		1.8		A
HO GATE DRIVER						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 100 mA		0.25		V
		I_{HO} = 100 mA, –40°C to +125°C			0.4	
V_{OHH}	High-Level Output Voltage	I_{HO} = –100 mA, V_{OHH} = V_{HB} – V_{HO}		0.35		V
		I_{HO} = –100 mA, V_{OHH} = V_{HB} – V_{HO}, –40°C to +125°C			0.55	
I_{OHH}	Peak Pullup Current	V_{HO} = 0 V		1.6		A
I_{OLH}	Peak Pulldown Current	V_{HO} = 12 V		1.8		A

6.6 Switching Characteristics

Specifications in standard typeface are for T_J = +25°C. Unless otherwise specified, V_{DD} = V_{HB} = 12 V, V_{SS} = V_{HS} = 0 V, No Load on LO or HO.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
t_{LPHL}	Lower Turn-Off Propagation Delay LM5102 (LI Falling to LO Falling)			27		ns
		–40°C to +125°C			56	
t_{HPHL}	Upper Turn-Off Propagation Delay LM5102 (HI Falling to HO Falling)			27		ns
		–40°C to +125°C			56	
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		15		ns
t_R, t_F	Either Output Rise/Fall Time (3 V to 9 V)	C_L = 0.1 µF		0.6		µs
t_{BS}	Bootstrap Diode Turn-Off Time	I_F = 20 mA, I_R = 200 mA		50		ns

(1) MIN and MAX limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI’s Average Outgoing Quality Level (AOQL).

6.7 Typical Characteristics

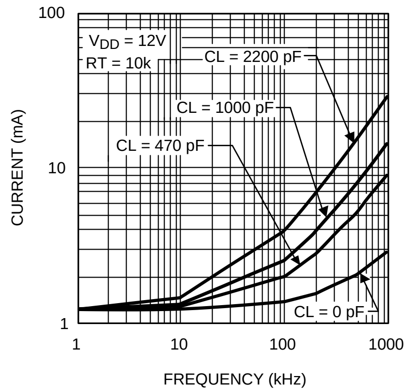


Figure 1. I_{DD} vs Frequency

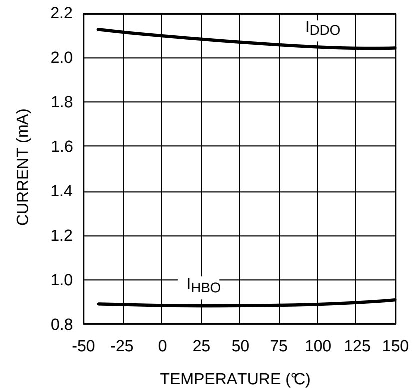


Figure 2. Operating Current vs Temperature

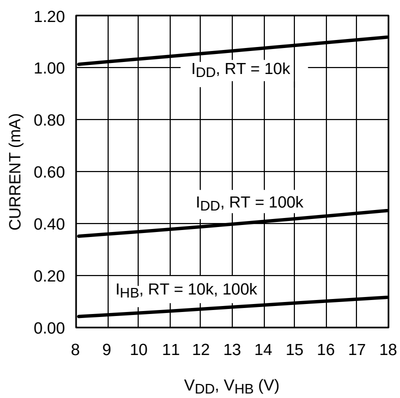


Figure 3. Quiescent Current vs Supply Voltage

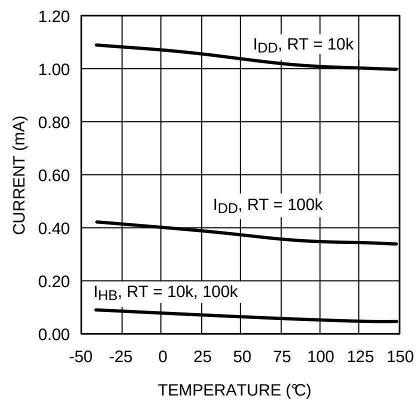


Figure 4. Quiescent Current vs Temperature

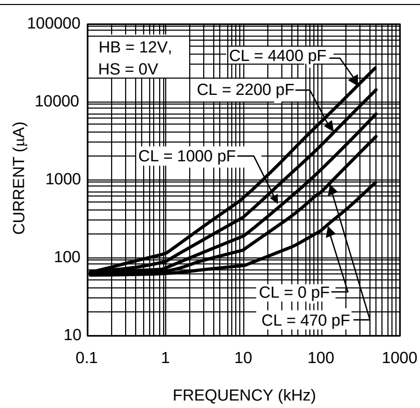


Figure 5. I_{HB} vs Frequency

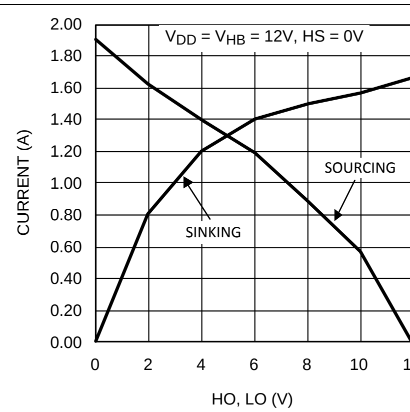


Figure 6. HO and LO Peak Output Current vs Output Voltage

Typical Characteristics (continued)

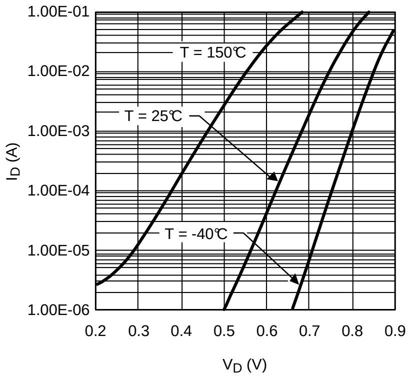


Figure 7. Diode Forward Voltage

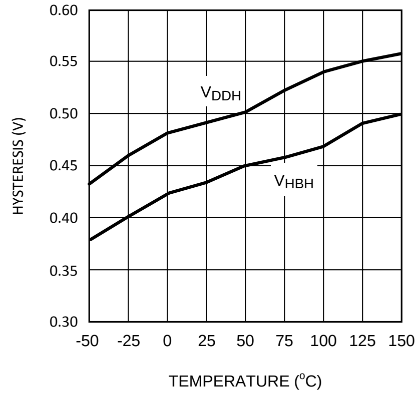


Figure 8. Undervoltage Threshold Hysteresis vs Temperature

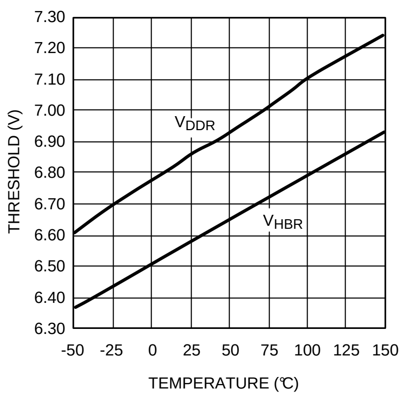


Figure 9. Undervoltage Rising Threshold vs Temperature

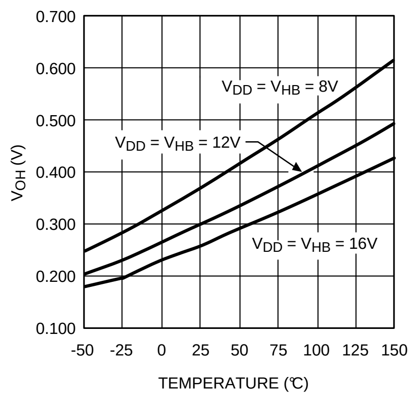


Figure 10. LO and HO Gate Drive — High Level Output Voltage vs Temperature

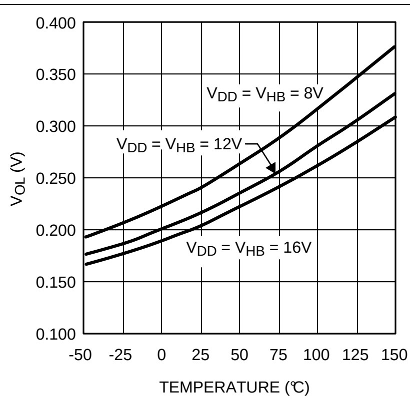


Figure 11. LO and HO Gate Drive — Low Level Output Voltage vs Temperature

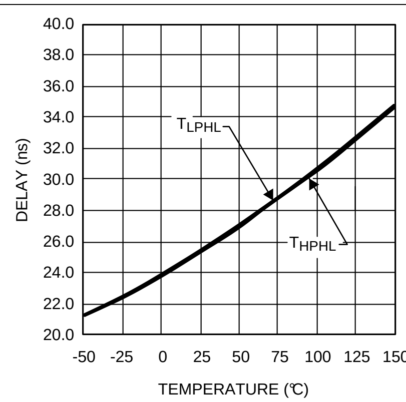


Figure 12. Turn Off Propagation Delay vs Temperature

Typical Characteristics (continued)

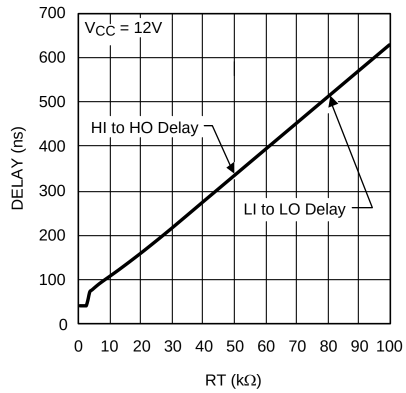


Figure 13. Turn On Delay vs RT Resistor Value

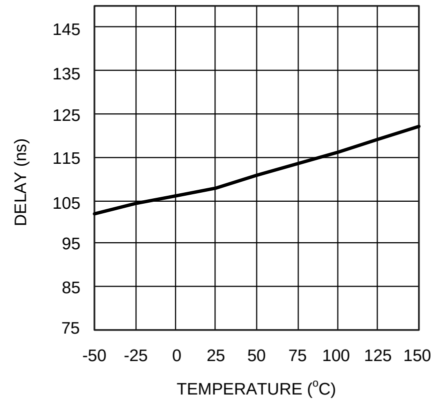


Figure 14. Turn On Delay vs Temperature (RT = 10 k)

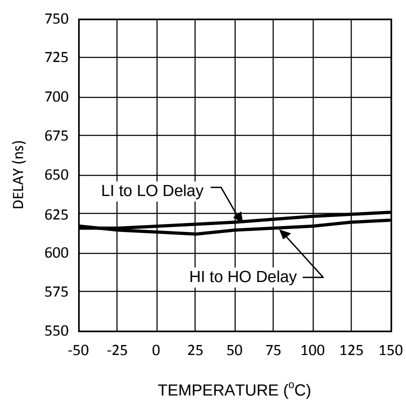


Figure 15. Turn On Delay vs Temperature (RT = 100 k)

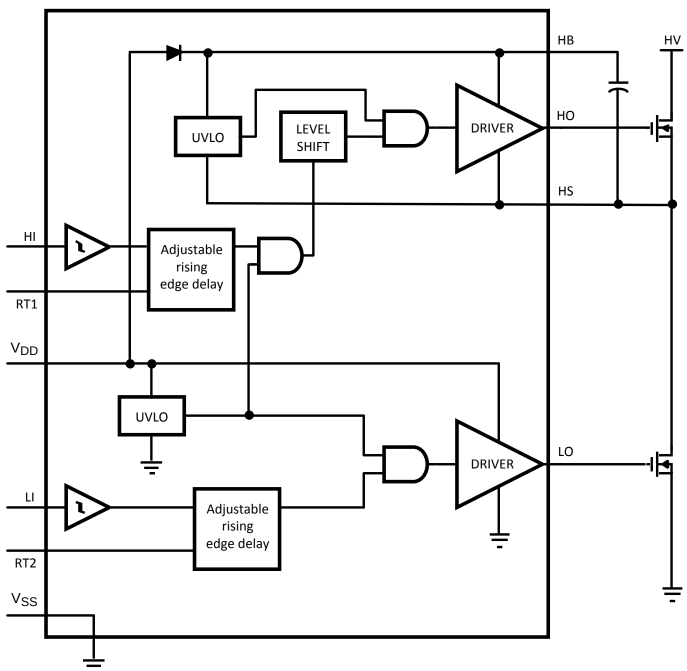
7 Detailed Description

7.1 Overview

The LM5102 device offers a unique flexibility with independently programmable delay of the rising edge for both high and low side driver outputs independently. The delays are set with resistors at the RT1 and RT2 pins, and can be adjusted from 100 ns to 600 ns. This feature reduces component count, board space and cost compared to discrete solutions for adjusting driver dead time. The wide delay programming range provides the flexibility to optimize drive signal timing for a wide range of MOSFETs and applications.

The RT pins are biased at 3 V and current limited to 1 mA maximum programming current. The time delay generator will accommodate resistor values from 5 k to 100 k with turn-on delay times that are proportional to the RT resistance. In addition, each RT pin is monitored by a comparator that will bypass the turn-on delay if the RT pin is pulled below the timer elimination threshold (1.8 V typical). Grounding the RT pins programs the LM5102 to drive both outputs with minimum turn-on delay.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Startup and UVLO

Both top and bottom drivers include undervoltage lockout (UVLO) protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (V_{HB} – V_{HS}) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn-on the external MOSFETs, and the built-in hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to V_{DD} pin of LM5102, the top and bottom gates are held low until V_{DD} exceeds UVLO threshold, typically about 6.9 V. Any UVLO condition on the bootstrap capacitor will disable only the high side output (HO).

7.4 Device Functional Modes

LI Pin	LO Pin	HI Pin	HO Pin
L	L	L	L
H	H	H	H

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5102 is one of the latest generation of high voltage gate drivers which are designed to drive both the high-side and low-side N-Channel MOSFETs in a half-bridge/full bridge configuration or in a synchronous buck circuit. The floating high side driver is capable of operating with supply voltages up to 100 V. This allows for N-Channel MOSFET control in half-bridge, full-bridge, push-pull, two switch forward and active clamp topologies.

In the LM5102 the outputs are independently controlled. The rising edge of each output can be independently delayed with a programming resistor.

Table 1. LM5102 Highlights

FEATURE	BENEFIT
Independently programmable high and low side delay	Allows optimisation of gate drive timings to account for device differences between high-side and low-side positions
Low power consumption	Improves light load efficiency figures
Internal bootstrap diode	Reduces parts count and PCB real estate

8.2 Typical Application

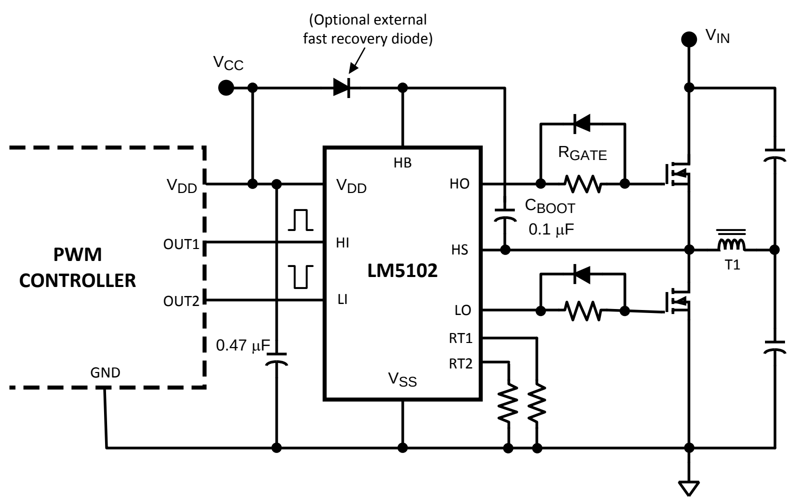


Figure 16. LM5102 Driving MOSFETS Connected in Half-Bridge Configuration

Typical Application (continued)

8.2.1 Design Requirements

PARAMETERS	VALUES
Gate Drive IC	LM5102
Mosfet	CSD18531Q5A
V_{DD}	10 V
Q_{gmax}	43 nC
F_{sw}	100 kHz
D_{Max}	95%
I_{HBO}	10 µA
V_{DH}	1.1 V
V_{HBR}	7.1 V
V_{HBH}	0.4 V

8.2.2 Detailed Design Procedure

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL}$$

where

- V_{DD} = Supply voltage of the gate drive IC
- V_{DH} = Bootstrap diode forward voltage drop
- V_{gsmin} = Minimum gate source threshold voltage (1)

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{HB}} \quad (2)$$

$$Q_{TOTAL} = Q_{gmax} + I_{HBO} \times \frac{D_{Max}}{F_{SW}} \quad (3)$$

The quiescent current of the bootstrap circuit is 10 µA which is negligible compared to the Qgs of the mosfet.

$$Q_{TOTAL} = 43nC + 10\mu A \times \frac{0.95}{100kHz} \quad (4)$$

$$Q_{TOTAL} = 43.01\ nC \quad (5)$$

In practice the value for the C_{BOOT} capacitor should be greater than that calculated to allow for situations where the power stage may skip pulse due to load transients. In this circumstance the boot capacitor must maintain the HB Pin voltage above the UVLO Voltage for the HB circuit.

As a general rule the local V_{DD} bypass capacitor should be 10 times greater than the value of C_{BOOT}.

$$V_{HBL} = V_{HBR} - V_{HBH} \quad (6)$$

$$V_{HBL} = 6.7\ V \quad (7)$$

$$\Delta V_{HB} = 10\ V - 1.1\ V - 6.7\ V \quad (8)$$

$$\Delta V_{HB} = 2.2\ V \quad (9)$$

$$C_{BOOT} = \frac{43.01nc}{2.2V} \quad (10)$$

$$C_{BOOT} = 19.54\ nF \quad (11)$$

The bootstrap and bias capacitors should be ceramic types with X7R dielectric. The voltage rating should be twice that of the maximum VDD to allow for loss of capacitance once the devices have a dc bias voltage across them and to ensure long term reliability of the devices.

The resistor values, RT1 and RT2, for setting turn on delay can be found in Figure 18.

8.2.3 Application Curves

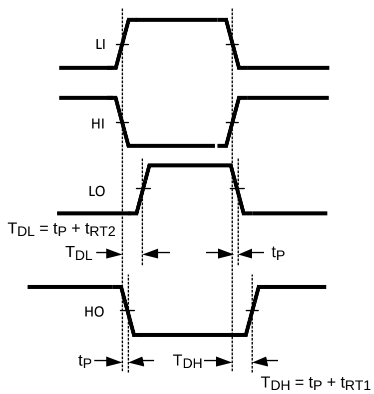


Figure 17. Application Timing Waveforms

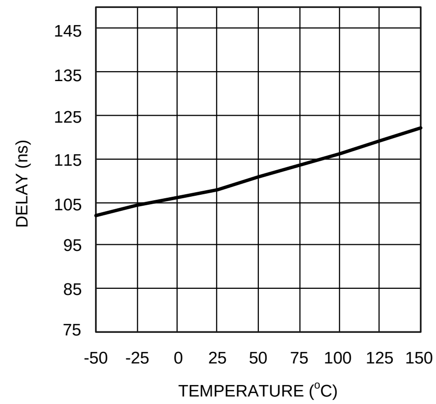


Figure 18. Turn On Delay vs Temperature (RT = 10 k)

9 Power Supply Recommendations

9.1 Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as shown in Equation 12.

$$P_{DGATES} = 2 \times f \times C_L \times V_{DD}^2 \quad (12)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

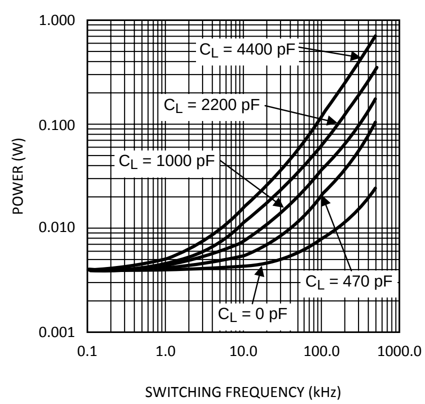


Figure 19. Gate Driver Power Dissipation (LO + HO) V_{CC} = 12 V, Neglecting Diode Losses

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Because each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. Figure 20 was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

Power Dissipation Considerations (continued)

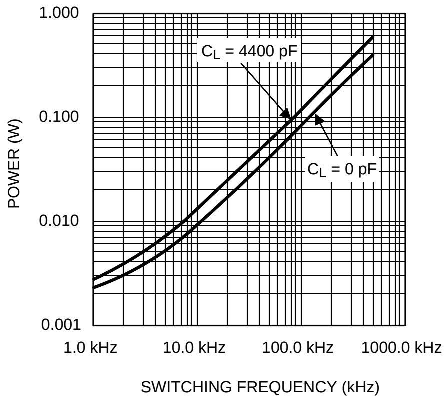


Figure 20. Diode Power Dissipation V_{IN} = 80 V

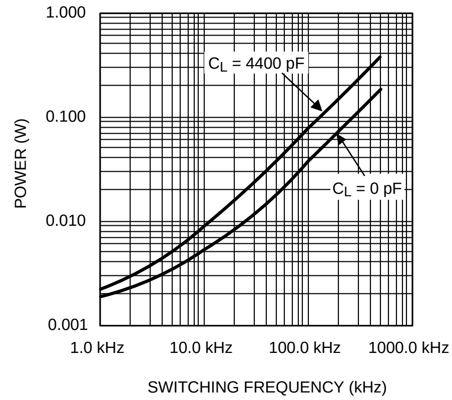


Figure 21. Diode Power Dissipation V_{IN} = 40 V

The total IC power dissipation can be estimated from the above plots by summing the gate drive losses with the bootstrap diode losses for the intended application. Because the diode losses can be significant, an external diode placed in parallel with the internal bootstrap diode (refer to Figure 16) and can be helpful in removing power from the IC. For this to be effective, the external diode must be placed close to the IC to minimize series inductance and have a significantly lower forward voltage drop than the internal diode.

10 Layout

10.1 Layout Guidelines

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR/ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from V_{DD} during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   – The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
   – The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistors on the RT1 and RT2 timer pins must be placed very close to the IC and seperated from high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

10.2 Layout Example

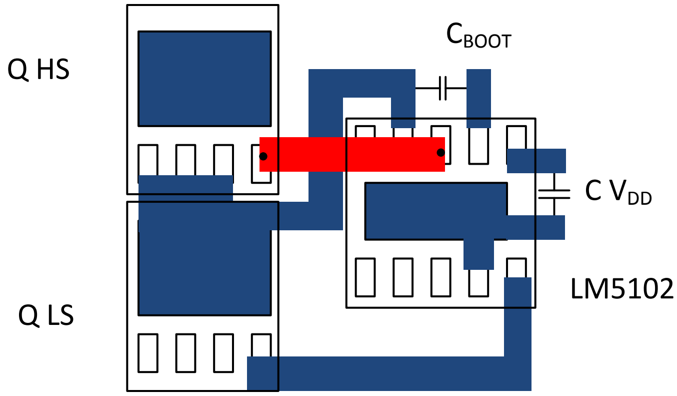


Figure 22. LM5102 Component Placement

11 デバイスおよびドキュメントのサポート

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11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5102MM/NOPB	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102
LM5102MM/NOPB.A	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102
LM5102MM/NOPB.B	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102
LM5102MMX/NOPB	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102
LM5102MMX/NOPB.A	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102
LM5102MMX/NOPB.B	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102
LM5102SD/NOPB	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102SD
LM5102SD/NOPB.A	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102SD
LM5102SD/NOPB.B	Active	Production	WSON (DPR) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102SD
LM5102SDX/NOPB	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102SD
LM5102SDX/NOPB.A	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102SD
LM5102SDX/NOPB.B	Active	Production	WSON (DPR) | 10	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5102SD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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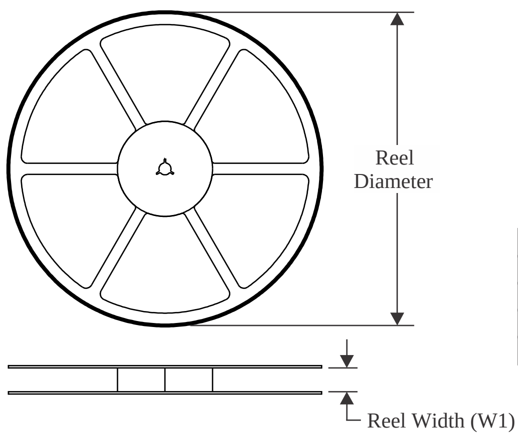
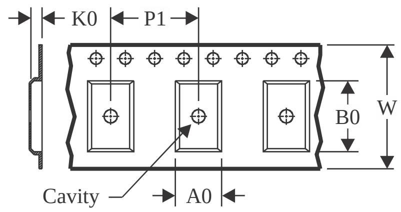
TAPE AND REEL INFORMATION

REEL DIMENSIONS

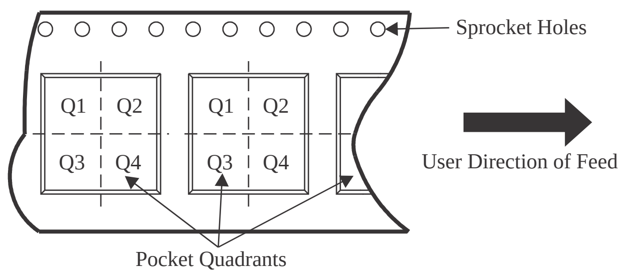


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

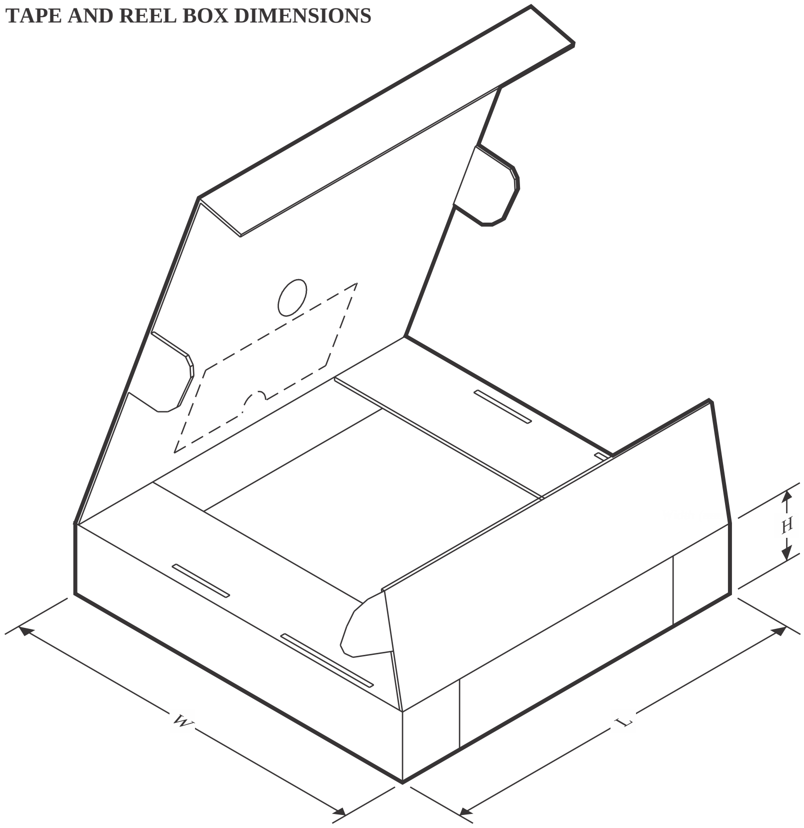
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

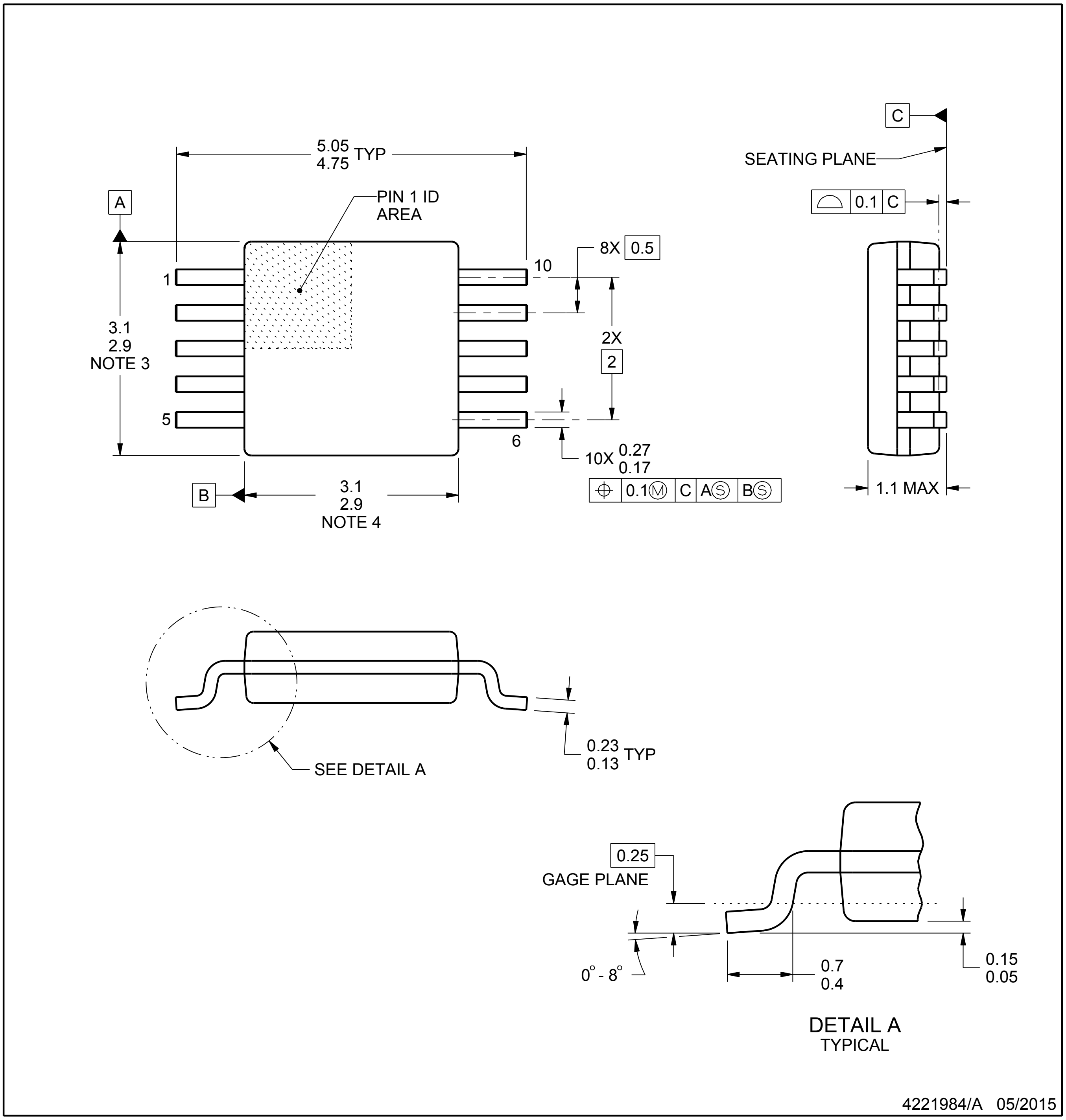
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5102MM/NOPB	VSSOP	DGS	10	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5102MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5102SD/NOPB	WSON	DPR	10	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5102SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



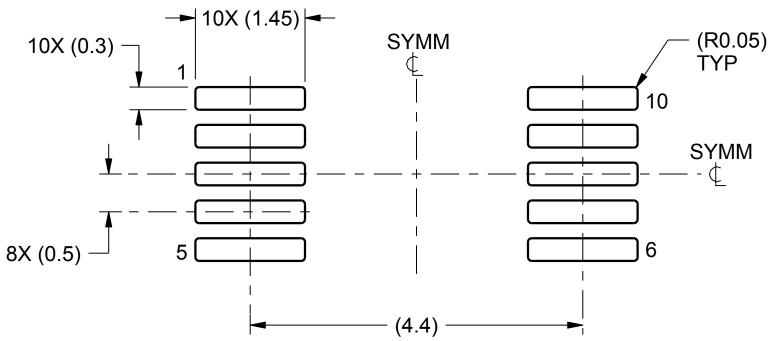
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5102MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5102MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5102SD/NOPB	WSON	DPR	10	1000	208.0	191.0	35.0
LM5102SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

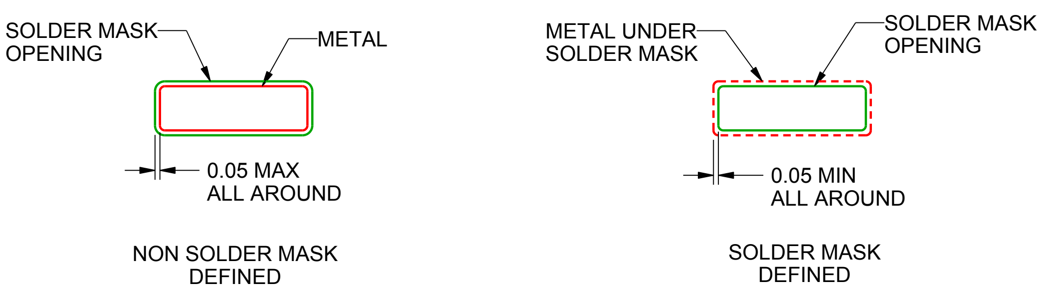


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

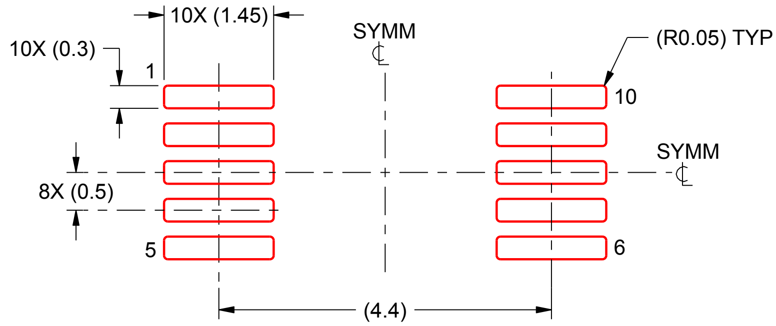


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

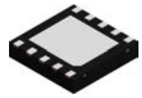


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

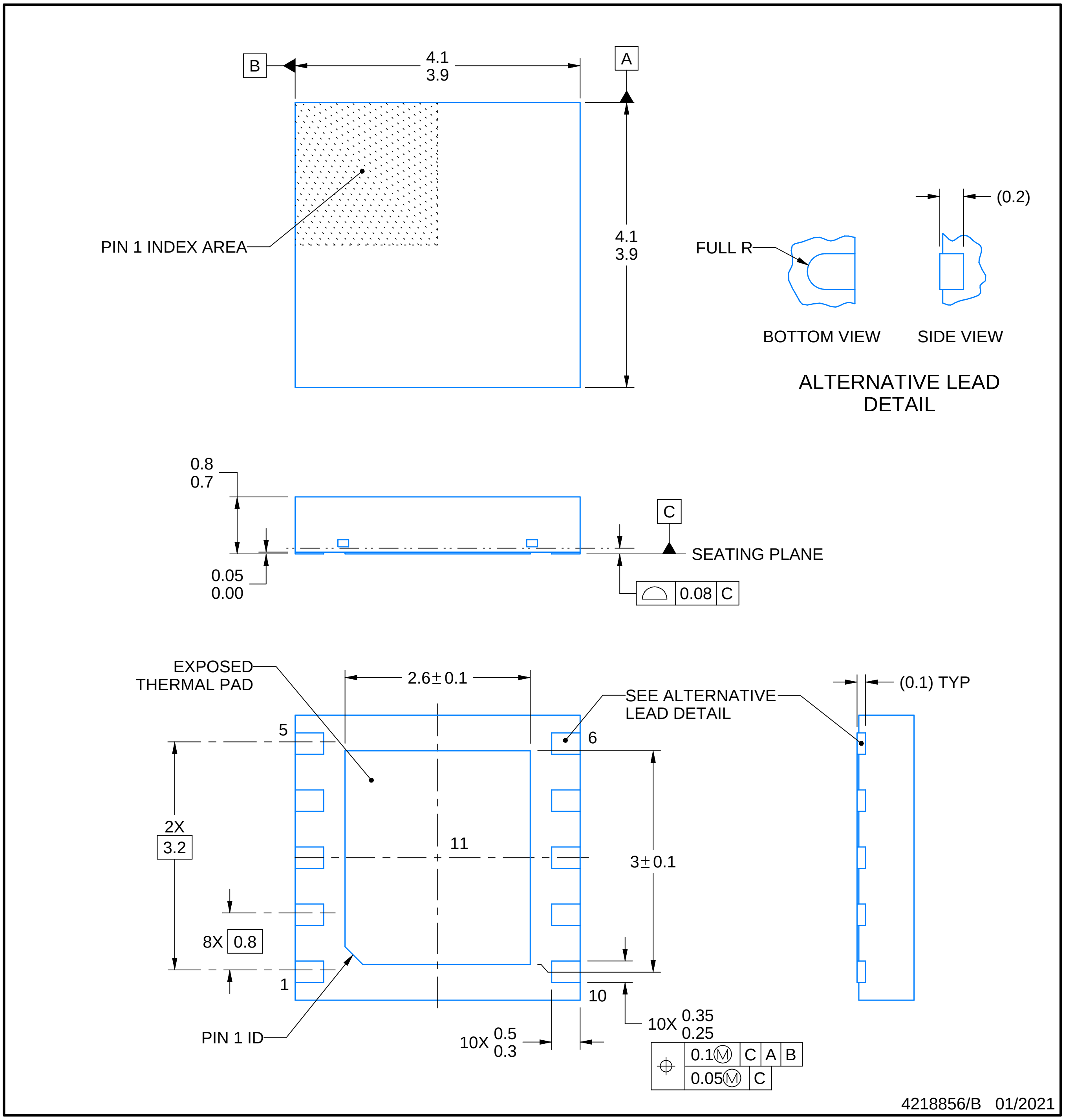


PACKAGE OUTLINE

DPR0010A

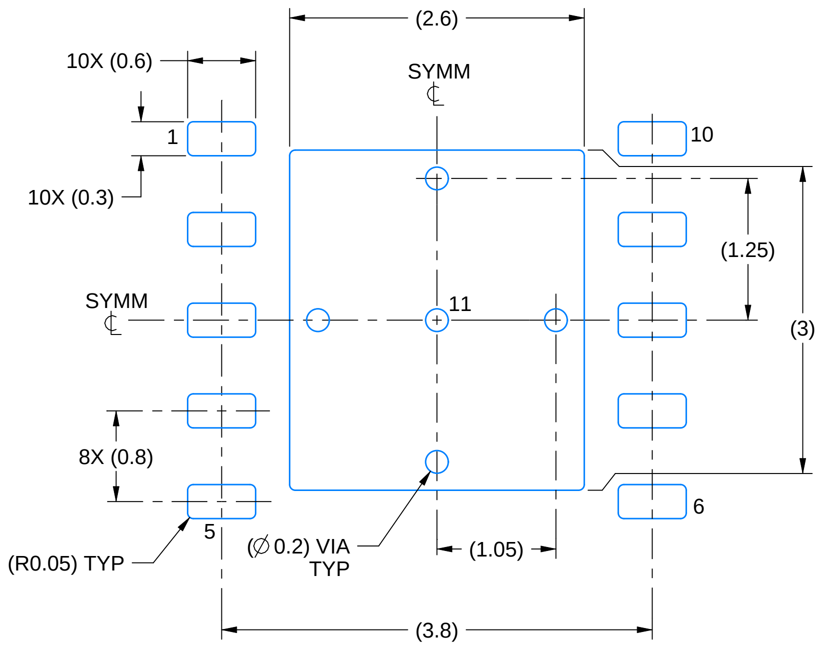
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

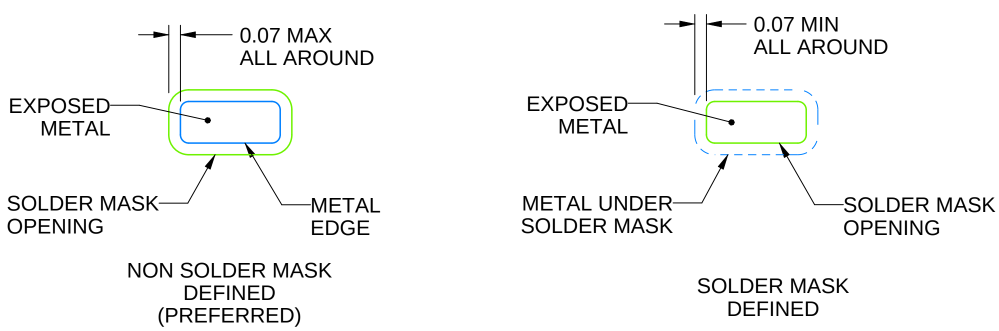


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

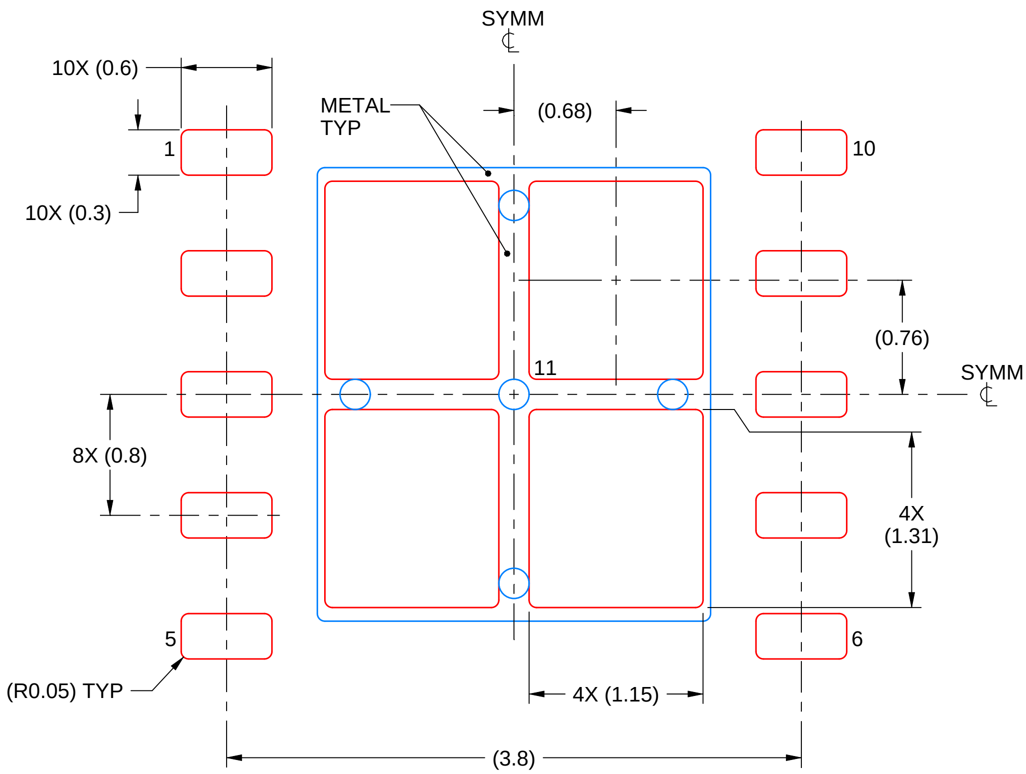


SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218856/B 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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