LM5109B、高電圧、1Aピーク、ハーフブリッジ・ゲート・ドライバ

1 特長

- ハイサイドとローサイド両方のNチャネルMOSFETを駆動
- ピーク出力電流：1A（シンク1.0Aおよびソース1.0A）
- TTLおよびCMOSに独立して互換性を持つ入力
- ブートストラップ電源電圧：108V DC
- 高速伝搬時間（標準30ns）
- 15nsの立ち上がり/立ち下がり時間で1000pFの負荷を駆動
- 優れた伝搬遅延マッチング（標準2ns）
- 電源レールの低電圧誤動作防止
- 低消費電力
- 8ピンSOICおよび熱特性強化型8ピンWSONパッケージ

2 アプリケーション

- 電流供給プッシュプル・コンバータ
- ハーフ/フルブリッジのパワー・コンバータ
- ソリッド・ステート・モーター・ドライブ
- 2スイッチのフォワード・パワー・コンバータ

3 概要

LM5109Bデバイスは、同期降圧型またはハーフブリッジの構成においてハイサイドとローサイド両方のNチャネルMOSFETを駆動するよう設計された、コスト効率の優れた高電圧ゲート・ドライバです。フローティング・ハイサイド・ドライバは、最大90Vのレール電圧で動作できます。各出力は、コスト効率の優れたTTLおよびCMOS互換の入力スレッショルドによって独立して制御されます。

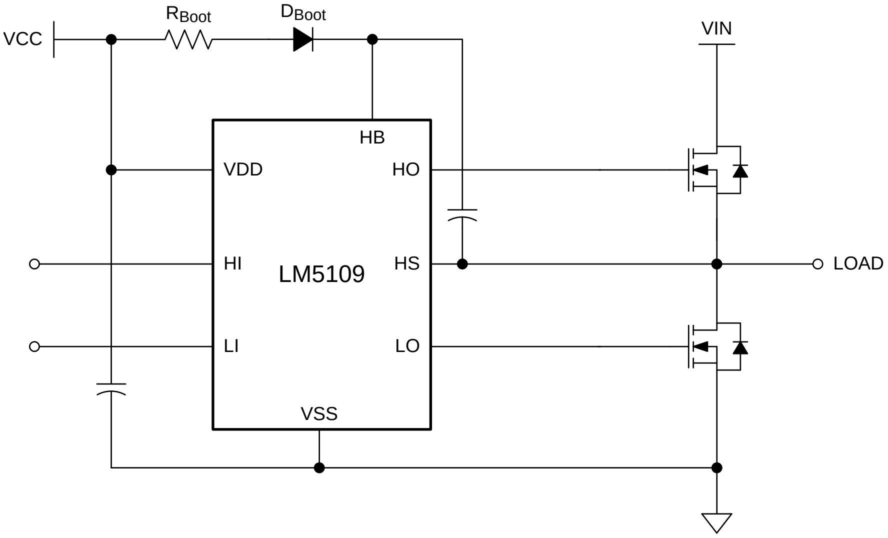
堅牢なレベル・シフト技術により、消費電力を抑えながら高速で動作し、制御入力ロジックからハイサイド・ゲート・ドライバへのクリーンなレベル遷移を実現します。ローサイドとハイサイド両方の電源レールに低電圧誤動作防止機能が搭載されています。このデバイスは、8ピンSOICパッケージ、および熱特性が強化された8ピンWSONパッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
LM5109B	SOIC (8)	4.90mm×3.91mm
	WSON (8)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

アプリケーション概略図



目次

4 改訂履歴

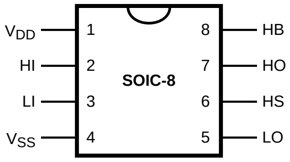
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision から変更 B (March 2013) to Revision C	**Page**
• 「*ESD定格*」の表、「*機能説明*」、「*デバイスの機能モード*」、「*アプリケーションと実装*」、「*電源に関する推奨事項*」、「*レイアウト*」、「*デバイスとドキュメントのサポート*」、「*メカニカル、パッケージ、および注文情報*」を追加	1

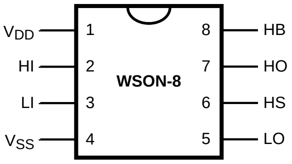
Revision から変更 A (March 2013) to Revision B	**Page**
• Nationalデータシートのレイアウトを TI形式に変更 変更	1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



NGT Package
8-Pin WSON
Top View



Pin Functions

PIN			DESCRIPTION
NO. (1)	**NAME**	**TYPE** (2)	
1	V_{DD}	P	Positive gate drive supply – Locally decouple to V_{SS} using low ESR and ESL capacitor located as close to IC as possible.
2	HI	I	High-side control input – The HI input is compatible with TTL and CMOS input thresholds. Unused HI input must be tied to ground and not left open.
3	LI	I	Low-side control input – The LI input is compatible with TTL and CMOS input thresholds. Unused LI input must be tied to ground and not left open.
4	V_{SS}	G	Ground – All signals are referenced to this ground.
5	LO	O	Low-side gate driver output – Connect to the gate of the low-side N-MOS device.
6	HS	P	High-side source connection – Connect to the negative terminal of the bootstrap capacitor and to the source of the high-side N-MOS device.
7	HO	O	High-side gate driver output – Connect to the gate of the high-side N-MOS device.
8	HB	P	High-side gate driver positive supply rail – Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal of the bootstrap capacitor to HS. The bootstrap capacitor must be placed as close to IC as possible.

(1) For 8-pin WSON package, TI recommends that the exposed pad on the bottom of the package be soldered to ground plane on the PCB and the ground plane must extend out from underneath the package to improve heat dissipation.

(2) G = Ground, I = Input, O = Output, and P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{DD} to V_{SS}	–0.3	18	V
HB to HS	–0.3	18	V
LI or HI to V_{SS}	–0.3	V_{DD} + 0.3	V
LO to V_{SS}	–0.3	V_{DD} + 0.3	V
HO to V_{SS}	V_{HS} – 0.3	V_{HB} + 0.3	V
HS to V_{SS}(2)	–5	90	V
HB to V_{SS}		108	V
Junction temperature	–40	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1 V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} – 15 V. For example, if V_{DD} = 10 V, the negative transients at HS must not exceed –5 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{DD}	8	14	V
HS(1)	–1	90	V
HB	V_{HS} + 8	V_{HS} + 14	V
HS slew rate		50	V/ns
Junction temperature	–40	125	°C

(1) In the application, the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1 V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} – 15 V. For example, if V_{DD} = 10 V, the negative transients at HS must not exceed –5 V.

6.4 Thermal Information

THERMAL METRIC(1)		LM5109B		UNIT
		D (SOIC)	NGT (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.6	42.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.9	34.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.1	19.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.4	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57.6	19.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	8.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = 25°C (unless otherwise specified), $V_{DD} = V_{HB}$ = 12 V, $V_{SS} = V_{HS}$ = 0 V, No Load on LO or HO

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENTS							
I_{DD}	V_{DD} quiescent current	LI = HI = 0 V	T_J = 25°C		0.3		mA
			T_J = –40°C to 125°C			0.6	
I_{DDO}	V_{DD} operating current	f = 500 kHz	T_J = 25°C		1.8		mA
			T_J = –40°C to 125°C			2.9	
I_{HB}	Total HB quiescent current	LI = HI = 0 V	T_J = 25°C		0.06		mA
			T_J = –40°C to 125°C			0.2	
I_{HBO}	Total HB operating current	f = 500 kHz	T_J = 25°C		1.4		mA
			T_J = –40°C to 125°C			2.8	
I_{HBS}	HB to V_{SS} current, quiescent	$V_{HS} = V_{HB}$ = 90 V	T_J = 25°C		0.1		µA
			T_J = –40°C to 125°C			10	
I_{HBSO}	HB to V_{SS} current, operating	f = 500 kHz			0.5		mA
INPUT PINS LI AND HI							
V_{IL}	Low level input voltage threshold	T_J = 25°C			1.8		V
		T_J = –40°C to 125°C		0.8			
V_{IH}	High level input voltage threshold	T_J = 25°C			1.8		V
		T_J = –40°C to 125°C				2.2	
R_I	Input pulldown resistance	T_J = 25°C			200		kΩ
		T_J = –40°C to 125°C		100		500	
UNDERVOLTAGE PROTECTION							
V_{DDR}	V_{DD} rising threshold	$V_{DDR} = V_{DD} – V_{SS}$	T_J = 25°C		6.7		V
			T_J = –40°C to 125°C	6.0		7.4	
V_{DDH}	V_{DD} threshold hysteresis				0.5		V
V_{HBR}	HB rising threshold	$V_{HBR} = V_{HB} – V_{HS}$	T_J = 25°C		6.6		V
			T_J = –40°C to 125°C	5.7		7.1	
V_{HBH}	HB threshold hysteresis				0.4		V
LO GATE DRIVER							
V_{OLL}	Low-level output voltage	I_{LO} = 100 mA, $V_{OHL} = V_{LO} – V_{SS}$	T_J = 25°C		0.38		V
			T_J = –40°C to 125°C			0.65	
V_{OHL}	High-level output voltage	I_{LO} = −100 mA, $V_{OHL} = V_{DD} – V_{LO}$	T_J = 25°C		0.72		V
			T_J = –40°C to 125°C			1.2	
I_{OHL}	Peak pullup current	V_{LO} = 0 V			1		A
I_{OLL}	Peak pulldown current	V_{LO} = 12 V			1		A

Electrical Characteristics (continued)

T_J = 25°C (unless otherwise specified), $V_{DD} = V_{HB}$ = 12 V, $V_{SS} = V_{HS}$ = 0 V, No Load on LO or HO

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HO GATE DRIVER							
V_{OLH}	Low-level output voltage	I_{HO} = 100 mA, $V_{OLH} = V_{HO} - V_{HS}$	T_J = 25°C		0.38		V
			T_J = –40°C to 125°C			0.65	
V_{OHH}	High-level output voltage	I_{HO} = −100 mA, $V_{OHH} = V_{HB} - V_{HO}$	T_J = 25°C		0.72		V
			T_J = –40°C to 125°C			1.2	
I_{OHH}	Peak pullup current	V_{HO} = 0 V			1		A
I_{OLH}	Peak pulldown current	V_{HO} = 12 V			1		A

6.6 Switching Characteristics

T_J = 25°C (unless otherwise specified), $V_{DD} = V_{HB}$ = 12 V, $V_{SS} = V_{HS}$ = 0 V, No Load on LO or HO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LPHL}	Lower turnoff propagation delay (LI falling to LO falling)	T_J = 25°C		30		ns
		T_J = –40°C to 125°C			56	
t_{HPHL}	Upper turnoff propagation delay (HI falling to HO falling)	T_J = 25°C		30		ns
		T_J = –40°C to 125°C			56	
t_{LPLH}	Lower turnon propagation delay (LI rising to LO rising)	T_J = 25°C		32		ns
		T_J = –40°C to 125°C			56	
t_{HPLH}	Upper turnon propagation delay (HI rising to HO rising)	T_J = 25°C		32		ns
		T_J = –40°C to 125°C			56	
t_{MON}	Delay matching: Lower turnon and upper turnoff	T_J = 25°C		2		ns
		T_J = –40°C to 125°C			15	
t_{MOFF}	Delay matching: Lower turnoff and upper turnon	T_J = 25°C		2		ns
		T_J = –40°C to 125°C			15	
t_{RC}, t_{FC}	Either output rise and fall time	C_L = 1000 pF		15		ns
t_{PW}	Minimum input pulse width that changes the output			50		ns

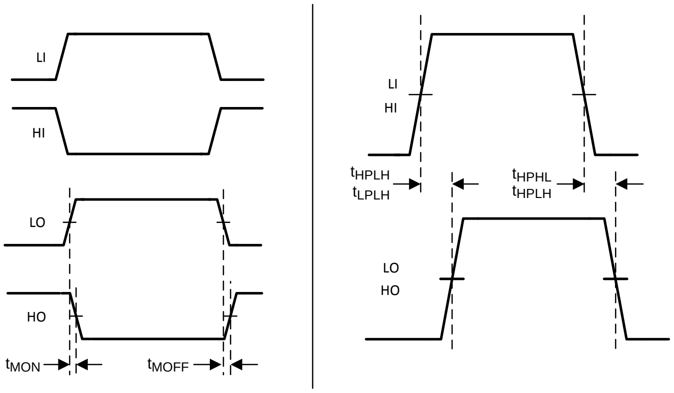


Figure 1. Typical Test Timing Diagram

6.7 Typical Characteristics

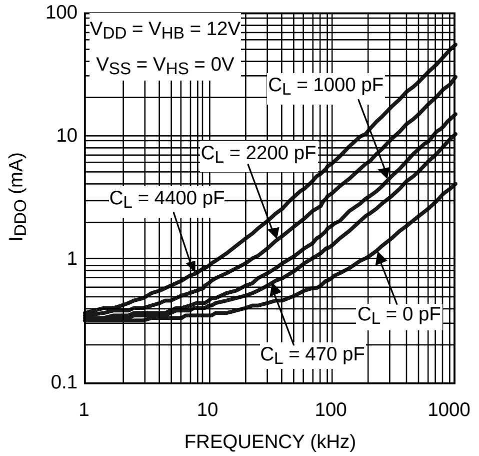
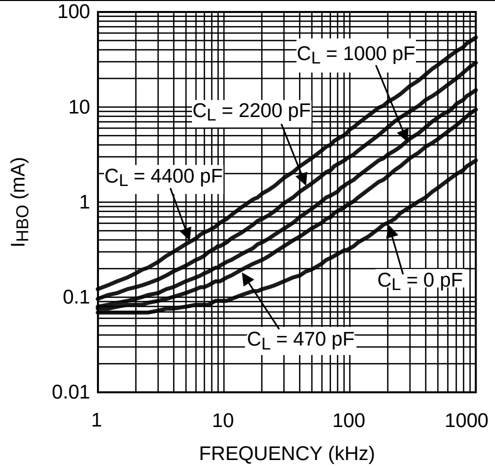


Figure 2. V_{DD} Operating Current vs Frequency



$V_{DD} = V_{HB} = 12$ V $V_{SS} = V_{HS} = 0$ V

Figure 3. HB Operating Current vs Frequency

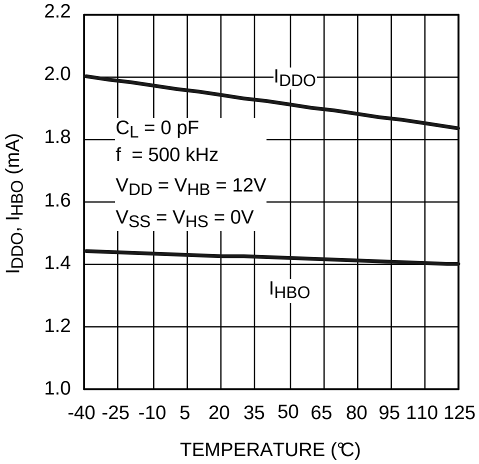


Figure 4. Operating Current vs Temperature

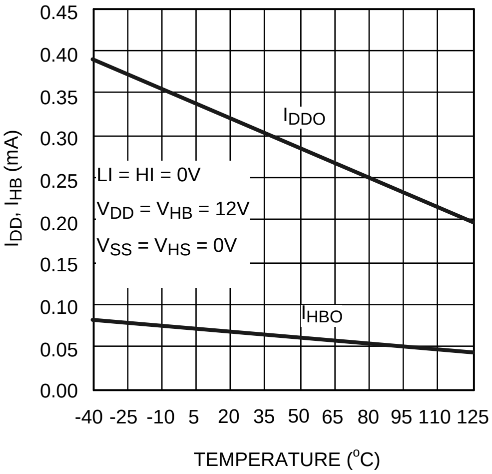


Figure 5. Quiescent Current vs Temperature

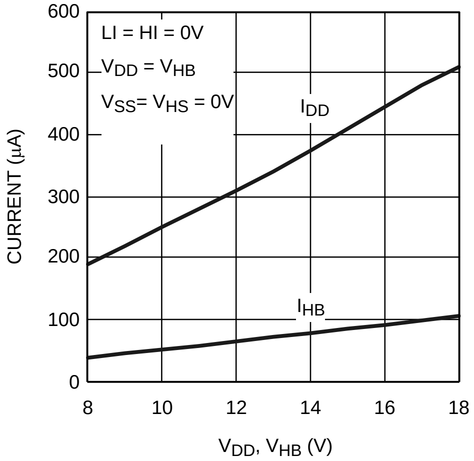


Figure 6. Quiescent Current vs Voltage

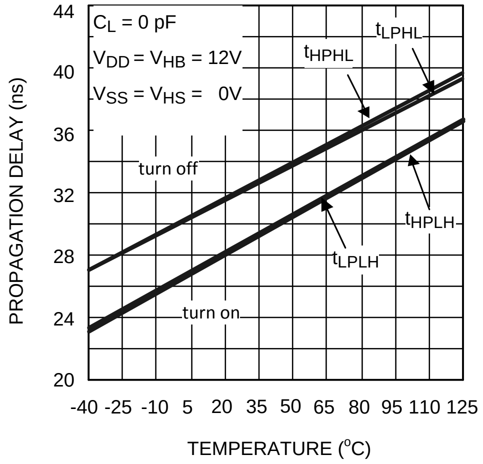


Figure 7. Propagation Delay vs Temperature

Typical Characteristics (continued)

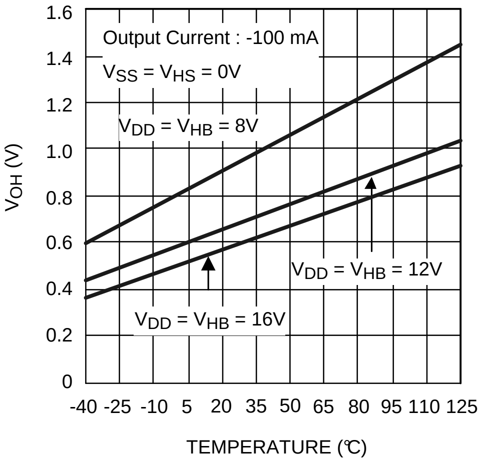


Figure 8. LO and HO High Level Output Voltage vs Temperature

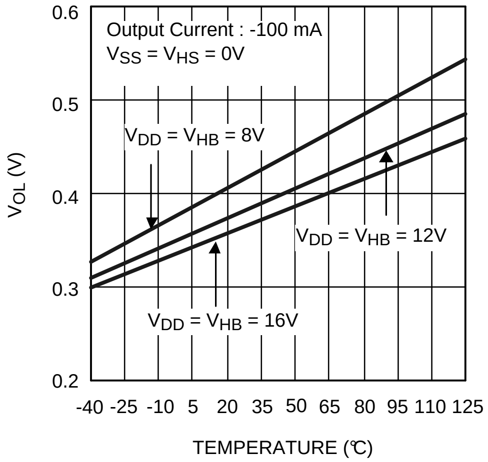


Figure 9. LO and HO Low Level Output Voltage vs Temperature

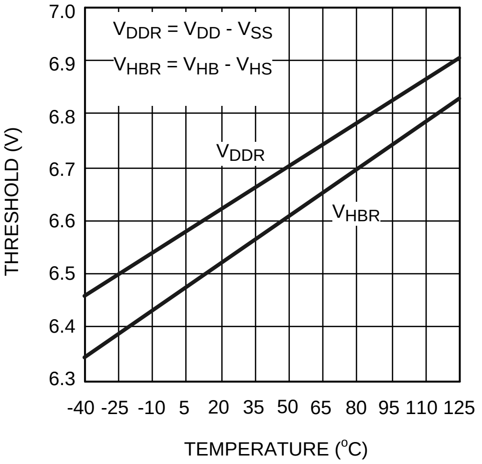


Figure 10. Undervoltage Rising Thresholds vs Temperature

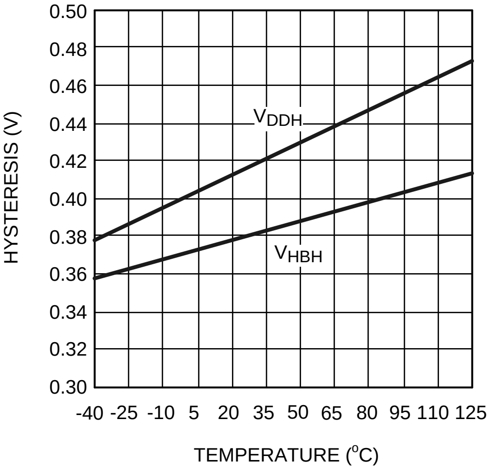


Figure 11. Undervoltage Hysteresis vs Temperature

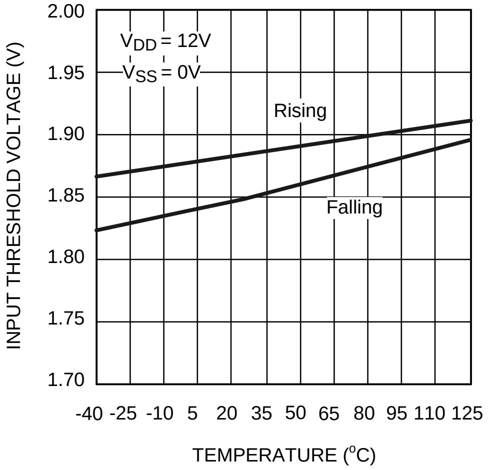


Figure 12. Input Thresholds vs Temperature

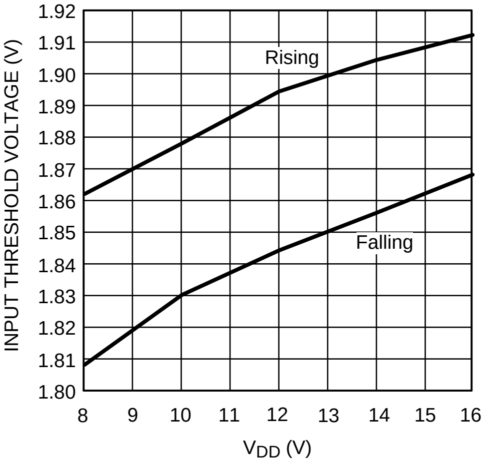


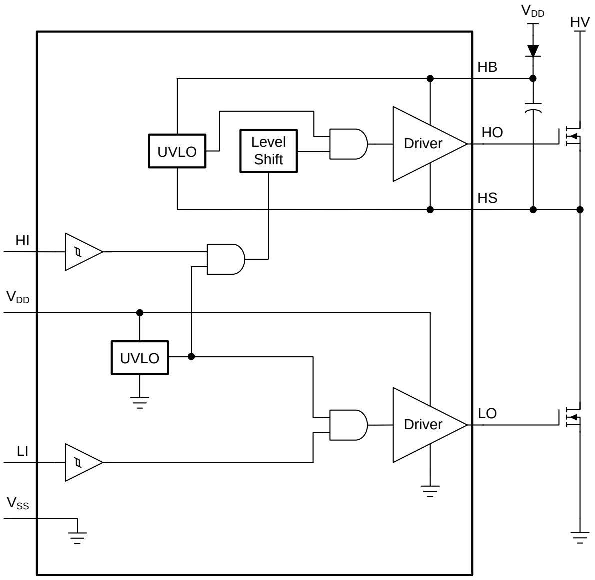
Figure 13. Input Thresholds vs Supply Voltage

7 Detailed Description

7.1 Overview

The LM5109B is a cost-effective, high-voltage gate driver designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configuration. The outputs are independently controlled with TTL and CMOS-compatible input thresholds. The floating high-side driver is capable of working with HB voltage up to 108 V. An external high-voltage diode must be provided to charge high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout (UVLO) is provided on both the low-side and the high-side power rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Start-Up and UVLO

Both top and bottom drivers include UVLO protection circuitry which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage ($V_{HB–HS}$) independently. The UVLO circuit inhibits each output until sufficient supply voltage is available to turn on the external MOSFETs, and the built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the VDD pin of the LM5109B, the top and bottom gates are held low until V_{DD} exceeds the UVLO threshold, typically about 6.7 V. Any UVLO condition on the bootstrap capacitor ($V_{HB–HS}$) will only disable the high-side output (HO).

Table 1. VDD UVLO Feature Logic Operation

CONDITION ($V_{HB-HS} > V_{HBR}$)	HI	LI	HO	LO
V_{DD}-V_{SS} < V_{DDR} during device start-up	H	L	L	L
V_{DD}-V_{SS} < V_{DDR} during device start-up	L	H	L	L
V_{DD}-V_{SS} < V_{DDR} during device start-up	H	H	L	L
V_{DD}-V_{SS} < V_{DDR} during device start-up	L	L	L	L
V_{DD}-V_{SS} < V_{DDR} – V_{DDH} after device start-up	H	L	L	L
V_{DD}-V_{SS} < V_{DDR} – V_{DDH} after device start-up	L	H	L	L
V_{DD}-V_{SS} < V_{DDR} – V_{DDH} after device start-up	H	H	L	L
V_{DD}-V_{SS} < V_{DDR} – V_{DDH} after device start-up	L	L	L	L

Table 2. VHB-HS UVLO Feature Logic Operation

CONDITION ($V_{DD} > V_{DDR}$)	HI	LI	HO	LO
$V_{HB\text{-}HS} < V_{HBR}$ during device start-up	H	L	L	L
$V_{HB\text{-}HS} < V_{HBR}$ during device start-up	L	H	L	H
$V_{HB\text{-}HS} < V_{HBR}$ during device start-up	H	H	L	H
$V_{HB\text{-}HS} < V_{HBR}$ during device start-up	L	L	L	L
$V_{HB\text{-}HS} < V_{HBR} – V_{HBH}$ after device start-up	H	L	L	L
$V_{HB\text{-}HS} < V_{HBR} – V_{HBH}$ after device start-up	L	H	L	H
$V_{HB\text{-}HS} < V_{HBR} – V_{HBH}$ after device start-up	H	H	L	H
$V_{HB\text{-}HS} < V_{HBR} – V_{HBH}$ after device start-up	L	L	L	L

7.3.2 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output which is referenced to the HS pin and provides excellent delay matching with the low-side driver.

7.3.3 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance, and high-peak current capability of both outputs allow for efficient switching of the power MOSFETs. The low-side output stage is referenced to VSS and the high-side is referenced to HS.

7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See *Start-Up and UVLO* for more information on UVLO operation mode. In normal mode when the V_{DD} and $V_{HB–HS}$ are above UVLO threshold, the output stage is dependent on the states of the HI and LI pins. The output HO and LO will be low if input state is floating.

Table 3. INPUT and OUTPUT Logic Table

HI	LI	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
Floating	Floating	L	L

(1) HO is measured with respect to the HS.
(2) LO is measured with respect to the VSS.

7.5 HS Transient Voltages Below Ground

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than –0.3 V below HS can activate parasitic transistors resulting in excessive current flow from the HB supply, possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible to be effective.
2. HB to HS operating voltage must be 15 V or less. Hence, if the HS pin transient voltage is –5 V, VDD must be ideally limited to 10 V to keep HB to HS below 15 V.
3. Low-ESR bypass capacitors from HB to HS and from VDD to VSS are essential for proper operation. The capacitor must be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To operate power MOSFETs at high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shift circuit is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN and PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LM5109B is the high-voltage gate drivers designed to drive both the high-side and low-side N-channel MOSFETs in a half-bridge configuration, full-bridge configuration, or in a synchronous buck circuit. The floating high-side driver is capable of operating with supply voltages up to 90 V. This allows for N-channel MOSFETs control in half-bridge, full-bridge, push-pull, two-switch forward and active clamp topologies. The outputs are independently controlled. Each channel is controlled by its respective input pins (HI and LI), allowing full and independent flexibility to control ON and OFF-time of the output.

8.2 Typical Application

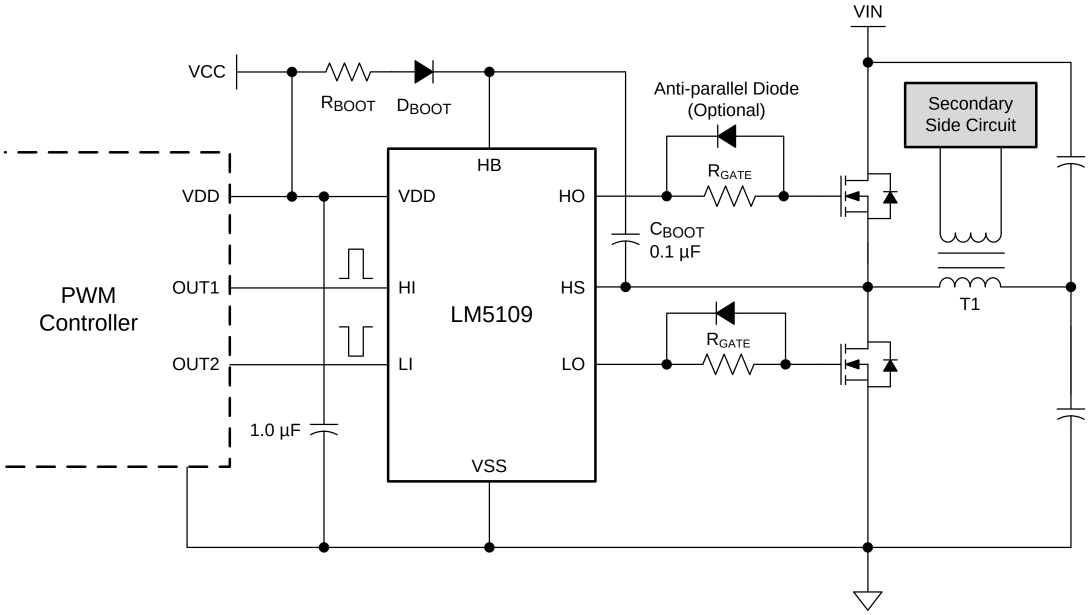


Figure 14. LM5109B Driving MOSFETs in a Half-Bridge Converter

Typical Application (continued)

8.2.1 Design Requirements

Table 4 lists the design parameters of the LM5109B.

Table 4. Design Example

PARAMETER	VALUE
Gate Driver	LM5109B
MOSFET	CSD19534KCS
V_{DD}	10 V
Q_G	17 nC
f_{SW}	500 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Select Bootstrap and VDD Capacitor

The bootstrap capacitor must maintain the $V_{HB\text{-}HS}$ voltage above the UVLO threshold for normal operation. Calculate the maximum allowable drop across the bootstrap capacitor with Equation 1.

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL} = 10\ \text{V} - 1\ \text{V} - 6.7\ \text{V} = 2.3\ \text{V}$$

where

- V_{DD} = Supply voltage of the gate drive IC
- V_{DH} = Bootstrap diode forward voltage drop
- $V_{HBL} = V_{HBRmax} - V_{HBH}$, HB falling threshold (1)

Then, the total charge needed per switching cycle is estimated by Equation 2.

$$Q_{Total} = Q_G + I_{HBS} \times \frac{D_{Max}}{f_{SW}} + \frac{I_{HB}}{f_{SW}} = 17\ \text{nC} + 10\ \mu\text{A} \times \frac{0.95}{500\ \text{kHz}} + \frac{0.2\ \text{mA}}{500\ \text{kHz}} = 17.5\ \text{nC}$$

where

- Q_G = Total MOSFET gate charge
- I_{HBS} = HB to VSS Leakage current
- D_{Max} = Converter maximum duty cycle
- I_{HB} = HB Quiescent current (2)

Therefore, the minimum C_{Boot} must be:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{HB}} = \frac{17.5\ \text{nC}}{2.3\ \text{V}} = 7.6\ \text{nF} \quad (3)$$

In practice, the value of the C_{Boot} capacitor must be greater than calculated to allow for situations where the power stage may skip pulse due to load transients. TI recommends having enough margins and place the bootstrap capacitor as close to the HB and HS pins as possible.

$$C_{Boot} = 100\ \text{nF} \quad (4)$$

As a general rule the local V_{DD} bypass capacitor must be 10 times greater than the value of C_{Boot}, as shown in Equation 5.

$$C_{VDD} = 1\ \mu\text{F} \quad (5)$$

The bootstrap and bias capacitors must be ceramic types with X7R dielectric. The voltage rating must be twice that of the maximum V_{DD} considering capacitance tolerances once the devices have a DC bias voltage across them and to ensure long-term reliability.

8.2.2.2 Select External Bootstrap Diode and Its Series Resistor

The bootstrap capacitor is charged by the V_{DD} through the external bootstrap diode every cycle when low-side MOSFET turns on. The charging of the capacitor involves high peak currents, and therefore transient power dissipation in the bootstrap diode may be significant and the conduction loss also depends on its forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

For the selection of external bootstrap diodes, refer to *AN-1317 Selection of External Bootstrap Diode for LM510X Devices*, SNVA083. Bootstrap resistor R_{BOOT} is selected to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of $V_{HB\text{-}HS}$ during each switching cycle, especially when HS pin have excessive negative transient voltage. R_{BOOT} recommended value is between 2 Ω and 10 Ω depending on diode selection. A current limiting resistor of 2.2 Ω is selected to limit inrush current of bootstrap diode, and the estimated peak current on the D_{Boot} is shown in Equation 6.

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{DH}}{R_{Boot}} = \frac{10\ \text{V} - 1\ \text{V}}{2.2\ \Omega} \approx 4\ \text{A}$$

where

- V_{DH} is the bootstrap diode forward voltage drop (6)

8.2.2.3 Selecting External Gate Driver Resistor

The external gate driver resistor, R_{GATE}, is sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver.

Peak HO pullup current are calculated in Equation 7.

$$I_{OHH} = \frac{V_{DD} - V_{DH}}{R_{HOH} + R_{Gate} + R_{GFET\_Int}} = \frac{10\ \text{V} - 1\ \text{V}}{1.2\ \text{V} / 100\ \text{mA} + 4.7\ \Omega + 2.2\ \Omega} = 0.48\ \text{A}$$

where

- I_{OHH} = Peak pullup current
- V_{DH} = Bootstrap diode forward voltage drop
- R_{HOH} = Gate driver internal HO pullup resistance, provide by driver data sheet directly or estimated from the testing conditions, that is $R_{HOH} = V_{OHH} / I_{HO}$
- R_{Gate} = External gate drive resistance
- R_{GFET_Int} = MOSFET internal gate resistance, provided by transistor data sheet (7)

Similarly, Peak HO pulldown current is shown in Equation 8.

$$I_{OLH} = \frac{V_{DD} - V_{DH}}{R_{HOL} + R_{Gate} + R_{GFET\_Int}}$$

where

- R_{HOL} is the HO pulldown resistance (8)

Peak LO pullup current is shown in Equation 9.

$$I_{OHL} = \frac{V_{DD}}{R_{LOH} + R_{Gate} + R_{GFET\_Int}}$$

where

- R_{LOH} is the LO pullup resistance (9)

Peak LO pulldown current is shown in Equation 10.

$$I_{OLL} = \frac{V_{DD}}{R_{LOL} + R_{Gate} + R_{FET\_Int}}$$

where

- R_{LOL} is the LO pulldown resistance (10)

For some scenarios, if the applications require fast turnoff, an anti-paralleled diode on R_{Gate} could be used to bypass the external gate drive resistor and speed up turnoff transition.

8.2.2.4 Estimate the Driver Power Loss

The total driver IC power dissipation can be estimated through the following components.

1. Static power losses, P_{QC}, due to quiescent current – I_{DD} and I_{HB}

   $$P_{QC} = V_{DD} \times I_{DD} + (V_{DD} - V_{DH}) \times I_{HB} \tag{11}$$

2. Level-shifter losses, P_{IHBS}, due high-side leakage current – I_{HBS}

   $$P_{IHBS} = V_{HB} \times I_{HBS} \times D$$

   where

   - D is the high-side switch duty cycle (12)

3. Dynamic losses, $P_{QG1\&2}$, due to the FETs gate charge – Q_G

   $$P_{QG1\&2} = 2 \times V_{DD} \times Q_G \times f_{SW} \times \frac{R_{GD\_R}}{R_{GD\_R} + R_{Gate} + R_{GFET\_Int}}$$

   where

   - Q_G = Total FETs gate charge
   - f_{SW} = Switching frequency
   - R_{GD_R} = Average value of pullup and pulldown resistor
   - R_{Gate} = External gate drive resistor
   - R_{GFET_Int} = Internal FETs gate resistor (13)

4. Level-shifter dynamic losses, P_{LS}, during high-side switching due to required level-shifter charge on each switching cycle – Q_P

   $$P_{LS} = V_{HB} \times Q_P \times f_{SW} \tag{14}$$

In this example, the estimated gate driver loss in LM5109B is shown in Equation 15.

$$P_{LM5109B} = 10\ \text{V} \times 0.6\ \text{mA} + 9\ \text{V} \times 0.2\ \text{mA} + 72\ \text{V} \times 10\ \mu\text{A} \times 0.95 + 2 \times 10 \times 17\ \text{nC} \times 500\ \text{kHz} \times \frac{12\ \Omega}{12\ \Omega + 4.7\ \Omega + 2.2\ \Omega} + 72\ \text{V} \times 0.5\ \text{nC} \times 500\ \text{kHz} = 0.134\ \text{W} \tag{15}$$

For a given ambient temperature, the maximum allowable power loss of the IC can be defined as shown in Equation 16.

$$P_{LM5109B} = \frac{T_J - T_A}{R_{\theta JA}}$$

where

- $P_{LM5109B}$ = The total power dissipation of the driver
- T_J = Junction temperature
- T_A = Ambient temperature
- $R_{\theta JA}$ = Junction-to-ambient thermal resistance (16)

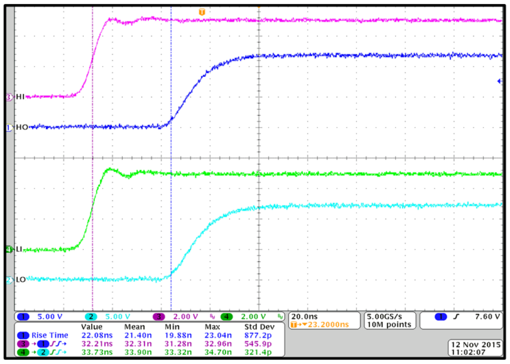
The thermal metrics for the driver package is summarized in the *Thermal Information* table of the data sheet. For detailed information regarding the thermal information table, please refer to the Texas Instruments application note entitled *Semiconductor and IC Package Thermal Metrics* (SPRA953).

8.2.3 Application Curves

Figure 15 and Figure 16 shows the rising and falling time as well as turnon and turnoff propagation delay testing waveform in room temperature, and waveform measurement data (see the bottom part of the waveform). Each channel (HI, LI, HO, and LO) is labeled and displayed on the left hand of the waveforms.

The testing condition: load capacitance is 1 nF, V_{DD} = 12 V, f_{SW} = 500 kHz.

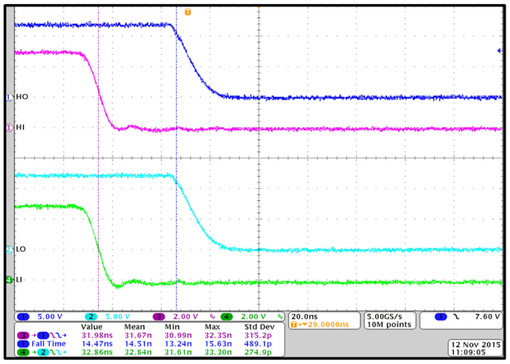
HI and LI share one same input from function generator, therefore, besides the propagation delay and rising and falling time, the difference of the propagation delay between HO and LO gives the propagation delay matching data.



	Value	Mean	Min	Max	Std Dev
1 Rise Time	22.08ns	21.40n	19.88n	23.04n	877.2p
3 → 1	32.21ns	32.31n	31.28n	32.96n	545.9p
4 → 2	33.73ns	33.90n	33.32n	34.70n	321.4p

C_L = 1 nF V_{DD} = 12 V f_{SW} = 500 kHz

Figure 15. Rising Time and Turnon Propagation Delay



	Value	Mean	Min	Max	Std Dev
3 → 1	31.98ns	31.67n	30.99n	32.35n	315.2p
1 Fall Time	14.47ns	14.51n	13.24n	15.63n	489.1p
4 → 2	32.86ns	32.84n	31.61n	33.30n	274.9p

C_L = 1 nF V_{DD} = 12 V f_{SW} = 500 kHz

Figure 16. Falling Time and Turnoff Propagation Delay

9 Power Supply Recommendations

The recommended bias supply voltage range for LM5109B is from 8 V to 14 V. The lower end of this range is governed by the internal undervoltage lockout (UVLO) protection feature of the V_{DD} supply circuit blocks. The upper end of this range is driven by the 18-V absolute maximum voltage rating of the V_{DD}. TI recommends keeping a 4-V margin to allow for transient voltage spikes.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the V_{DD} voltage drops, the device continues to operate in normal mode as long as the voltage drop does not exceed the hysteresis specification, V_{DDH}. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 8-V range, the voltage ripple on the auxiliary power supply output must be smaller than the hysteresis specification of LM5109B to avoid triggering device-shutdown.

A local bypass capacitor must be placed between the VDD and GND pins. And this capacitor must be located as close to the device as possible. A low-ESR, ceramic surface mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100-nF, ceramic surface-mount capacitor for high-frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220-nF to 10-µF, for IC bias requirements. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore a 22-nF to 220-nF local decoupling capacitor is recommended between the HB and HS pins.

10 Layout

10.1 Layout Guidelines

Optimum performance of high-side and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low-ESR and low-ESL capacitors must be connected close to the IC between VDD and VSS pins and between HB and HS pins to support high peak currents being drawn from VDD and HB during the turnon of the external MOSFETs.
2. To prevent large voltage transients at the drain of the top MOSFET, a low-ESR electrolytic capacitor and a good-quality ceramic capacitor must be connected between the MOSFET drain and ground (VSS).
3. To avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the source of the top MOSFET and the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   - The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver must be placed as close as possible to the MOSFETs.
   - The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

10.2 Layout Example

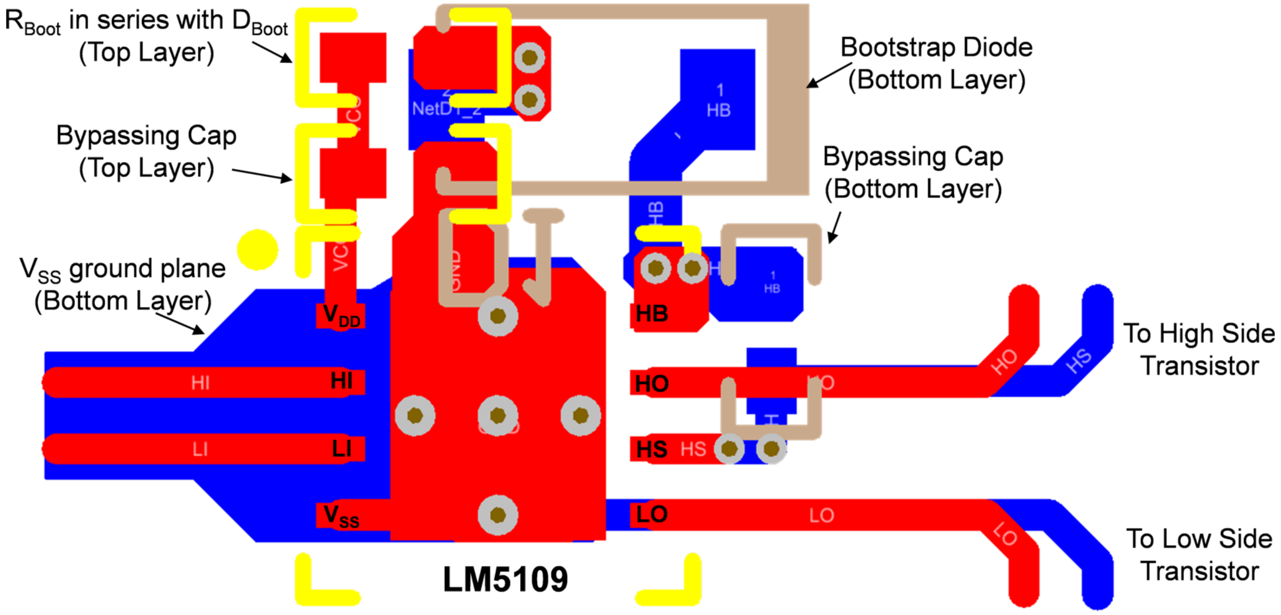


Figure 17. Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- 『*AN-1317 Selection of External Bootstrap Diode for LM510X Devices*』、SNVA083
- 『*Semiconductor and IC Packaging Thermal Metrics*』、SPRA953

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5109BMA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5109 BMA	Samples
LM5109BMAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5109 BMA	Samples
LM5109BSD/NOPB	ACTIVE	WSON	NGT	8	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	5109BSD	Samples
LM5109BSDX/NOPB	ACTIVE	WSON	NGT	8	4500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	5109BSD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM5109B :

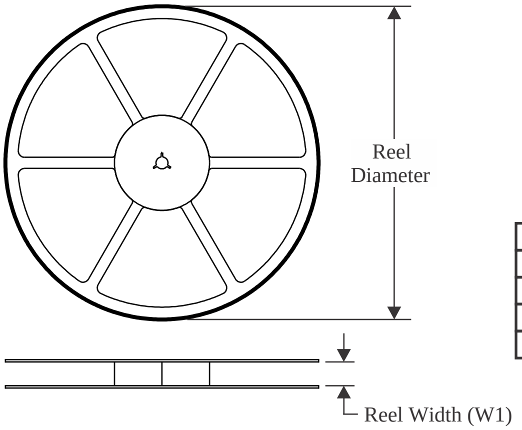
- Automotive : LM5109B-Q1

NOTE: Qualified Version Definitions:

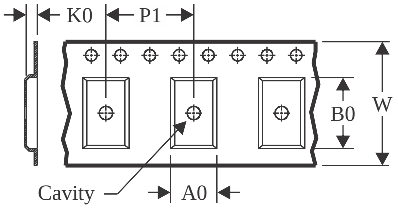
  - Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

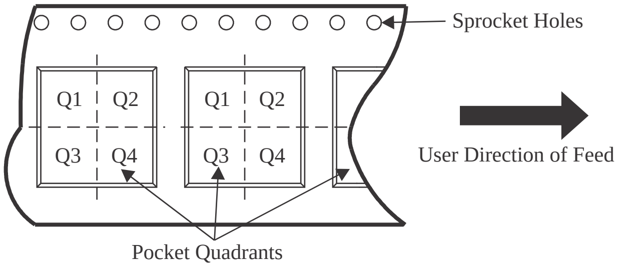


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

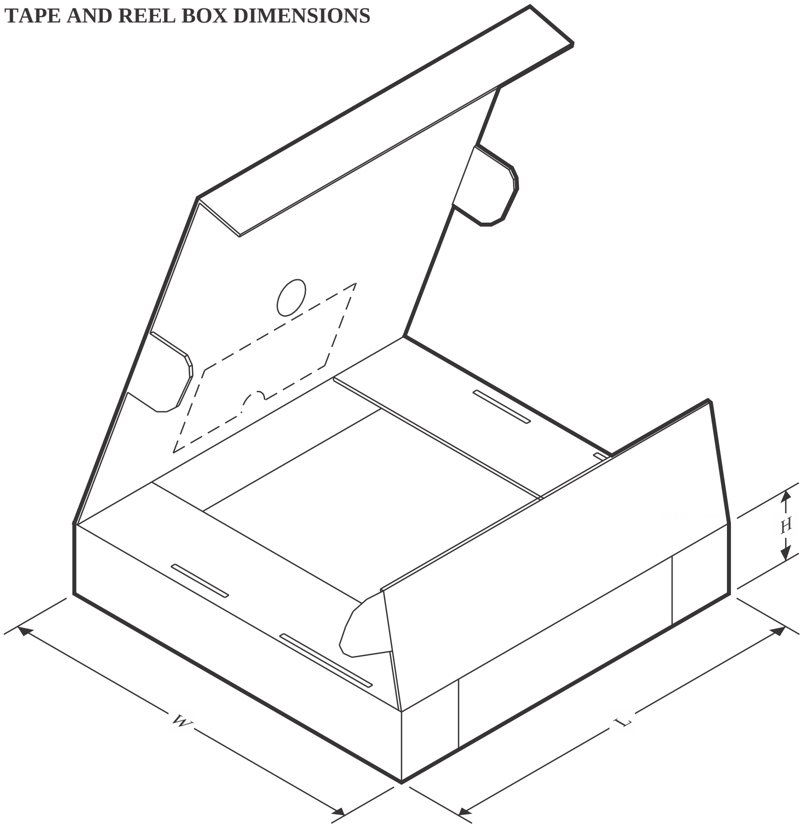
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5109BMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5109BSD/NOPB	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5109BSDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

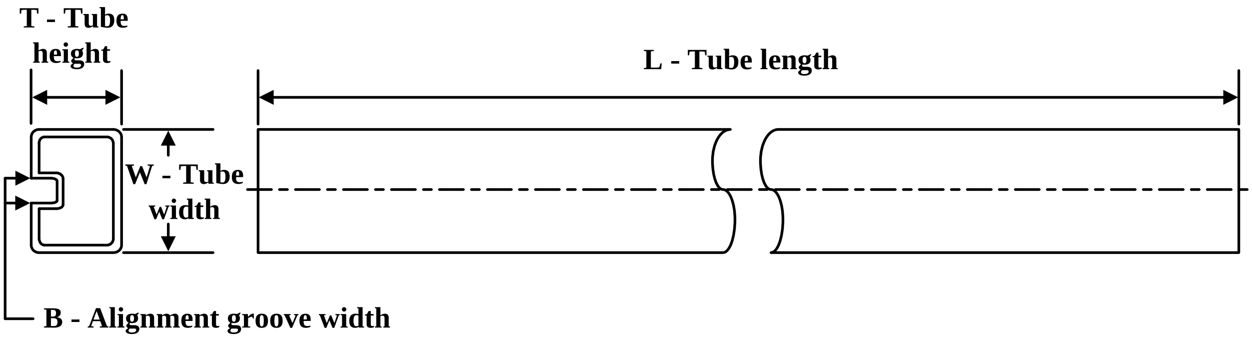
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

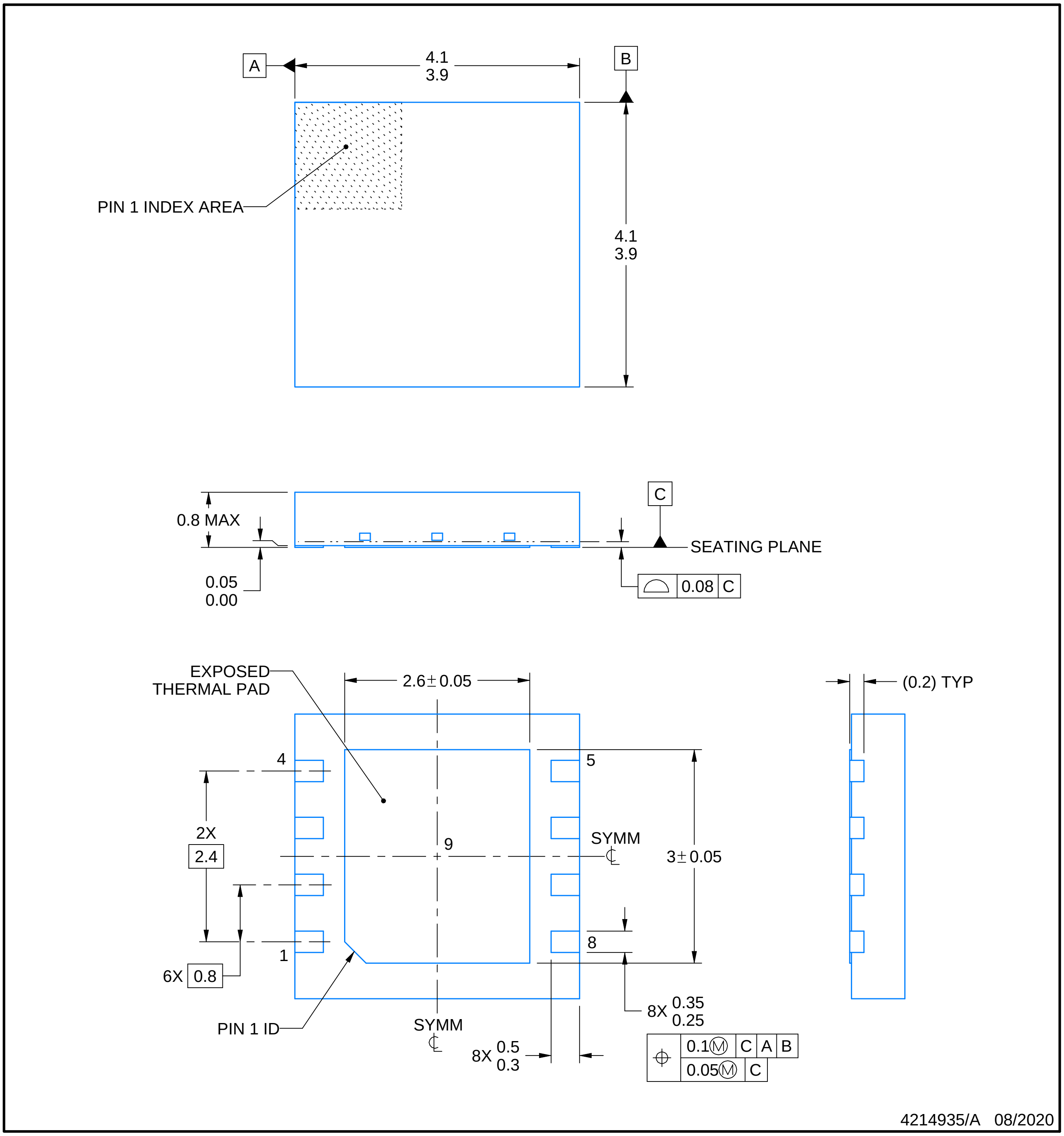
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5109BMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5109BSD/NOPB	WSON	NGT	8	1000	208.0	191.0	35.0
LM5109BSDX/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0

TUBE



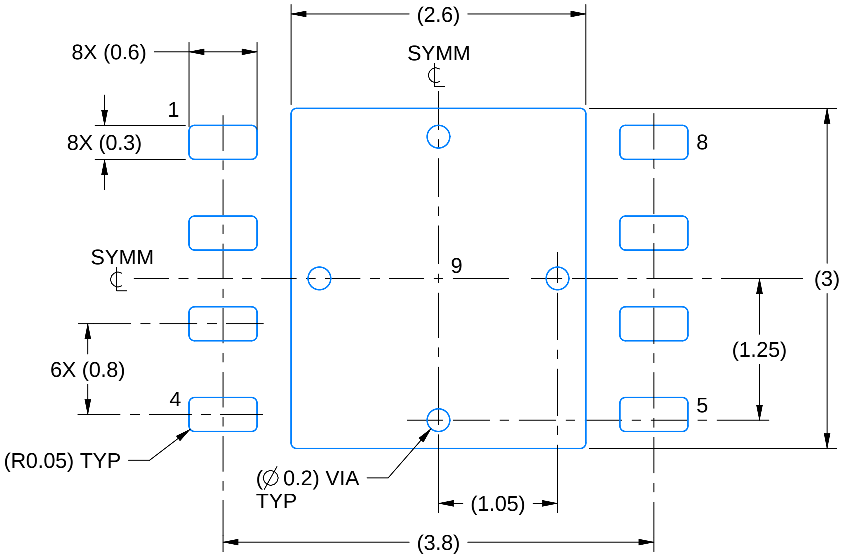
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5109BMA/NOPB	D	SOIC	8	95	495	8	4064	3.05

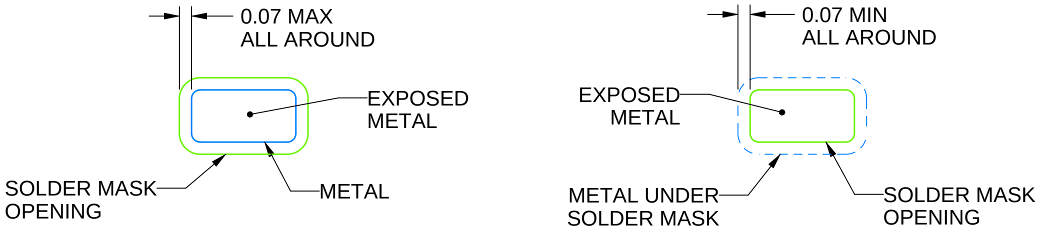


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



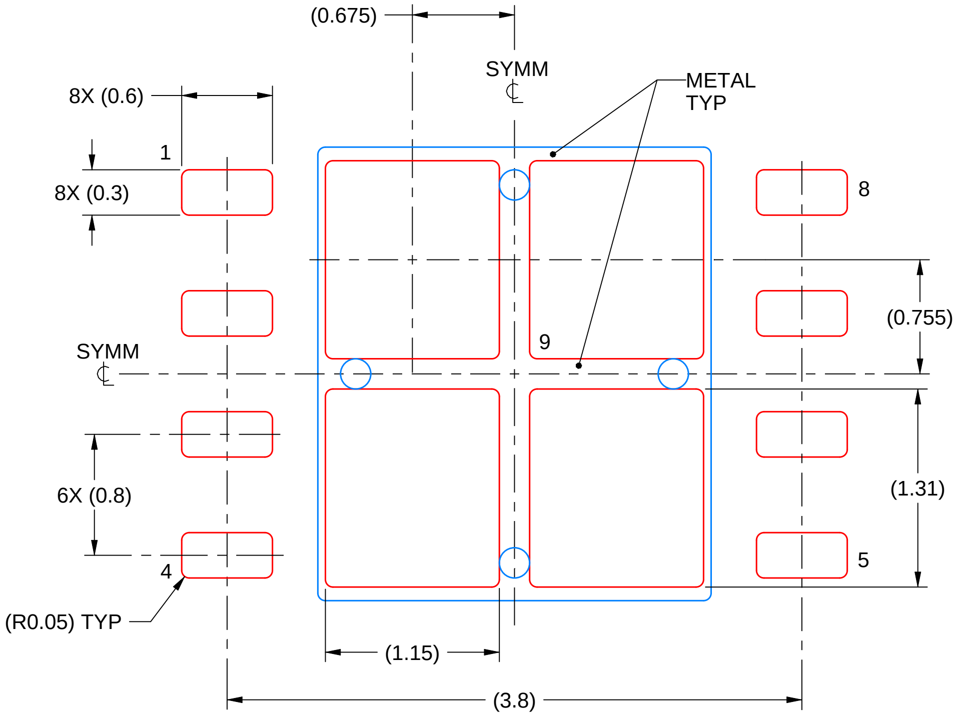
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

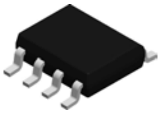


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

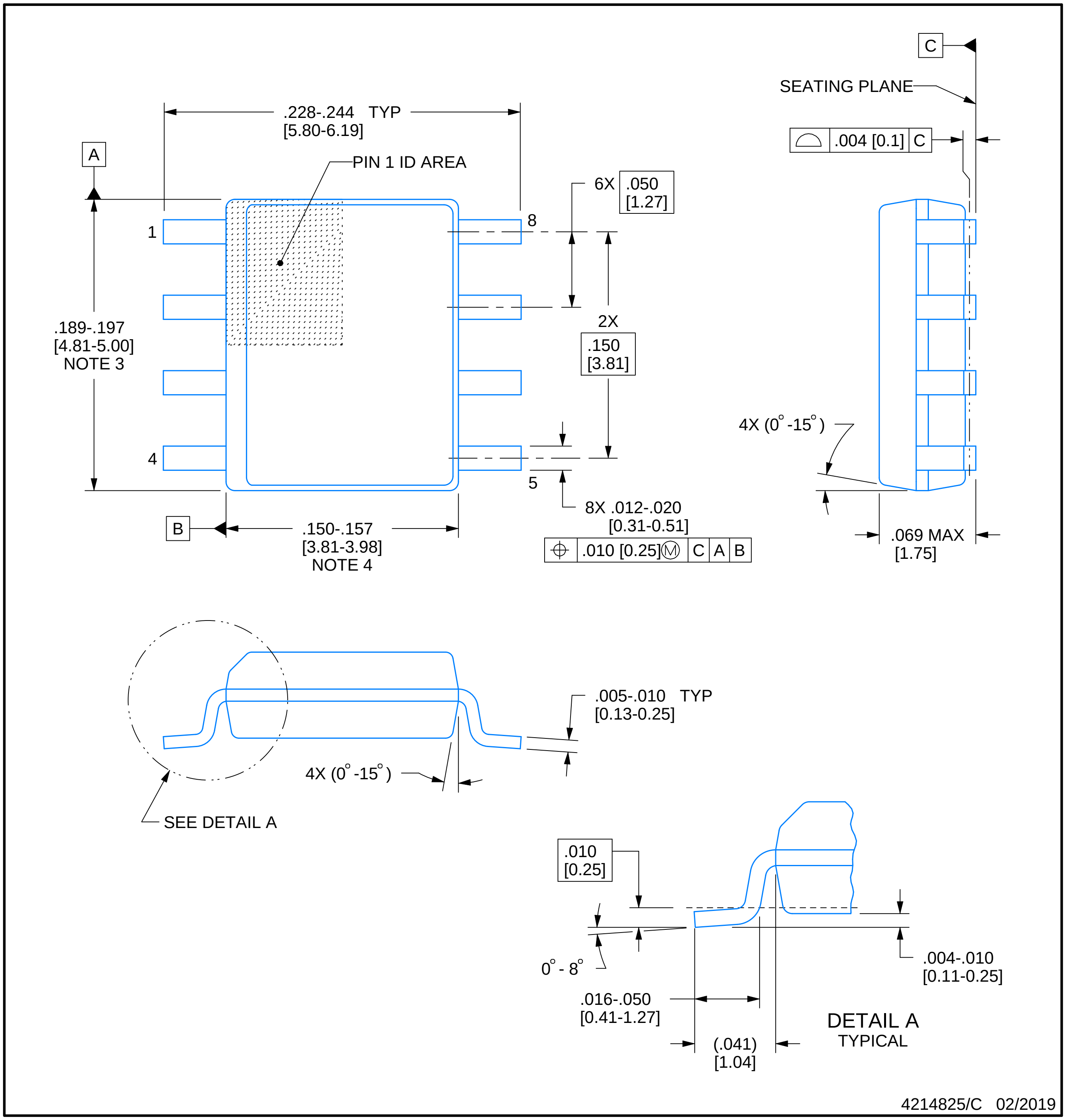
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



PACKAGE OUTLINE

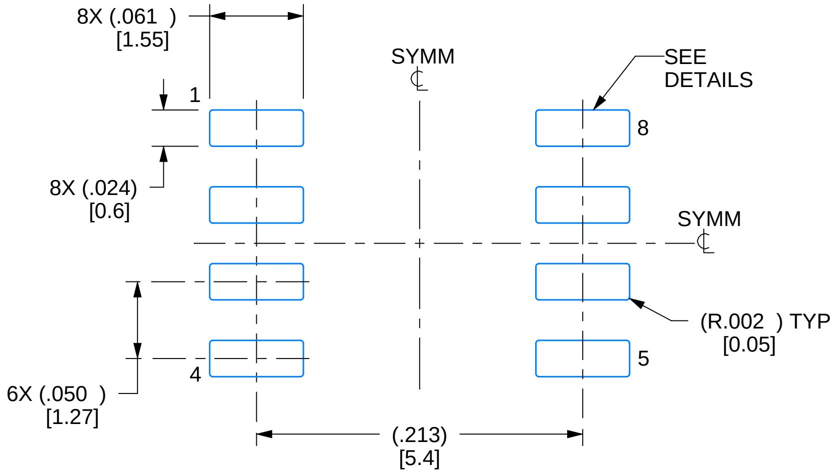
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

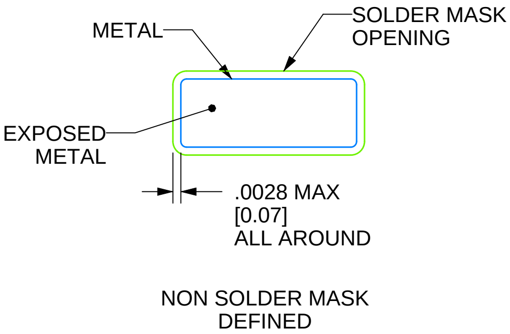


NOTES:

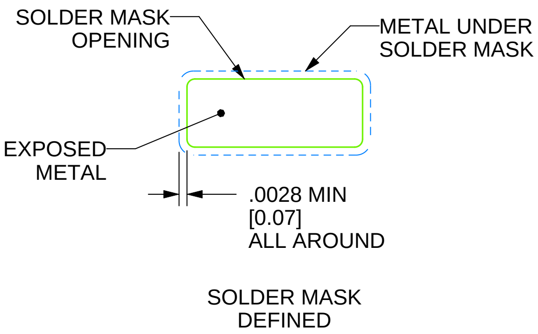
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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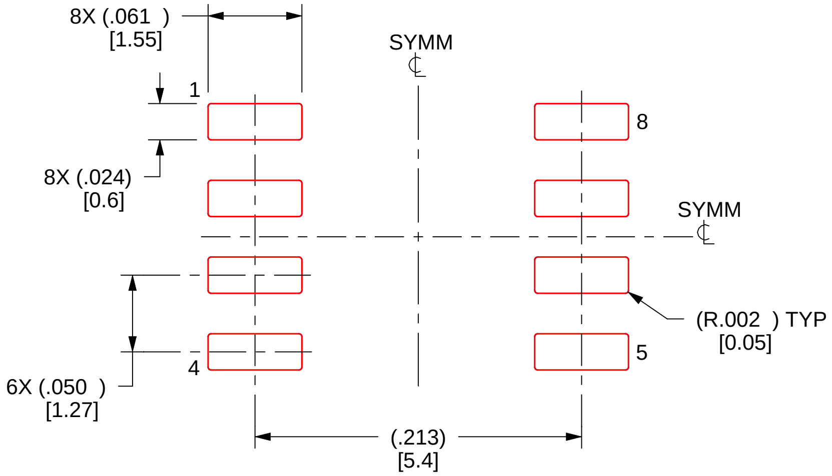
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265