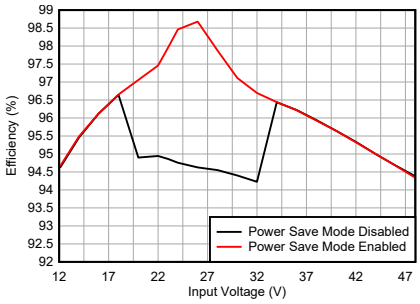
LM51770 78V、広い V_{IN} 双方向 4 スイッチ昇降圧コントローラ

1 特長

- 3.5V～78V の広い入力範囲 (絶対最大定格 85V)
  - $V_{(BIAS)}$ > 3.5V のとき、最小 2.8V
- 3.3V～78V の出力電圧
- 低シャットダウン I_Q:3μA
- 低静止電流 I_Q:60μA
- 3% の逆電流制限精度により、精度の高い充電電流を実現
- 平均入出力電流モニタまたはリミッタ
- PWM またはアナログ入力信号の動的な出力電圧トラッキング
- 負荷がきわめて軽い時の効率を向上させるパワーセーブ モード (PSM) を選択可能
- 自動選択機能を備えた 2 つの高電圧電源 LDO を内蔵
- 全動作モードにわたる固定周波数 (昇圧、昇降圧、降圧)
  - 強制 PWM モードを選択可能
  - 小規模ソリューションと部品サイズ用の最大 1.8MHz のスイッチング
  - 外部クロック同期
- スペクトラム拡散動作を選択可能
- 可変低電圧保護
- ヒカップ過電流および短絡保護

2 アプリケーション

- 非絶縁型 DC/DC 電源 (商用 DC/DC、リモート無線ユニット、モーター駆動制御)



効率と入力電圧との関係 (V_O = 24V、I_O = 5A)

- バックアップ電源システム (バッテリ バックアップ、防火)
- 産業用 PC (シングル ボード コンピュータ)
- 医療用 PSU (酸素濃縮器)
- PoE (Power over Ethernet) (ルータ)
- 太陽光発電 (ソーラー充電コントローラ)

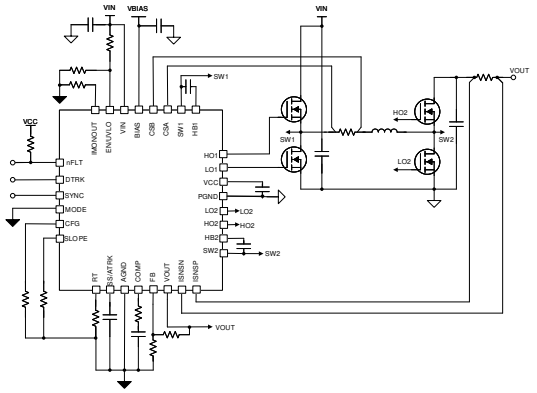
3 概要

LM51770 は、4 スイッチ昇降圧コントローラです。本デバイスは入力電圧が、調整された出力電圧よりも高い、等しい、または低い場合に、レギュレートされた出力電圧を供給します。このデバイスは、パワーセーブ モードでの静止電流が小さいため、出力負荷が小さくても高効率をサポートします。パワーセーブ モードでは、出力電流の全範囲にわたって 99% に近い高効率をサポートします。LM51770 は、固定スイッチング周波数で動作します。これは、RT または SYNC ピンで設定できます。降圧、昇圧、昇降圧動作中も、スイッチング周波数は同一に維持されます。内蔵、オプションの平均電流モニタは、LM51770 の入出力電流の監視と制限に役立ちます。また、この機能は、定電流 (CC) と定電圧 (CV) を使用する、バッテリまたはコンデンサなどのバックアップ電源要素の充電もサポートしています。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
LM51770	DCP038	9.7mm × 4.4mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



概略回路図

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4 Device Comparison

表 4-1. Device Comparison

FUNCTION	LM51770	LM5177	LM251772	LM51772
Maximum Recommended Input Voltage	78V	60V	36V	55V
Absolute Maximum Input Voltage	85V	85V	48V	59V
Maximum Recommended Switching Frequency	1.8MHz	600kHz	600kHz	2.2MHz
Default Output Voltage Value	n/a	n/a	5.1V	12V
Default Output Current Limit Value	n/a	n/a	900mA	5A
I^2C interface	no	no	yes	yes
Output Start-up State Without Programming	Enabled	Enabled	Disabled	Enabled
PSM - Automatic Conduction Mode	yes	no	yes	yes
PSM - Programmable Conduction Mode	no	no	no	yes
Output Discharge	no	no	yes	yes
Input voltage regulation	with external circuit	with external circuit	yes	yes
Analog Current Limit Setting	no	no	no	yes
T_j Temperature Range	-40°C to 125°C	-40°C to 125°C	0°C to 70°C	-40°C to 125°C

5 Pin Configuration and Functions

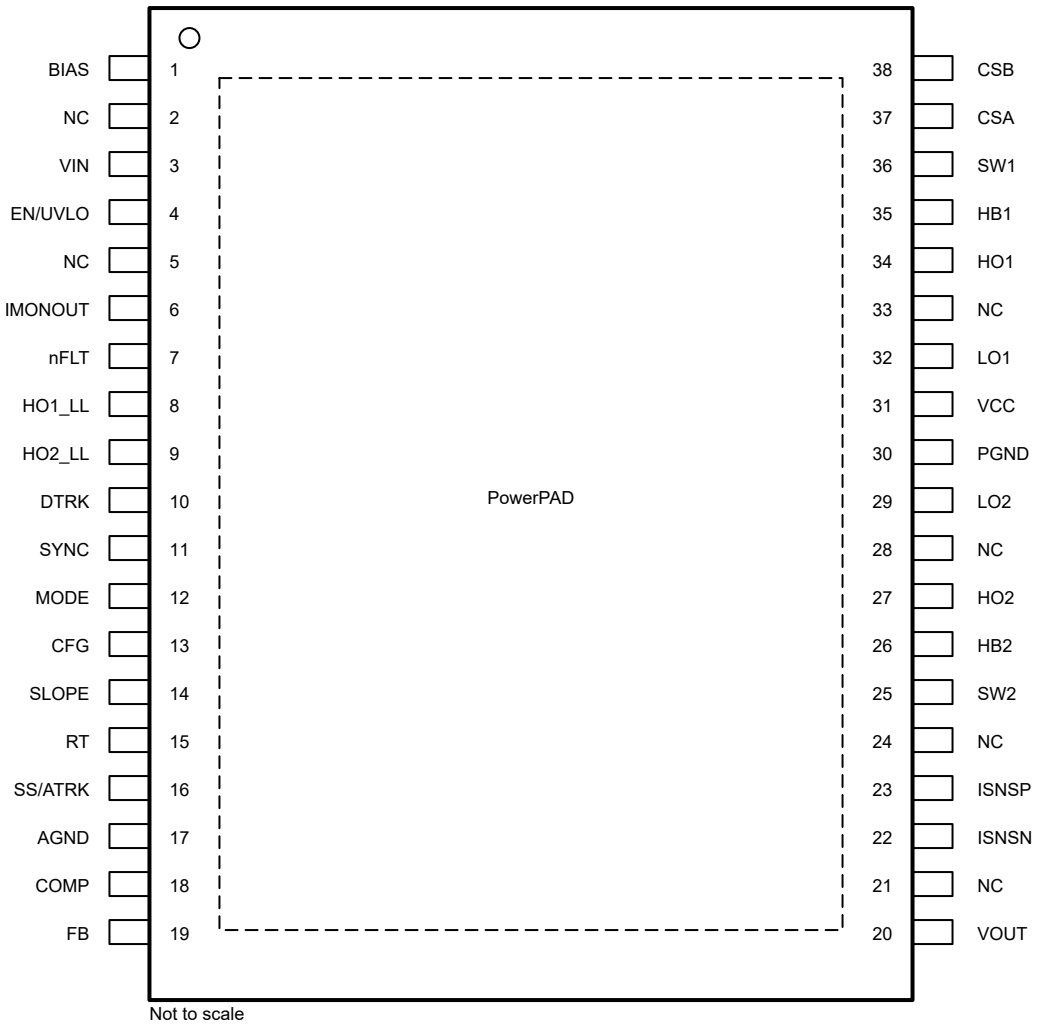


図 5-1. 38-Pin DCP HTSSOP Pin Diagram

表 5-1. Pin Functions LM5177

Pin		Type[1]	Description
Name	No.		
AGND	17	G	Analog ground of the device
BIAS	1	I	Optional input to the VCC bias regulator. Powering VCC from an external supply instead of VIN can reduce power loss at high V_{IN}. If the bias pin supply is not used in the application connect the pin GND
CFG	13	I/O	Device configuration pin. Connect a resistor between the CFG pin to select the device operation for spread spectrum (DRSS), short circuit protection (hiccup mode), current limit, or current monitor.
COMP	18	O	Output of the error amplifier. An external RC network connected between COMP and AGND compensates the regulator of the output voltage feedback loop.
CSA	37	I	Inductor peak current sensor positive input. Connect CSA to the positive side of the external current sense resistor using a low-current Kelvin connection.
CSB	38	I	Inductor peak current sense negative input. Connect CSB to the negative side of the external current sense resistor using a low-current Kelvin connection.

表 5-1. Pin Functions LM5177 (続き)

Pin		Type[1]	Description
Name	No.		
DTRK	10	I	Digital PWM input pin for the dynamical output voltage tracking. *Do not leave this pin floating.* If this function is not used, connect the pin to VCC or GND.
EN/UVLO	4	I	Enable pin. The pin enables or disables the device. If the pin is less than 0.6 V, the device shuts down. The pin must be raised above 0.65 V to enable the device. This pin is the enable pin for the device internal reference circuit and input voltage UVLO comparator input.
FB	19	I	Feedback pin for output voltage regulation. Connect a resistor divider network from the output of the converter to the FB pin.
HB1	35	P	Bootstrap supply pin for buck half-bridge. An external capacitor is required between the HB1 pin and the SW1 pin, respectively, to provide bias to the high-side MOSFET gate driver.
HO1	34	O	High-side gate driver output for the buck half-bridge
HO1_LL	8	O	Logic level output of the HO1 gate signal. Connect this ground reference PWM signal to an optional external gate-driver input. If the function is not used, make no external connection to this pin.
HB2	26	P	Bootstrap supply pin for boost half-bridge. An external capacitor is required between the HB2 pin and the SW2 pin, respectively, to provide bias to the high-side MOSFET gate driver.
HO2	27	O	High-side gate driver output for the boost half-bridge
HO2_LL	9	O	Logic level output of the HO2 gate signal. Connect this ground reference PWM signal to an optional external gate-driver input. If the function is not used, make no external connection to this pin.
IMONOUT	6	O	Current monitor output pin. Output of the voltage-controlled current source of the optional current monitor. Connect the pin to a resistor to sense the voltage across. If the output or input current sense amplifier is configured as current limiter, an external RC network connected between IMONOUT and AGND compensates the regulator of the current feedback loop. Connect the IMONOUT pin to VCC to disable the block and reduce the quiescent current
ISNSN	22	I	Negative sense input of the output or input current sense amplifier. An optional current sense resistor connected between ISNSN and ISNSP can be located either on the input side or on the output side of the power stage. In case the current monitor is disabled connect ISNSN to ground
ISNSP	23	I	Positive sense input of the output or input current sense amplifier. An optional current sense resistor connected between ISNSN and ISNSP can be located either on the input side or on the output side of the power stage. In case the current monitor is disabled connect ISNSN to ground
LO1	32	O	Low-side gate driver output for the buck half-bridge
LO2	29	O	Low-side gate driver output for the boost half-bridge
MODE	12	I	Digital input to select device operation mode. If the pin is pulled low, power save mode (PSM) is enabled. If the pin is pulled high, the forced PWM or CCM operation is enabled. The configuration can be changed dynamically during operation. *Do not leave this pin floating*.
NC	2	NC	No internal connection
NC	5	NC	No internal connection
NC	21	NC	No internal connection
NC	24	NC	No internal connection
NC	28	NC	No internal connection
NC	33	NC	No internal connection
nFLT	7	O	Open-drain output pin for fault indication or power good. This pin is pulled low when FB is outside a ±10% regulation window around the regulation window of the nominal output voltage. If the nFLT pin function is not used the pin can be kept floating.
PowerPAD	PAD	G	Connect the PowerPAD to the analog ground. Use thermal vias to connect to a PCB ground plane for improved power dissipation.
PGND	30	G	Power ground. This pin is the high current ground connection to the low-side gate drivers and for the internal VCC regulator.

表 5-1. Pin Functions LM5177 (続き)

Pin		Type(1)	Description
Name	No.		
RT	15	I/O	Switching frequency programming pin. An external resistor is connected to the RT pin and AGND to set the switching frequency.
SLOPE	14	I	A resistor connected between the SLOPE pin and AGND provides the slope compensation ramp for stable current mode operation in both buck and boost mode.
SS/ATRK	16	I/O	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start time. Analog output voltage tracking pin. The VOUT regulation target can be programmed by connecting the pin to variable voltage reference (for example, through a digital to analog converter). The internal circuit selects the lowest voltage applied to the pin.
SW1	36	P	Inductor switch node for the buck half-bridge
SW2	25	P	Inductor switch node for the boost half-bridge
SYNC	11	I	Synchronization clock input. The internal oscillator can be synchronized to an external clock during operation. If the output or input current sense amplifier is configured as a current limiter pulling, this pin is low during start-up, device switches the current limit direction to a negative polarity. *Do not leave this pin floating*. If this function is not used, connect the pin to VCC.
VCC	31	P	Internal linear bias regulator output. Connect a ceramic decoupling capacitor from VCC to PGND.
VIN	3	I	The input supply and sense input of the device. Connect VIN to the supply voltage of the power stage.
VOUT	20	I	VOUT sense input. Connect to the power stage output rail.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise specified)[1]

		MIN	MAX	UNIT
Input	BIAS to AGND	–0.3	50	V
Input	VIN to AGND	–0.3	85	V
Input	UVLO/EN to AGND	–0.3	$V_{(VIN)}$ + 0.3	V
Input	ATRK/SS, DTRK, RT, SYNC, MODE,,SLOPE, CFG, to AGND[2]	–0.3	5.8	V
Input	FB to AGND	–0.3	5.8	V
Input	CSA, CSB to AGND(DC)	–5	85	V
Input	SW1, SW2 to AGND(DC)	–5	85	V
Input	HB1 to SW1, CSA, CSB	–0.3	5.5[5]	V
Input		–0.3	6.4	V
Input	HB2 to SW2, CSA, CSB	–0.3	5.5[5]	V
Input		–0.3	6.4	V
Input	SW1 to CSA, CSB	–0.3	0.3	V
Input	PGND to AGND	–0.3	0.3	V
Output	VCC to AGND	–0.3	5.5	V
Output	VOUT to AGND	–0.3	85	V
Output	LO1, LO2, to AGND (DC)	–5	$V_{(VCC)}$+0.3	V
Output	nFLT to AGND	–0.3	5.8	V
Output	HO1 to SW1	–0.3	$V_{(HB1)}$ + 0.3	V
Output	HO2 to SW2	–0.3	$V_{(HB2)}$ + 0.3	V
Output	HO1, HO2, ISNSP, ISNSN, HB1, HB2 to AGND (DC)	–0.3	85	V
Output	COMP, IMONOUT to AGND[3]	–0.3	5.8	V
Storage temperature, T_{STG}		–55	150	°C
Operating junction temperature, T_J [4]		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This pin is not specified to have an external voltage applied.
(3) This pin has an internal max voltage clamp which can handle up to 1.6mA.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
(5) Operating lifetime is de-rated for voltage bigger than the specified maximum

6.2 Handling Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]		±2000	V
		Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002[2]	Corner pins	±750	
			Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise specified)(1)

		MIN	NOM	MAX	UNIT
$V_{(VIN)}$	Input Voltage Sense	2.9		78	V
$V_{(VOUT)}$	Output Voltage Sense	3.3		78	V
$V_{(ISNSx)}$	ISNSP;ISNSN	2.8		78	V
$V_{(BIAS)}$	Bias Input Voltage Supply	3.5		42	V
$V_{(VCC)}$	VCC Voltage	3.6		5.3	V
$C_{(VCC)}$	VCC regulator effective output capacitance	10			µF
V_{FB}	FB Input	0		$V_{(VCC)}$ +0.3	V
V_{IL}	Logic pin low-level			0.4	V
V_{IH}	Logic pin high-level	1.3			V
f_{SW}	Typical Switching Frequency	100		1800	kHz
$f_{(SYNC)}$	Synchronization switching frequency limits	100		1800	kHz
	Maximum recommended gate charge per driver output. f_{sw} = 600kHz $V_{(BIAS)}$ = 12V		42		nC
	Maximum recommended gate charge per driver output. f_{sw} = 1.8 MHz $V_{(BIAS)}$ = 12V		13		nC
	Synchronization frequency range relative to RT center frequency			±45	%
	Synchronization input minimum off- or ontime	120			ns
$f_{(DTRK)}$	Tracking input frequency range	150	500		kHz
	Tracking input minimum off- or ontime	120			ns
	Differential voltage for ISNSN to ISNSP		50	55	mV
T_J	Operating Junction Temperature(2)	–40		125	°C

(1) Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		LM51770 HTSSOP 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125℃. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER				MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
	Shutdown current into VIN	$V_{(VIN)}$ = 12 V, $V_{(BIAS)}$ = 0 V $V_{(EN)}$ = 0 V	T_J = 25°C		2.8	4	µA
			T_J = –40°C to 125°C		2.8	5	µA
	Shutdown current into VIN	$V_{(VIN)}$ = 78 V, $V_{(BIAS)}$ = 0 V $V_{(EN)}$ = 0 V	T_J = 25°C		4	5.5	µA
			T_J = –40°C to 125°C		4	8	µA
	Stand-by current into VIN	$V_{(VIN)}$ = 78 V, $V_{(BIAS)}$ = 0 V; 0.7V > $V_{(EN)}$ ≤ 1.25 V	T_J = 25°C		60	80	µA
			T_J = –40°C to 125°C		60	100	µA
	Shutdown current into BIAS	$V_{(VIN)}$ = 0 V, $V_{(EN)}$ = 0 V	T_J = 25°C		2.8	4	µA
			T_J = –40°C to 125°C		2.8	5	µA
	Shutdown current into BIAS	$V_{(BIAS)}$ = 42 V, $V_{(VIN)}$ = 0 V, $V_{(EN)}$ = 0 V	T_J = 25°C		3.5	5.5	µA
			T_J = –40°C to 125°C		3.5	7	µA
	Quiescent current into BIAS	$V_{(EN)}$ = 3.3 V, $V_{(FB)}$ > 1 V, uSleep disabled	T_J = 25°C		1.8	2.5	mA
			T_J = –40°C to 125°C		1.8	2.6	mA
	Quiescent current into BIAS	$V_{(EN)}$ = 3.3 V, $V_{(FB)}$ > 1 V, uSleep enabled	T_J = 25°C		60	80	µA
			T_J = –40°C to 125°C		60	90	µA
I_{IL}	Low-level input current (EN/UVLO)	$V_{(EN/UVLO)}$ ≤ 0.55 V			±0.01	±0.1	µA
VCC REGULATOR							
	VCC regulation	V_{BIAS} 12.0 V ,$I_{(VCC)}$ = 20 mA		4.75	5	5.25	V
		V_{VIN} 12.0 V ,$I_{(VCC)}$ = 20 mA		4.75	5	5.25	V
	VCC line regulation	$I_{(VCC)}$ = 1 mA	$V_{(VIN)}$ =3.5V $V_{(BIAS)}$ = 6.7 V to 42 V			±1	%
			$V_{(BIAS)}$ =0 V $V_{(VIN)}$ = 6.7 V to 78 V			±1	%
	BIAS LDO dropout load regulation	$V_{(BIAS)}$= 6.7V, $V_{(VIN)}$ = 3.5 V,	$I_{(VCC)}$ = 1 mA to 200 mA		65	120	mV
		V_{BIAS} = 3.5V, $V_{(VIN)}$ = 2.8 V, $I_{(VCC)}$ = 35 mA				200	mV
	VIN LDO dropout load regulation	$V_{(BIAS)}$= 0V, $V_{(VIN)}$ = 6.7V,	$I_{(VCC)}$ = 1 mA to 175 mA		65	120	mV
		$V_{(BIAS)}$= 0V, $V_{(VIN)}$ = 3.5V, $I_{(VCC)}$ = 15 mA			100	200	mV
	VCC UVLO delay	VCC rising			6		us
	VCC sourcing current limit	VCC ≥ 4.5 V	$V_{(BIAS)}$= 0V, $V_{(VIN)}$ = 12 V,	200			mA
			$V_{(VIN)}$ = 3.5 V,	200			mA
$V_{T+(VCC)}$	Positive going threshold	V(VCC) rising		3.4	3.45	3.5	V
$V_{T-(VCC)}$	Negative going threshold	V(VCC) falling		3.2	3.25	3.3	V
$V_{T+(VCC,SUP)}$	Positive going threshold for LDO switch-over			6.35	6.5	6.7	V
$V_{hyst(VCC,SUP)}$	LDO switch-over hysteresis			60			mV
ENABLE							
$V_{T+(EN)}$	Enable positive-going threshold	EN rising		0.47	0.63	0.8	V
$V_{T-(EN)}$	Enable negative-going threshold	EN falling		0.45	0.6	0.75	V
Vhyst(EN)	Enable threshold hysteresis	EN falling		20		100	mV
$t_{d(EN)}$	Shutdown delay time			14	20		us
UVLO							
	VDET positive-going threshold	$V_{(VIN)}$ rising		3.3	3.4	3.55	V

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER				MIN	TYP	MAX	UNIT
	VDET negative-going threshold	$V_{(VIN)}$ falling		2.6	2.7	2.85	V
$V_{T+(UVLO)}$	UVLO positive-going threshold	$V_{(EN/UVLO)}$ rising		1.22	1.25	1.28	V
$V_{T-(UVLO)}$	UVLO negative-going threshold	$V_{(EN/UVLO)}$ falling		1.17	1.2	1.23	V
I_{UVLO}	UVLO hysteresis sinking current	0.7 V ≤ $V_{(EN/UVLO)}$ < 1.22 V		4	5	6	µA
	Enable time to start switching	VCC = 5V, $V_{T+(UVLO)}$ > 1.3V			95	100	us
$t_{d(UVLO)}$	UVLO and VDET detection delay time	$V_{(EN/UVLO)}$ falling; V(VDET) falling		25.5	30	34.5	µs
SYNC							
$V_{T+(SYNC)}$	Sync input positive going threshold					1.19	V
$V_{T-(SYNC)}$	Sync input negative going threshold			0.41			V
	Sync activity detection frequency			99			kHz
$t_{d(Det,Sync)}$	Sync activity detection delay	referred to $f_{(SYNC)}$				3	cycles
	Sync PLL lock time	referred to $f_{(SYNC)}$	until $f_{(SYNC)}$ - 5% < $f_{(sw)}$ < $f_{(SYNC)}$ + 5%		10		cycles
SOFT-START							
$I_{(SS)}$	Soft-start current			8.9	10	11	uA
	SS pull-down switch $R_{DS(on)}$	$V_{(SS)}$ = 1 V			23	40	Ω
$t_{d(DISCH;SS)}$	SS Pin discharge time	Time from internal SS discharge until the soft-start current can charge the pin again		500			µs
$V_{(SS,clamp)}$	Clamp Voltage for SS pin			3	5	5.25	V
PULSE WIDTH MODULATION							
	Switching frequency	R_{RT} = 16.2 kΩ		1600	1800	2000	kHz
	Switching frequency	R_{RT} = 316 kΩ		90	100	110	kHz
	Minimum controllable on-time	fPWM, R_{RT} = 16.2 kΩ, positive inductor current	Boost Mode		88		ns
			Buck Mode		128		ns
	Minimum controllable off-time		Boost Mode		152		ns
			Buck Mode		148		ns
	RT regulation voltage				0.75		V
	RT regulation voltage			0.7	0.75	0.8	V
SPREAD SPECTRUM							
	Switching frequency modulation range	upper limit			7.8		%
		lower limit			–7.8		%
VOUT TRACKING							
$V_{T+(DTRK)}$	DTRK positive-going threshold	$V_{(DTRK)}$ rising				1.19	V
$V_{T-(DTRK)}$	DTRK negative-going threshold	$V_{(DTRK)}$ falling		0.41			V
$t_{d(Det,DTRK)}$	DTRK activity detection delay	referred to $f_{(DTRK)}$				3	cycles
fc(LPF)	Corner frequency of internal low pass				35		kHz
	$V_{(REF)}$voltage offset error	$f_{(DTRK)}$ = 500kHz, duty = 50%				±10	mV
MODE SELECTION							
$V_{T+(MODE)}$	Mode input positive going threshold					1.19	V

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER					MIN	TYP	MAX	UNIT
$V_{T-(MODE)}$	Mode input negative going threshold				0.41			V
CURRENT SENSE								
	Positive peak current limit threshold				42.5	50	57.5	mV
				T_J = 25°C to 85°C	43.9	50	54.1	mV
	Negative peak current limit threshold				-57.5	-50	-42.5	mV
				T_J = 25°C to 85°C	-56.3	-50	-42.9	mV
	PSM entry threshold			PSM ENTRY = 10 %	1.2	5.0	9.2	mV
				PSM ENTRY = 15 %	3.4	7.5	11.9	mV
	Peak current limit threshold part to part matching						±10	%
				T_J = 25°C to 85°C			±8.5	%
CURRENT MONITOR/LIMITER								
	Current sense amplifier transconductance		IMON_LIMITER_EN = 0b0	0 mV ≤ $\Delta V_{(ISNS)}$ ≤ 50 mV	0.9	1	1.1	mS
	Offset voltage (1)		IMON_LIMITER_EN = 0b0	T_J= 25°C			±1	mV
	Current sense amplifier bandwidth				1	2		MHz
	Output current IMONOUT		IMON_LIMITER_EN = 0b0, T_J=-40°C to 125°C	$\Delta V_{(IMON)}$ = 45 mV	39	45	49.5	µA
				$\Delta V_{(IMON)}$ = 5 mV	1	5	8.1	µA
	Current sense amplifier transconductance		IMON_LIMITER_EN = 0b1		170	200	220	µS
$\Delta V_{(ISNS)}$	Current sense offset and threshold voltage		IMON_LIMITER_EN = 0b1	T_J= 25°C	49	50	51.7	mV
	ISNS pin input bias currents		ISNSP = ISNSN = 12 V			80	115	µA
	IMONOUT negative output headroom		$V_{(BIAS)}$ > 6.5V; $I_{(IMONOUT)}$ = $I_{(IMONOUT)}$ x 0.975 at $V_{(IMONOUT)}$ = 1V	ΔV = 50mV ,referred to VCC		300	500	mV
				ΔV = –50mV, referred to GND		300	500	mV
$V_{T+(DIS,IMON)}$	Positive going threshold to disable IMON		referred to VCC		55	65	75	%
HICCUP MODE PROTECTION								
	Hiccup mode on time					1		ms
	Hiccup mode off time					24		ms
ERROR AMPLIFIER								
V_{REF}	FB reference Voltage	FB reference			0.99	1	1.01	V
	FB reference Voltage		forced $V_{(SS)}$ = 0.95 V		0.92	0.95	0.98	V
	FB pin leakage current		$V_{(FB)}$ = 1 V				60	nA
	Transconductance					600		µS
	Output resistance				13	96		MΩ
	COMP sourcing current				65	150		uA
	COMP sinking current				65	150		uA
	COMP clamp voltage		$V_{(FB)}$ = 990 mV		1.2	1.25	1.3	V
	COMP clamp voltage		$V_{(FB)}$ = 1.01 V		0.225	0.240	0.255	V
	Unity gain bandwidth					4.5		MHz
OVP								
VT+(OVP)	Over-voltage rising threshold		FB rising reference to V_{REF}		107	110	115	%
VT-(OVP)	Over-voltage falling threshold		FB falling reference to V_{REF}		101	105	109	%

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER					MIN	TYP	MAX	UNIT
	Over-voltage de-glitch time				9	10	12.5	µs
VT+(OVP2)	Over-voltage 2 rising threshold		$V_{(VOUT)}$ rising		80.5	83.5	86	V
	Over-voltage 2 typical programming range		$V_{(VOUT)}$ rising		3.33		83.5	V
VT+(IVP)	Over-voltage rising threshold		$V_{(VIN)}$ rising		80.5		86	V
nFLT								
	nFLT pull-down switch on resistance		1mA sinking			100		Ω
	Power good positive going threshold		FB rising (reference to V_{REF})			95		%
	Power good negative going threshold		FB falling (reference to V_{REF})			90		%
	nFLT off-state leakage		$V_{(nFLT)}$=5V				100	nA
$t_{d(nFLT-PIN)}$	nFLT pin reaction time		Measured from a fault event until nFLT goes low				37	µs
MOSFET DRIVER								
t_r	Rise time	HG1, HG2, LG1, LG2	C_G = 3.3nF			12		ns
t_f	Fall time	HG1, HG2, LG1, LG2	C_G = 3.3nF			12		ns
t_t	Dead-time	HOx from High to Low and LOx from Low to High		$R_{(RT)}$ = 16.2 kΩ		19		ns
		HOx from Low to High and LOx from High to Low		$R_{(RT)}$ = 16.2 kΩ		36		ns
		HOx from High to Low and LOx from Low to High		$R_{(RT)}$ = 316 k Ω		26		ns
		HOx from Low to High and LOx from High to Low		$R_{(RT)}$ = 316 k Ω		44		ns
	Gate driver low side PMOS on-resistance	LO1, LO2	$I_{(test)}$ = 200 mA			1.6		Ω
	Gate driver high side PMOS on-resistance	HO1, HO2	$I_{(test)}$ = 200 mA			1.3		Ω
	Gate driver low side NMOS on-resistance	LO1, LO2	$I_{(test)}$ = 200 mA			0.6		Ω
	Gate driver high side NMOS on-resistance	HO1, HO2	$I_{(test)}$ = 200 mA			0.7		Ω
$V_{TH-(BST\_UV)}$	Negative going boot-strap		$V_{(HBx)}$ - $V_{(SWx)}$ falling		2.4	2.8	3.1	V
$V_{TH+(BST\_UV)}$	Positive going boot-strap		$V_{(HBx)}$ - $V_{(SWx)}$ rising		2.6	3	3.35	V

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, $V_{(BIAS)}$ =12 V

PARAMETER					MIN	TYP	MAX	UNIT
V_{TH+} (BST_OV)	Positive going boot-strap over-voltage threshold	Positive going boot-strap over-voltage threshold	$V_{(HBx)}$ - $V_{(SWx)}$ rising, $I_{(HBx)}$=25uA		4.8	5.5	6.3	V
V_{TH} (GATEOUT)	Low/High Side Gate driver output switching detection		referenced to VCC			37		%
			referenced to V(HBx) - V(SWx)			37		%
THERMAL SHUTDOWN								
T_{T+J}	Thermal shutdown threshold	Thermal shutdown threshold	T_J rising			164		°C
	Thermal shutdown hysteresis	Thermal shutdown hysteresis				15		°C
R2D INTERFACE								
	Internal reference resistor				31.77	33	34.23	kΩ
R_{CFG}	External selection resistor resistance	R2D setting #0				0	0.1	kΩ
		R2D setting #1			0.49567	0.511	0.52633	kΩ
		R2D setting #2			1.1155	1.15	1.1845	kΩ
		R2D setting #3			1.8139	1.87	1.9261	kΩ
		R2D setting #4			2.6578	2.74	2.8222	kΩ
		R2D setting #5			3.7151	3.83	3.9449	kΩ
		R2D setting #6			4.9567	5.11	5.2633	kΩ
		R2D setting #7			6.2953	6.49	6.6847	kΩ
		R2D setting #8			8.0025	8.25	8.4975	kΩ
		R2D setting #9			10.185	10.5	10.815	kΩ
		R2D setting #10			12.901	13.3	13.699	kΩ
		R2D setting #11			15.714	16.2	16.686	kΩ
		R2D setting #12			19.885	20.5	21.115	kΩ
		R2D setting #13			24.153	24.9	25.647	kΩ
		R2D setting #14			29.197	30.1	31.003	kΩ
		R2D setting #15			35.405	36.5	37.595	kΩ

(1) Zero Offset is determined by interpolation

6.6 Typical Characteristics

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC)}$ = 5V

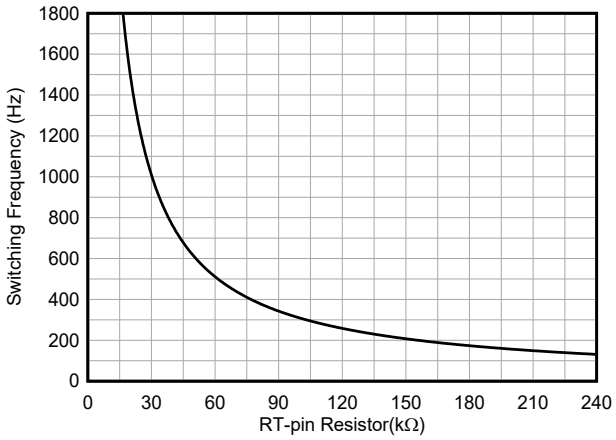


図 6-1. Switching Frequency Versus RT Resistance

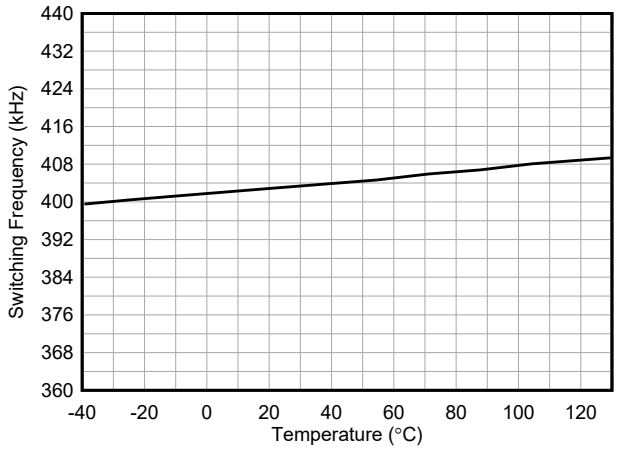


図 6-2. Switching Frequency Versus Temperature $R_{(RT)}$ = 75 kΩ

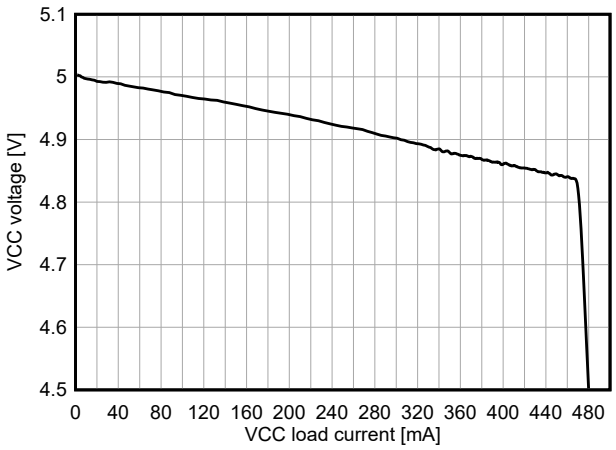


図 6-3. VIN LDO - VCC Voltage versus VCC Load Current

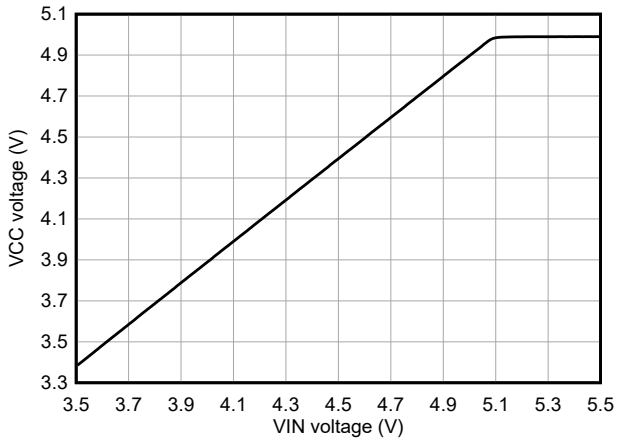


図 6-4. VIN LDO - VCC Voltage versus VIN Voltage $I_{(VCC)}$ = 20 mA

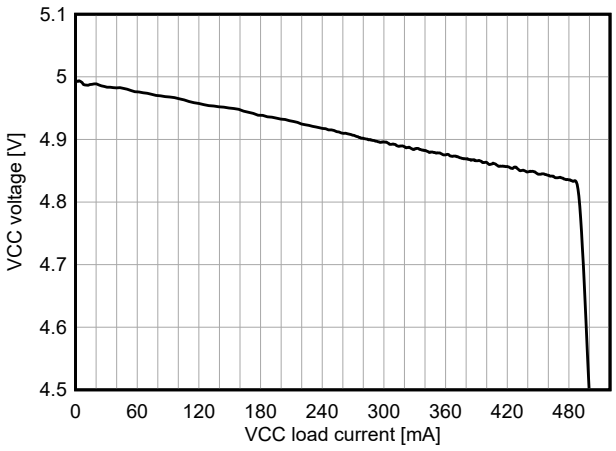


図 6-5. BIAS LDO - VCC Voltage versus VCC Load Current

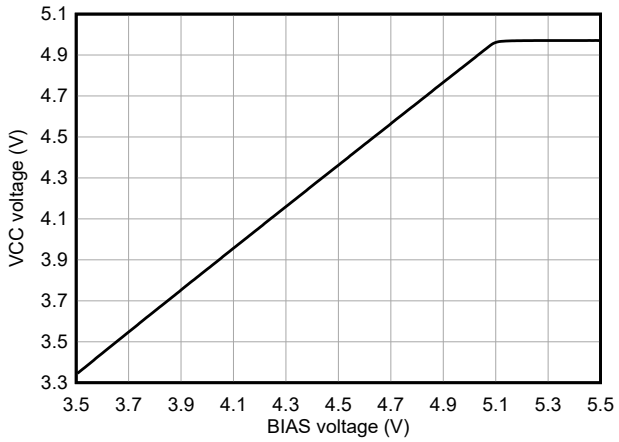


図 6-6. BIAS LDO - VCC Voltage versus BIAS Voltage $I_{(VCC)}$ = 50 mA

6.6 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC)}$ = 5V

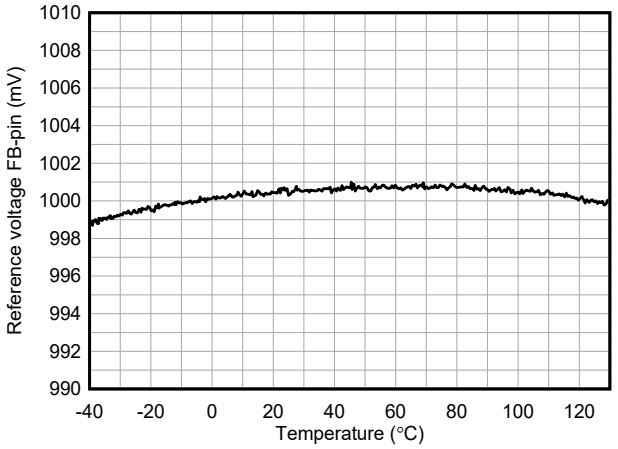


図 6-7. FB Pin Reference Voltage versus Temperature

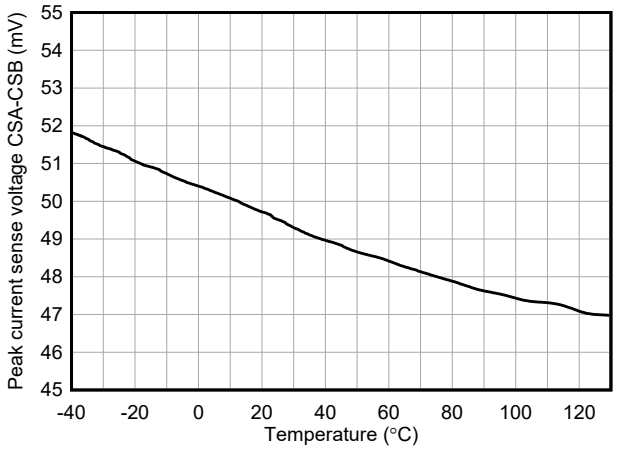


図 6-8. Current Limit Threshold Voltage Versus Temperature

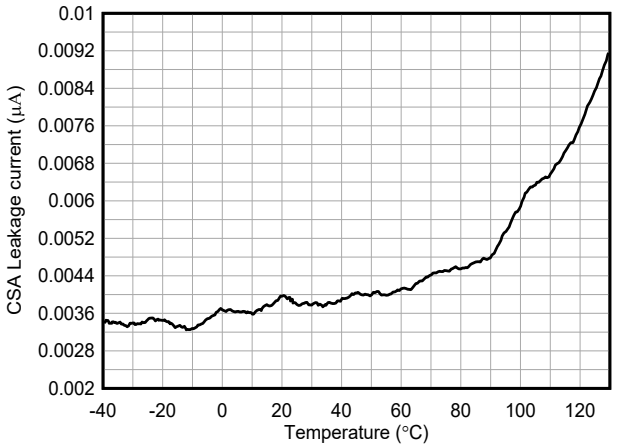


図 6-9. CSA Input Current versus Temperature

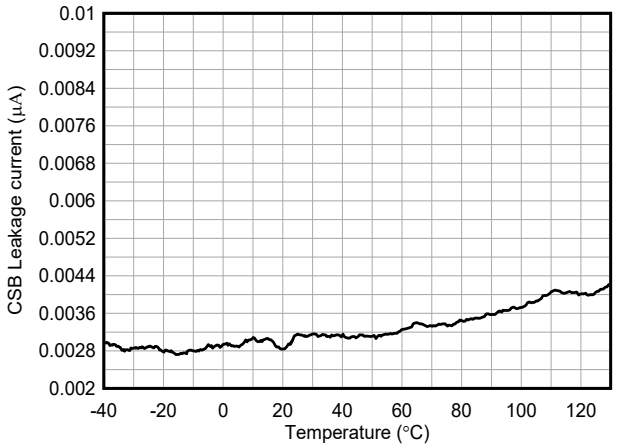


図 6-10. CSB Input Current versus Temperature

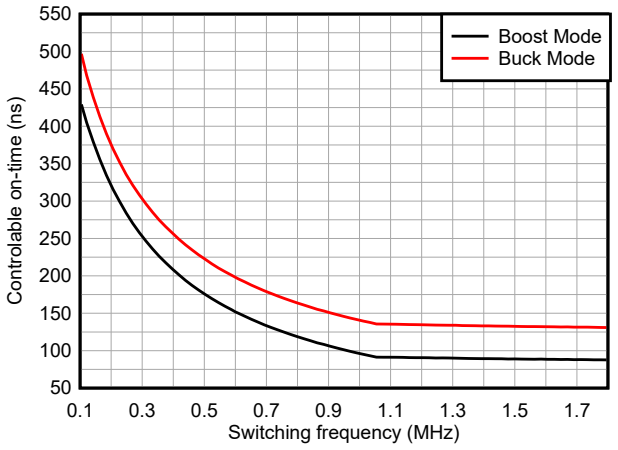


図 6-11. Minimum Controllable On-time versus Switching Frequency

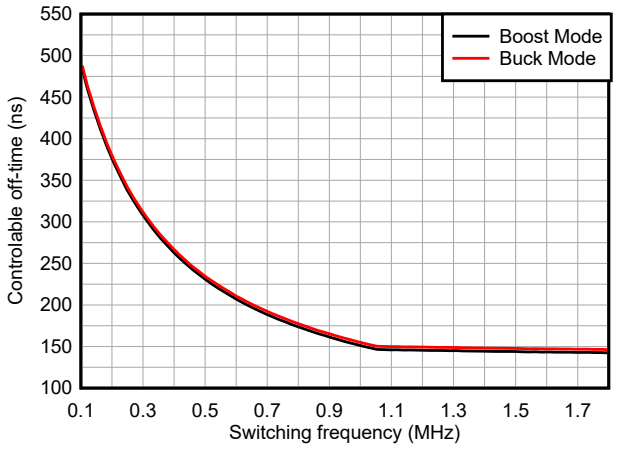


図 6-12. Minimum Controllable Off-time versus Switching Frequency

6.6 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC)}$ = 5V

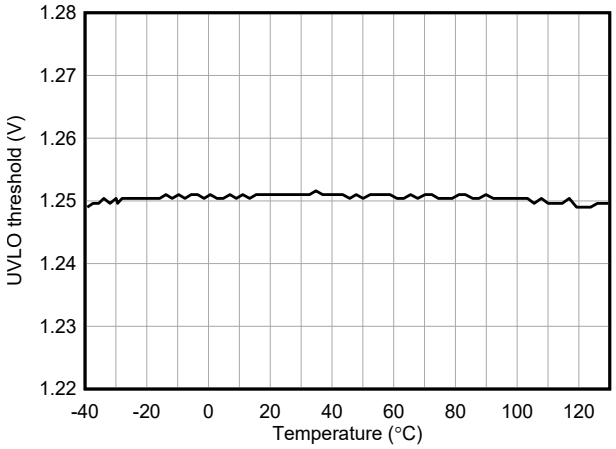


図 6-13. UVLO Threshold Voltage versus Temperature

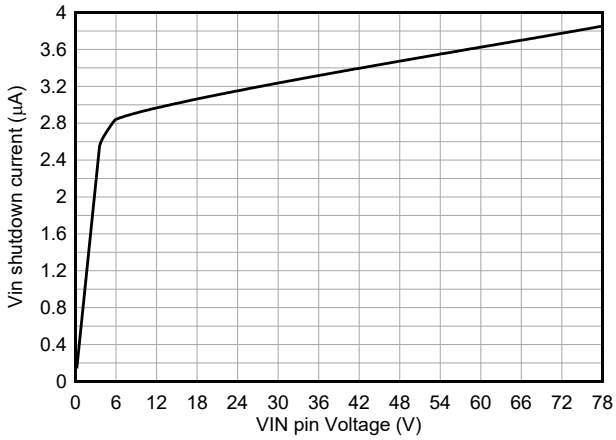


図 6-14. Shutdown Current into VIN versus Pin Voltage
$V_{EN/UVLO}$ = 0 V ,$V_{(VIN)}$ = 12 V, $V_{(BIAS)}$ = 0 V

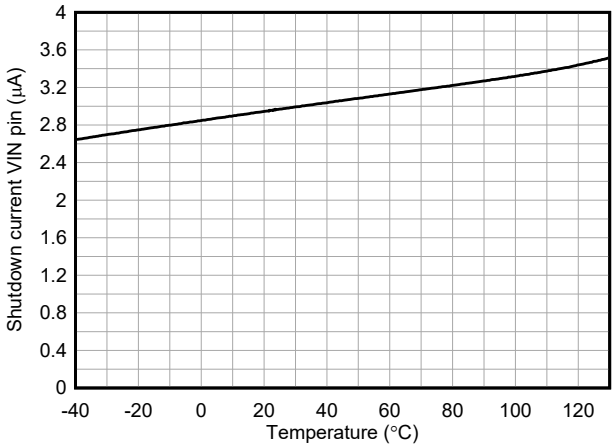


図 6-15. Shutdown Current into VIN versus Temperature
$V_{EN/UVLO}$ = 0V ,$V_{(VIN)}$ = 12V,$V_{(BIAS)}$ = 0V

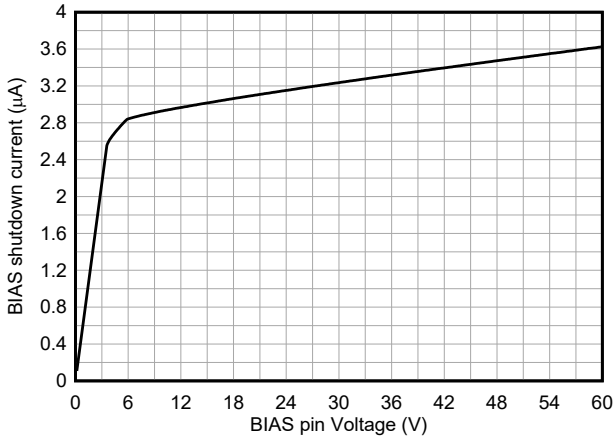


図 6-16. Shutdown Current into BIAS versus Pin Voltage
$V_{EN/UVLO}$ = 0 V ,$V_{(VIN)}$ = 12 V, $V_{(VIN)}$ = 3.5 V

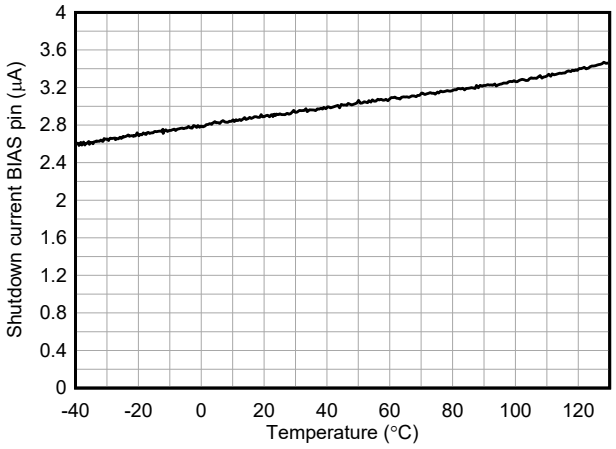


図 6-17. Shutdown Current into VIN versus Temperature
$V_{EN/UVLO}$ = 0 V ,$V_{(BIAS)}$ = 12 V, $V_{(VIN)}$ = 3.5 V

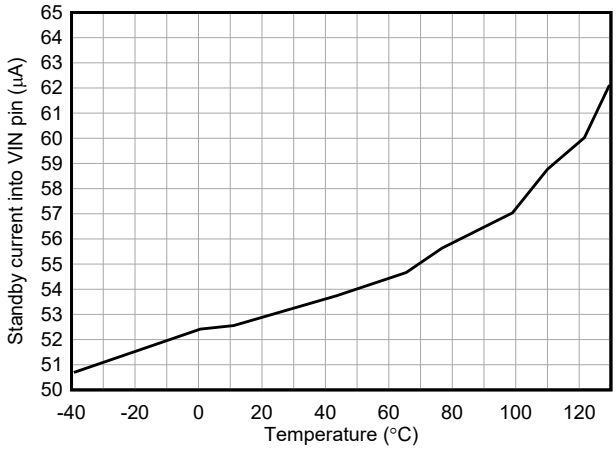


図 6-18. Standby Current into VIN versus Temperature
$V_{EN/UVLO}$ = 0.8 V, $V_{(VIN)}$ = 12 V

6.6 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; $V_{(VCC)}$ = 5V

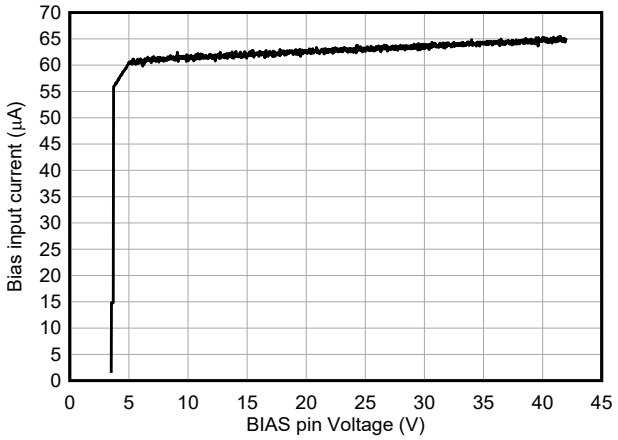


図 6-19. Quiescent Current into BIAS versus Pin Voltage
$V_{EN/UVLO}$ = 3.3 V, $V_{(VIN)}$ = 12 V

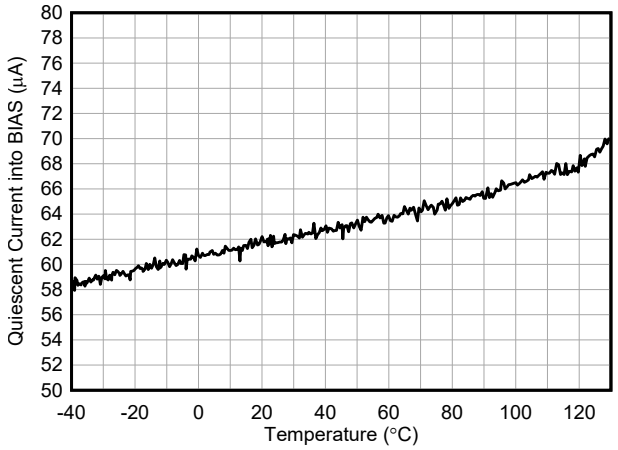


図 6-20. Quiescent Current into BIAS versus Temperature
$V_{EN/UVLO}$ = 3.3 V, $V_{(VIN)}$ = 12 V

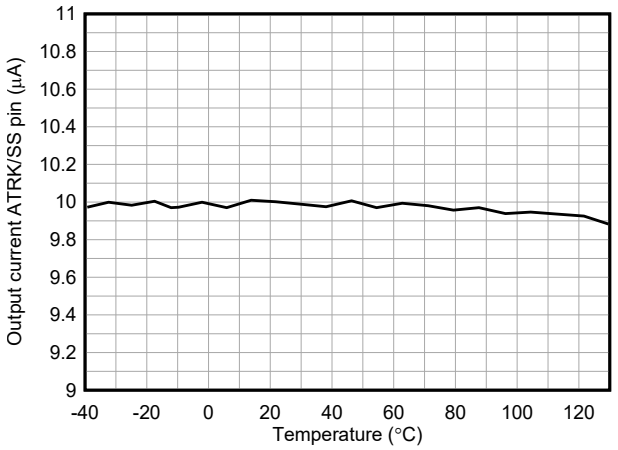


図 6-21. Soft-Start current versus Temperature

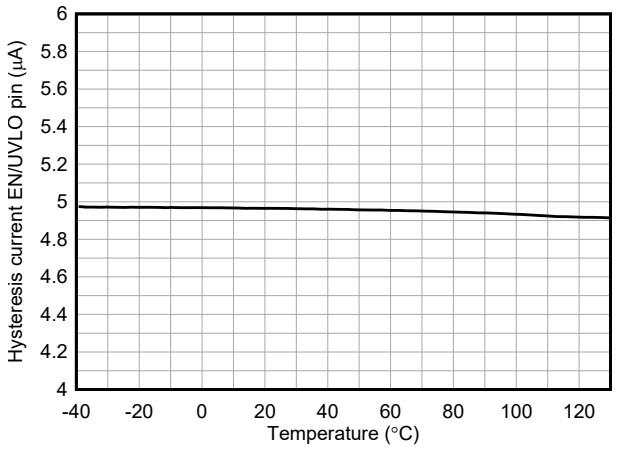


図 6-22. Hysteresis Current on EN/UVLO versus Temperature

7 Parameter Measurement Information

7.1 Gate Driver Rise Time and Fall Time

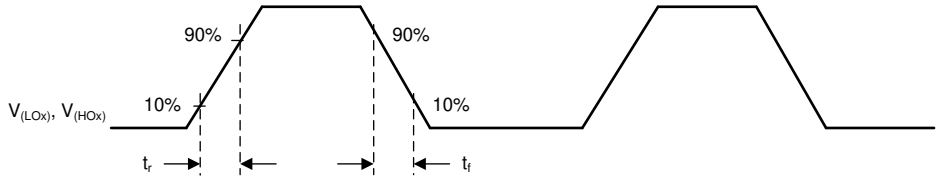


図 7-1. Timing Diagram Gate Driver, t_r, t_f

7.2 Gate Driver Dead (Transition) Time

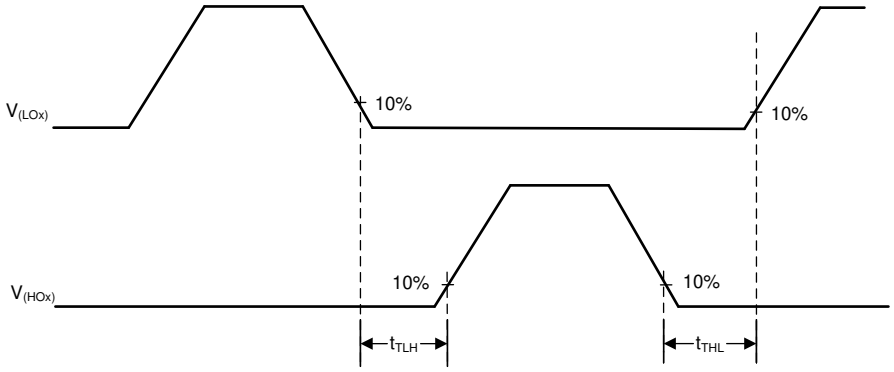


図 7-2. Timing Diagram Gate Driver, t_t

8 Detailed Description

8.1 Overview

The LM51770 is a four switch buck-boost controller. The device provides a regulated output voltage if the input voltage is higher, equal, or lower than the adjusted output voltage.

In power save mode, the LM51770 supports superb efficiency over the full rage of the output current. The operation modes are on-the-fly pin-selectable during operation. The proprietary buck-boost modulation scheme also runs at a fixed switching frequency, which can be set through the RT/SYNC pin. The switching frequency remains constant during buck, boost, and buck-boost operation. The device maintains small mode transition ripple over all operating modes. Through the activation of the dual random spread spectrum operation, EMI mitigation is achievable at any time of the design process.

The integrated and optional average current monitor can help monitor or limit input and output current of the LM51770. This feature also supports charging backup power elements, like batteries with constant current (CC) and constant voltage (CV).

The output voltage of the LM51770 can be dynamically adjusted during operation (dynamic voltage scaling and envelope tracking). The adjustment is either possible by changing the analog reference voltage of the SS/ATRK pin or it can be done directly with a PWM input signal on the DTRK pin.

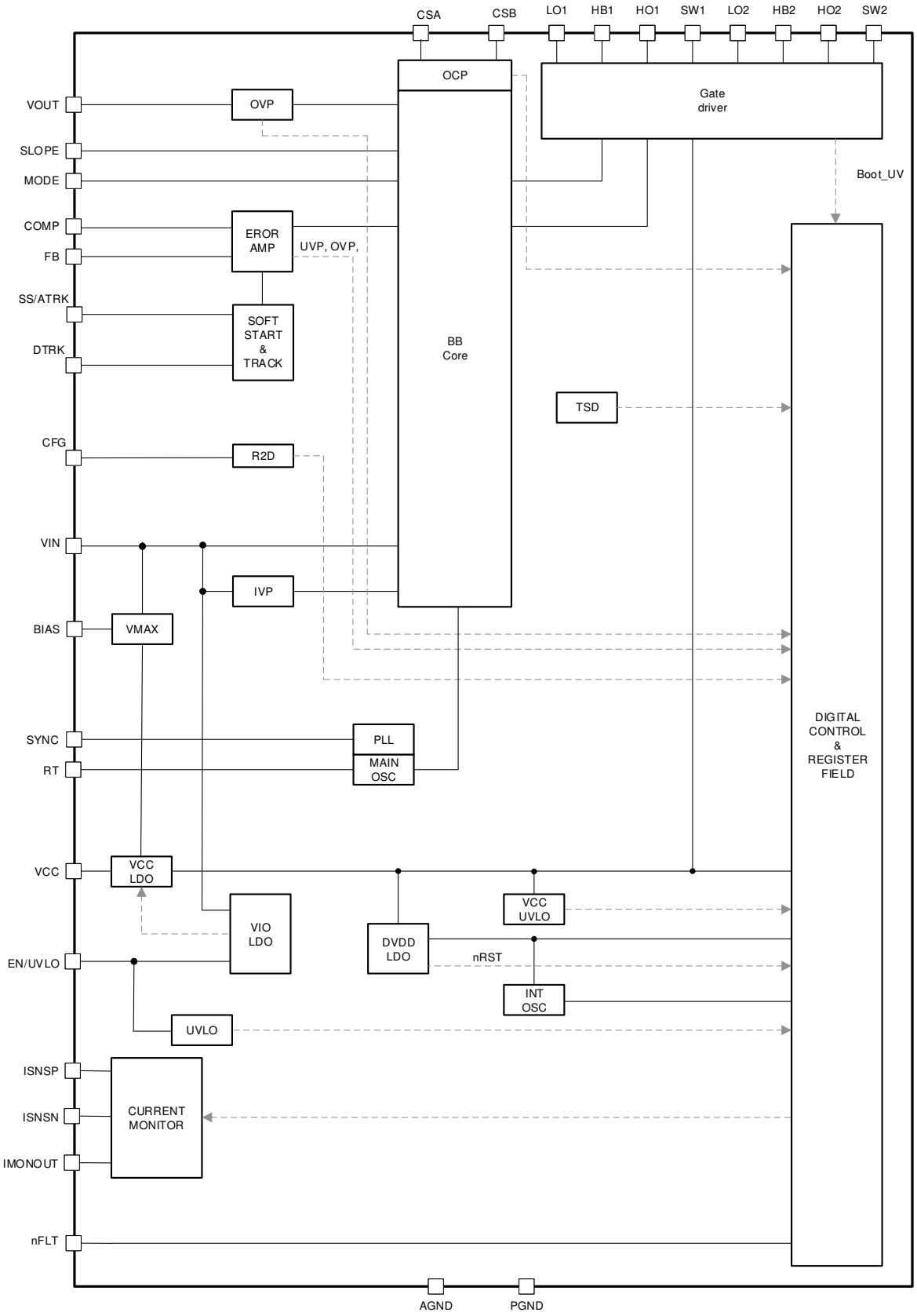
The internal wide input LDOs ensure a robust supply of the device functionality under different input and output voltage conditions. Due to the high drive capability and the automatic and headroom depended voltages selection, the power losses are kept at a minimum at high switching frequency operation. The separate bias pin can be connected to the input, output, or an external supply to further reduce power losses in the device. At all times, the internal supply voltage is monitored to avoid undefined failure handling.

The LM51770 integrates a full bridge N-channel MOSFET driver. The gate driver circuit has a high driving capability to ensure high efficiency targets over the wide range of the supported application. The gate driver features an integrated high voltage low dropout bootstrap diode. The internal bootstrap circuit has a protection against an overvoltage that can be injected by negative spikes and an undervoltage lockout protection to avoid a linear operation of the external power FET. The bootstrap circuit ensures 100% duty cycle operation in pure boost or buck mode.

The resistor-to-digital (R2D) interface offers the user a simple and robust selection of all the device functionality where the analog settings of the soft start minimize the inrush current. Additionally, the control loop and slope compensation ensure a best-in-class output performance for the wide range of supported application cases.

The devices built-in protection features ensure a safe operation under different fault conditions. There is a V_{IN} undervoltage lockout protection to avoid brownout situations. Because the input UVLO threshold and hysteresis can be configured through an external feedback divider, the brownout is avoided under the different designs. The device has an output overvoltage protection and an input overvoltage protection for negative current operation. The selectable hiccup overcurrent protection avoids excessive short circuit currents by using the internal cycle-by-cycle peak current protection. Due to the integrated thermal shutdown, the device is protected against thermal damage caused by an overload condition of the internal VCC regulators. All output-related fault events are monitored and indicated at the open-drain nFLT pin of the device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-On Reset (POR System)

The integrated power-on reset system supplies all internal functional circuits other than the gate drivers and handles the supervision for the internal logic. The low quiescent current design of this block enables an extremely low shutdown current of the whole system. There is a power ORing between the VIN and BIAS pin for the POR system to ensure functionality even under extreme operation conditions, like an output or input short.

Once the voltage on VIN or BIAS rises above the POR threshold, the device logic starts the initialization process and is continuously monitoring the EN/UVLO pin to start or stop the converter operation at the selected UVLO thresholds. The POR-system contains an additional voltage detection for the VIN pin. This block supervises the input voltage and ensures the controllers power stage operation is blocked outside the min. recommended operating input voltage.

8.3.2 Buck-Boost Control Scheme

The LM51770 buck-boost control algorithm makes sure there is a seamless transition between the different operation modes, the fixed frequency operation, and the power stage protection features. The internal state machines controls the flowing three active switching states:

State I: Transistor Q1 and Q3 are conducting. Q2 and Q4 are not conducting (boost mode magnetization state).

State II: Transistor Q1 and Q4 are conducting. Q2 and Q3 are not conducting (boost demagnetization or buck magnetization state).

State III: Transistor Q2 and Q4 are conducting. Q1 and Q3 are not conducting (buck demagnetization state).

Switch	State I	State II	State III
Q1	ON	ON	OFF
Q2	OFF	OFF	ON
Q3	ON	OFF	OFF
Q4	OFF	ON	ON

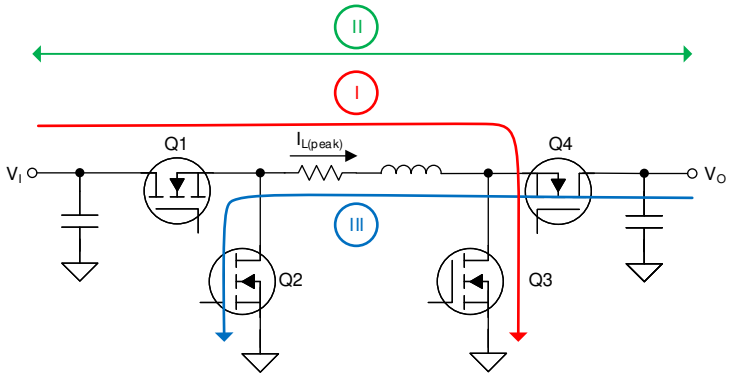


図 8-1. Buck-Boost Active Switching States

8.3.2.1 Boost Mode

In boost mode operation, the converter starts a boost magnetization cycle (switching state I) with the internal clock signal. After it samples the inductor current, the device transitions to switching state II, which is the boost demagnetization state. The maximum duty cycle in boost mode is limited by the minimum boost on time and the selected switching frequency.

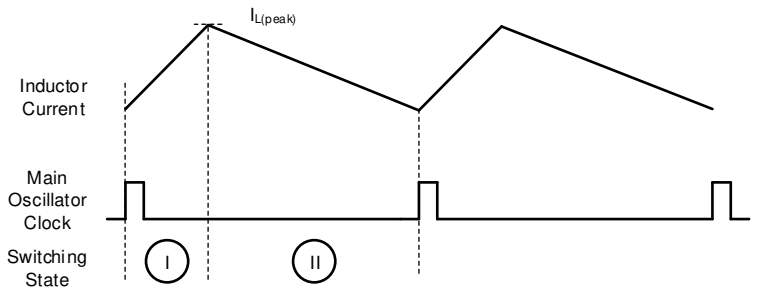


図 8-2. Inductor Current in Continuous Current Boost Operation

8.3.2.2 Buck Mode

In buck mode operation, the converter starts a buck magnetization cycle (state II) with the internal clock signal. When the inductor reaches its peak current, the converter proceeds to the buck demagnetization state III. With the next clock signal, the converter changes back to a buck magnetization cycle and starts a new switching cycle with sampling the peak current. As long as the duty cycle does not reach the minimum off time, the current control remains in buck operating mode.

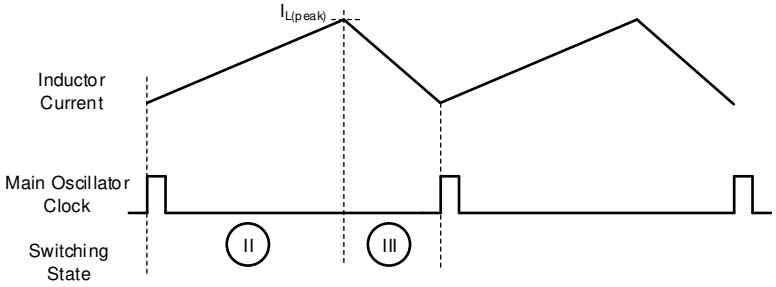


図 8-3. Inductor Current in Continuous Current Buck Operation

8.3.2.3 Buck-Boost Mode

As soon as the on time in boost mode operation is lower then the minimum on time or the off time in buck mode is lower then the minimum off time, the control transits into the buck-boost operation. In the continuous current buck-boost mode, the control adds a boost magnetization (state I) switching cycle before the peak current is reached. Therefore, buck-boost operation mode always consists of all three switching cycles state I, state II, and state III. The peak current detection in this mode happens at the end of switching state I.

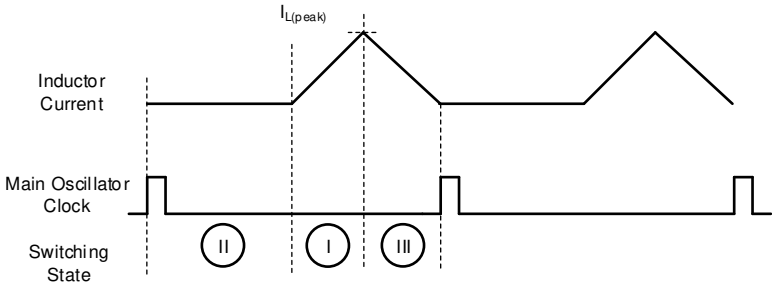


図 8-4. Inductor Current in Continuous Buck-Boost Operation

8.3.3 Power Save Mode

With the MODE pin low, power save mode (PSM) is active. In this operating mode, the switching activity is reduced and efficiency is maximized. If the mode pin is high, power save mode is disabled. The converter then operates in continuous conduction mode (CCM) or forced PWM mode (fPWM).

In PFM boost, buck or in buck-boost mode, the converter is operating down to the minimum defined peak current. If this minimum current (PSM entry threshold) is reached the PWM changes the operation to single pulse. The single pulse operation consists all three states (I, II.III). The duty cycles in single pulse operation are timer based and adopt to the different VIN and VOUT sense voltages. To get a small output voltage ripple the converter modulation scheme uses one or multiply single pulses for the switching activity below the PSM entry threshold.

If the inductor current (load current) further decreases, the frequency of the single pulses are reduced to approximately one quarter of the selected switching frequency. With a further decrease of the inductor (load current) the output voltage increases, as the energy consumed by the load is less than what the converter generates during switching. If the V_O increase the voltage regulation loop detects the increase and turns the device into the sleep mode (uSleep).

In uSleep mode, both low sides are turned on to provide the high-side gate supply for HB1 and HB2 are charged. Other internal circuits are partially turned off to reduce the current consumption of the converter to a minimum possible. In case the output voltage reaches the nominal output voltage set point, the switching activity starts again after a short wake-up time.

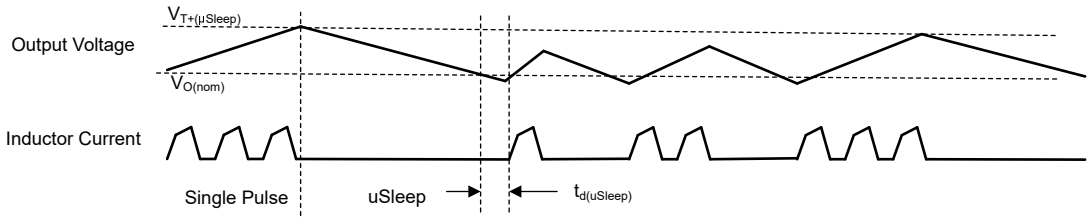


図 8-5. Timing Diagram for the Power Save Mode (uSleep Enabled)

If a signal within the recommended range on the SYNC pin is applied, the device does not enter uSleep mode. This keeps the internal PLL in operation to react fast to load changes when a clock synchronization is used. The pauses between the single pulse remain the same but the quiescent current with a clock synchronization signal is higher than in the normal operation with uSleep.

The PSM - ACM (automated conduction mode) is a high output current power save mode for the 4 switch buck-boost operation. In the buck-boost operation area with loads higher than the PSM entry threshold, switching pulses are skipped and the control enters ACM. Here the device regulation maintains in State II and conducts the input to the output of the power stage. When necessary, the control initiates switching activities with a minimum time of state I or state III to maintain the inductor current as required by the voltage regulation loop. Hence the output voltage is still fully regulated and the device maintains all protection features like the OCP.

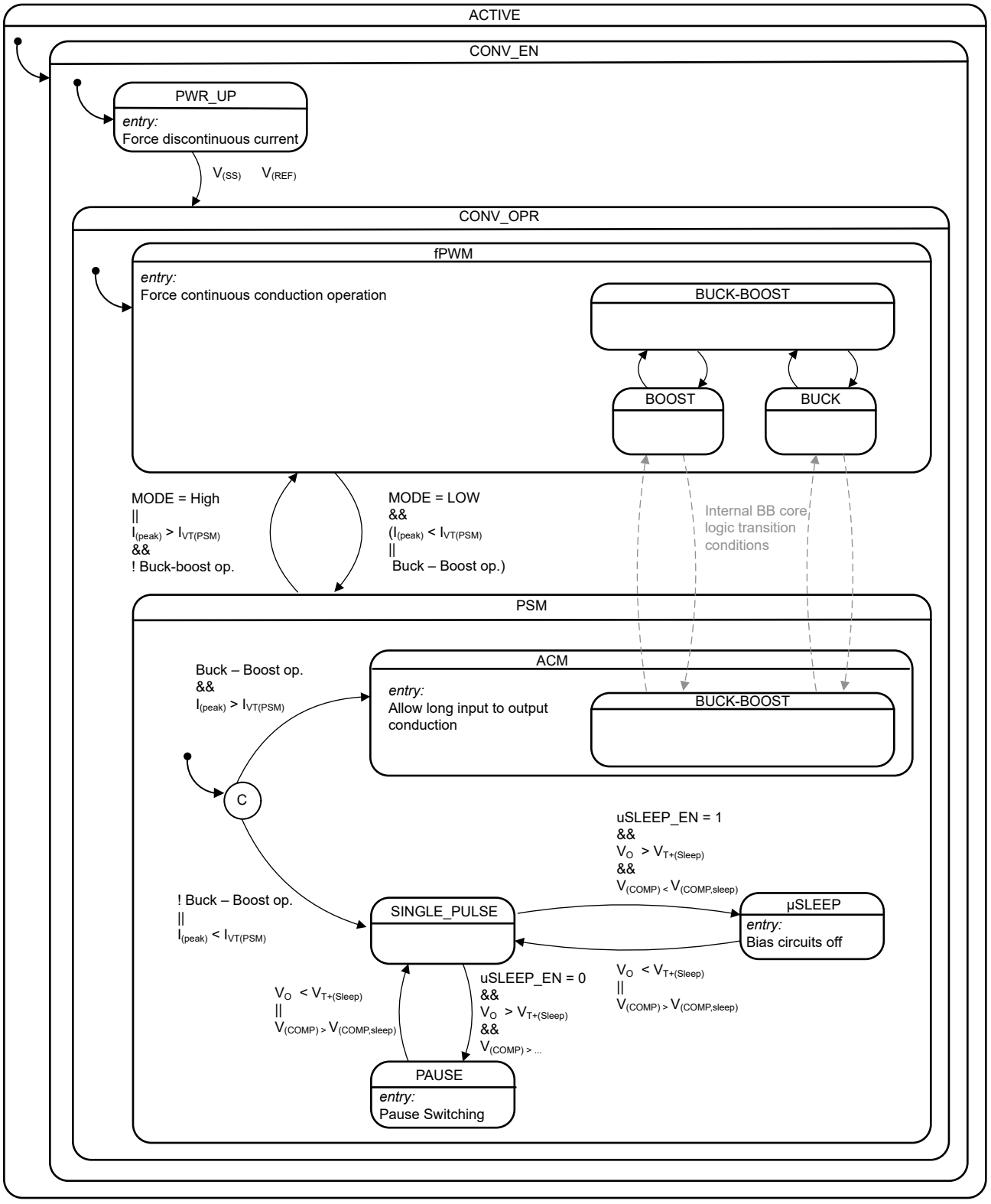


図 8-6. Functional State Diagram for the PSM with default register settings

8.3.4 Supply Voltage Selection – VMAX Switch

There are two pins to supply the internal voltage regulators. Due to the internal supply voltage selection circuit, the device can reduce the power dissipation through a seamless operation at low input or output voltages as well as in transient operating conditions like an output short. The VMAX switch selects the pin with the lower voltage from the VIN or BIAS pin once the voltage on both is above the switch-over threshold ($V_{T(VCC, SUP)}$). If one pin voltage is lower than the threshold, the other supply pin is selected. And if both pins are lower than the switch-over threshold, the higher voltage of VIN or BIAS is selected as supply. The following are common configurations for the supply pins:

- The VIN pin is connected to the supply voltage. The BIAS pin is connected to VO. During start-up, that is as long as the output voltage is not higher than the supply switch-over threshold, the VIN supplies the internal regulators. Once V_O is high enough, the supply current comes from the BIAS pin.
- Both the VIN pin and the BIAS pin are connected together to the input supply voltage. This configuration is often used in applications where the input supply voltage is usually lower or equal than the output voltage. As the BIAS pin is connected to the input voltage, the device has the full current capability of the internal regulators at low input voltages for start-up.
- The VIN is connected to the input supply voltage and the BIAS pin is connected to an auxiliary supply (for example, an existing 12V DC/DC converter). This configuration is commonly used at high voltage applications on the input and output voltages where the power dissipation over the integrated linear regulators must be further minimized.

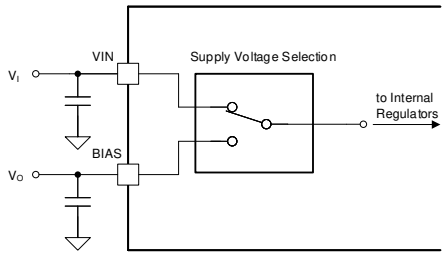


図 8-7. VMAX Supply Scenario 1

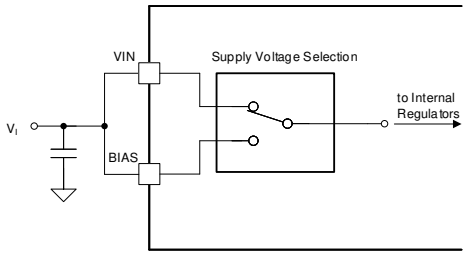


図 8-8. VMAX Supply Scenario 2

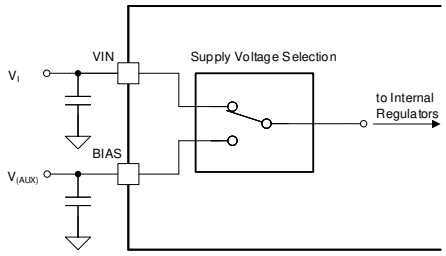


図 8-9. VMAX Supply Scenario 3

8.3.5 Enable and Undervoltage Lockout

The LM51770 has a dual function enable and undervoltage lockout (UVLO) pin. The internal device logic and reference system powers up once the pin voltage is above the $V_{T+(EN)}$ threshold. Once this condition is met, the device is in standby mode. If the EN/UVLO pin voltage is below the $V_{T-(EN)}$ threshold, the device is in shutdown mode to save quiescent current. Find the device operation modes description in セクション 8.4.

The UVLO function of the device can detect an low input voltage condition for the power stage to avoid a brownout condition. The detection threshold as well as the required hysteresis are adjustable with an external voltage divider on the EN/UVLO pin.

If the EN/UVLO pin voltage is above the $V_{T+(EN)}$ threshold, the internal current source for the UVLO hysteresis is active. If the EN/UVLO pin voltage is above the $V_{T+(UVLO)}$ threshold, the internal current source for the UVLO hysteresis is off.

The UVLO features an internal delay time ($t_{d(UVLO)}$) for the shutdown to avoid any undesired converter shutdown due to input noise on the UVLO detection pin. The voltage on the EN/UVLO pin must be below the $V_{T-(UVLO)}$ threshold for the delay time, $t_{d(UVLO)}$. Once these conditions are met, the device logic immediately stops the converter operation.

The UVLO threshold is typically set by a resistor divider from VIN to AGND. The effective turn-on threshold is calculated using 式 1. The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor and the internal hysteresis current.

$$V_{(VIN,IT+,UVLO)} = V_{IT+(UVLO)} \times \left(1 + \frac{R_{UVLO,top}}{R_{UVLO,bot}}\right) + R_{UVLO,top} \times I_{(UVLO,hyst)} \quad (1)$$

where

- $R_{(UVLO,top)}$ is the upper resistor.
- $R_{(UVLO,bot)}$ is the lower resistor in the divider.

8.3.6 Oscillator Frequency Selection

The LM51770 has a low tolerance internal trimmed oscillator. With the RT pin left open, the oscillator frequency is 75 kHz. With the RT pin grounded, the switching frequency is at the maximum of 2.5 MHz. The oscillator frequency can be programmed up or down by connecting a resistor from the RT pin to ground. To calculate the RT resistor for a specific oscillator frequency, use 式 2.

$$R_{(RT)} = \left(\frac{1}{f_{(sw)}} - 20ns\right) \times 30.3\frac{G\Omega}{s} \quad (2)$$

The RT pin is regulated to 0.75 V by an internal voltage source when the device is in active mode. Therefore, the switching frequency can be dynamically changed during operation by changing the current flowing through the resistor. 図 8-10 and 図 8-11 show two examples for changing the frequency by the switching the resistor value or applying a external voltage source through a resistor. It is not recommended to connect any additional capacitance directly to the RT pin.

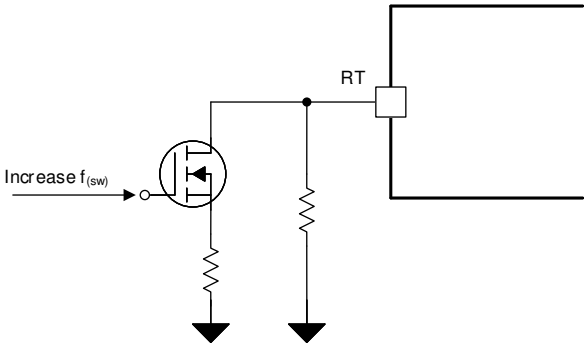


図 8-10. Frequency Hopping Example

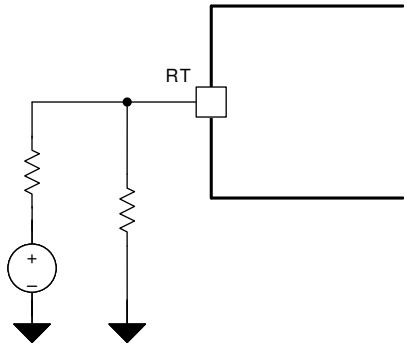


図 8-11. Dynamic Frequency Changing Example

8.3.7 Frequency Synchronization

The device features an internal phase looked loop (PLL), which is designed to transition the switching frequency seamlessly between the frequency set by the RT pin and the external frequency synchronization signal. If no external frequency is provided, the RT pin sets the center frequency of the PLL. The external synchronization signal can change the switching frequency ±50%. To ensure low quiescence current, the input buffer of the SYNC pin is disabled if no valid sync frequency, that is a frequency signal outside the recommended synchronization range is applied.

If a valid synchronization frequency is applied, the device does not enter uSleep during the PSM pause. The internal PLL is kept active to quickly re-syncs to the external synchronization signal in case of a increased load e.g. due to a load step on the output. This behavior improves the transient responds but causes higher quiescent currents for light load operation because the uSleep is disabled if a synchronization signal is provide to the SYNC pin.

The synchronization timings are given in 図 8-13.

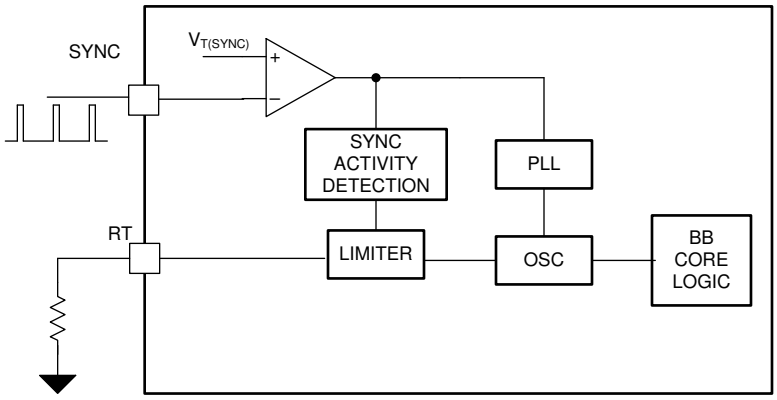


図 8-12. Main Oscillator Functional Block Diagram

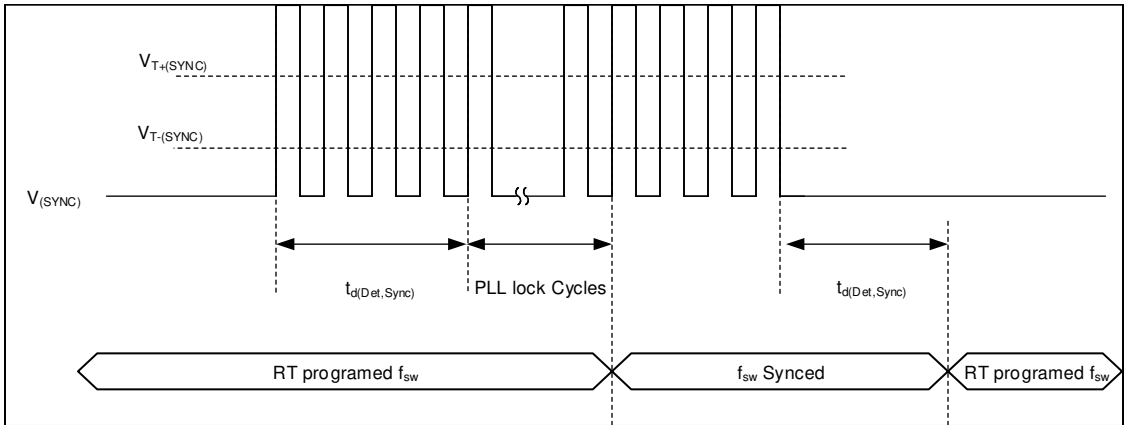


図 8-13. Timing Diagram SYNC Function

The sync pin has a dual function to configure the current limit direction during the initialization phase. If pulled low during this time the negative current limit is selected. Otherwise the positive current limit is selected.

8.3.8 Voltage Regulation Loop

The LM51770 features an internal error amplifier (EA) to regulate the output voltage. The output voltage gets sensed on the FB pin through external resistors, which determine the target or nominal output voltage. The reference for the EA builds the soft-start and analog output voltage tracking pin (SS/ATRK). The COMP pin is the output of the internal gm-stage and gets connected to the external compensation network. The voltage over the compensation network is the nominal value for the inner peak current control loop of the device.

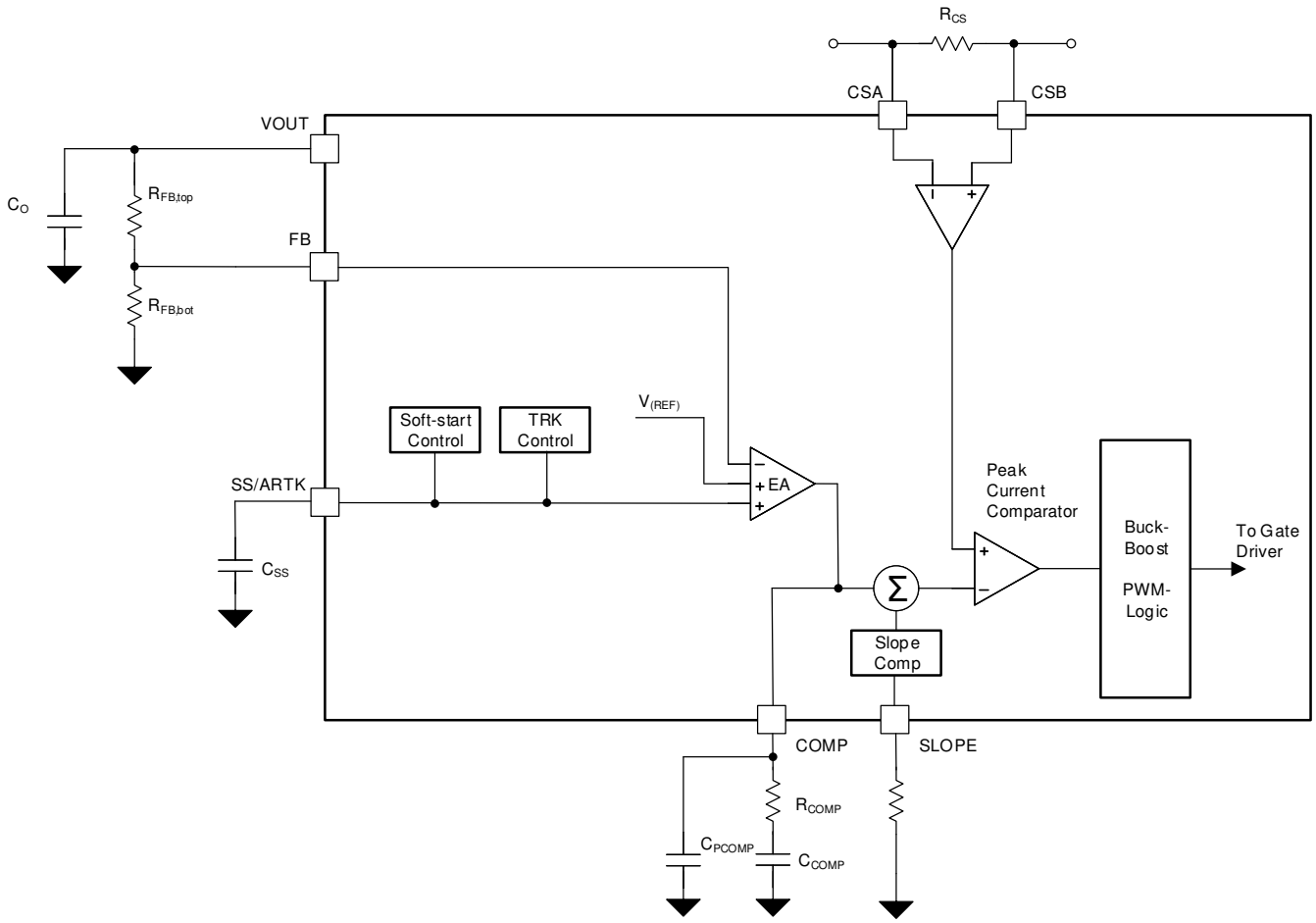


図 8-14. Functional Block Diagram of the Voltage and Peak Current Control Loop

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Use the following equations to calculate the external components:

External Feedback:

$$R_{(COMP)} = \frac{2\pi \times f_{(BW)}}{gm_{(ea)}} \times \frac{R_{(FB,bot)} + R_{(FB,top)}}{R_{(FB,bot)}} \times \frac{10 \times R_{(CS)} \times C_O}{1 - D_{max}} \quad (3)$$

$$C_{(COMP)} = \frac{1}{2\pi \times f_{(CZ)} \times R_{(COMP)}} \quad (4)$$

$$C_{(PCOMP)} = \frac{1}{2\pi \times 10 \times f_{(BW)} \times R_{(COMP)}} \quad (5)$$

For most applications, TI recommends the following guidelines for bandwidth selection of the compensation. The hard limit of the bandwidth ($f_{(BW)}$) is the right half plane zero of the boost operation:

$$f_{RHPZ} = \frac{1}{2\pi} \times \frac{V_{(VOUT)} \times \left(1 - D_{max}\right)^2}{I_{o,max} \times L} \quad (6)$$

The maximum recommended bandwidth must be within the following boundaries:

$$f_{(BW)} < \frac{1}{3} \times f_{RHPZ} \quad (7)$$

$$f_{(BW)} < \frac{1}{10} \times \left(1 - D_{max}\right) \times f_{(SW)} \quad (8)$$

The compensation zero (f_{CZ}) must be placed in relation to the dominating pole of the boost.

$$f_{CZ} = 1.5 \times f_{pole,boost} \quad (9)$$

$$f_{pole,\,boost} = \frac{1}{2\pi} \times \frac{2 \times I_{o,\,max}}{V_{(VOUT)} \times C_o} \quad (10)$$

Due to the precise implementation of the error amplifier, the voltage on the LM51770 COMP pin is accurately reflecting the nominal peak current value of the inductor. 図 8-15 shows the control V/I-characteristics of the error amplifier in FPWM mode. Use this as a guidance for applicative designs where you need to manipulate the inner current loop regulation.

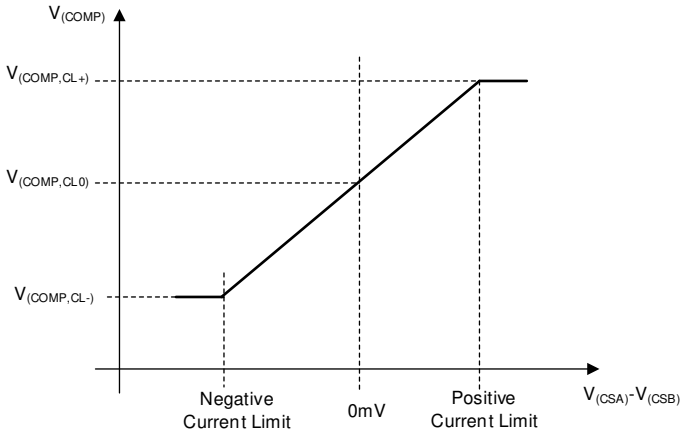

図 8-15. Control Function for the Peak Current Sense Voltage Versus V_{COMP}

8.3.9 Output Voltage Tracking

There are two kinds of output voltage tracking features integrated in the device.

- Analog voltage tracking function through the SS/ATRK pin
- Digital voltage tracking function through the DTRK pin

Analog Voltage Tracking

For the analog output voltage tracking, an external applied voltage overwrites the reference voltage for the output regulation loop. Although it is possible, it is not recommended to apply this voltage before the soft start is finished because the soft-start ramp time and, therefore, the input current during the start-up is changed.

As the internal error amplifier is designed to use the lowest reference input voltage, the applied voltage on the SS/ATRK pin is only effective for voltages lower than the V_{ref} of the feedback pin. Hence, the maximum voltage for the output is determined by the resistor network on the FB pin.

If the analog voltage tracking is used to start-up the converter voltage a change at the MODE pin from high to low or low to high will indicate the logic that the soft-start is completed.

Digital Voltage Tracking

The DTRK input of the LM51770 directly modulates the internal reference voltage. This function activates if the voltage on the DTRK pin is higher than the rising threshold of $V_{T(DTRK)}$ and a PWM signal in the recommended frequency is applied to the pin.

The maximum output voltage during digital tracking cannot exceed the nominal reference voltage for the FB resistor divider. The applied PWM signal reduces the internal reference voltage in relation with the duty cycle on the DTRK pin. A small duty cycle means less output voltage and a high duty cycle of the PWM input represents a high output voltage. For example, a duty cycle of 30% causes a output voltage of 30% of the selected voltage by the FB divider resistors.

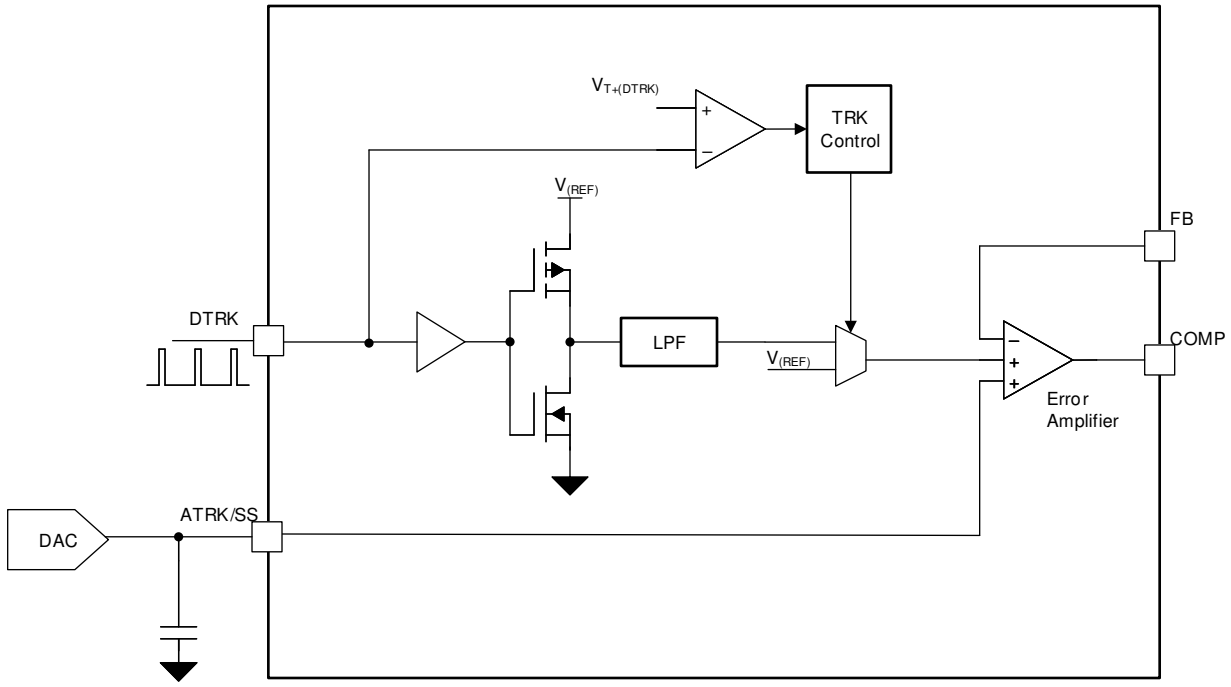

図 8-16. Output Voltage Tracking Functional Block Diagram

8.3.10 Slope Compensation

The provides a slope compensation pin to ensure stable operation and the best transient performance over a wide operating range. According to peak current mode control theory, slope compensation is required at operation with duty cycle greater than 50%. The value for the resistor on the SLOPE pin is calculated with 式 11.

$$R_{(SLOPE)} = \frac{L}{R_{(CS)}} \times 50 \times 10^6 \frac{V}{As} \tag{11}$$

During the design process, consider the following guidelines for the slope compensation:

1. The quotient of peak current sense resistor, $R_{(CS)}$, and the main inductor, L, need to be smaller than the factor given by 式 12.

$$\frac{R_{(CS)}}{L} < \frac{1V \times f_{(sw)}}{V_O \times 10} \tag{12}$$

   where

   - V_O is the maximum output voltage of a system with dynamic voltage changes.

2. The quotient is within the limits given by 式 13.

$$100\ Hz < \frac{R_{(CS)}}{L} < 8000\ Hz \tag{13}$$

8.3.11 Configurable Soft Start

The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

The LM51770 features an adjustable soft start that determines the charging time of the output. The soft-start feature limits inrush current as a result of high output capacitance to avoid an over-current condition.

At the beginning of the soft-start sequence, the SS voltage is 0 V. If the SS pin voltage is below the feedback reference voltage, V_{REF}, the soft-start pin controls the regulated FB voltage and the internal soft-start current source gradually increases the voltage on an external soft-start capacitor connected to the SS pin, resulting in a gradual rise of the output voltage and FB pin. Once the voltage on the SS exceeds the internal reference voltage, the soft-start interval is complete and the error amplifier is referenced to $V_{(REF)}$.

The soft-start time ($t_{(ss)}$) is given by:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{Ref}} \tag{14}$$

The soft-start capacitor is internally discharged when the converter is disabled because of the following:

- EN/UVLO falling below the operating threshold
- VCC falling below the VCC UV threshold
- The device is in hiccup mode current limiting.
- The device is in thermal shutdown.

8.3.12 Peak Current Sensor

The integrated peak current sensor enables a low inductive sensing. The sensor is located in series with the main inductor and can also can monitor the peak inductor current under all operation modes (boost, buck-boost and buck) as well as for both current directions i.e. the bi-directional operation.

As the integrated sensor supports high bandwidth signals a differential mode filter adopted to the selected operating point is recommended for best performance. For most applications we recommend a resistor value for $R_{(DIFF1/2)}$ of 10Ω. You can use the equation below to determine the filter capacitor:

$$C_{(DIFF)} = \frac{t_{on,min}}{2\pi \cdot \left(R_{(DIFF1)} + R_{(DIFF2)}\right) \cdot 10} \tag{15}$$

The differential filter can be set to a 10th of the minimum on-time of Buck or Boost mode.

Current sense resistors consist a parasitic inductance based on geometry and the selected component vendors design. If the desired application requires high currents the impact of the external component parasitic can be reduced by placing multiple sense resistors in parallel.

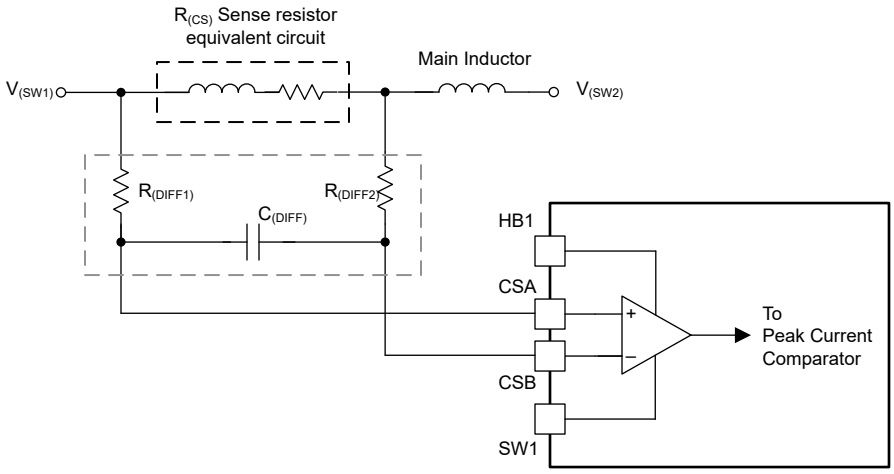

図 8-17. Simplified Schematic of the peak current sensor

8.3.13 Current Monitoring and Current Limit Control Loop

The LM51770 features two high voltage current sensors. The first one maintains the peak current sensing between the CSA and CSB pins. The second current sensor inputs are connected to the ISNSP and ISNSN pins.

This optional current sensing provides the capability to monitor or to limit either the input or the output current of the DC/DC converter If the optional current sense amplifier is not used, the user can disable it to reduce the bias current consumption of the whole device by connecting the IMONOUT pin to VCC. Do not do this dynamical during the operation of the device because the configuration gets latched at start-up of the converter. Use the CFG pin to select one of the following desired operation modes.

Current Monitor Operation:

In case the current sense amplifier is configured as a monitor, the output voltage on the IMONOUT pin is a linear relation between the sense voltage between ISNSP and ISNSN pins and the sense amplifier transcendence as well as the resistor placed on the IMONOUT pin:

$$V_{(IMONOUT)} = \left(V_{(ISNSP)} - V_{(ISNSN)}\right) \times gm \times R_{(IMONOUT)} \quad (16)$$

The output voltage of the IMONOUT pin is clamped to the values given in specifications section.

If the user intends to reduce the bandwidth of the current monitor, the user can place an optional capacitor in parallel to the IMONOUT pin like it is indicated in 図 8-18.

Current Limit Operation:

In this configuration, the current sense gm amplifier monitors the voltage across the sense resistor and compares it with an internal reference voltage. If the drop across the sense resistor is greater than the reference threshold the gm amplifier gradually reduces the peak current capability of the DC/DC converter until the differential voltage is equal the reference voltage. This function of the LM51770 can be used to do the following:

- Regulate the current into the load from the power stage
- Regulate the current from the output into the power stage
- Regulated the current from the input supply to the power stage
- Regulated the current into the device input from the power stage

To select a negative current limit direction, the SYNC pin needs to be pulled low for the time when EN/UVLO goes above the EN rising threshold until the soft-start ramp starts the converter operation. The configuration gets latched and the SYNC pin can be used for the synchronization afterward. If the synchronization function is not used it can be pulled low continuously. For a positive current limit protection the SYNC pin can be pulled high or

connected to a valid synchronization signal during the time when EN/UVLO goes above the EN rising threshold until the soft-start ramp starts the converter operation

Once the current limit operation mode is selected, a RC compensation network must be placed on the IMONOUT pin. For most applications, a compensation bandwidth with a factor of 3× to 5× faster than the compensation of the output voltage loop has given good results.

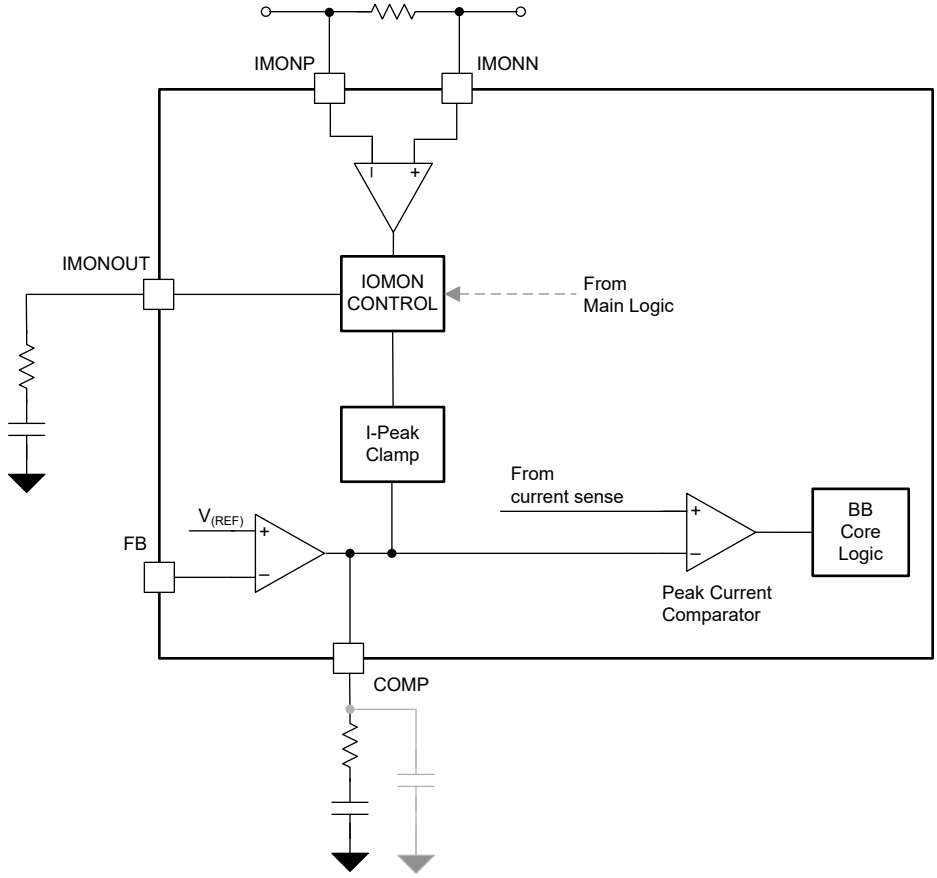

図 8-18. Current Monitor Functional Block Diagram

8.3.14 Short Circuit - Hiccup Protection

The LM51770 features a short circuit protection or over current protection. This protection uses cycle-by-cycle peak current sensor connected to the CSA and CSB-pin. There are two modes for this protection. In hiccup mode, the controller stops the converter operation after detecting cycle-by-cycle peak current longer as the hiccup mode on-time. The converter logic initiates a discharge of the soft-start capacitor and the output stays off until the hiccup mode off-time elapses. Then the logic will exit the hiccup mode and re-start the output with a normal soft-start sequence were the soft-start capacitor is charged with the internal current source. If the short or overload persist the hiccup timer starts again after the soft-ramp finishes. If hiccup mode protection is not enabled, the device will operate in cycle-by-cycle current limiting as long as the overload condition persists.

8.3.15 nFLT Pin and Protections

The open-drain nFLT ouput directly follows the input signals of monitoring features. For instance if the power good flag triggers because the output voltage is falling below the power good threshold the nFLT pins pulls low. After a power-cycle of the device or in case the internal failure signal disappears the nFLT pin will go back to HighZ. The input signals to the nFLT pin are digitally de-glitched. Due to this the maximum reaction time of the FLT pin is given by $t_{d(nFLT-PIN)}$

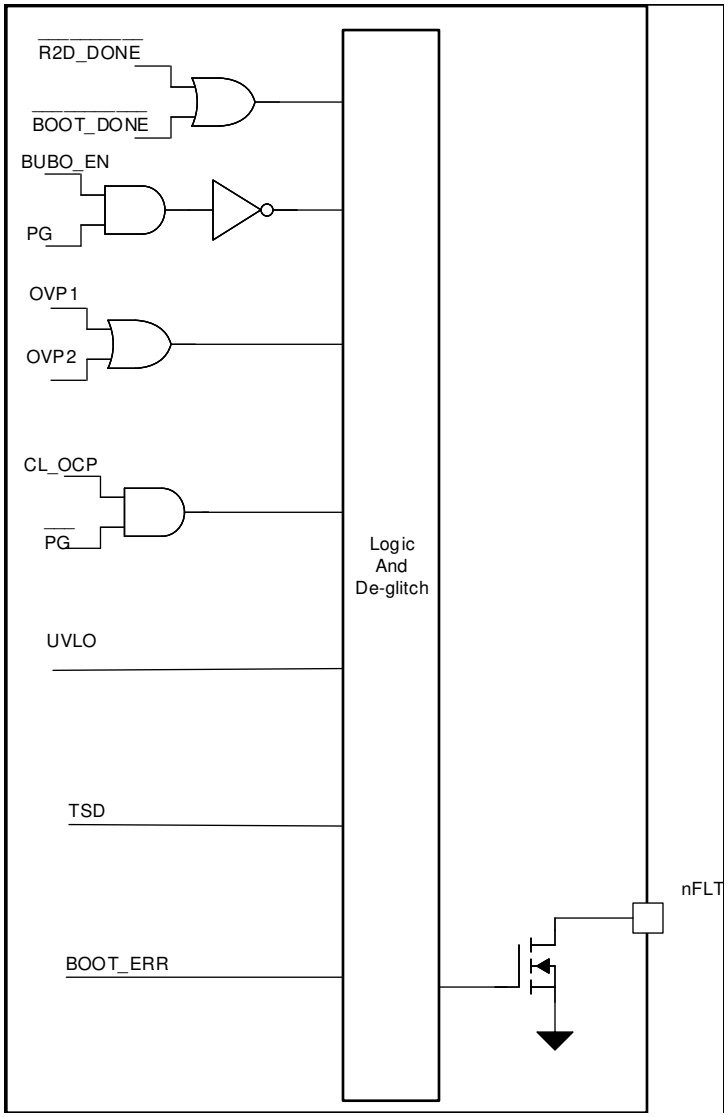

図 8-19. Functional Block Diagram nFLT-pin Logic

Thermal Shutdown (TSD)

To avoid the case of a thermal damage of the device the die temperature of the die is monitored. The device will stop operation once the sensed temperature rises over the thermal shutdown threshold. After the temperature drops below the thermal shutdown hysteresis the TSD signal goes back to normal and the converter will return to normal operation according to the main FSM definition.

Over Current or Short Circuit Protection

The device features a hiccup mode short circuit protection to avoid excessive power dissipation in the die or at the fault of the application in the System. The OCP triggers if the peak current sensing voltage between CSA-pin and CSB-pin is exceeded.

The protection feature will stop and restart the converter operation in case of a short is event is detected.

Output Over Voltage Protection 1 (OVP1)

This over voltage protection monitors the voltage of the FB-pin.

As this threshold is referenced to the $V_{(REF)}$ the OVP1 continues its operation even if of tracking features has changed the V_o target value.

The converter maintains in regulation even the OVP1 threshold triggers.

The OVP1 is disabled during PSM to avoid additional leakage current. The OVP signal gets masked to avoid that a fault is indicated from this signal during the PSM operation.

This protection is disabled during the soft-start procedure.

Output Over Voltage protection 2 (OVP2)

This feature shall avoid any damage to the device in case the external feedback pin is not working properly i.e. is shorted to GND

If the output voltage threshold $V_{T+(OVP2)}$ is reached on the VOUT-pin the buck-boost core logic disables the converter power stage and enters a high impedance state at the switch nodes. If the output voltage falls back under this threshold the convert operation is resumed.

Input Voltage Protection (IVP)

The input over voltage protection is part of the converter core modulation scheme. The IVP avoids any damage to the device in case the current flows from the output to the input and the input source can not sink current e.g. there is a diode in the supply path. If the converter forced PWM mode is active the current can go negative until the sink current limit. Once the input voltage threshold $V_{T+(IVP)}$ is reach on the VIN-pin the protection disables the forced PWM mode and only allows current to flow from VIN to VOUT. After the input voltage drops under the input voltage protection threshold, the fPWM mode activates again.

Power Good

The device features a power good detection. The FB pin voltages gets contentiously monitors. If the sensed voltage drops below the PG falling threshold the signal is pulling low the nFLT pin.

This protection is disabled during the soft-start procedure.

Boot-strap Under Voltage Protection

The high side supply voltage for the gate driver are monitored by an UVLO comparator (BST_UV). This comparator monitors the differential voltage between SWx pin and HBx pin. If the measured voltage drops below $V_{TH-(BST\_UV)}$ the converter stops operation

Boot-strap Over Voltage Clamp

To protect the internal gate driver circuit the external FET gates and the internal circuit features an over voltage clamp. If the voltage goes above $V_{TH(BST\_OV)}$ the linear regulator sinks a current from HBx pin to SWx-pin as long as the voltage is above the threshold.

8.3.16 Device Configuration Pin

The resistor selection on the CFG pin is read and latched during the power-up sequence of the device. The selection cannot be changed until the voltage on the EN or UVLO reaches the falling threshold or VCC voltage drops below the $V_{CCT-(UVLO)}$ threshold. 表 8-1 shows the possible device configurations versus the different resistor values on the CFG pin.

表 8-1. CFG Pin Configuration Overview

#	$R_{(CFG)}$ / kΩ	DRSS	SCP – Hiccup Mode	PSM Entry Threshold	Current Limit
1	0	DISABLED	DISABLED	10%	DISABLED
2	0.511	ENABLED	DISABLED		
3	1.15	DISABLED	ENABLED		
4	1.9	ENABLED	ENABLED		
5	2.7	DISABLED	DISABLED	10%	ENABLED
6	3.8	ENABLED	DISABLED		
7	5.1	DISABLED	ENABLED		
8	6.5	ENABLED	ENABLED		
9	8.3	DISABLED	DISABLED	15%	DISABLED
10	10.5	ENABLED	DISABLED		
11	13.3	DISABLED	ENABLED		
12	16.2	ENABLED	ENABLED		
13	20.5	DISABLED	DISABLED	15%	ENABLED
14	24.9	ENABLED	DISABLED		
15	30.1	DISABLED	ENABLED		
16	36.5	ENABLED	ENABLED		

8.3.17 Dual Random Spread Spectrum – DRSS

The device provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. This function is enabled by the CFG pin. When the spread spectrum is enabled, the internal modulator dithers the internal clock. When an external synchronization clock is applied to the SYNC pin, the internal spread spectrum is disabled. DRSS combines a low frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low frequency triangular modulation improves performance in lower radio frequency bands (for example, AM band), while the high frequency random modulation improves performance in higher radio frequency bands (for example, FM band). In addition, the frequency of the triangular modulation is further modulated randomly to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by spread spectrum, duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled.

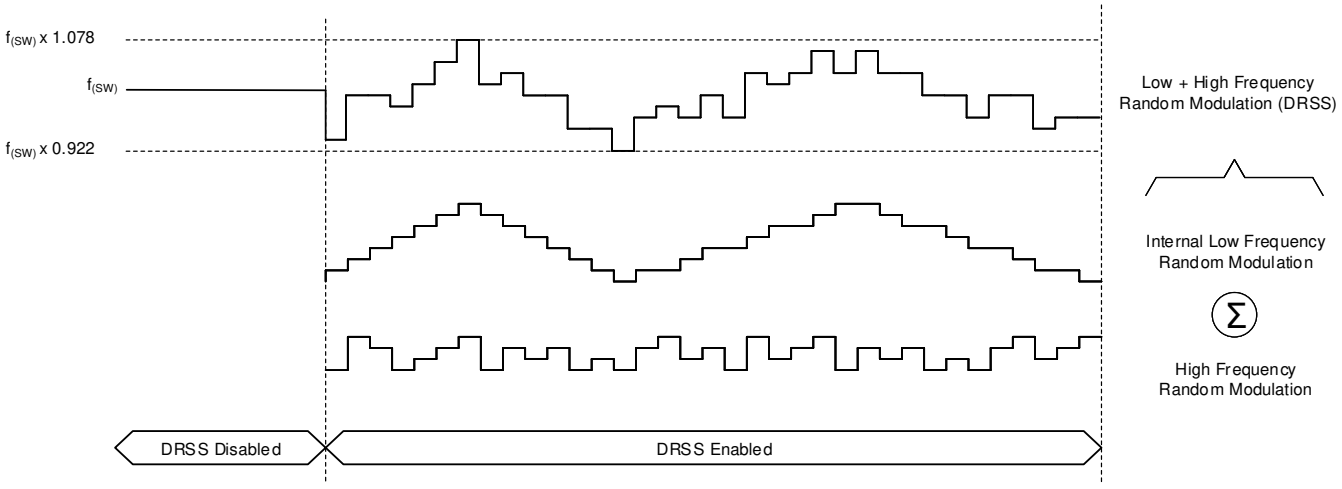

図 8-20. Dual Random Spread Spectrum

8.3.18 Gate Driver

The LM51770 features four internal logic-level nMOS gate drivers. The drivers maintain the high frequency switching of both half bridges needed for a buck-boost operation. If the device is in boost or buck mode, the other half bridge high-side switch needs to be permanent on. The internal gate drivers support this by sharing the current from the other half bridge, which is switching. Therefore, a minimum of quiescent current can be assured as no additional char pump is needed. Due to the high drive current, it can support a wide range of external power FETs as well as a parallel operation of them.

The LO and HO outputs are protected with a shoot-through protection, which ensures that both outputs are not turned on at the same time. If the PWM modulation logic of the buck-boost turns the LOx pin off, the HOx pin is not turned on until the following are all true (AND not OR) true:

1. A minimum internal transition time ($t_{t(dead)}$) is reached.
2. The voltage on the LOx pin drops below the detection threshold $V_{TH(GATEOUT)}$.

This behavior is maintained and vice versa if the HOx pin turns off first.

The high-side supply voltage for the gate driver are monitored by an additional bootstrap UVLO comparator. This comparator monitors the differential voltage between SWx and HBx. If the voltage drops below the threshold the buck-boost converter operation turns off. The device restarts automatically once the positive going threshold is reached with the soft-start scheme.

Additionally, the LM51770 monitors the upper voltage between SWx and HBx. If this voltage exceeds the threshold voltage of the clamping circuit, it activates a internal current source to pull the voltage down.

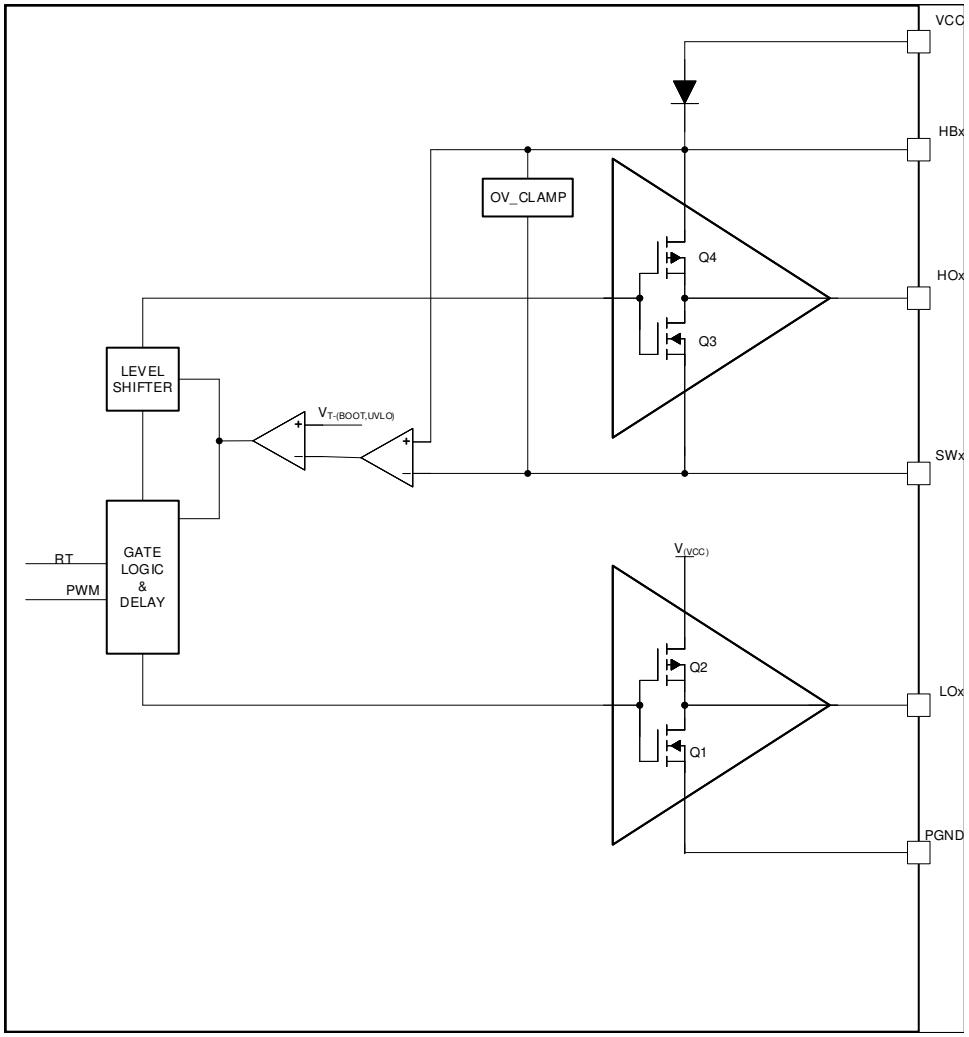

図 8-21. Functional Block Diagram Gate Driver

8.4 Device Functional Modes

図 8-22 describes the functional behavior of the internal device logic.

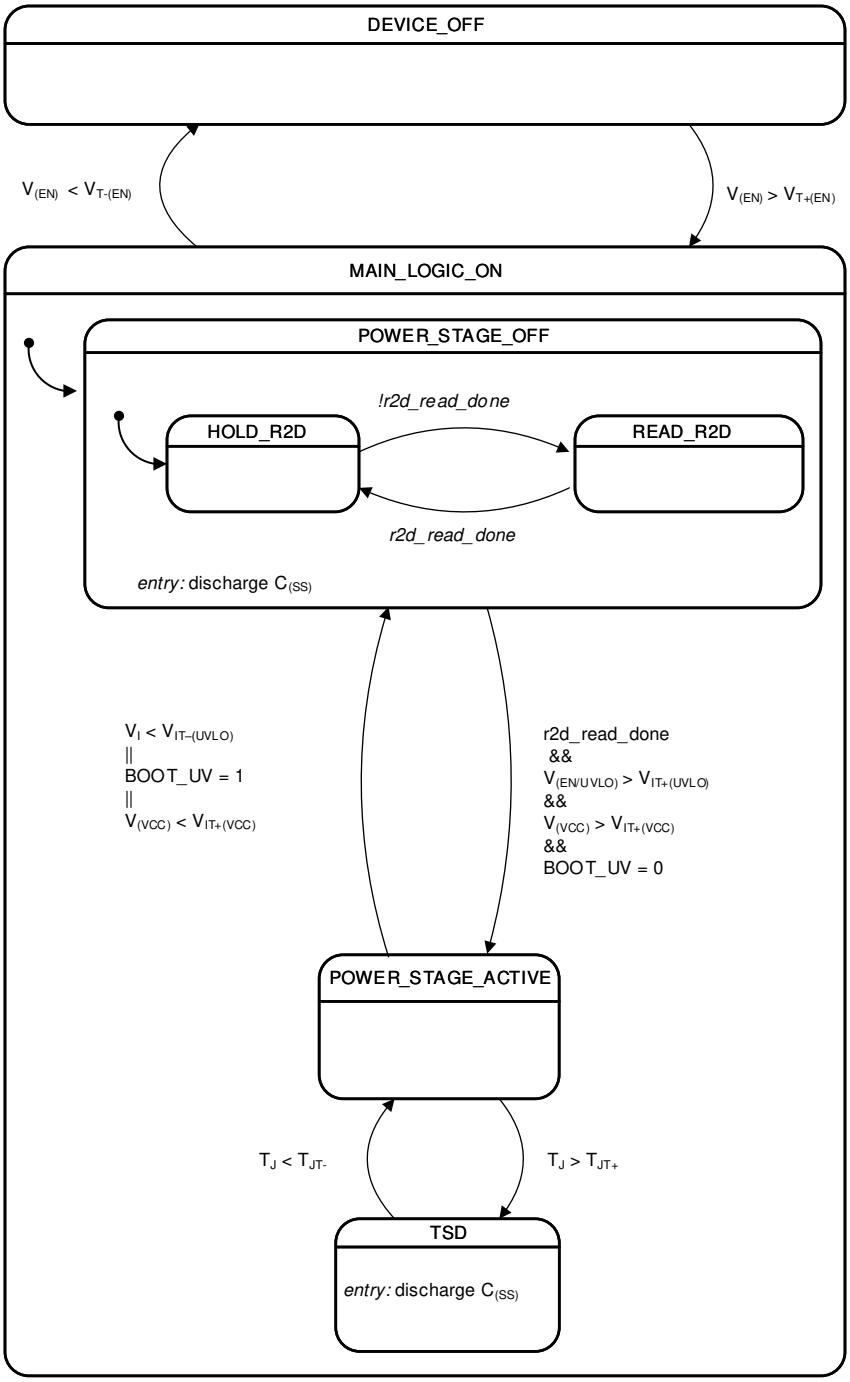

図 8-22. Functional State Diagram

DEVICE_OFF

During the DEVICE_OFF state the LM51770 is in shutdown. All internal logic and the DC/DC converter as well as the gate driver are off. The internal POR- system monitors the EN threshold to start the initialization of the reference system an device logic. The device current consumption is given by the shutdown current.

MAIN_LOGIC_ON

Once the LM51770 transits to the MAIN_LOGIC_ON state it will first stay in the POWER_STAGE_OFF state. Here the necessary checks and preparation for the start up are taken. The current consumption is given by the standby current.

HOLD-R2D

In this state the CFG-pin settings are read and the logic is storing this settings until the next EN -pin cycle.

READ_R2D

During the READ-R2D state the LM51770 executives the reading of the CFG-pin to get the selected settings determined by placed resistor.

POWER_STAGE_ACTIVE

The device executes the soft-start ramp during each entry to this state to avoid excessive inrush currents. In this state the power stage is active and the converter in operation. The current consumption is given by the active quiescent current of the electrical specification table.

TSD

The device enters the TSD-state if the silicon junction temperature exceeds the thermal shutdown limit. It automatically transits back to the POWER_STAGE_ACTIVE -state once the hysteresis of the thermal shutdown triggers.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The LM51770 is a wide input voltage, synchronous, non-inverting buck-boost controller, suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage. To expedite and streamline the process of designing the external circuits and select the components, a comprehensive quickstart calculator is available for download to assist the designer with component selection for a given application.

9.2 Typical Application

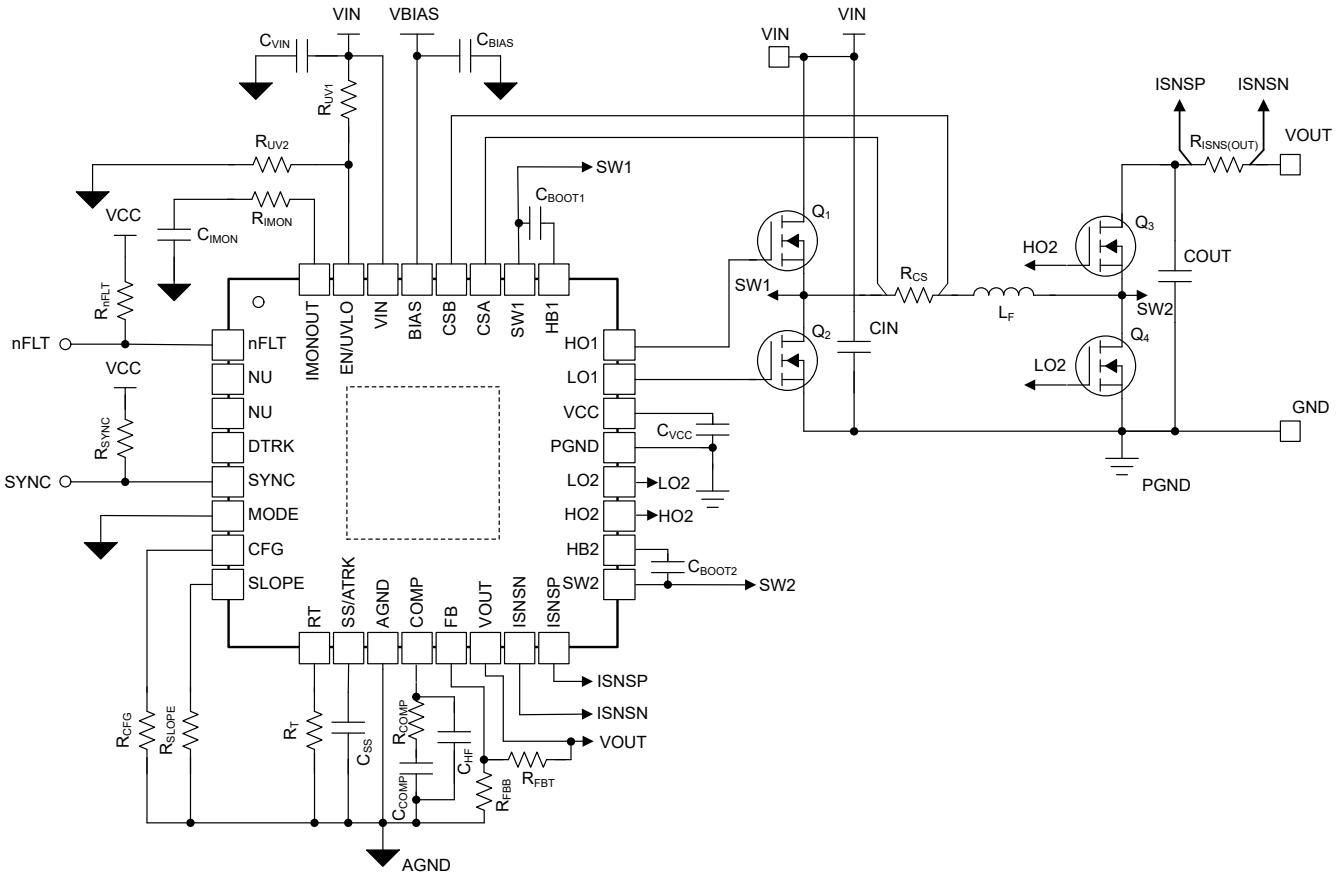

図 9-1. Simplified Schematic of a Typical Application

9.2.1 Detailed Design Procedure

9.2.1.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM51770 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.

3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

9.2.1.2 Frequency

The switching frequency of LM51770 is set by an R_T resistor connected from the RT pin to AGND. The R_T resistor required to set the desired frequency is calculated using 式 17. A 1% standard resistor of 78.7 kΩ is selected for f_{SW} = 400 kHz.

$$R_{(RT)} = \left(\frac{1}{f_{SW}} - 20ns\right) \times 30.3 \frac{G\Omega}{s} \quad (17)$$

9.2.1.3 Feedback Divider

The feedback voltage divider is found with 式 18:

$$R_{FB,top} = \left(V_{(VOUT)} - V_{(REF)}\right) \times R_{FB,bot} \quad (18)$$

For the 16V output, an upper resistor of 71.5kΩ and a lower resistor of 4.7kΩ have been selected.

表 9-1 shows an overview of a possible selection for the feedback divider resistors over common output voltages.

表 9-1. FB Pin Resistor Divider Examples with $R_{FB,top}$ = 71.5kΩ

V_O – Target	$R_{FB,bot}$ – Calculation	$R_{FB,bot}$ – E48 Series	V_O Nominal	Error from FB Resistor
5V	17.9kΩ	17.8kΩ	5.02V	0.3%
9V	8.94kΩ	9.09kΩ	8.87V	–1.5%
12V	6.50kΩ	6.49kΩ	12.02V	0.1%
16V	4.77kΩ	4.87kΩ	15.68V	–2.0%
24V	3.11kΩ	3.16kΩ	23.63V	–1.6%
28V	2.65kΩ	2.61kΩ	28.39V	1.4%
36V	2.04kΩ	2.05kΩ	35.88V	–0.3%
42V	1.74kΩ	1.78kΩ	41.17V	–2.0%
48V	1.5kΩ	1.5kΩ	47.43V	–1.2%
60V	1.2kΩ	1.2kΩ	60.09V	0.2%

9.2.1.4 Inductor and Current Sense Resistor Selection

For boost mode, the inductor selection is based on limiting the peak-to-peak current ripple, ΔI_L, to approximately 20% of the maximum inductor current at the minimum input voltage. The target inductance for boost mode is:

$$L_{BOOST} = \frac{V_{IN(MIN)}^2 \times \left(V_{OUT} - V_{IN(MIN)}\right)}{0.2 \times I_{OUT(MAX)} \times f_{SW} \times V_{OUT}^2} = 2.21\ \mu H \quad (19)$$

For this application, an inductor with 1.8 µH was selected.

When selecting the current sense resistor it needs to be ensured the peak inductor current will not hit the over current limit at maximum output current. For that the peak inductor current needs to be calculated with the sum of the average and ripple current through the inductor.

The maximum peak to peak inductor current occurs at minimum input voltage and is given by:

$$I_{L(PEAK,PEAK)} = \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right) \times \frac{V_{IN(MIN)}}{L \times f_{SW}} = 5.23\ A \tag{20}$$

The average input current at the maximum output current with an estimated efficiency of 95% is calculated by:

$$I_{IN,AVG(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{95\% \times V_{IN(MIN)}} = 22.5\ A \tag{21}$$

For the current sense Resistor a margin of 20% is considered to have enough headroom for the dymamic responses, e.g. load step regulation. To ensure the maximum output current can be delivered the mimium level of the peak current limit threshold is used.

$$R_{CS} = \frac{38.5\ mV}{\left(I_{IN,AVG(MAX)} + \frac{1}{2} I_{L(PEAK,PEAK)}\right) \times 1.2} = 1.28\ m\Omega \tag{22}$$

The standard value of R_{CS} = 1 mΩ with 3 times 3 mΩ is selected. With the 3 resistors in parallel it also reduces the parasitic inductance.

The maximum power dissipation in R_{CS} happens at $V_{IN(MAX)}$:

$$P_{R_{CS(MAX)}} = \left(\frac{58.5\ mV}{R_{CS}}\right)^2 \times R_{CS} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) = 1.90\ W \tag{23}$$

Therefore, for the 3 resistors in parallel a sense resistor with 1-W power rating is sufficient for this application.

A filter network to attenuate noise in the CSA and CSB sense lines should be added. For most applications it is recommended to use a filter resistance R_{DIFF1} and R_{DIFF2} of 10 Ω. The capacitance C_{DIFF} for the filter can be calculated with 式 15. In this configuration 180pF is used.

9.2.1.5 Slope Compensation

For stable current loop operation and to avoid subharmonic oscillations, the slope resistor must be selected based on 式 24:

$$R_{SLOPE} = \frac{L_1}{R_{CS}} \times 50\ \frac{MV}{As} \tag{24}$$

This slope compensation results in “dead-beat” operation, in which the current loop disturbances die out in one switching cycle. Theoretically, a current mode loop is stable with half the “dead-beat” slope (considered already in the calculated slope resistor value in 式 24). A smaller slope resistor results in larger slope signal, which is better for noise immunity in the transition region (V_{IN} is approximately equal to V_{OUT}). A larger slope signal, however, restricts the achievable input voltage range for a given output voltage, switching frequency, and inductor. For this design, R_{SLOPE} = 69.8 kΩ is selected for better transition region behavior while still providing the required V_{IN} range. This selection of slope resistor, inductor, switching frequency, and inductor satisfies guidelines given by 式 12 and 式 13.

9.2.1.6 Output Capacitor

In boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by 式 25 where the minimum V_{IN} corresponds to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \tag{25}$$

In this example, the maximum output ripple RMS current is $I_{COUT(RMS)}$ = 10.3 A. A 2-mΩ output capacitor ESR causes an output ripple voltage of 42.6 mV as given by:

$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(MIN)}} \times ESR \quad (26)$$

A 130-µF output capacitor causes a capacitive ripple voltage of 96 mV as given by:

$$\Delta V_{RIPPLE(COUT)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)}{C_{OUT} \times f_{SW}} \quad (27)$$

Typically, a combination of ceramic and bulk capacitors is needed to provide low ESR and high ripple current capacity. The complete schematic in 図 9-1 shows a good starting point for C_{OUT} for typical applications.

9.2.1.7 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (28)$$

The maximum RMS current occurs at D = 0.5, which gives $I_{CIN(RMS)} = I_{OUT} / 2$ = 4.0 A. A combination of ceramic and bulk capacitors must be used to provide a short path for high di/dt current and to reduce the input voltage ripple. The complete schematic in 図 9-1 shows a good starting point for C_{IN} for typical applications.

9.2.1.8 UVLO Divider

The UVLO resistor divider must be designed for turn-on below 5.5 V. Selecting $R_{UVLO,top}$ = 75 kΩ gives a UVLO hysteresis of 0.375 V based on 式 29. The lower UVLO resistor is selected using:

$$V_{(VIN,\,IT+,\,UVLO)} = V_{IT+(UVLO)} \times \left(1 + \frac{R_{UVLO,top}}{R_{UVLO,bot}}\right) + R_{UVLO,top} \times I_{(UVLO,hyst)} \quad (29)$$

A standard value of 20.5 kΩ is selected for $R_{UVLO,bot}$.

When programming the UVLO threshold for lower input voltage operation, it is important to choose MOSFETs with gate (Miller) plateau voltage lower than the minimum V_{IN}.

9.2.1.9 Soft-Start Capacitor

The soft-start time is programmed using the soft-start capacitor. The relationship between C_{SS} and the soft-start time is given by:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{Ref}} = 18\ nF \quad (30)$$

C_{SS} = 18 nF gives a soft-start time of 1.8 ms.

9.2.1.10 MOSFETs QH1 and QL1

The input side MOSFETs QH1 (Q1) and QL1 (Q2) need to withstand the maximum input voltage of 36 V. In addition, they must withstand the transient spikes at SW1 during switching. Therefore, QH1 and QL1 must be rated for 50 V or higher. The gate plateau voltages of the MOSFETs must be smaller than the minimum input voltage of the converter, otherwise, the MOSFETs may not fully enhance during start-up or overload conditions.

The power loss in QH1 in boost mode is approximated by:

$$P_{COND(QH1)} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,\,On(QH1)} \quad (31)$$

The power loss in QH1 in buck mode consists of both conduction and switching loss components given by 式 32 and 式 33, respectively:

$$P_{COND(QH1)} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,\,On(QH1)} \quad (32)$$

$$P_{SW(QH1)} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW} \quad (33)$$

The rise (t_r) and the fall (t_f) times are based on the MOSFET data sheet information or measured in the lab. Typically, a MOSFET with smaller R_{DSON} (smaller conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QL1 in the buck mode of operation is shown in 式 34:

$$P_{COND(QL1)} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times {I_{OUT}}^2 \times R_{DS,\,On(QL1)} \quad (34)$$

9.2.1.11 MOSFETs QH2 and QL2

The output side MOSFETs QH2 (Q3) and QL2 (Q4) see the output voltage of 16 V and additional transient spikes at SW2 during switching. Therefore, QH2 and QL2 must be rated for 25 V or more. The gate plateau voltages of the MOSFETs must be smaller than the minimum input voltage of the converter, otherwise, the MOSFETs may not fully enhance during start-up or overload conditions.

The power loss in QH2 in buck mode of operation is approximated by:

$$P_{COND(QH2)} = {I_{OUT}}^2 \times R_{DS,\,On(QH2)} \quad (35)$$

The power loss in QL2 in the boost mode of operation consists of both conduction and switching loss components given by 式 36 and 式 37, respectively:

$$P_{COND(QL2)} = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,\,On(QL2)} \quad (36)$$

$$P_{SW(QL2)} = \frac{1}{2} \times V_{OUT} \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right) \times (t_r + t_f) \times f_{SW} \quad (37)$$

The rise (t_r) and the fall (t_f) times can be based on the MOSFET data sheet information or measured in the lab. Typically, a MOSFET with smaller R_{DSON} (lower conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QH2 in the boost mode of operation is shown in 式 38:

$$P_{COND(QH2)} = \frac{V_{IN}}{V_{OUT}} \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS,\,On(QH2)} \quad (38)$$

9.2.1.12 Frequency Compensation

This section presents the control loop compensation design procedure for the LM51770 buck-boost controller. The LM51770 operates mainly in buck or boost modes, separated by a transition region, and therefore, the control loop design is done for both buck and boost operating modes. Then, a final selection of compensation is made based on the mode that is more restrictive from a loop stability point of view. Typically, for a converter designed to go deep into both buck and boost operating regions, the boost compensation design is more restrictive due to the presence of a right half plane zero (RHPZ) in boost mode.

The boost power stage output pole location is given by:

$$f_{p1(boost)} = \frac{1}{2\pi}\left(\frac{2}{R_{OUT} \times C_{OUT}}\right) = 1.22\ kHz \quad (39)$$

where

- R_{OUT} = 2.0 Ω corresponds to the maximum load of 8.0 A.

The boost power stage ESR zero location is given by:

$$f_{z1} = \frac{1}{2\pi}\left(\frac{1}{R_{ESR} \times C_{OUT}}\right) = 61.2\ kHz \quad (40)$$

The boost power stage RHP zero location is given by:

$$f_{RHP} = \frac{1}{2\pi}\left(\frac{R_{OUT} \times (1 - D_{MAX})^2}{L_1}\right) = 24.87\ kHz \quad (41)$$

where

- D_{MAX} is the maximum duty cycle at the minimum V_{IN}.

The buck power stage output pole location is given by:

$$f_{p1(buck)} = \frac{1}{2\pi}\left(\frac{1}{R_{OUT} \times C_{OUT}}\right) = 612\ Hz \quad (42)$$

The buck power stage ESR zero location is the same as the boost power stage ESR zero.

It is clear from 式 43 that RHP zero is the main factor limiting the achievable bandwidth. For a robust design, the crossover frequency must be less than 1/3 of the RHP zero frequency. Given the position of the RHP zero, a reasonable target bandwidth in boost operation is around 5 kHz:

$$f_{bw} = 5\ kHz \quad (43)$$

For some power stages, the boost RHP zero may not be as restrictive, which happens when the boost maximum duty cycle (D_{MAX}) is small, or when a really small inductor is used. In those cases, compare the limits posed by the RHP zero (f_{RHP} / 3) with 1/20 of the switching frequency and use the smaller of the two values as the achievable bandwidth.

The compensation zero can be placed at 1.5 times the boost output pole frequency. Keep in mind that this locates the zero at three times the buck output pole frequency, which results in approximately 30 degrees of phase loss before crossover of the buck loop and 15 degrees of phase loss at intermediate frequencies for the boost loop:

$$f_{ZC} = 1.8\ kHz \quad (44)$$

The compensation gain resistor, R_{c1}, is calculated with:

$$R_{C1} = \frac{2\pi \times f_{bw}}{gm_{EA}} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times \frac{A_{CS} \times R_{CS} \times C_{OUT}}{1 - D_{MAX}} \times \frac{1}{\sqrt{1 + \left(\frac{f_{bw}}{f_{RHP}}\right)^2}} = 1.9\ k\Omega \quad (45)$$

where

- D_{MAX} is the maximum duty cycle at the minimum V_{IN} in boost mode.
- A_{CS} is the current sense amplifier gain.

The compensation capacitor, C_{c1}, is then calculated from:

$$C_{C1} = \frac{1}{2\pi \times f_{ZC} \times R_{c1}} = 45.8\text{nF} \quad (46)$$

The standard values of compensation components are selected to be R_{c1} = 1.91 kΩ and C_{c1} = 47 nF.

A high frequency pole (f_{pc2}) is placed using a capacitor (C_{c2}) in parallel with R_{c1} and C_{c1}. Set the frequency of this pole at seven to ten times of f_{bw} to provide attenuation of switching ripple and noise on COMP while avoiding excessive phase loss at the crossover frequency. For a target f_{pc2} = 6 kHz, C_{c2} is calculated using 式 47:

$$C_{C2} = \frac{1}{2\pi \times f_{pc2} \times R_{c1}} = 1.68\ \text{nF} \quad (47)$$

Select a standard value of 1.8 nF for C_{c2}. These values provide a good starting point for the compensation design. Each design must be tuned in the lab to achieve the desired balance between stability margin across the operating range and transient response time.

9.2.1.13 External Component Selection

表 9-2. Components Example for Typical Application

Reference	Description	Part Number
R_{COMP}	1.91kΩ	
C_{COMP1}	47nF, 50V Ceramic Capacitor	
C_{COMP2}	1.8nF, 50V Ceramic Capacitor	
C_{SS}	18nF, 50V Ceramic Capacitor or 20nF, 80V Ceramic Capacitor	GCM21B5C1H183JA16 or GCM21B5C1K203JA16
$R_{FB,top}$	71.5kΩ	
$R_{FB,bot}$	4.7kΩ	
R_{nFLT}	10kΩ	
$R_{IMONOUT}$	82kΩ	
C_{IN1}	2× 10µF, 50V Ceramic Capacitor	GCM32EC71H106KA03
C_{IN2}	1× 100µF, 63V Aluminum Capacitor	PCR1J101MCL1GS
M_1	N-Channel 40V MOSFET, $R_{DS(on)}$ = 4.3mΩ	SQJ422EP
M_2	N-Channel 40V MOSFET, $R_{DS(on)}$ = 4.3mΩ	SQJ422EP
M_3	N-Channel 40V MOSFET, $R_{DS(on)}$ = 4.3mΩ	SQJ422EP
M_4	N-Channel 40V MOSFET, $R_{DS(on)}$ = 4.3mΩ	SQJ422EP
R_{CS}	1.00mΩ	3xKRL2012E-C-R003-F
L_1	1.8µH, DCR = 3.2mΩ	IHLP-5050FD-A1
C_{OUT1}	5× 10µF, 50V Ceramic Capacitor	GCM32EC71H106KA03
C_{OUT2}	1× 100µF, 63V Aluminum Capacitor	PCR1J101MCL1GS
R_{ISNS}	4mΩ	KRL2012E-C-R004-F
C_{BST1}	0.1µF, 35V Ceramic Capacitor	GRT033R6YA104KE01
C_{BST2}	0.1µF, 35V Ceramic Capacitor	GRT033R6YA104KE01
C_{VCC}	47µF, 6.3V Ceramic Capacitor	GRM188R60J476ME15D
$R_{UVLO,top}$	75kΩ	
$R_{UVLO,bot}$	20.5kΩ	
R_{SLOPE}	69.8kΩ	
R_{CFG}	13.3kΩ	
R_{RT}	75kΩ	

9.2.2 Application Curves

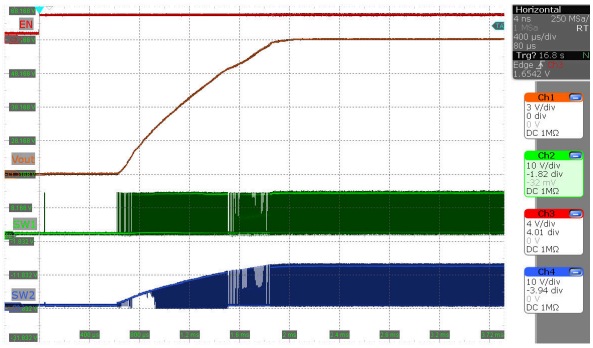

図 9-2. Start-up waveform standby to active operation
(MODE = $V_{(VCC)}$, V_o = 12 V, I_o = 0 A, $V_{(VIN)}$ = 12 V)

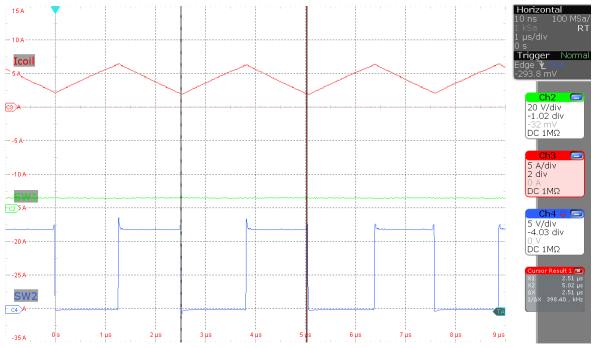

図 9-3. Inductor current boost operation
(MODE = $V_{(VCC)}$, V_o = 12 V, I_o = 0 A, $V_{(VIN)}$ = 6 V)

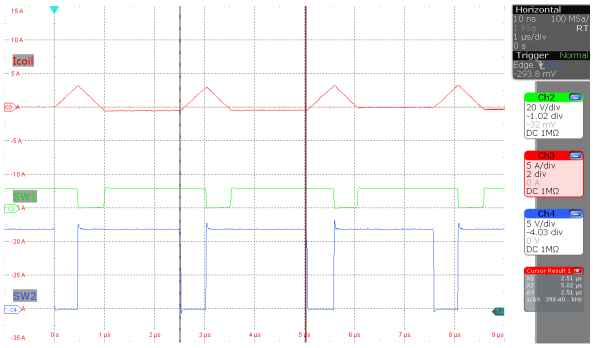

図 9-4. Inductor current buck-boost operation
(MODE = $V_{(VCC)}$, V_o = 12 V, I_o = 0 A, $V_{(VIN)}$ = 12 V)

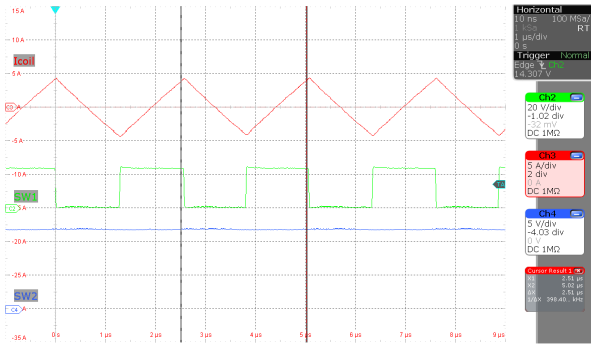

図 9-5. Inductor current buck operation
(MODE = $V_{(VCC)}$, V_o = 12 V, I_o = 0 A, $V_{(VIN)}$ = 24 V)

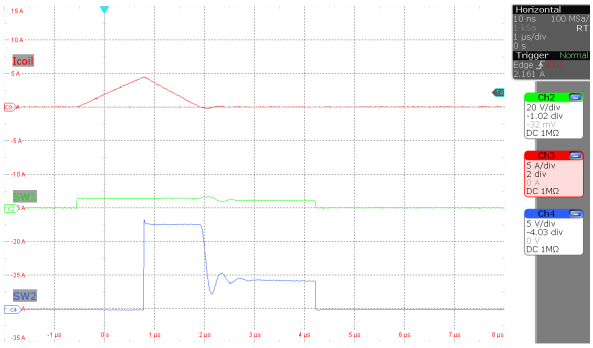

図 9-6. Inductor current boost operation
(MODE = 0 V, V_o = 12 V, I_o = 10 mA, $V_{(VIN)}$ = 6 V)

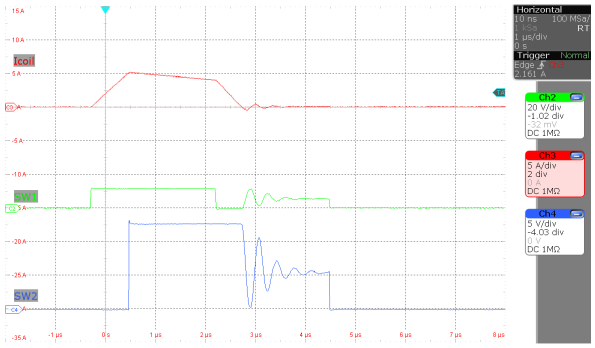

図 9-7. Inductor current buck-boost operation
(MODE = 0 V, V_o = 12 V, I_o = 10 mA, $V_{(VIN)}$ = 12 V)

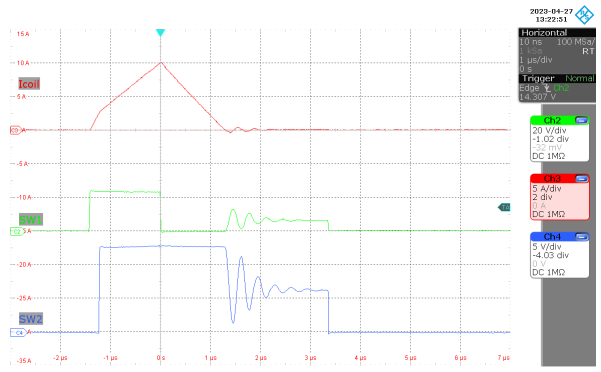

図 9-8. Inductor current buck operation (MODE = 0 V, V_o = 12 V, I_o = 10 mA, $V_{(VIN)}$ = 24 V)

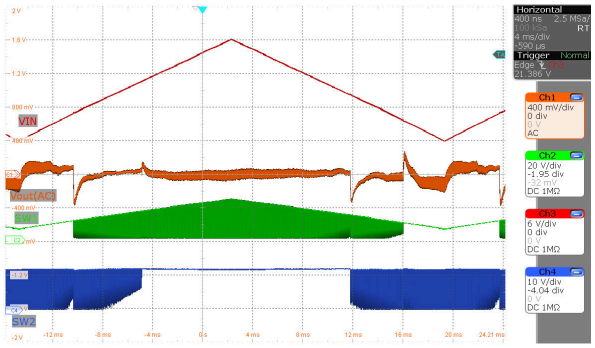

図 9-9. Input voltage ramp from 6V to 24V (MODE = $V_{(VCC)}$, V_o = 12 V, I_o = 6A

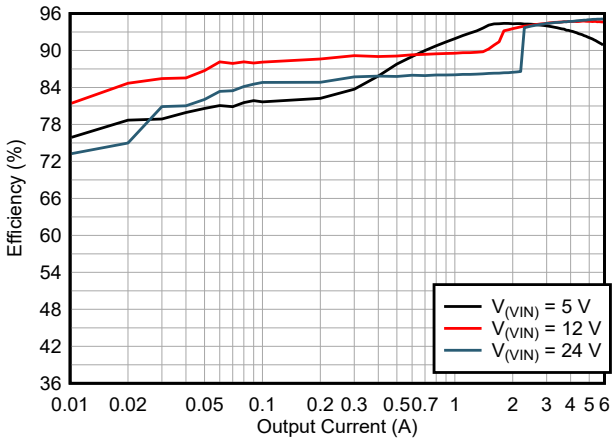

図 9-10. Efficiency Versus I_O (MODE = 0V V_o = 12 V)

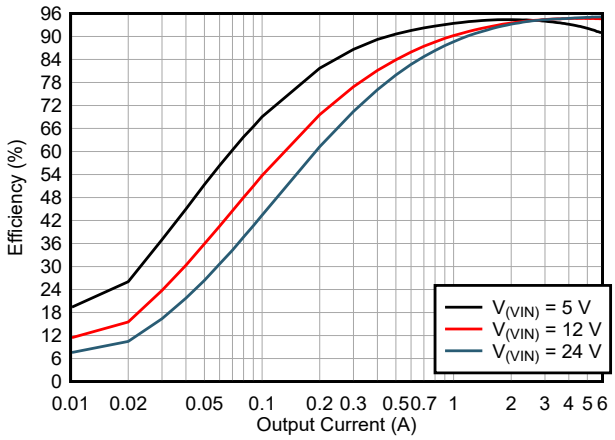

図 9-11. Efficiency Versus I_O (MODE = VCC V_o = 12 V)

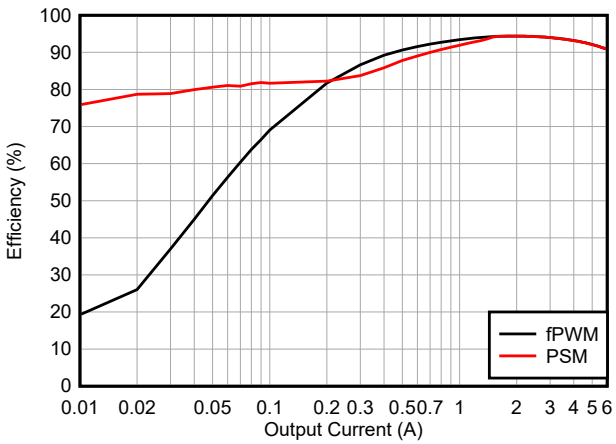

図 9-12. Efficiency Versus I_O in Boost Mode (V_{IN} = 5 V, V_o = 12 V)

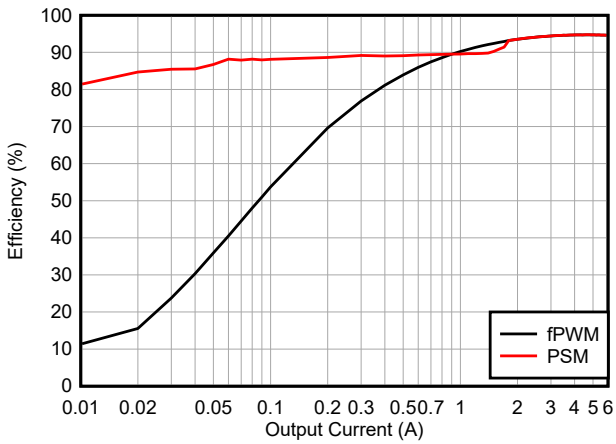

図 9-13. Efficiency Versus I_O in Buck-Boost Mode V_{IN} = 12 V, V_o = 12 V)

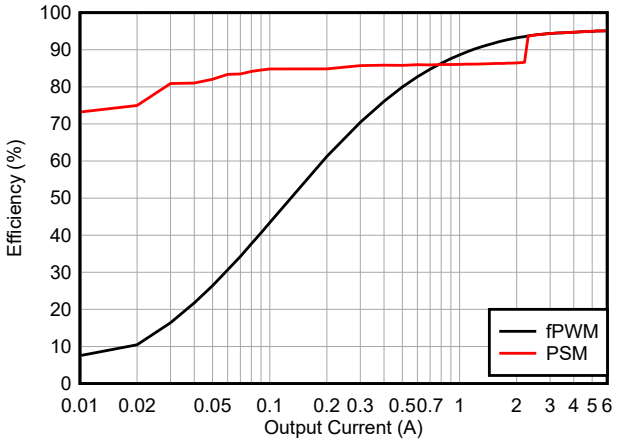

図 9-14. Efficiency Versus I_O in Buck Mode (V_{IN} = 24 V, V_o = 12 V)

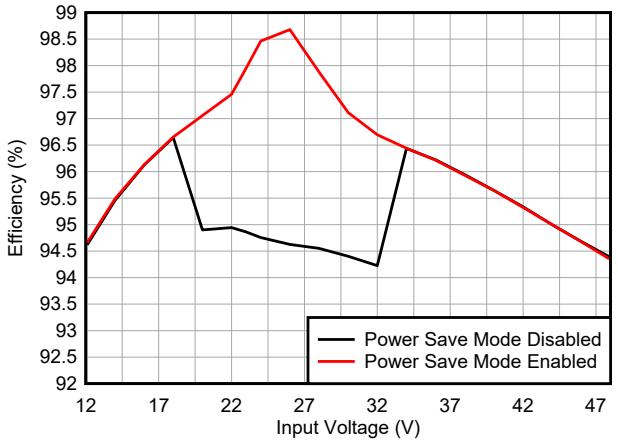

図 9-15. Efficiency Versus V_{IN} (V_o = 24 V, I_O = 5 A)

10 Power Supply Recommendations

The LM51770 is designed to operate over a wide input voltage range. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use 式 48 to estimate the average input current.

$$I_I = \frac{P_O}{V_I \eta} \tag{48}$$

where

- η the efficiency.

One way to get a value for the efficiency is the data from the efficiency graphs in セクション 9.2.2 in the worst case operation mode. For most applications, the boost operation is the region of highest input current.

If the device is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. One way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. An EMI input filter is often used in front of the controller power stage. Unless carefully designed, it can lead to instability as well as some of the previously mentioned affects.

11 Layout

A proper PCB design and layout is important in high-current, fast-switching circuits (with high current and voltage slew rates) to achieve a robust and reliable design. As expected, certain topics must be considered for the design of the PCB layout for the LM51770.

11.1 Layout Guidelines

11.1.1 Power Stage Layout

Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of the buck-boost regulator and are typically placed on the top side of the PCB. The benefits of convective heat transfer are maximized when leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side. Insert at least one inner plane, connected to ground, to shield, and isolate the small-signal traces from noisy power traces.

The DC/DC regulator has several high-current loops. Minimize the area of these loops to suppress generated switching noise and optimize switching performance.

- The most important loop areas to minimize are the path from the input capacitors through the buck high-side and low-side MOSFETs, and back to the ground connection of the input capacitor and the path from the output capacitors through the boost high-side and low-side MOSFETs, and back to the ground connection of the output capacitor. Connect the negative terminal of the capacitor close to the source of the low-side MOSFETs (at ground). Similarly, connect the positive terminal of the capacitor or capacitors close to the drain of the high-side MOSFETs of both loops.
- In addition to these recommendations, follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.

11.1.2 Gate Driver Layout

The LM51770 high-side and low-side gate drivers incorporate short propagation delays, frequency depended dead-time control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the external power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths are not well controlled. Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, and thereby increasing MOSFET switching times.

Connections from the gate driver outputs, HO1 and HO2, to the respective gates of the high-side MOSFETs must be as short as possible to reduce series parasitic inductance. Route HO1 and HO2 and SW1 and SW2 gate traces as a differential pair from the device pin to the high-side MOSFET, taking advantage of flux cancellation by reducing the loop area.

Connections from gate driver outputs, LO1 and LO2, to the respective gates of the low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Route LO1 and LO2, and PGND traces as a differential pair from the device pin to the low-side MOSFET, taking advantage of flux cancellation by reducing the loop area.

Minimize the current loop path from the VCC, HB1, and HB2 pins through their respective capacitors as these provide the high instantaneous current.

11.1.3 Controller Layout

With the provision to locate the controller as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:

- Separate power and signal traces, and use a ground plane to provide noise shielding.
- Place all sensitive analog traces and components related to COMP, FB, SLOPE, SS/ATRK, and RT away from high-voltage switching nodes such as the following to avoid mutual coupling:

  - SW1
  - SW2
  - HO1
  - HO2
  - LO1
  - LO2
  - HB1
  - HB2
- Use an internal layer or layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.
- Route the CSA and CSB and ISNSP and ISNSN traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor.
- Locate the upper and lower feedback resistors close to the FB pins, keeping the FB traces as short as possible. Route the trace from the upper feedback resistor or resistors to the output voltage sense point.
- Use a common ground node for power ground and a different one for analog ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.
- The HTSSOP package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally connected to the substrate (ground) of the device. This connection allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem.

11.2 Layout Example

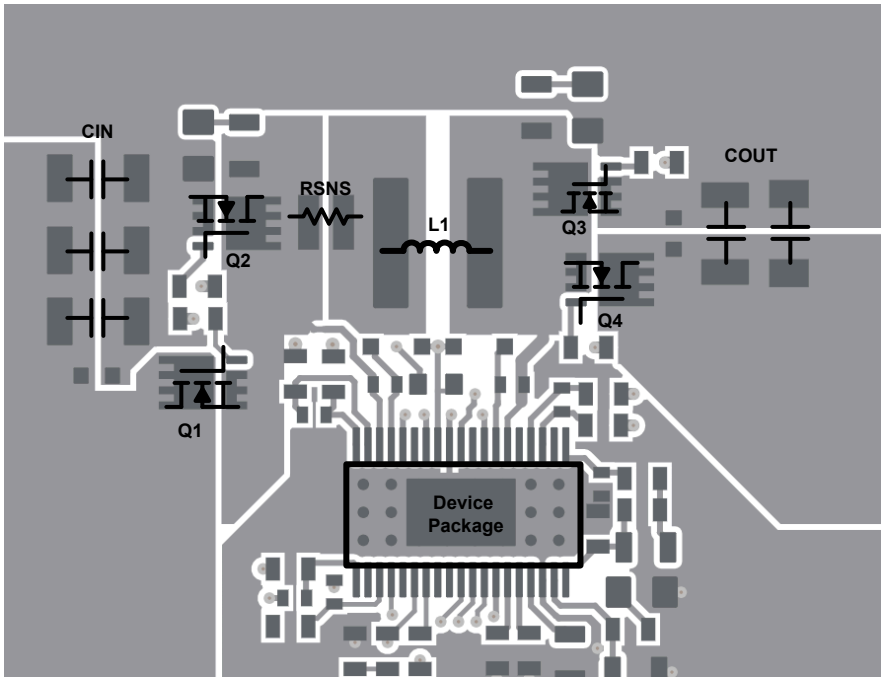

図 11-1. LM51770 Top Layer Routing Example

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Device Support

12.1.1 サード・パーティ製品に関する免責事項

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12.1.2 Development Support

12.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM51770 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

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12.4 Trademarks

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2024	*	Initial Release

14 Mechanical, Packaging, and Orderable Information

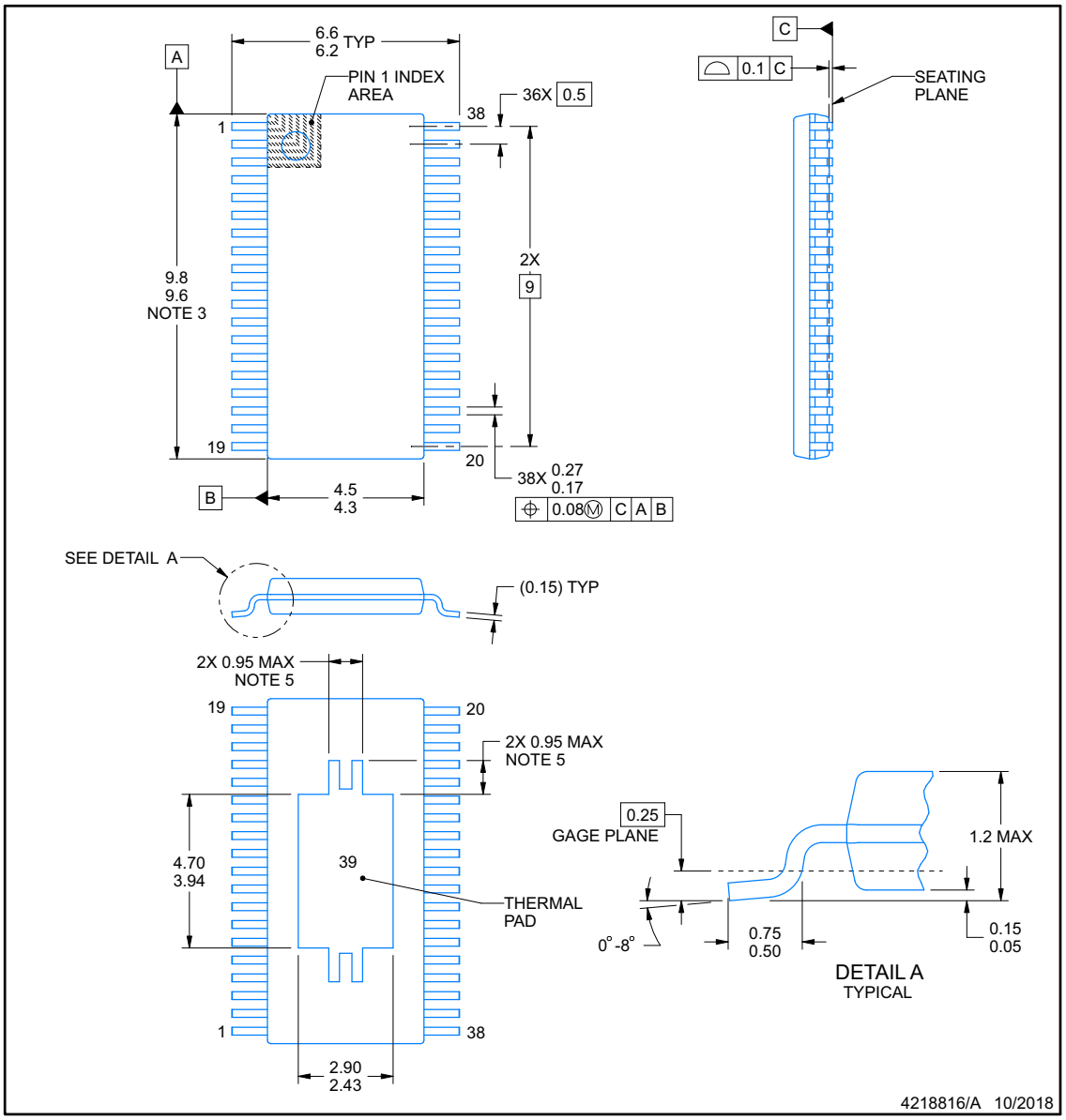
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

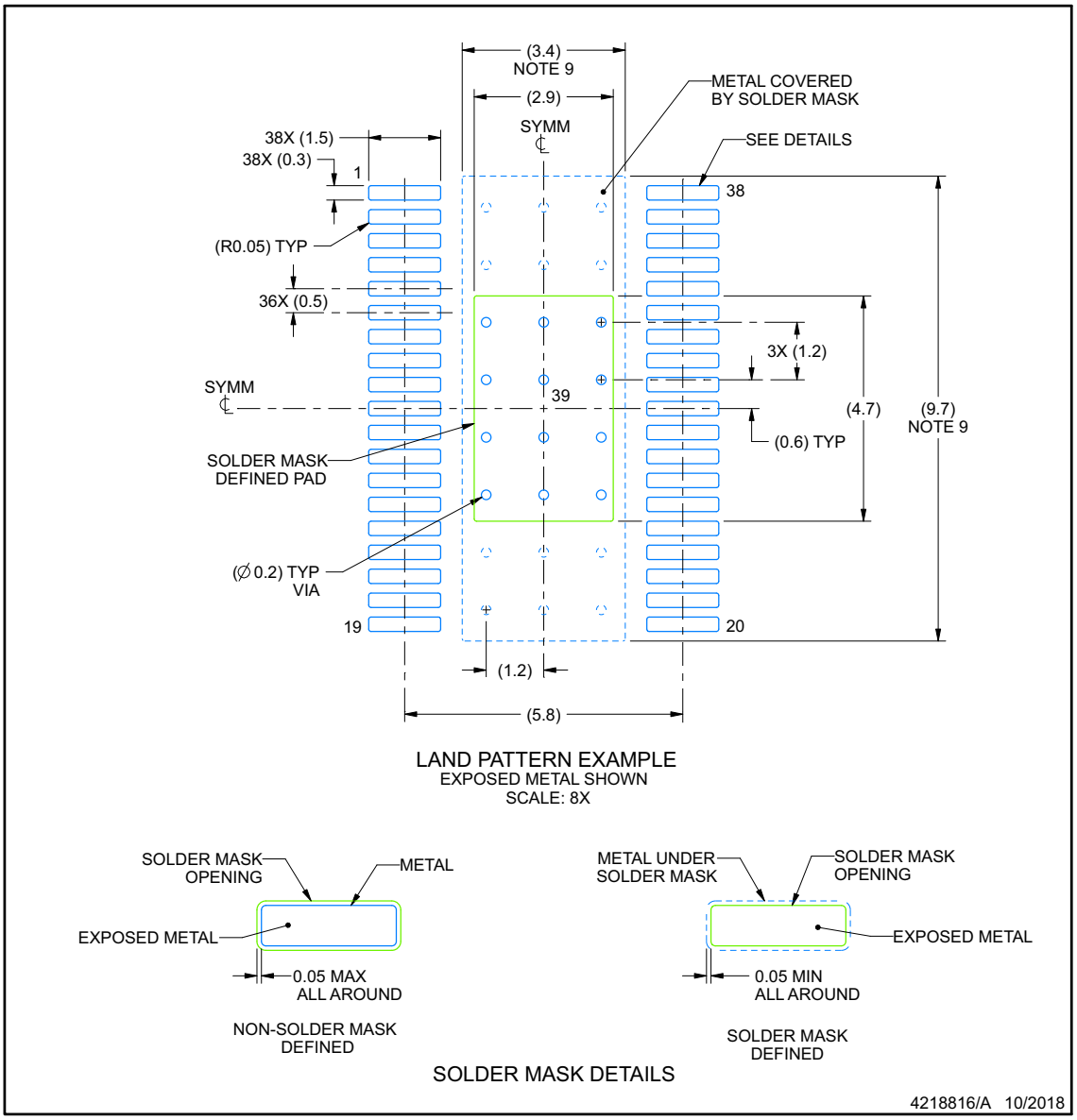
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

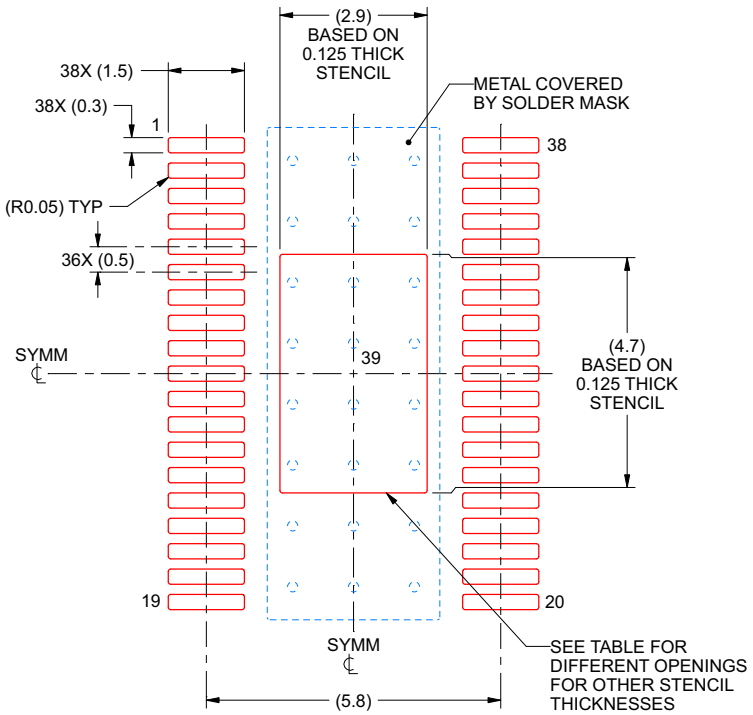
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

4218816/A 10/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM51770DCPR	ACTIVE	HTSSOP	DCP	38	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	LM51770	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

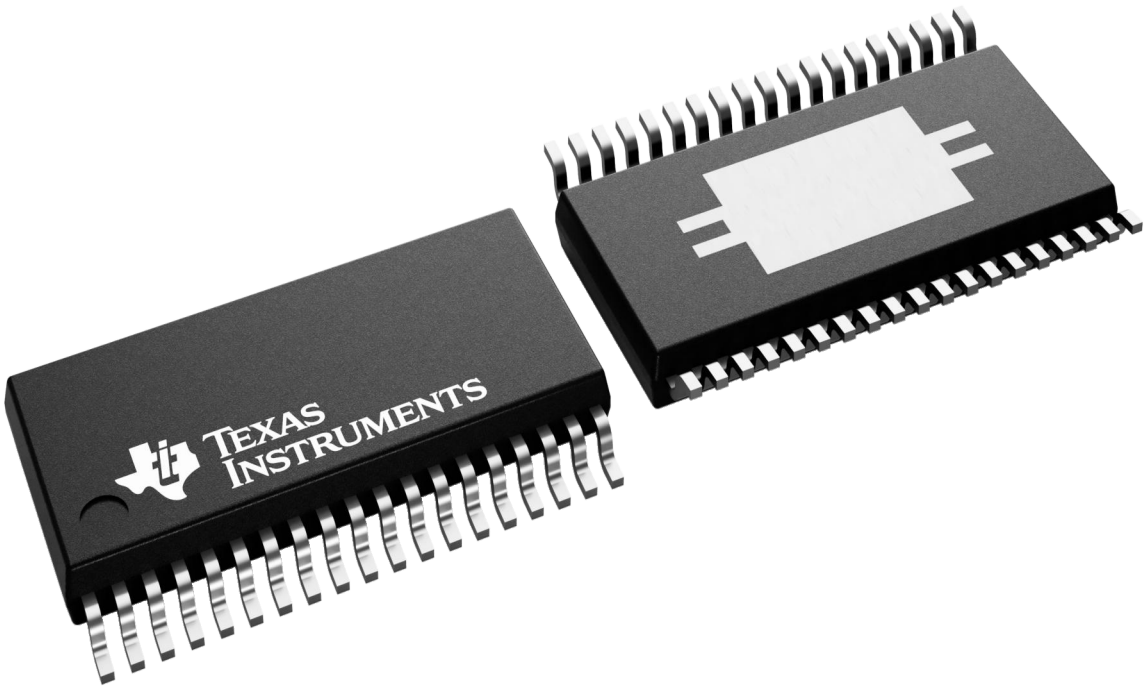
DCP 38

PowerPAD TSSOP - 1.2 mm max height

4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

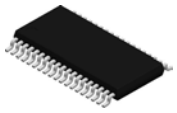
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224560/B

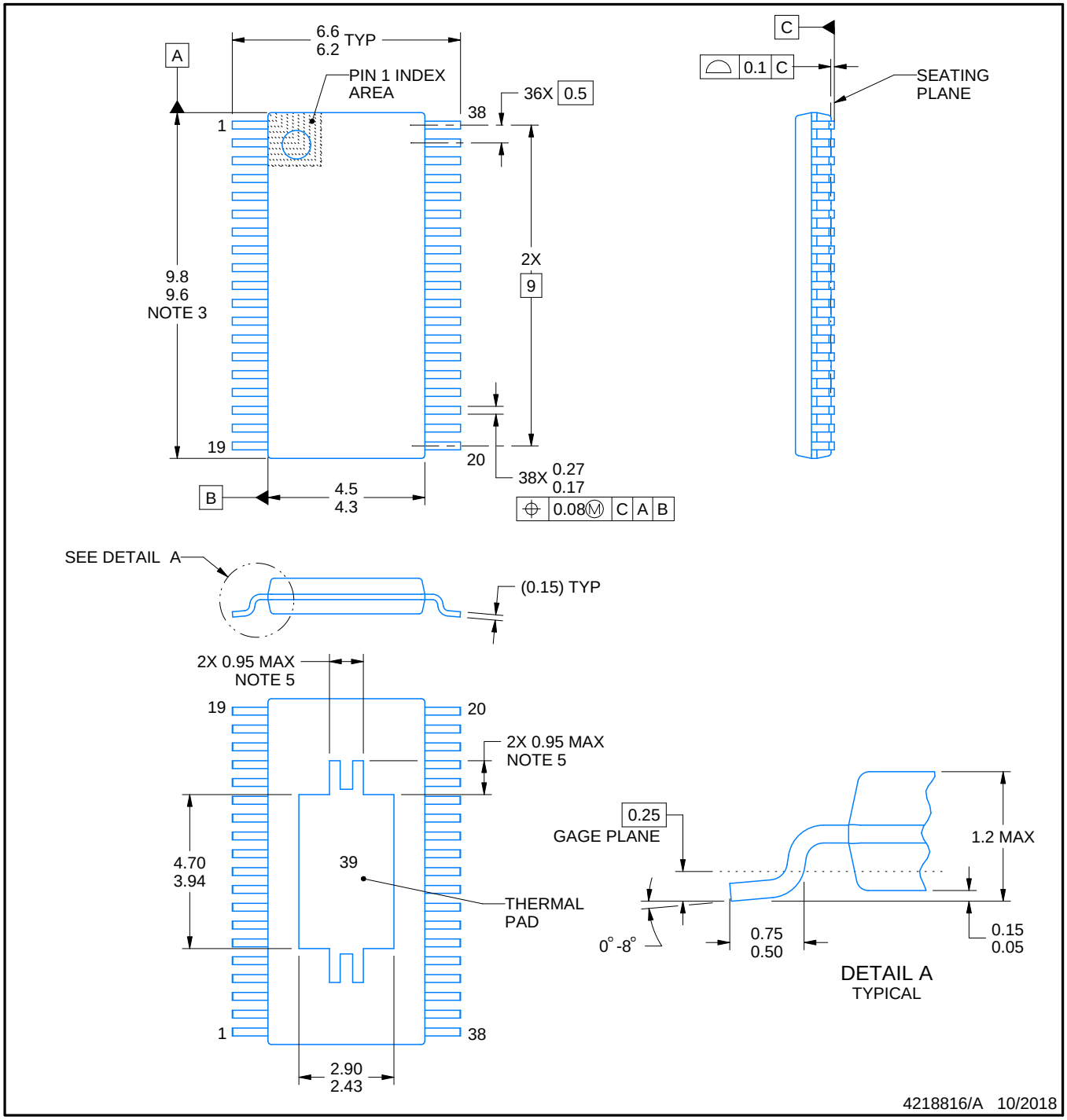
PACKAGE OUTLINE

DCP0038A



PowerPAD™ TSSOP - 1.2 mm max height

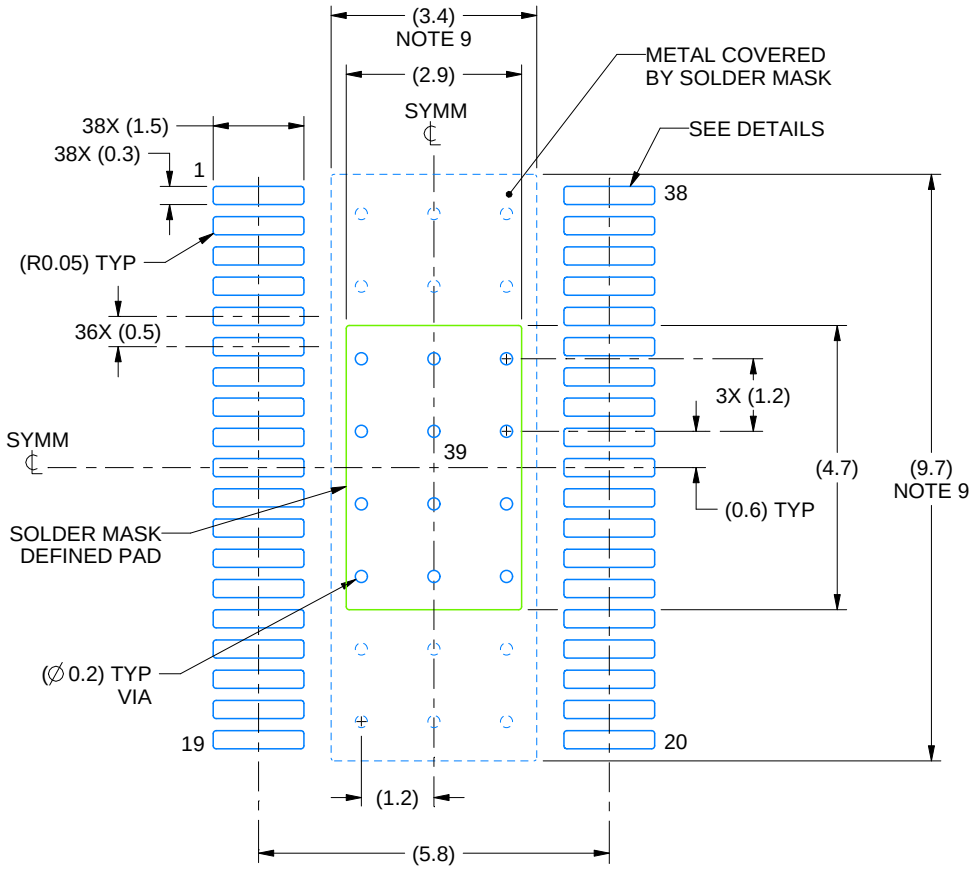
SMALL OUTLINE PACKAGE



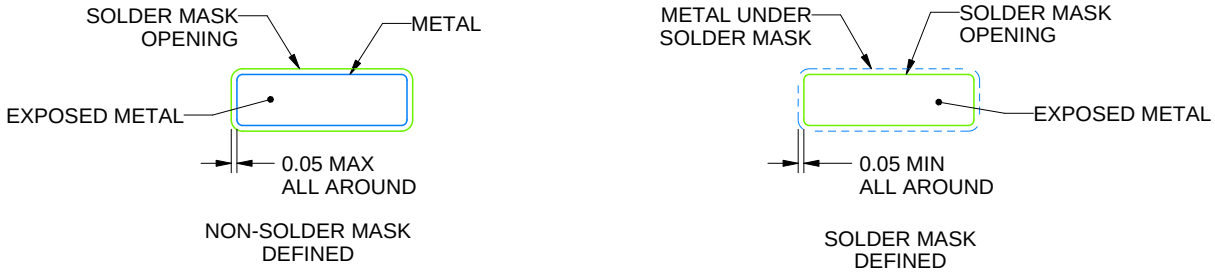
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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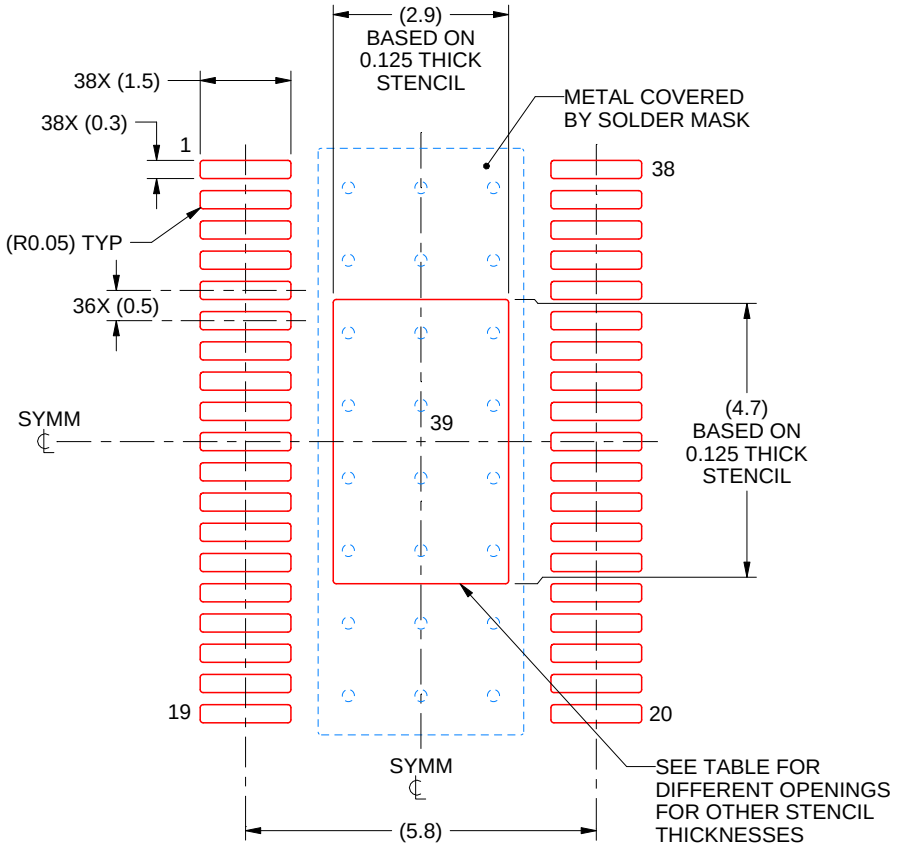
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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