TEXAS INSTRUMENTS
LM5190-Q1
JAJSP12 – JULY 2024

LM5190-Q1 80V、車載用、同期整流降圧コントローラ、定電流および定電圧レギュレーション付き

ADVANCE INFORMATION

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲:-40℃～+125℃
- 広い入力電圧動作範囲:5V～80V
- 0.8V～80V の調整可能な出力電圧、または 5V もしくは 12V の固定出力
- 定電流定電圧 (CC-CV) 動作
  - 電流レギュレーション精度:±4.5%
  - 電圧レギュレーション精度:±1%
- 電流監視機能および定電流機能
  - 出力電流に比例するアナログ電圧 (IMON)
  - プログラマブルな平均出力電流制限 (ILIM)
  - 動的平均出力電流制限 (ISET)
- シャットダウン モード I_Q 2.3μA (標準値)、スリープ モード I_Q 15μA (標準値)
- 標準レベル MOSFET ドライバ
- パワー グッド出力電圧ステータス インジケータ (PGOOD)
- プログラム可能なスイッチング周波数:100kHz～2.2MHz
- オプションの外部クロック同期
- 低周波数帯域と高周波数帯域にわたり EMI 性能を向上させる選択可能なデュアル ランダム スペクトラム拡散 (DRSS)
- 内部スロープ補償および内部ブートストラップ ダイオード
- デュアル入力 VCC レギュレータにより消費電力を低減 (BIAS)

2 アプリケーション

- スーパー キャパシタによるエネルギー バックアップ
- USB パワー デリバリ
- 電動アシスト自転車
- 電動工具
- サーバー バッテリ バックアップ ユニット (BBU)
- エネルギー ストレージ システム および ソーラーエネルギー

3 概要

LM5190-Q1 は、80V、超低静止電流 (I_Q) の同期整流降圧 DC/DC コントローラであり、定電流定電圧 (CC-CV) レギュレーションを備えています。本コントローラはピーク電流モード制御アーキテクチャを採用しているため、ループ補償が簡単で、過渡応答が高速であり、負荷およびラインレギュレーションが非常に優れています。内蔵の CC-CV 動作は、電圧 (± 1%) および電流 (± 4.5%) レギュレーションについて高い精度を備えています。また、CC-CV 動作により、定電流モードと定電圧モードの間をシームレスに移行できます。CC-CV 動作により、平均出力電流制御が必要なアプリケーションで、BOM (部品表) 点数とコストを効果的に低減できます。出力電流制限はプログラム可能で、動的に変更できます。LM5190-Q1 は、出力電流モニタを備えています。

LM5190-Q1 にはデュアル ランダム拡散スペクトラム (DRSS) と呼ばれる独自の EMI 削減機能を備えています。低周波数の三角波変調と高周波数のランダム変調を組み合わせると、低周波数帯域から高周波数帯域にわたり EMI 障害がそれぞれ緩和されます。このハイブリッド手法は、業界標準の EMC テストで規定されている複数分解能帯域幅 (RBW) 設定に適合します。

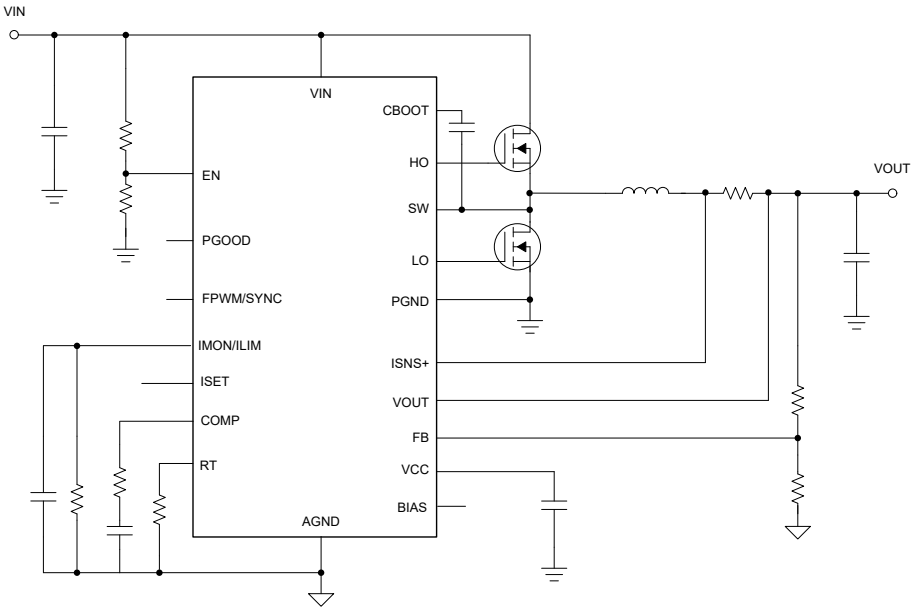
LM5190-Q1 の追加機能として、最大 150℃の接合部温度での動作、ユーザー選択可能なダイオード エミュレーションによる軽負荷時消費電流の低減、オープンドレインのパワー グッド フラグによるフォルト報告と出力監視、高精度イネーブル入力、プリバイアスされた負荷への単調なスタートアップ、デュアル入力 VCC バイアス電源レギュレータ内蔵、内蔵 2.75ms ソフトスタート時間、自動回復機能付きサーマル シャットダウン保護があります。

LM5190-Q1 コントローラは、3.5mm × 4.5mm の放熱特性に優れた 19 ピン VQFN パッケージで供給されます。ウェッタブル フランク ピンが付いているため、製造現場で光学検査を容易に行えます。

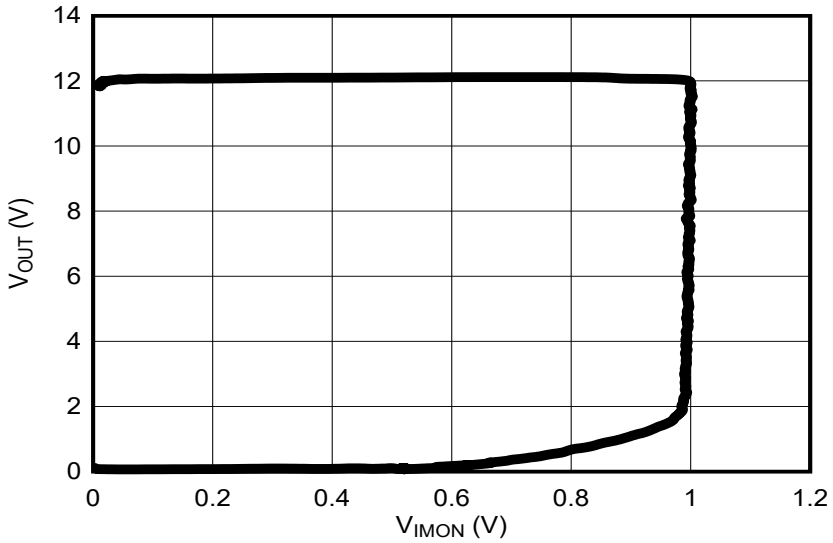
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LM5190-Q1	RGY (VQFN、19)	3.5mm × 4.5mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路図



充電過渡時の定電流定電圧動作

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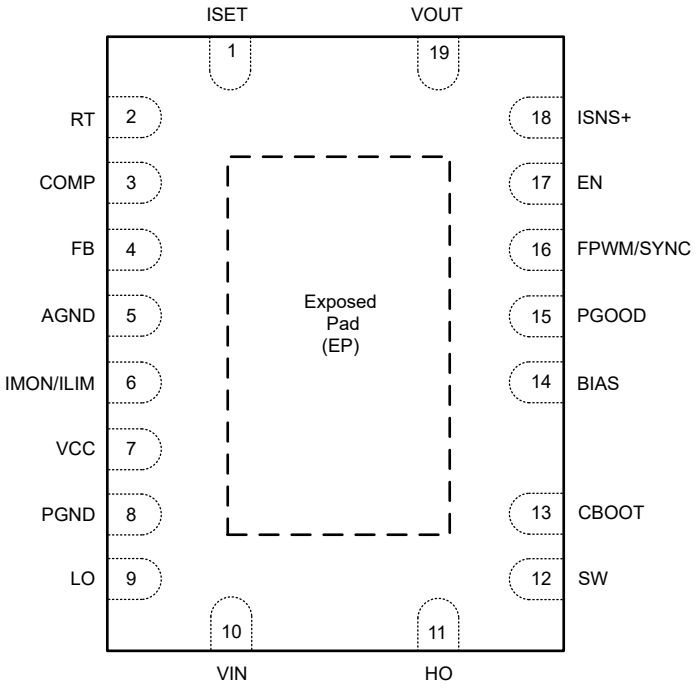
4 Pin Configuration and Functions



Connect the exposed pad to AGND and PGND on the PCB.

図 4-1. 19-Pin VQFN RGY Package With Wettable Flanks (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	ISET	I/O	Dynamic current setting pin for the constant current operation
2	RT	I	Frequency programming pin. A resistor from RT to AGND sets the oscillator frequency between 100kHz and 2.2MHz and DRSS disabled. A resistor from RT to VCC sets the oscillator frequency between 100kHz and 2.2MHz and DRSS enabled.
3	COMP	O	Transconductance error amplifier output. Connect the compensation network from COMP to AGND.
4	FB	I	Connect FB to VCC to set the output voltage to pre-programmed fixed 12V. Connect FB to AGND to set the output voltage to pre-programmed fixed 5V. Alternatively, install a resistor divider from VOUT to AGND to set the output voltage setpoint between 0.8V and 80V. The FB regulation voltage is 0.8V.
5	AGND	G	Analog ground connection. Ground return for the internal voltage reference and analog circuits.
6	IMON/ILIM	O	Current monitor and current limit programming pin
7	VCC	P	VCC bias supply pin. Connect a ceramic capacitor between VCC and PGND.
8	PGND	G	Power ground connection pin for low-side MOSFET gate driver.
9	LO	O	Low-side power MOSFET gate driver output.
10	VIN	P	Supply voltage input source for the VCC regulator.
11	HO	O	High-side power MOSFET gate driver output.
12	SW	P	Switching node of the buck regulator and high-side gate driver return. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET, and the drain terminal of the low-side MOSFET.
13	CBOOT	P	High-side driver supply for bootstrap gate drive.
14	BIAS	P	Optional supply voltage input source for VCC regulator. This input takes over if V_{BIAS} > 9V (typcial) and VIN supply is disabled.
15	PGOOD	O	Power-good pin. An open-collector output that goes low if VOUT is outside the specified regulation window.

表 4-1. Pin Functions (続き)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
16	FPWM/SYNC	I	Connect FPWM/SYNC to VCC to enable forced PWM (FPWM) mode with continuous conduction at light loads. Connect FPWM/SYNC to AGND to operate the LM5190-Q1 in diode emulation mode. FPWM/SYNC can also be used as a synchronization input to synchronize the internal oscillator to an external clock signal.
17	EN	I	An active-high precision input with rising threshold of 1V and hysteresis voltage of 100mV. If the EN voltage is less than 0.55V, the LM5190-Q1 is in shutdown mode.
18	ISNS+	I	Current sense amplifier input. Connect this pin to the inductor side of the external current sense resistor using a low-current Kelvin connection.
19	VOUT	I	Output voltage sense and the current sense amplifier input. Connect VOUT to the output side of the current sense resistor.

(1) P = Power, G = Ground, I = Input, O = Output

4.1 Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet reliability and robustness standards. Standard quad-flat no-lead (QFN) packages do not have solderable or exposed pins and terminals that are easily viewed. Visually determining whether or not the package is successfully soldered onto the printed-circuit board (PCB) is difficult. The wettable-flank process was developed to resolve the issue of side-lead wetting of leadless packaging. The LM5190-Q1 is assembled using a custom 19-pin VQFN package with wettable flanks to provide a visual indicator of solderability, which reduces the inspection time and manufacturing costs.

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5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40℃ to 150℃ (unless otherwise noted). (1)

		MIN	MAX	UNIT
Input voltage	VIN to AGND	–0.3	85	V
Input voltage	SW to AGND	–0.3	85	V
Input voltage	SW to AGND, transient < 20ns	–5		V
Input voltage	CBOOT to SW	–0.3	8	V
Input voltage	EN to AGND	–0.3	85	V
Input voltage	BIAS to AGND	-0.3	30	V
Input voltage	VCC, FB, PGOOD, FPWM/SYNC, RT to AGND	-0.3	8	V
Input voltage	ISET, IMON/ILIM to AGND	–0.3	5.5	V
Input voltage	VOUT, ISNS+ to AGND	–0.3	85	V
Input voltage	VOUT to ISNS+	–0.3	0.3	V
Output voltage	HO to SW, transient < 20ns	–5		V
Output voltage	LO to PGND, transient < 20ns	–1.5		V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 2, 11, 12, 13, 14, 23, and 24)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over the operating junction temperature range of –40℃ to 150℃ (unless otherwise noted). (1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	5		80	V
V_{OUT}	Output voltage range	0.8		80	V
Pin Voltage	PGOOD, FB, FPWM/SYNC, RT	0		8	V
Pin Voltage	COMP, ISET, IMON	0		5.25	V
Pin Voltage	EN	0		80	V
Pin Voltage	BIAS	0		28	V
Pin Voltage	VOUT, ISNS+	0		80	V
T_J	Operating junction temperature	–40		150	°C

(1) Recommended operating conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

5.4 Thermal Information

THERMAL METRIC(1)		LM5190-Q1 RGY (VQFN) 19 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

T_J = –40°C to 125°C. Typical values are at T_J = 25°C, V_{IN} = 12V, and EN tied to VIN (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VIN)						
I_{Q-SD}	VIN shutdown current	V_{EN} = 0V		2.3	4.5	µA
I_{Q-SBY}	VIN standby current	Non-switching, 0.5V ≤ V_{EN} ≤ 1V		100		µA
I_{SLEEP1}	Sleep current, 5V	V_{IN} = 24V, V_{VOUT} = V_{BIAS} = 5.0V, in sleep mode, $V_{FPWM/SYNC}$ = AGND, ISET floating		15	30	µA
I_{SLEEP2}	Sleep current, 12V	V_{IN} = 24V, V_{VOUT} = V_{BIAS} = 12V, in sleep mode, $V_{FPWM/SYNC}$ = AGND, ISET floating		20	35	µA
ENABLE (EN)						
V_{SBY-TH}	Shutdown to standby threshold	V_{EN} rising		0.55		V
V_{EN-TH}	Enable voltage rising threshold	V_{EN} rising, enable switching	0.95	1.0	1.05	V
V_{EN-HYS}	Enable hysteresis voltage			100		mV
INTERNAL LDO (VCC)						
$V_{VCC-REG}$	VCC regulation voltage	I_{VCC} = 0mA to 110mA	7.125	7.5	7.875	V
$V_{VCC-UVLO}$	VCC UVLO rising threshold		4.65	4.8	4.95	V
$V_{VCC-HYS}$	VCC UVLO hysteresis			425		mV
$I_{VCC-LIM}$	Internal LDO short-circuit current limit		135	220	350	mA
EXTERNAL BIAS (BIAS)						
$V_{BIAS-TH}$	V_{IN} to V_{BIAS} switchover rising threshold		8.55	9	9.45	V
$V_{BIAS-HYS}$	V_{IN} to V_{BIAS} switchover hysteresis			400		mV
REFERENCE VOLTAGE						
V_{REF-V}	Regulated FB voltage	V_{IMON} = 0 V	792	800	808	mV
V_{REF-I}	Current loop reference voltage	V_{FB} = 0V	0.99	1	1.01	V
OUTPUT VOLTAGE (VOUT)						
V_{OUT-5V}	5V output voltage setpoint	FB to AGND	4.95	5.0	5.05	V
$V_{OUT-12V}$	12V output setpoint	FB to VCC, V_{IN} = 24V	11.88	12	12.12	V
ERROR AMPLIFIER (COMP)						
g_{m-VEA}	Voltage loop EA transconductance	ΔV_{FB} = 100mV		1000		µS
g_{m-IEA}	Current loop EA transconductance	ΔV_{IMON} = 100mV		1000		µS
I_{FB}	Error amplifier input bias current				75	nA
$I_{COMP-SRC}$	EA source current	V_{COMP} = 1V		120		µA
$I_{COMP-SINK}$	EA sink current	V_{COMP} = 1V		120		µA
OUTPUT CURRENT MONITOR (IMON/ILIM)						
g_{m-IMON}	Monitor amplifier gain from V_{CS}	V_{CS} = 40mV	1.91	2	2.09	µA/mV
I_{OFFSET}	Monitor amplifier offset current	V_{CS} = 0mV	22.5	25	27.5	µA
CURRENT SETTING (ISET)						

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5.5 Electrical Characteristics (続き)

T_J = –40°C to 125°C. Typical values are at T_J = 25°C, V_{IN} = 12V, and EN tied to VIN (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ISET}	ISET source current		9	10	11	µA
FORCED PWM MODE (FPWM/SYNC)						
V_{ZC-SW}	Zero-cross threshold	SW-PGND threshold		–5.5		mV
SWITCHING FREQUENCY						
V_{RT}	RT pin regulation voltage	10kΩ < R_{RT} < 220kΩ		1		V
F_{SW1}	Switching frequency 1	V_{IN} = 12V, R_{RT} = 242kΩ to AGND	90	100	110	kHz
F_{SW2}	Switching frequency 2	V_{IN} = 12V, R_{RT} = 10kΩ to AGND	2	2.2	2.4	MHz
V_{SLOPE}	Peak slope compensation amplitude	Referenced to ISNS+ to VOUT input		45		mV
t_{ON-MIN}	Minimum on-time			26	50	ns
$t_{OFF-MIN}$	Minimum off-time			80	125	ns
POWER GOOD (PGOOD)						
V_{PG-UV}	Power-Good UV trip level	Falling with respect to the regulated voltage	90%	92%	94%	
V_{PG-OV}	Power-Good OV trip level	Rising with respect to the regulated voltage	108%	110%	112%	
$V_{PG-UV-HYST}$	Power-Good UV hysteresis			3.7%		
$V_{PG-OV-HYST}$	Power-Good OV hysteresis			3.7%		
V_{PG-OL}	PG voltage	Open collector, I_{PG} = 4mA			0.8	V
OVERVOLTAGE PROTECTION						
$V_{OVTH-RISING}$	Overvoltage threshold	Rising with respect to regulated voltage	108%	110%	112%	
$V_{OVTH-HYST}$	Overvoltage threshold hysteresis			3.7%		
STARTUP (Soft Start)						
t_{SS-INT}	Internal fixed soft-start time		1.9	2.75	3.6	ms
BOOT CIRCUIT						
$V_{BOOT-DROP}$	Internal diode forward drop	I_{CBOOT} = 20mA, VCC to CBOOT		0.8	1	V
I_{BOOT}	CBOOT to SW quiescent current, not switching	V_{EN} = 5V, $V_{CBOOT-SW}$ = 7.5V			25	µA
$V_{BOOT-SW-UV-F}$	CBOOT to SW UVLO falling threshold	$V_{CBOOT-SW}$ falling	2.75	3.1	3.75	V
$V_{BOOT-SW-UV-HYS}$	CBOOT to SW UVLO hysteresis			0.3		V
HIGH-SIDE GATE DRIVER (HO)						
$V_{HO-HIGH}$	HO high-state output voltage	I_{HO} = –100mA, $V_{HO-HIGH}$ = V_{CBOOT} – V_{HO}		300		mV
V_{HO-LOW}	HO low-state output voltage	I_{HO} = 100mA		75		mV
$t_{HO-RISE}$	HO rise time (10% to 90%)	C_{LOAD} = 2.7nF		20		ns
$t_{HO-FALL}$	HO fall time (90% to 10%)	C_{LOAD} = 2.7nF		8		ns
LOW-SIDE GATE DRIVER (LO)						
$V_{LO-HIGH}$	LO high-state output voltage	I_{LO} = –100mA		300		mV
V_{LO-LOW}	LO low-state output voltage	I_{LO} = 100mA		75		mV
$t_{LO-RISE}$	LO rise time (10% to 90%)	C_{LOAD} = 2.7nF		20		ns
$t_{LO-FALL}$	LO fall time (90% to 10%)	C_{LOAD} = 2.7nF		8		ns
ADAPTIVE DEADTIME CONTROL						
t_{DEAD1}	HO off to LO on deadtime			21		ns
t_{DEAD2}	LO off to HO on deadtime			21		ns
OVERCURRENT PROTECTION						
V_{CS-TH}	Current limit threshold	Measured from ISNS+ to VOUT	54	60	66	mV
$V_{CS-TH-MIN}$	Minimum peak current limit threshold	Measured from ISNS+ to VOUT		12		mV
A_{CS}	CS amplifier gain		9.7	10	10.3	V/V
$I_{BIAS-CS}$	CS amplifier input bias current	V_{VOUT} = 5.0V			15	nA
V_{CS-NEG}	CS negative voltage threshold			–30		mV
THERMAL SHUTDOWN						
T_{J-SD}	Thermal shutdown threshold (1)	Temperature rising		175		°C

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5.5 Electrical Characteristics (続き)

T_J = –40°C to 125°C. Typical values are at T_J = 25°C, V_{IN} = 12V, and EN tied to VIN (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{J-HYS}	Thermal shutdown hysteresis (1)			15		°C

(1) Specified by design. Not production tested.

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6 Detailed Description

6.1 Overview

The LM5190-Q1 is a switching DC/DC controller that features all of the functions necessary to implement a high-efficiency constant-current constant-voltage synchronous buck converter operating over a wide input voltage range from 5V to 80V. The LM5190-Q1 is configured to provide a fixed 5V or 12V output, or an adjustable output from 0.8V to 80V. This easy-to-use controller integrates high-side and low-side MOSFET gate drivers capable of sourcing and sinking peak currents of 1.5A and 2.5A, respectively. Adaptive dead-time control is designed to minimize body diode conduction during switching transitions.

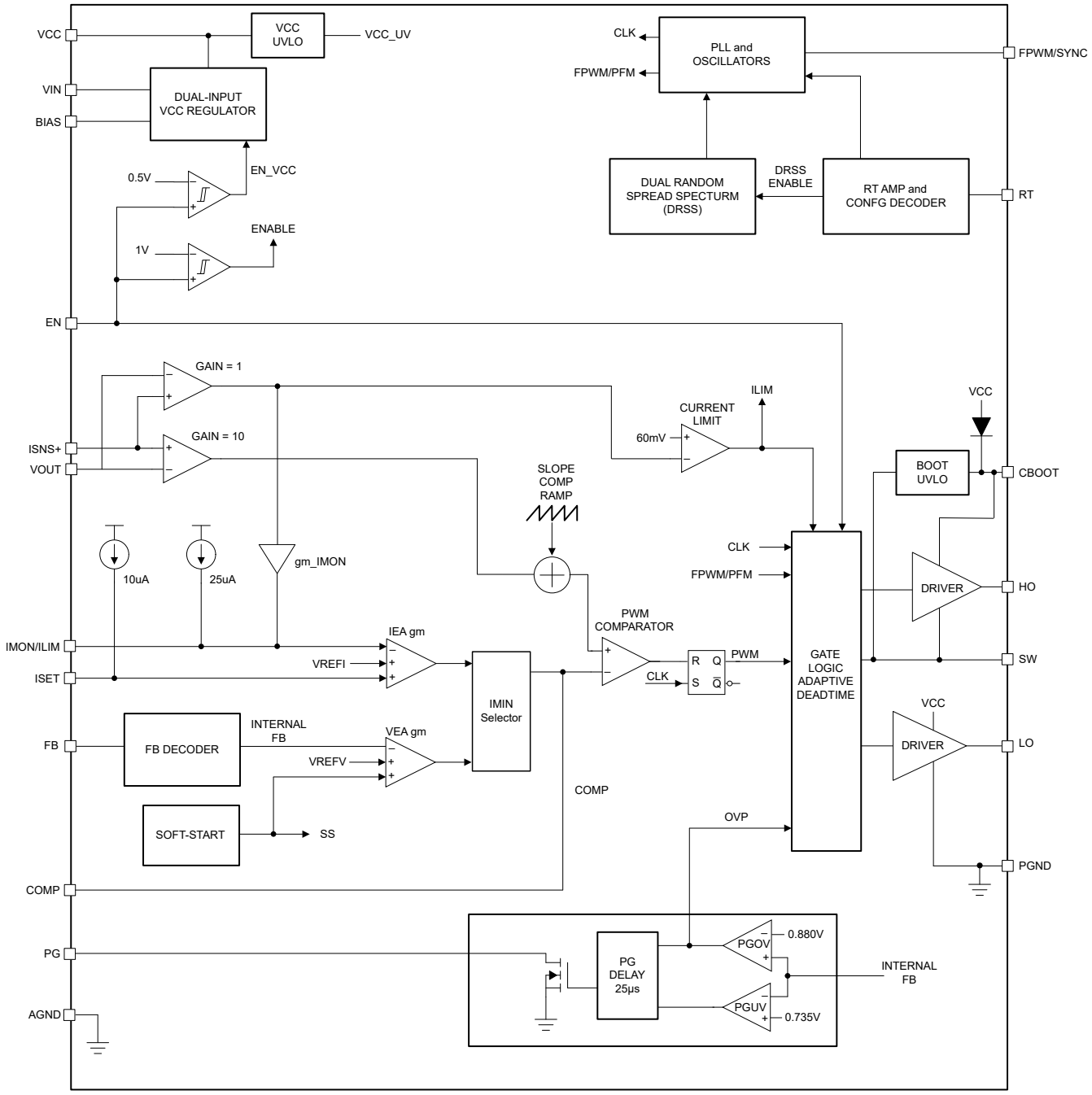
The current-mode control using a shunt resistor current sensing provides inherent line feedforward, cycle-by-cycle peak current limiting, and easy loop compensation. The current-mode control also supports a wide duty cycle range for high input voltage and low-dropout applications as well as when application require a high step-down conversion ratio (for example, 10-to-1). The oscillator frequency is user-programmable between 100kHz to 2.2MHz, and the frequency can be synchronized as high as 2.5MHz by applying an external clock to the FPWM/SYNC pin.

An external bias supply can be connected to BIAS to maximize efficiency in high input voltage applications. A user-selectable diode emulation feature enables discontinuous conduction mode (DCM) operation to further improve efficiency and reduce power dissipation during light-load conditions. Fault protection features include current limiting, thermal shutdown, UVLO, and remote shutdown capability.

The LM5190-Q1 incorporates features to simplify the compliance with various EMI standards, for example CISPR 25 Class 5 automotive EMI requirements. DRSS techniques reduce the peak harmonic EMI signature.

The LM5190-Q1 is provided in a custom 19-pin VQFN package with a wettable flank pinout and an exposed pad to aid in thermal dissipation.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Input Voltage Range (V_{IN})

The LM5190-Q1 operational input voltage range is from 5V to 80V. The device is intended for step-down conversions from 12V, 24V, and 48V supply rails. The LM5190-Q1 uses an internal LDO to provide a 7.5V VCC bias rail for the gate drive and control circuits (assuming the input voltage is higher than 7.5V with additional voltage margin necessary for the subregulator dropout specification).

In high input voltage applications, take extra care to make sure that the VIN and SW pins do not exceed the absolute maximum voltage rating of 85V during line or load transient events. Voltage excursions that exceed the applicable voltage specifications can damage the device.

6.3.2 High-Voltage Bias Supply Regulator (VCC, BIAS)

The LM5190-Q1 contains an internal high-voltage VCC bias regulator that provides the bias supply for the PWM controller and the gate drivers for the external MOSFETs. The input voltage pin (VIN) can be connected directly to an input voltage source up to 80V. However, when the input voltage is below the VCC setpoint level, the VCC voltage tracks V_{IN} minus a small voltage drop.

The VCC regulator output current limit is 135mA (minimum). At power up, the controller sources current into the capacitor connected at the VCC pin. When the VCC voltage exceeds 4.8V and the EN pin is connected to a voltage greater than 1V, the soft-start sequence begins. The output remains active unless the VCC voltage falls below the VCC UVLO falling threshold of 4.5V (typical) or EN is switched to a low state. Connect a ceramic capacitor from VCC to PGND. The recommended range of the VCC capacitor is from 2.2µF to 10µF.

The VCC regulator is a dual-input regulator which uses BIAS pin as the other input in addition to the VIN pin. A lower voltage supply such as the buck output (VOUT) or other applicable system rails can be tied to BIAS to reduce the power dissipation of the internal VCC regulator. The VCC regulator switches over to use BIAS voltage as the input when rising across 9V (typical). The switchover voltage hysteresis is 400mV. When using BIAS as the supply, VIN voltage must be greater than VCC voltage during all conditions to avoid damage to the controller. Tie BIAS to PGND if unused. The operational maximum voltage of BIAS is 28V.

6.3.3 Precision Enable (EN)

The EN pin can be connected to a voltage as high as 80V. The LM5190-Q1 has a precision enable. When the EN voltage is greater than 1V, controller switching is enabled. If the EN pin is pulled below 0.5V, the LM5190-Q1 is in shutdown with an I_Q of 2.3µA (typical) current consumption from V_{IN}. When the enable voltage is between 0.5V and 1V, the LM5190-Q1 is in standby mode with the VCC regulator active but the controller is not switching. In standby mode, the non-switching input quiescent current is 100µA typical. The LM5190-Q1 is enabled with a voltage greater than 1.0V. Many applications benefit from using a resistor divider R_{ENT} and R_{ENB} to establish a precision UVLO level from V_{SUPPLY} (supply voltage of power stage tied to VIN pin). TI does not recommend leaving the EN pin floating.

6.3.4 Power-Good Monitor (PGOOD)

The LM5190-Q1 includes an output voltage monitoring signal for V_{OUT} to simplify sequencing and supervision. The power-good signal is used for start-up sequencing of downstream converters, fault protection, and output monitoring. The power-good output (PGOOD) switches to a high impedance open-drain state when the output voltage is in regulation. The PGOOD switches low when the output voltage drops below the lower power-good threshold (92% typical) or rises above the upper power-good threshold (110% typical). A 25µs deglitch filter prevents false tripping of the power-good signal during transients. TI recommends a pullup resistor of 100kΩ (typical) from PGOOD to the relevant logic rail. PGOOD is asserted low during soft start and when the buck regulator is disabled.

6.3.5 Switching Frequency (RT)

Program the LM5190-Q1 oscillator with a resistor from RT to AGND or VCC to set an oscillator frequency from 100kHz and 2.2MHz. If the resistor is connected between RT and VCC, the dual random spread spectrum

(DRSS) is on. If the resistor is connected between RT and AGND, the DRSS is off. See more details about DRSS in セクション 6.3.7. Calculate the RT resistance for a given switching frequency using 式 1.

$$R_{RT}\,[\mathrm{k\Omega}] = \frac{\frac{10^6}{f_{SW}\,[\mathrm{kHz}]} - 59}{41} \quad (1)$$

6.3.6 Low Dropout Mode

For extended minimum input voltage, LM5190-Q1 enters the low dropout (LDO) mode if the required duty cycle is greater than the maximum duty cycle which is limited by the minimum off time. During the LDO mode, the LM5190-Q1 extends the on-time pulse until the PWM latch is reset by the current sense ramp exceeding the controller compensation voltage. The LM5190-Q1 skips up to 15 t_{OFF} cycles to allow the controller to extend the duty cycle. 図 6-1 shows the normal PWM mode to LDO mode transition.

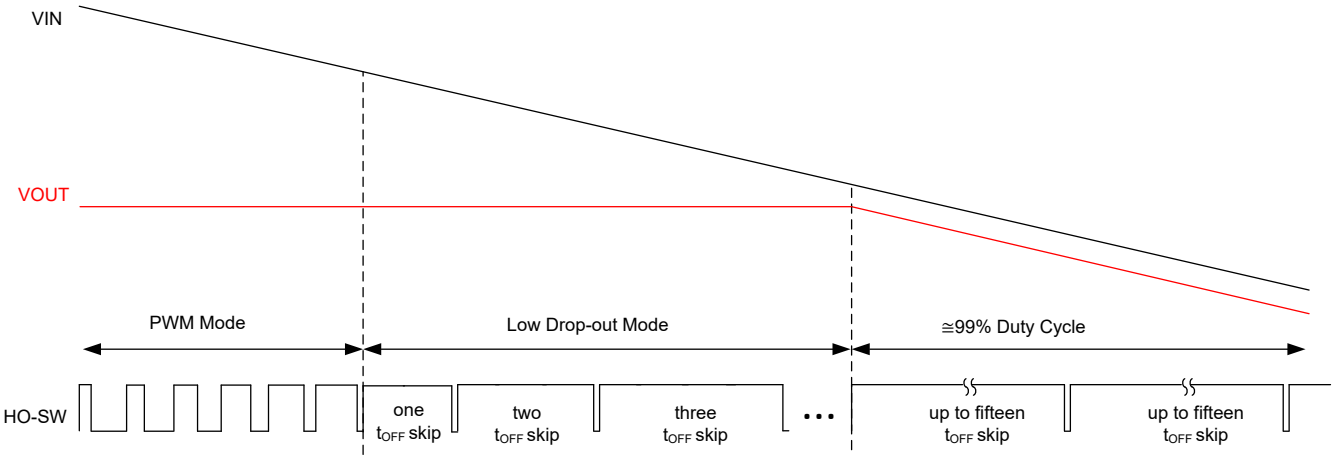

図 6-1. PWM to LDO Mode Transition

The approximate input voltage level at which this occurs is given by 式 2.

$$V_{IN(MIN)} = V_{OUT} \times \frac{t_{SW}}{t_{SW} - t_{OFF(MIN)}} \quad (2)$$

where

- t_{SW} is the switching period.
- $t_{OFF(MIN)}$ is the minimum off time of 80ns.

6.3.7 Dual Random Spread Spectrum (DRSS)

The LM5190-Q1 provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. DRSS combines a low-frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low-frequency triangular modulation improves performance in lower radio-frequency bands, while the high-frequency random modulation improves performance in higher radio frequency bands.

Spread spectrum works by converting a narrowband signal into a wideband signal that spreads the energy over multiple frequencies. Because industry standards require different EMI receiver resolution bandwidth (RBW) settings for different frequency bands, the RBW has an impact on the spread spectrum performance. For example, the CISPR 25 spectrum analyzer RBW in the frequency band from 150kHz to 30MHz is 9kHz. For frequencies greater than 30MHz, the RBW is 120kHz. DRSS is able to simultaneously improve the EMI performance in the low and high RBWs using the low-frequency triangular modulation profile and at high frequency cycle-by-cycle random modulation, respectively. DRSS can reduce conducted emissions up to

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15dBµV in the low-frequency band (150kHz to 30MHz) and 5dBµV in the high-frequency band (30MHz to 108MHz).

To enable DRSS, connect RT to VCC through a resistor. The resistor is still used to set the switching frequency with the same equation in 式 1.

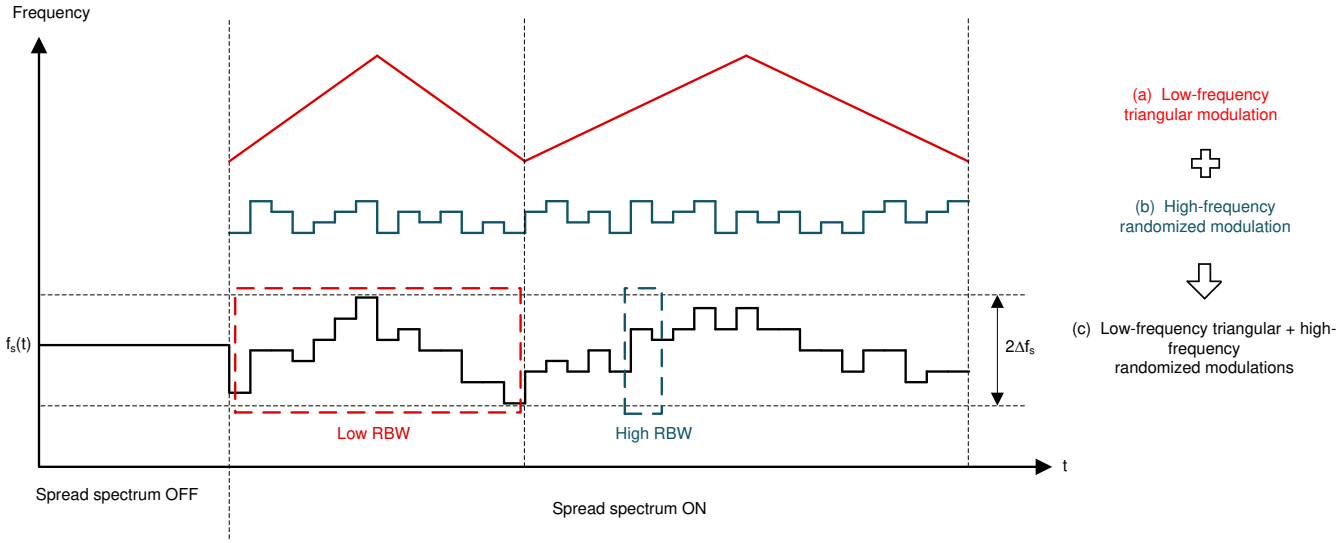

図 6-2. Dual Random Spread Spectrum Implementation

6.3.8 Soft Start

The LM5190-Q1 has an internal 2.75ms soft-start timer (typical). The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

6.3.9 Output Voltage Setpoint (FB)

The LM5190-Q1 output can be independently configured for one of two fixed output voltages without external feedback resistors, or adjusted to a desired voltage using an external resistor divider. Set the output to 5V by connecting FB to AGND with a maximum resistance of 2.0kΩ. Set the output to 12V by connecting FB to VCC with a maximum resistance of 2.0kΩ. See 表 6-1.

表 6-1. Output Regulation Targets

FB SELECTION	V_{OUT} SETPOINT
FB = VDD	12V
FB = AGND	5V
FB = FB resistors	Adjustable

The configuration settings are latched and cannot be changed until the LM5190-Q1 is powered down (with the VCC voltage decreasing below the falling UVLO threshold) and then powered up again (VCC rises above 4.8V typical). Alternatively, the output regulation target can be adjusted during operation by connecting external feedback divider resistors whose parallel resistance is greater than 5.0kΩ (see 式 3).

$$5\ \text{k}\Omega < \frac{R_{FBT} \times R_{FBB}}{R_{FBT} + R_{FBB}} \tag{3}$$

The output voltage adjustment range is between 0.8V and 80V. The regulation voltage at FB is 0.8V (V_{REF-V}). Use 式 4 to calculate the top and bottom feedback resistors, designated as R_{FBT} and R_{FBB}, respectively.

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$$R_{FBT} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_{FBB} \quad (4)$$

If low-I_Q operation is required, take care when selecting the external feedback resistors. The current consumption of the external divider adds to the LM5190-Q1 sleep current (15µA typical). The divider current reflected to V_{IN} is scaled by the ratio of V_{OUT} / V_{IN}.

6.3.10 Minimum Controllable On Time

There are two limitations to the minimum output voltage adjustment range: the LM5190-Q1 voltage reference of 0.8V and the minimum controllable switch-node pulse width, $t_{ON(min)}$.

$t_{ON(min)}$ effectively limits the voltage step-down conversion ratio V_{OUT} / V_{IN} at a given switching frequency. For fixed-frequency PWM operation, the voltage conversion ratio must satisfy 式 5.

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(min)} \times f_{SW} \quad (5)$$

where

- $t_{ON(min)}$ is 26ns (typical).
- f_{SW} is the switching frequency.

If the desired voltage conversion ratio does not meet the above condition, the LM5190-Q1 transitions from fixed switching frequency operation to a pulse-skipping mode to maintain output voltage regulation. For example, if the desired output voltage is 5V with an input voltage of 24V and switching frequency of 2.1MHz, use 式 6, 式 7 to check the conversion ratio.

$$\frac{5\ \text{V}}{24\ \text{V}} > 26\ \text{ns} \times 2.1\ \text{MHz} \quad (6)$$

$$0.208 > 0.055 \quad (7)$$

For wide V_{IN} applications and low output voltages, an alternative is to reduce the LM5190-Q1 switching frequency to meet the requirement of 式 5.

6.3.11 Inductor Current Sense (ISNS+, VOUT)

Shunt Current Sensing Implementation illustrates inductor current sensing using a shunt resistor. This configuration continuously monitors the inductor current to provide accurate overcurrent protection across the operating temperature range. For optimal current sense accuracy and overcurrent protection, use a *low inductance* ±1% tolerance shunt resistor between the inductor and the output, with a Kelvin connection to the LM5190-Q1 current sense amplifier.

If the peak voltage signal sensed from ISNS+ to VOUT exceeds the current limit threshold of 60mV, the current limit comparator immediately terminates the HO output for cycle-by-cycle peak current limiting. Calculate the shunt resistance using 式 8.

$$R_S = \frac{V_{CS-TH}}{I_{out(CL)} + \frac{\Delta I_L}{2}} \quad (8)$$

where

- V_{CS-TH} is current sense threshold of 60mV.
- $I_{OUT(CL)}$ is the overcurrent setpoint that is set higher than the maximum load current to avoid tripping the overcurrent comparator during load transients.
- ΔI_L is the peak-to-peak inductor ripple current.

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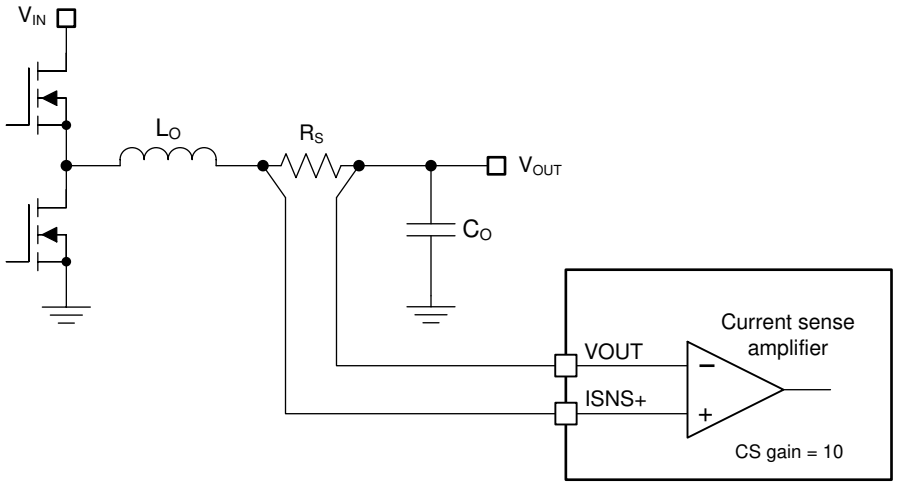

図 6-3. Shunt Current Sensing Implementation

The soft-start voltage is clamped 60mV above FB if the converter is in an overcurrent condition or if the output is in UV (undervoltage) condition in CC mode operation. Eight overcurrent events must occur before the SS clamp is enabled. This requirement makes sure that SS can be pulled low during brief overcurrent events, preventing output voltage overshoot during recovery.

6.3.12 Voltage Loop Error Amplifier

In the voltage loop, the LM5190-Q1 has a high-gain transconductance amplifier that generates an error current proportional to the difference between the feedback voltage and an internal precision reference (0.8V). The transconductance of the amplifier is 1000µS. The voltage loop error amplifier only takes control when the internal minimum function block IMIN selector selects the current from the voltage loop error amplifier. See セクション 6.3.14 for more details regarding the constant-current constant-voltage operation.

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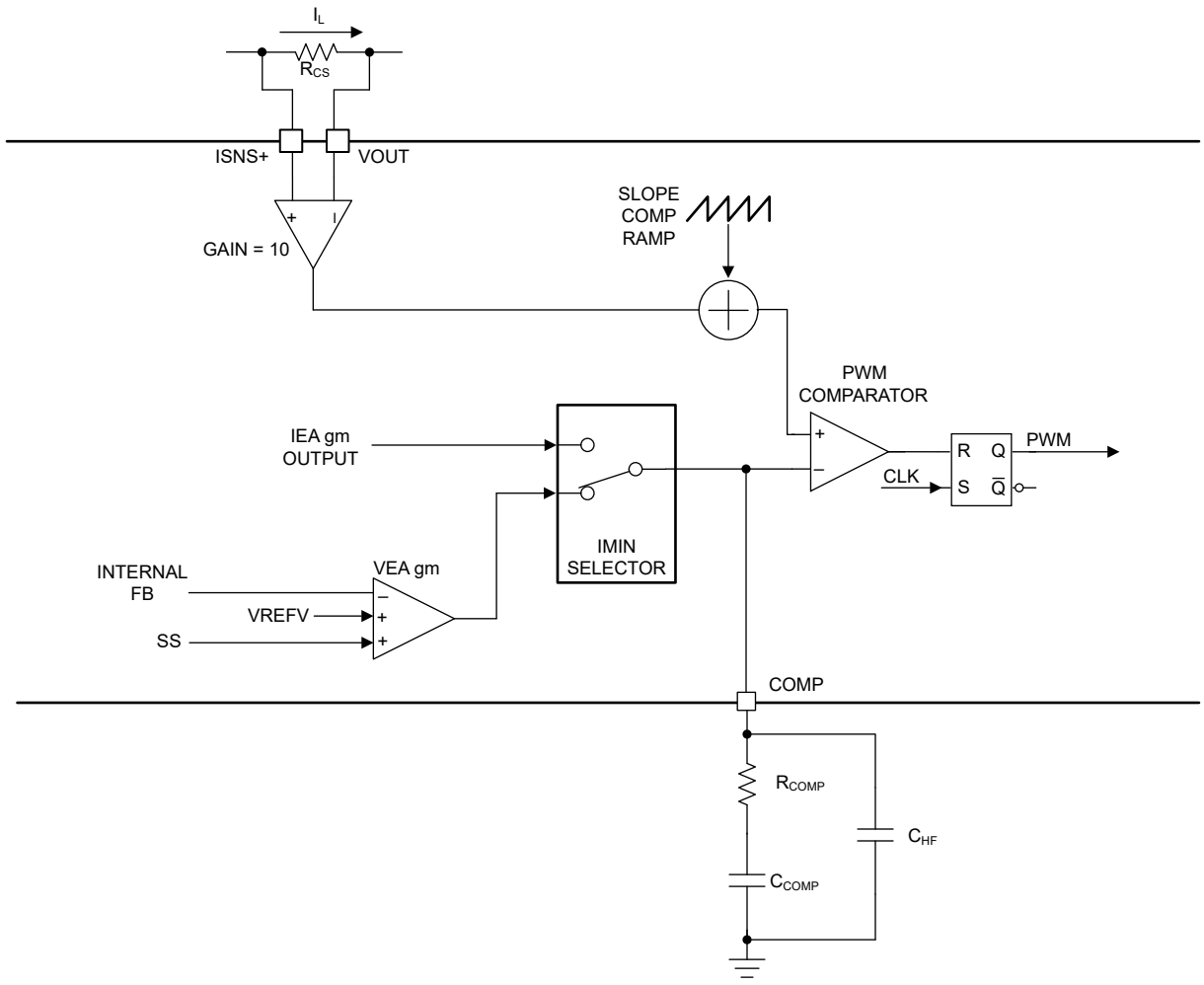

図 6-4. Voltage Loop Functional Block Diagram

A type-II compensation network is generally recommended for peak current-mode control.

6.3.13 Current Monitor, Programmable Current Limit, and Current Loop Error Amplifier (IMON/ILIM, ISET)

In the current loop, the LM5190-Q1 has a high-gain transconductance amplifier that generates an error current proportional to the difference between the IMON voltage and an internal precision reference (1V). The transconductance of the amplifier is 1000µS. The current loop error amplifier only takes control when the internal minimum function block IMIN selector selects the current from the current loop error amplifier. See セクション 6.3.14 for more details regarding the constant-current constant-voltage operation.

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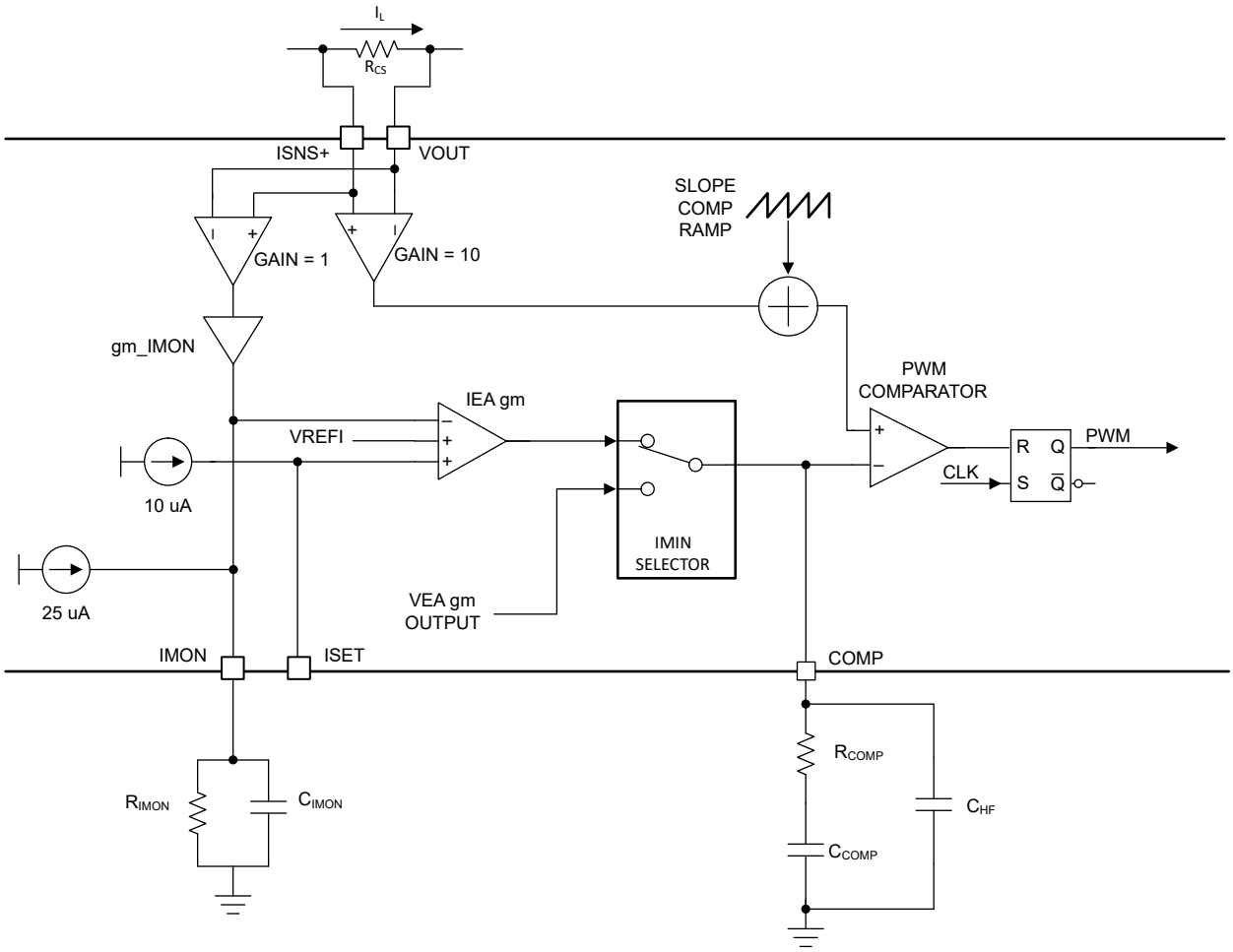

図 6-5. Current Loop Functional Block Diagram

The R_{IMON} is used to programmed the CC regulation target. The CC regulation target is usually defined to be smaller than the maximum current defined by the cycle-by-cycle peak current limit in Inductor Current Sense (ISNS+, VOUT) . The R_{IMON} is selected by 式 9.

$$R_{IMON} = \frac{V_{refI}}{R_{CS} \times g_{m\_IMON} \times I_{CC} + I_{IMON\_offset}} \quad (9)$$

where

- V_{refI} is 1V (typical).
- R_{CS} is the current sensing resistance.
- g_{m_IMON} is the current monitor gain of 2μA/mV.
- I_{CC} is the CC regulation target.
- I_{IMON_offset} is the IMON offset current of 25μA.

The C_{IMON} is used to form the RC filter with R_{IMON} and filter out the sensed inductor current ripple to the achieve average current regulation. The C_{IMON} also sets the response of the current loop. With R_{IMON} and C_{IMON} selected, IMON/ILIM multi-functional pin can be used as the current monitor when the converter is operating in CV loop. The average inductor current can be read from IMON/ILIM voltage by using 式 10.

$$I_{AVG} = \frac{\frac{V_{IMON}}{R_{IMON}} - I_{IMON\_offset}}{R_{CS} \times g_{m\_IMON}} \quad (10)$$

where V_{IMON} is the voltage on IMON/ILIM pin and I_{AVG} is the average inductor current. The DC offset current is introduced at IMON/ILIM pin to raise the no-load signal above the possible ground noise floor.

ISET can be used to dynamically program the CC regulation current. An external voltage forced at ISET can set the CC regulation current by 式 11.

$$V_{ISET} = R_{IMON} \times \left(I_{CCset} \times R_{CS} \times g_{m_{IMON}} + I_{IMON\_offset}\right) \quad (11)$$

where I_{CCset} is the desired average current to be programmed by ISET. ISET is only functional when ISET voltage is smaller than V_{refI} (1V typical). ISET has an internal current source of 10µA typical so ISET can be used with a capacitor at the pin to achieve the current soft start during CC transient such as super capacitor and battery charging conditions.

6.3.14 Dual Loop Architecture

In セクション 6.3.12 and セクション 6.3.13, the voltage loop and current loop operation have been discussed respectively. To have a seamless transition between CC and CV operation, a minimum function block called IMIN selector is used for the dual loop architecture.

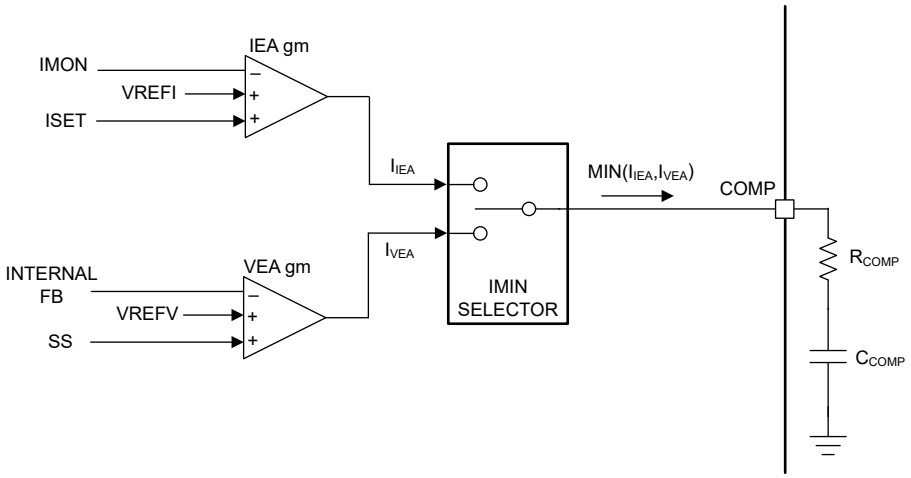

図 6-6. Dual Loop Architecture

6.3.15 PWM Comparator

The PWM comparator compares the sum of the amplified sensed inductor current and the slope compensation ramp with the COMP pin voltage minus a 0.6V internal offset, and terminates the present cycle if the sum of the amplified sensed inductor current and the slope compensation ramp is greater than the COMP pin voltage minus the 0.6V internal offset.

6.3.16 Slope Compensation

The LM5190-Q1 provides internal slope compensation for stable operation with peak current-mode control and a duty cycle greater than 50%. Calculate the buck inductance to provide a slope compensation contribution equal to one times the inductor downslope using 式 12.

$$L_{O-IDEAL}\left[\mu H\right] = \frac{V_{OUT}\,[V] \times R_{CS}\,[m\Omega]}{40 \times f_{SW}\,[MHz]} \quad (12)$$

- A lower inductance value generally increases the peak-to-peak inductor current, which minimizes size and cost, and improves transient response at the cost of reduced light-load efficiency due to higher cores losses and peak currents.
- A higher inductance value generally decreases the peak-to-peak inductor current, reducing switch peak and RMS currents at the cost of requiring larger output capacitors to meet load-transient specifications.

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6.3.17 High-Side and Low-Side Gate Drivers (HO, LO)

The LM5190-Q1 contains gate drivers and an associated high-side level shifter to drive the external N-channel power MOSFETs. The high-side gate driver works in conjunction with an internal bootstrap diode D_{BOOT} and bootstrap capacitor C_{BOOT}. During the conduction interval of the low-side MOSFET, the SW voltage is approximately 0V and CBOOT charges from VCC through the internal D_{BOOT}. TI recommends a 0.1µF ceramic capacitor connected with short traces between the CBOOT and SW pins.

The HO and LO outputs are controlled with an adaptive dead-time methodology so that both outputs (HO and LO) are never on at the same time, preventing cross conduction. Before the LO driver output is allowed to turn on, the adaptive dead-time logic first disables HO and waits for the HO voltage to drop below 1.5V typical. LO is allowed to turn on after a small delay (HO fall to LO rising delay). Similarly, the HO turn-on is delayed until the LO voltage has dropped below 1.5V. This technique makes sure of adequate dead-time for any size N-channel power MOSFET implementations, including parallel MOSFET configurations.

Caution is advised when adding series gate resistors, as this can impact the effective dead-time. The selected high-side MOSFET determines the appropriate bootstrap capacitance value C_{BOOT} in accordance with 式 13.

$$C_{BOOT} = \frac{Q_G}{\Delta V_{CBOOT}} \tag{13}$$

where

- Q_G is the total gate charge of the high-side MOSFET at the applicable gate drive voltage.
- ΔV_{CBOOT} is the voltage variation of the high-side MOSFET driver after turn-on.

To determine C_{BOOT}, choose ΔV_{CBOOT} such that the available gate drive voltage is not significantly impacted. An acceptable range of ΔV_{CBOOT} is 100mV to 300mV. The bootstrap capacitor must be a low-ESR ceramic capacitor, typically 0.1µF. Select FETs to make sure that the minimum input supply voltage is higher than gate plateau voltage of the FET plus 0.5V so that the FET works in the ohmic region when turned on.

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6.4 Device Functional Modes

6.4.1 Sleep Mode

The LM5190-Q1 operates with peak current-mode control such that the compensation voltage is proportional to the peak inductor current. During no-load or light-load conditions, the output capacitor discharges very slowly. As a result, the compensation voltage does not demand the driver output pulses on a cycle-by-cycle basis. When the LM5190-Q1 controller detects 16 missed switching cycles, the controller enters sleep mode and switches to a low I_Q state to reduce the current drawn from the input. For the LM5190-Q1 to go into sleep mode, the controller must be programmed for diode emulation (tie FPWM/SYNC to AGND).

The typical controller I_Q in sleep mode is 15µA with a 12V output.

6.4.2 Forced PWM Mode and Synchronization (FPWM/SYNC)

A synchronous buck regulator implemented with a low-side synchronous MOSFET rather than a diode has the capability to sink negative current from the output during conditions of, light-load, output overvoltage, and pre-bias start-up conditions. The LM5190-Q1 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation mode, the low-side MOSFET is switched off when reverse current flow is detected by sensing the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss during light-load conditions. The disadvantage of diode emulation mode is slower light-load transient response.

The FPWM/SYNC pin configures diode emulation mode and forced PWM mode. To enable diode emulation and thus achieve low-I_Q current at light loads, connect FPWM/SYNC to AGND. If FPWM with continuous conduction mode (CCM) operation is desired, tie FPWM/SYNC to VCC. Note that diode emulation is automatically engaged to prevent reverse current flow during a prebias start-up. A gradual change from DCM to CCM operation provides monotonic start-up performance.

To synchronize the LM5190-Q1 to an external source, apply a logic-level clock to the FPWM/SYNC pin. The LM5190-Q1 can be synchronized to ±20% of the programmed frequency up to a maximum of 2.5MHz. When the LM5190-Q1is operating in synchronization mode, LM5190-Q1 operates in FPWM mode. If there is an RT resistor tied to AGND and a synchronization signal, the LM5190-Q1 ignores the RT resistor and synchronizes to the external clock. If there is an RT resistor tied to VCC and a synchronization signal, the synchronization signal is ignored and the LM5190-Q1operates in RT defined frequency with DRSS. Under low V_{IN} conditions when the minimum off time is reached, the synchronization signal is ignored, allowing the switching frequency to reduce to maintain output voltage regulation.

6.4.3 Thermal Shutdown

The LM5190-Q1 includes an internal junction temperature monitor. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

1. Turns off the high-side and low-side MOSFETs.
2. PG/SYNCOUT switches low.
3. Turns off the VCC regulator.
4. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 15°C (typical).

This protection is a non-latching protection, and, as such, the device cycles into and out of thermal shutdown if the fault persists.

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7 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Power Train Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing a synchronous buck regulator design. The following sections discuss the output inductor, input and output capacitors, power MOSFETs, and EMI input filter.

7.1.1.1 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at typical input voltage. Choose the inductance using 式 14.

$$L_O = \frac{V_{OUT}}{\Delta I_L \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (14)$$

Check the inductor data sheet to make sure that the saturation current of the inductor is above the peak inductor current of a particular design. Ferrite cores have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This action results in an abrupt increase in inductor ripple current and higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as the core temperature increases.

7.1.1.2 Output Capacitors

The output capacitor combined with the control loop response make sure the output voltage stays within the dynamic transient tolerance specifications. The usual boundaries restricting the output capacitor are driven by finite available PCB area, component size, and cost. The equivalent series resistance (ESR) and equivalent series inductance (ESL) of the output capacitor dominates shaping the load transient response as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for load transient events. Typically, ceramic capacitors provide low ESR to reduce the output voltage ripple and noise spikes, while tantalum or electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

図 7-1 conceptually illustrates the relevant current waveforms during both load step-down and step-up transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as fast as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

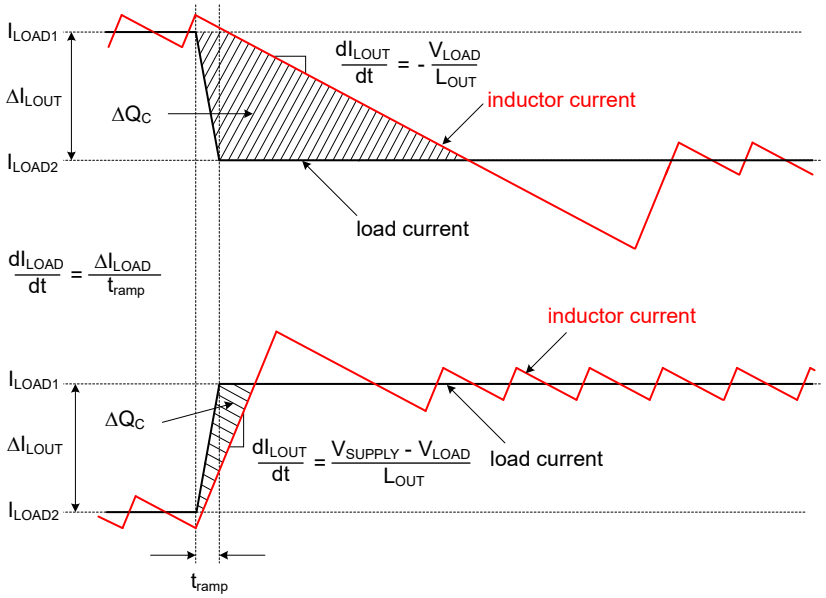

図 7-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

For example, in a typical regulator application of 12V input to 3.3V output voltage, the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 28% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{LOAD} / L_{OUT}$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below the nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and minimize the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{LOAD}), the output capacitance must be larger than:

$$C_{OUT} \geq \frac{L_{OUT} \times \Delta I_{LOAD}^2}{(V_{LOAD} + \Delta V_{OVERSHOOT})^2 - V_{LOAD}^2} \quad (15)$$

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{LOAD}, choose an output capacitance that is larger than that given by 式 16.

$$C_{OUT} \geq \frac{\Delta I_{LOUT}}{8 \times f_{SW} \times \sqrt{\Delta V_{LOAD}^2 - (R_{ESR} \times \Delta I_{LOUT})^2}} \quad (16)$$

The ESR of a capacitor is provided in the manufacturer data sheet, either explicitly as a specification or implicitly in the impedance versus frequency curve. Depending on type, size, and construction, electrolytic capacitors have significant ESR, 5mΩ and above, and relatively large ESL, 5nH to 20nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors have low-ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in 式 16 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Use 式 15 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

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A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with the low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with the large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

7.1.1.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. The input capacitor RMS current for a single-channel buck regulator is given by 式 17.

$$I_{CIN,rms} = \sqrt{D \times \left({I_{LOAD}}^2 \times (1 - D) + \frac{{\Delta I_{LOUT}}^2}{12} \right)} \tag{17}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point, the RMS current rating of the input capacitors must be greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{LOAD} − I_{SUPPLY}) during the D interval and sinks I_{SUPPLY} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak ripple voltage amplitude is given by 式 18.

$$\Delta V_{SUPPLY} = \frac{I_{LOAD} \times D \times (1 - D)}{f_{SW} \times C_{IN}} + I_{LOAD} \times R_{ESR} \tag{18}$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{SUPPLY}, is given by 式 19.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{LOAD}}{f_{SW} \times (\Delta V_{SUPPLY} - I_{LOAD} \times R_{ESR})} \tag{19}$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. Select the input bulk capacitor based on the ripple current rating and operating temperature range.

7.1.1.4 Power MOSFETs

The choice of power MOSFETs has significant impact on DC/DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS}, respectively), and vice versa. As a result, the product of $R_{DS(on)}$ and Q_G is commonly specified as a MOSFET figure-of-merit. Low thermal resistance of a given package makes sure that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection are as follows:

- $R_{DS(on)}$ at 7.5V.
- Drain-source voltage rating, BV_{DSS}.
- Gate charge parameters at 7.5V.

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- Output charge, Q_{OSS}, at the relevant input voltage.
- Body diode reverse recovery charge, Q_{RR}.
- Gate threshold voltage, $V_{GS(th)}$, derived from the Miller plateau evident in the Q_G versus V_{GS} plot in the MOSFET data sheet. To enhance MOSFET adequately, the miller plateau voltage must be 2V to 3V lower than the gate drive amplitude, especially at the minimum input voltage.

The MOSFET-related power losses for one channel are summarized by the equations presented in 表 7-1, where suffixes one and two represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and SW node ringing, are not included.

表 7-1. MOSFET Power Losses

POWER LOSS MODE	HIGH-SIDE MOSFET	LOW-SIDE MOSFET
MOSFET conduction (2) (3)	$P_{cond1} = D \times \left({I_{LOAD}}^2 + \frac{{\Delta I_{LOUT}}^2}{12} \right) \times R_{DS(on)1}$ (20)	$P_{cond2} = D' \times \left({I_{LOAD}}^2 + \frac{{\Delta I_{LOUT}}^2}{12} \right) \times R_{DS(on)2}$ (21)
MOSFET switching	$P_{sw1} = \frac{V_{SUPPLY} \times f_{SW}}{2} \times \left[\left(I_{LOAD} - \frac{\Delta I_{LOUT}}{2} \right) \times t_R + \left(I_{LOAD} + \frac{\Delta I_{LOUT}}{2} \right) \times t_F \right]$ (22)	Negligible
MOSFET gate drive(1)	$P_{gate1} = V_{CC} \times f_{SW} \times Q_{G1}$ (23)	$P_{gate2} = V_{CC} \times f_{SW} \times Q_{G2}$ (24)
MOSFET output charge(4)	$P_{Coss} = f_{SW} \times (V_{SUPPLY} \times Q_{OSS2} + E_{oss1} - E_{oss2})$ (25)	
Body diode conduction	N/A	$P_{condBD} = V_F \times f_{SW} \times \left[\left(I_{LOAD} + \frac{\Delta I_{LOUT}}{2} \right) \times t_{dt1} + \left(I_{LOAD} - \frac{\Delta I_{LOUT}}{2} \right) \times t_{dt2} \right]$ (26)
Body diode reverse recovery(5)	$P_{RR} = V_{SUPPLY} \times f_{SW} \times Q_{RR2}$ (27)	

(1) Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally added series gate resistance and the relevant driver resistance of the device.
(2) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500ppm/°C. The MOSFET junction temperature, T_J, and the rise over ambient temperature is dependent upon the device total power dissipation and the thermal impedance. When operating at or near minimum input voltage, make sure that the MOSFET $R_{DS(on)}$ is rated for the available gate drive voltage.
(3) D' = 1–D is the duty cycle complement.
(4) MOSFET output capacitances, C_{oss1} and C_{oss2}, are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turn-off. During turn-on, however, a current flows from the input to charge the output capacitance of the low-side MOSFET. E_{oss1}, the energy of C_{oss1}, is dissipated at turn-on, but this dissipation is offset by the stored energy E_{oss2} on C_{oss2}.
(5) MOSFET body diode reverse recovery charge, Q_{RR}, depends on many parameters, particularly forward current, current transition speed, and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on-time (or D interval) and typically incurs most of the switching losses. Choosing a high-side MOSFET that balances conduction and switching loss contributions is imperative. The total power dissipation in the high-side MOSFET is the sum of the losses due to conduction, switching (voltage-current overlap), output charge, and typically two-thirds of the net loss attributed to body diode reverse recovery.

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1–D interval). The low-side MOSFET switching loss is negligible as the low-side MOSFET switching loss is switched

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at zero voltage – current just communicates from the channel to the body diode or vice versa during the transition dead-times. The device, with the adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, optimizing the low-side MOSFET for low $R_{DS(on)}$ is critical. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery.

7.1.1.5 EMI Filter

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{SUPPLY(MIN)}^{2}}{P_{SUPPLY}} \right| \tag{28}$$

The passive EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.
- Input filter inductor L_F is usually selected between 1µH and 10µH, but can be lower to reduce losses in a high-current design.
- Calculate input filter capacitor C_F.

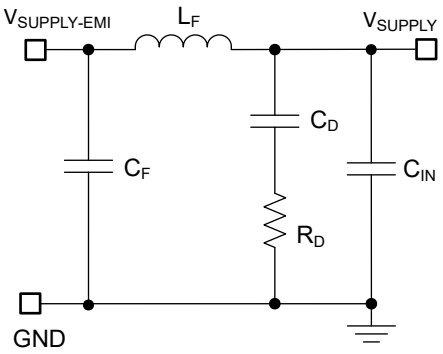

図 7-2. Passive π-Stage EMI Filter for Buck Regulator

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by 式 29.

$$Attn = 20\log\left(\frac{I_{LOUT(PEAK)}}{\pi^2 \times f_{SW} \times C_{IN}} \times \sin(\pi \times D_{MAX}) \times \frac{1}{1\mu V}\right) - V_{MAX} \tag{29}$$

where

- V_{MAX} is the allowed dBµV noise level for the applicable conducted EMI specification.
- C_{IN} is the existing input capacitance of the buck regulator.
- D_{MAX} is the maximum duty cycle.
- $I_{LOUT(PEAK)}$ is the peak inductor current.

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the passive EMI filter capacitance C_F from 式 30.

$$C_F = \frac{1}{L_F}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \times f_{SW}}\right)^2 \quad (30)$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small so that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. The resonant frequency of the passive filter is given by 式 31.

$$f_{res} = \frac{1}{2\pi \times \sqrt{L_F \times C_F}} \quad (31)$$

The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This requirement prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added input damping is needed when the output impedance of the filter is high at the resonant frequency (Q of filter formed by L_F and C_{IN} is too high). An electrolytic capacitor C_D can be used for input damping with a value given by 式 32.

$$C_D \geq 4 \times C_{IN} \quad (32)$$

Select the input damping resistor R_D using 式 33.

$$R_D = \sqrt{\frac{L_F}{C_{IN}}} \quad (33)$$

7.1.2 Error Amplifier and Compensation

図 7-3 shows a type-II compensator using a transconductance error amplifier (EA). The dominant pole of the EA open-loop gain is set by the EA output resistance, $R_{O(EA)}$, and effective bandwidth-limiting capacitance, C_{BW}, as shown by 式 34.

$$G_{EA}(s) = -\frac{g_{m(EA)} \times R_{O(EA)}}{1 + s \times R_{O(EA)} \times C_{BW}} \quad (34)$$

The EA high-frequency pole is neglected in the above expression. 式 35 calculates the compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network.

$$G_{COMP}(s) = \frac{V_{COMP}(s)}{V_{LOAD}(s)} = -\frac{V_{REF}}{V_{LOAD}} \times \frac{g_m \times R_{O(EA)} \times \left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right)} \quad (35)$$

where

- V_{REF} is the feedback voltage reference.
- $g_{m(EA)}$ is the EA gain transconductance of 1mS.
- $R_{O(EA)}$ is the error amplifier output impedance of 70MΩ.

$$\omega_{Z1} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (36)$$

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$$\omega_{P1} = \frac{1}{R_{O(EA)} \times (C_{COMP} + C_{HF} + C_{BW})} \cong \frac{1}{R_{O(EA)} \times C_{COMP}} \quad (37)$$

$$\omega_{P2} = \frac{1}{R_{COMP} \times (C_{COMP} || (C_{HF} + C_{BW}))} \cong \frac{1}{R_{COMP} \times C_{HF}} \quad (38)$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, R_{COMP} << $R_{O(EA)}$ and C_{COMP} >> C_{BW} and C_{HF}, so the approximations are valid.

LM5190-Q1 uses FB as the feedback pin for the sensed output voltage. If there is a ground offset between local ground and remote output ground, there is a regulation error due to the sensing error. In this case, AGND pin can be used with FB pin to provide a more accurate regulation. LM5190-Q1 allows AGND to deviate as much as +/-300mV with respect to PGND.

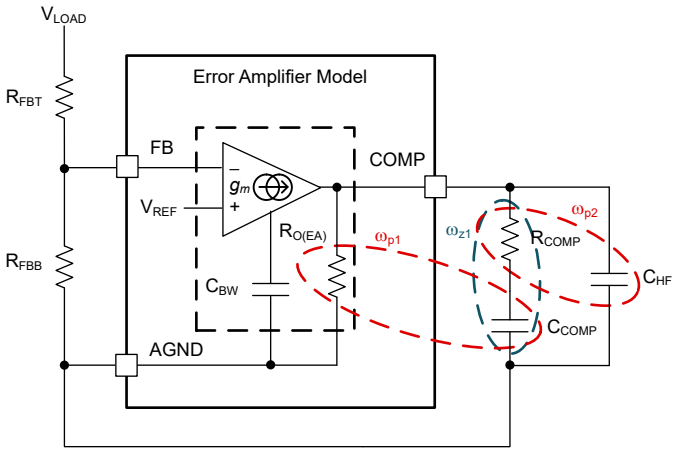

図 7-3. Error Amplifier and Compensation Network

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7.2 Typical Applications

7.2.1 High Efficiency 400kHz CC-CV Regulator

図 7-4 shows the typical schematic diagram of a CC-CV buck regulator. In this example, the CV regulation target is 12V and the CC regulation target is 8A. Full-load efficiency is 95% at 48V input. The switching frequency is set at 400kHz by resistor R_{RT}. The 12V output is connected to BIAS to reduce IC bias power dissipation and improve efficiency.

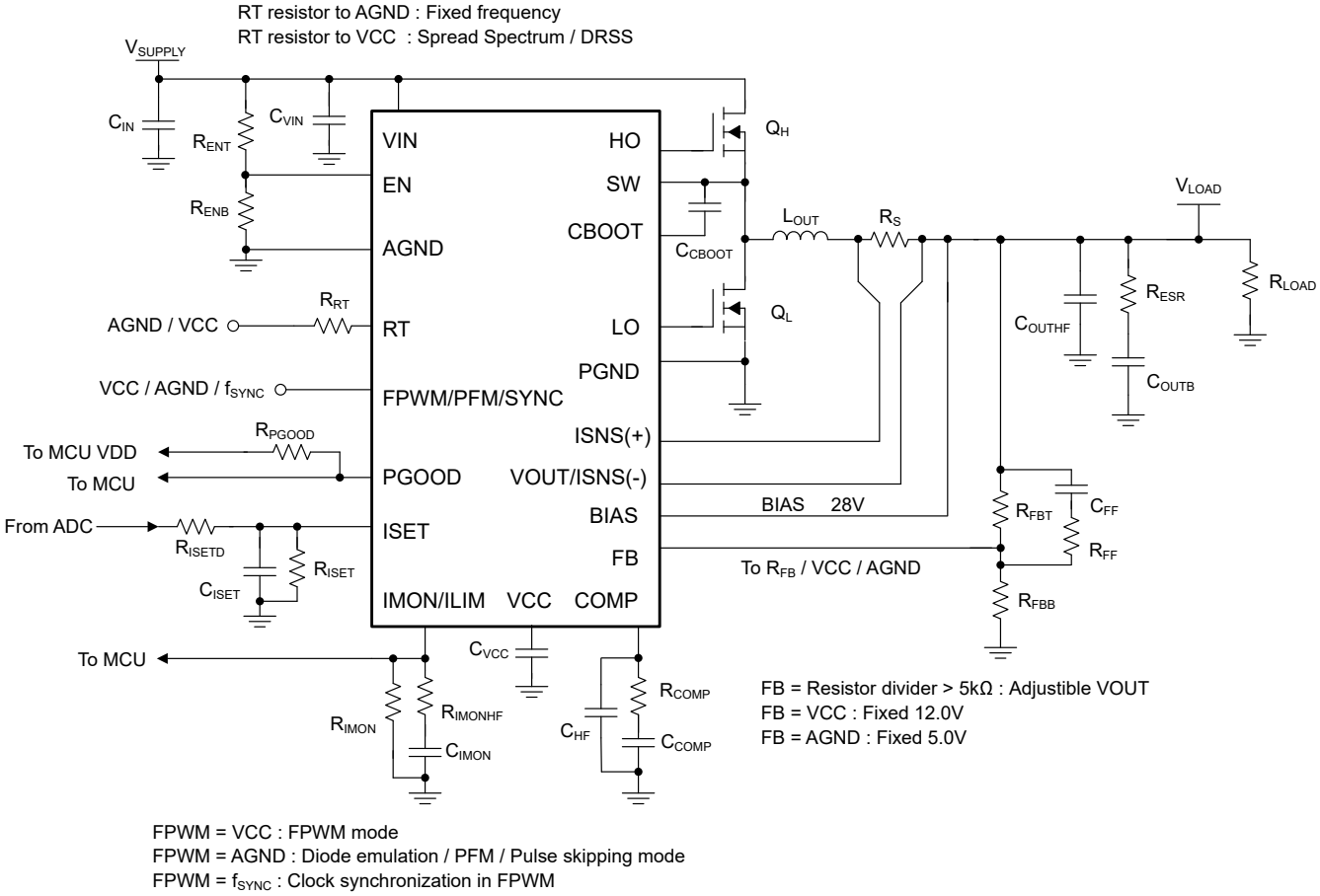

図 7-4. Typical CC-CV Buck Regulator Circuit

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Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to make sure of stability, particularly at low input voltage and high output current operating conditions. See セクション 7.3 for more details.

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7.2.1.1 Design Requirements

表 7-2 shows the intended input, output, and performance parameters for this design example.

表 7-2. Design Parameters

DESIGN PARAMETER	VALUE
Input operating range	15V / 48V / 72V (minimum/typical/maximum)
CV regulation target	12V
CC regulation target	8A
Switching frequency	400kHz

The switching frequency is set at 400KHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 28kHz with a phase margin greater than 60°.

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Custom Design With Excel Quickstart Tool

Use the Quick Start Calculator to expedite the process of designing of a regulator for a given application. Download the *Quickstart Calculator* for detailed design procedure.

7.2.1.2.2 Recommended Components

表 7-3 shows a recommended list of materials for 図 7-4. Please refer to the *LM5190-Q1 CCCV Buck Controller Evaluation Module* EVM user's guide for the complete list of materials.

表 7-3. List of Materials

QTY	REF DES	DESCRIPTION	PART NUMBER	MFR
1	C_{IN}	CAP, AL, 100uF, 100V, +/- 20%, 0.33ohm, SMD	EMVY101ATR101MKE0S	Chemi-Con
2	C_{CBOOT}, C_{ISET}	CAP, CERM, 0.1µF, VAC/100 VDC,+/- 20%, X7R, AEC-Q200 Grade 1, 0603	HMK107B7104MAHT	Taiyo Yuden
6	C_{IN}	4.7µF ±10% 100V Ceramic Capacitor X7R 1210 (3225 Metric)	CNC6P1X7R2A475K250AE	TDK
1	C_{IMON}	CAP, CERM, 0.01µF, 100V,+/- 10%, X7R, 0603	885012206114	Wurth Elektronik
1	C_{VIN}	CAP, CERM, 0.22µF, 100V,+/- 20%, X7S, AEC-Q200 Grade 1, 0603	HMK107C7224MAHTE	Taiyo Yuden
4	C_{OUT}	CAP, CERM, 22µF, 25V,+/- 10%, X7R, 1210	C1210C226K3RAC7800	Kemet
1	C_{VCC}	CAP, CERM, 2.2uF, 16V, +/- 20%, X7S, AEC-Q200 Grade 1, 0603	CGA3E1X7S1C225M080AC	TDK
1	C_{COMP}	CAP CER 0.012UF 25V C0G/NP0 0603	C0603C123J3GACTU	Kemet
1	C_{HF}	CAP, CERM, 47pF, 50V,+/- 5%, C0G/NP0, AEC-Q200 Grade 0, 0603	CGA3E2NP01H470J080AA	TDK
1	L_{OUT}	6.8µH Shielded Molded Inductor 14.8A 12.5mOhm Max Nonstandard	XGL1060-682MEC	Coilcraft
2	Q_H, Q_L	N-Channel 80V 13A (Ta), 57A (Tc) 3.7W (Ta), 73W (Tc) Surface Mount 5-DFN (5x6) (8-SOFL)	NTMFS6H848NT1G	onsemi
1	R_{IMONHF}	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
3	R_{ENT}, R_{PGOOD}, R_{FBT}	RES, 100 k, 1%, 0.1 W, 0603	RC0603FR-07100KL	Yageo
1	R_{ENB}	RES, 8.87 k, 1%, 0.1 W, 0603	RC0603FR-078K87L	Yageo
1	R_{FBB}	RES, 7.15 k, 1%, 0.1 W, 0603	RC0603FR-077K15L	Yageo
1	R_S	RES, 0.005, 1%, 2 W, 2512 WIDE	FCSL64R005FER	Ohmite
1	R_{RT}	RES, 54.9 k, 1%, 0.1 W, 0603	RC0603FR-0754K9L	Yageo
1	R_{ISETD}	RES, 4.99 k, 1%, 0.1 W, 0603	RC0603FR-074K99L	Yageo
1	R_{IMON}	RES, 9.53 k, 1%, 0.1 W, 0603	RC0603FR-079K53L	Yageo
1	R_{COMP}	RES, 5.90 k, 1%, 0.1 W, 0603	RC0603FR-075K9L	Yageo

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7.2.1.3 Application Curves

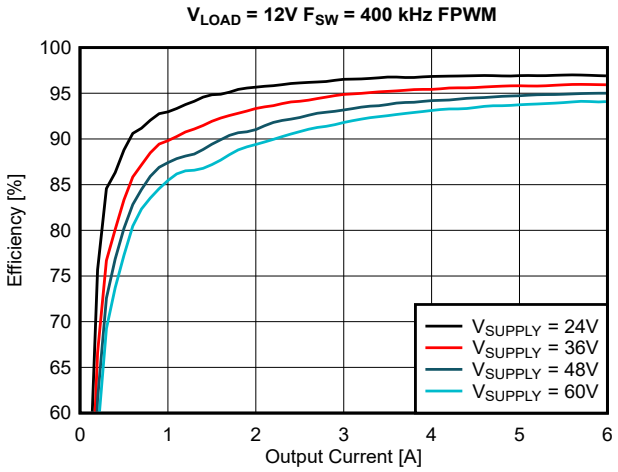

図 7-5. FPWM Mode Efficiency, Linear Scale

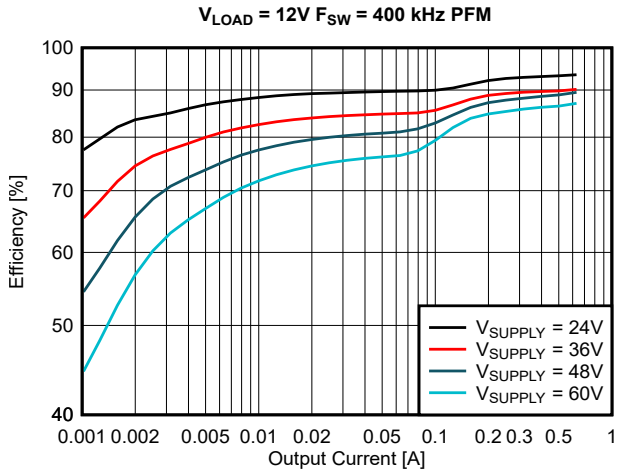

図 7-6. PFM Mode Efficiency, Log Scale

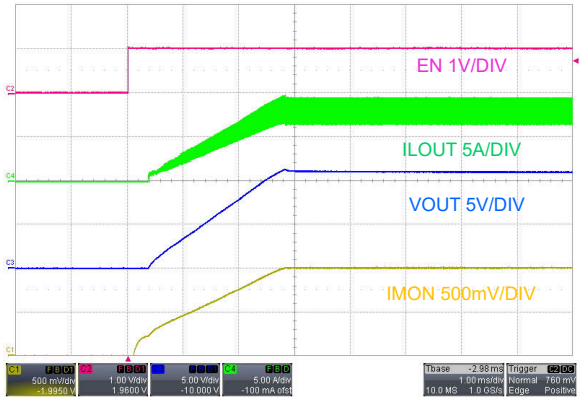

図 7-7. Start-Up, EN ON, V_{SUPPLY} = 48V, I_{LOAD} = 8A Resistive Load

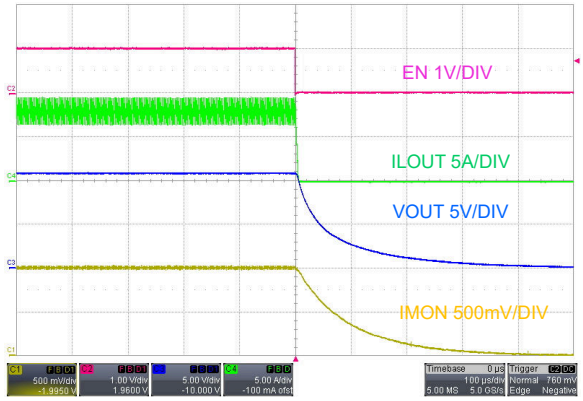

図 7-8. Shutdown, EN OFF, V_{SUPPLY} = 48V, I_{LOAD} = 8A Resistive Load

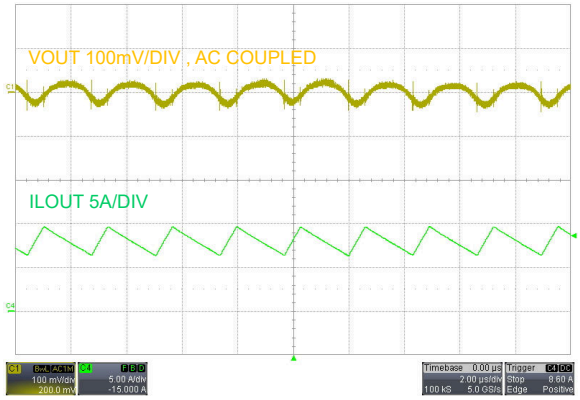

図 7-9. Output Ripple, , V_{SUPPLY} = 48V, I_{LOAD} = 8A

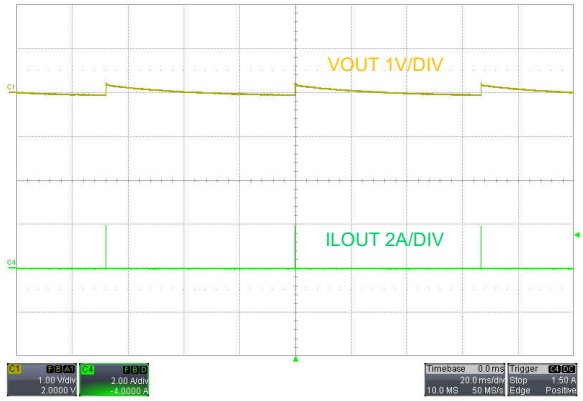

図 7-10. No Load Operation in PFM Mode, V_{SUPPLY} = 48V, I_{LOAD} = 0A

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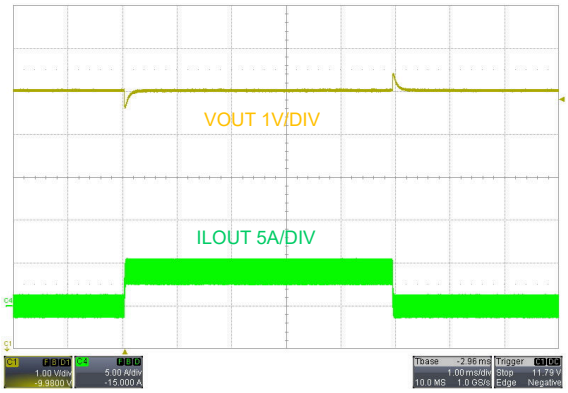

図 7-11. Load Transient Response, V_{SUPPLY} = 48V, FPWM, 0A to 4A

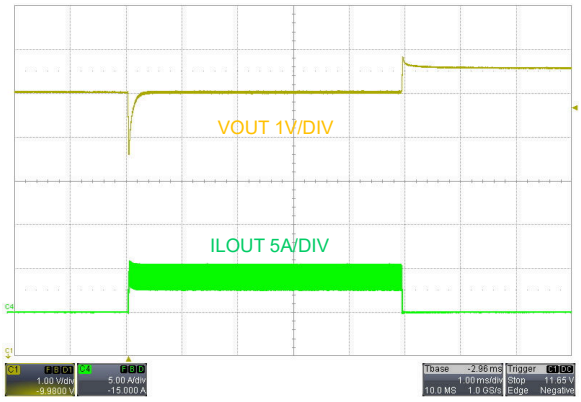

図 7-12. Load Transient Response, V_{SUPPLY} = 48V, PFM, 0A to 4A

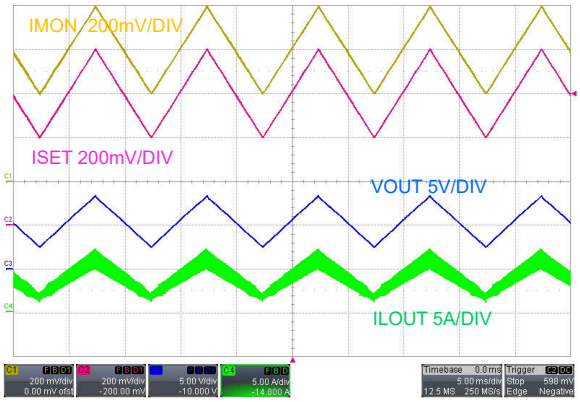

図 7-13. ISET Modulation, V_{SUPPLY} = 48V, R_{LOAD} = 1.35Ω

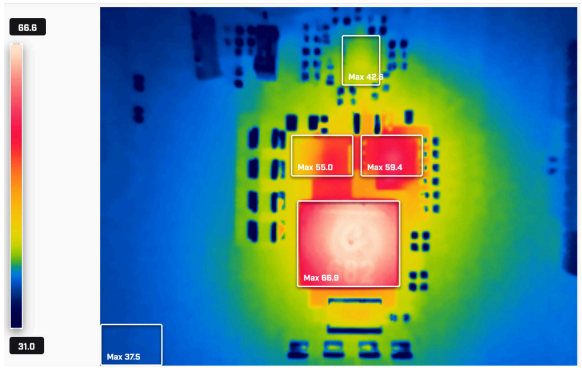

図 7-14. V_{SUPPLY} = 48V, I_{LOAD} = 8A, T_A = 25°C, No Airflow

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7.3 Power Supply Recommendations

The device is designed to operate from a wide input supply voltage range . The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* . In addition, the input supply must be capable of delivering the required input supply current to the fully loaded regulator. Estimate the average input supply current with 式 39.

$$I_{SUPPLY} = \frac{V_{LOAD} \times I_{LOAD}}{V_{SUPPLY} \times \text{Efficiency}} \quad (39)$$

If the regulator is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at the regulator input each time the input supply is cycled ON and OFF. The parasitic resistance causes the input supply voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps damp the input resonant circuit and reduce any voltage overshoots.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The *AN-2162 Simple Success With Conducted EMI From DCDC Converters* application report provides helpful suggestions when designing an input filter for any switching regulator.

7.4 Layout

7.4.1 Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuit to achieve a robust and reliable design. The high power switching loop of a buck regulator power stage is denoted by loop 1 in the shaded area of 図 7-15. The topological architecture of a buck regulator means that particularly high di/dt current flows in the components of loop 1, reducing the parasitic inductance of this loop by minimizing the effective loop area becomes mandatory. Also important are the gate drive loops of the high-side and low-side MOSFETs, denoted by 3 and 4, respectively.

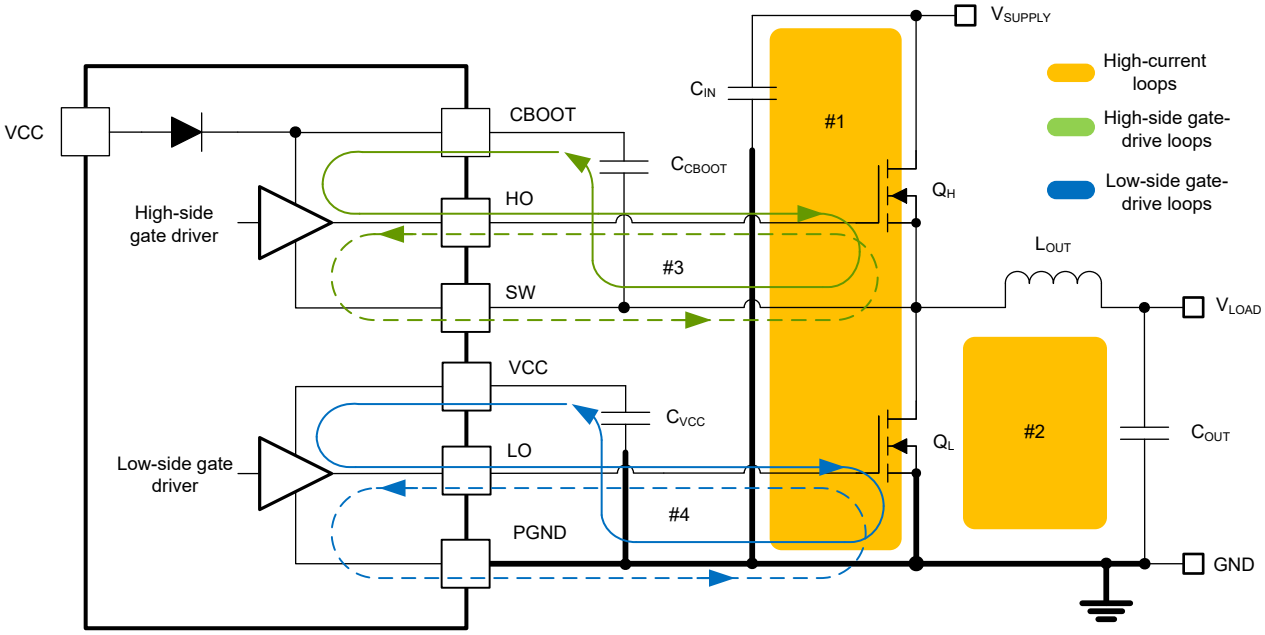

図 7-15. DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

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7.4.1.1 Power Stage Layout

- Input capacitors, output capacitors, and MOSFETs are the constituent components of the power stage of a buck regulator and are typically placed on the top side of the PCB. The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side. Insert at least one inner plane, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
- The DC/DC regulator has several high-current loops. Minimize the area of these loops to suppress generated switching noise and optimize switching performance.
  - Loop 1: The most important loop area to minimize. The path is from the input capacitor or capacitors through the high- and low-side MOSFETs, and back to the capacitor or capacitors through the ground connection. Connect the input capacitor or capacitors negative terminal close to the source of the low-side MOSFET. Similarly, connect the input capacitor or capacitors positive terminal close to the drain of the high-side MOSFET.
  - Loop 2 : Loop 2 is not as critical as loop 1. The path is from the low-side MOSFET through the inductor and output capacitor or capacitors, and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor or capacitors at ground as close as possible.
- The PCB trace defined as SW node, which connects to the source of the high-side MOSFET, the drain of the low-side MOSFET and the high-voltage side of the inductor, must be short and wide. However, the SW connection is a source of injected EMI and thus must not be too large.
- Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
- The SW pin connects to the switch node of the power conversion stage and acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop 1 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (> 50MHz) ringing at the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Make sure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

7.4.1.2 Gate-Drive Layout

Minimizing stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether series gate inductance resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop 3: high-side MOSFET, Q_H. During the high-side MOSFET turn-on, high current flows from the bootstrap capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace.
- Loop 4: low-side MOSFET, Q_L. During the low-side MOSFET turn-on, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground.

TI recommends following circuit layout guidelines when designing with high-speed MOSFET gate drive circuits.

- Connections from gate driver outputs, HO and LO, to the respective gates of the high-side or low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Be aware that peak gate drive currents can be as high as a few amperes. Use 0.65mm (25mils) or wider traces. Use via or vias, if necessary, of at least 0.mm (20 mils) diameter along these traces. Route HO and SW traces as a differential pair from the device to the high-side MOSFET, taking advantage of flux cancellation. Also, route LO trace and

PGND trace/copper area as a differential pair from the device to the low-side MOSFET, taking advantage of flux cancellation.
- Locate the bootstrap capacitor, C_{CBOOT}, close to the CBOOT and SW pins of the device to minimize the area of loop 3 associated with the high-side driver. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the device to minimize the area of loop 4 associated with the low-side driver.

7.4.1.3 PWM Controller Layout

Locate the device as close as possible to the power MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals as well as current sensing are considered in the following:
- Separate power and signal/analog traces, and use a ground plane to provide noise shielding.
- Place all sensitive analog traces and components related to COMP, FB, ISNS+, IMON, ISET, and RT away from high-voltage switching nodes such as SW, HO, LO, or CBOOT to avoid mutual coupling. Use internal layer or layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) and current sense (ISNS+ and VOUT) traces from power traces and components.
- Locate the upper and lower feedback resistors close to the FB pin, keeping the FB trace as short as possible. Route the trace from the upper feedback resistor to the required output voltage sense point at the load.
- Route the ISNS+ and VOUT sense traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor.
- Minimize the loop area from the VCC and VIN pins through the respective decoupling capacitors to the PGND pin. Locate these capacitors as close as possible to the device.

7.4.1.4 Thermal Design and Layout

The operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by the following:

- Average gate drive current requirements of the power MOSFETs
- Switching frequency
- Operating input supply voltage (affecting bias regulator LDO voltage drop and hence the power dissipation)
- Thermal characteristics of the package and operating environment

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits.

The VQFN package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. The exposed pad of the package is thermally connected to the substrate of the device. This connection allows a significant improvement in heat sinking and becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The exposed pad of the device is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value.

Numerous vias with a 0.3mm diameter connected from the thermal land to the internal and solder-side ground plane or planes are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this placement provide a plane for the power stage currents to flow but this placement also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The drain pads of the high-side MOSFETs are normally connected to a VIN plane for heat sinking. The drain pads of the low-side MOSFETs are tied to the SW plane, but the SW plane area is purposely kept as small as possible to mitigate EMI concerns.

7.4.1.5 Ground Plane Design

TI recommends using one or more of the inner PCB layers as a solid ground plane. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. In particular, a full ground plane on the layer directly underneath the power stage components is essential. Connect the source terminal of the low-side MOSFET and return terminals of the input and output capacitors to this

ground plane. Connect the PGND and AGND pins of the device at the exposed pad and then connect to the system ground plane using an array of vias under the exposed pad. The PGND nets contain noise at the switching frequency and can bounce because of load current variations. The power traces for PGND, VIN, and SW can be restricted to one side of the ground plane, for example on the top layer. The other side of the ground plane contains much less noise and is deigned for sensitive analog trace routes.

7.4.2 Layout Example

図 7-16 shows a layout example of a synchronous buck regulator with discrete power MOSFETs. The design uses an inner layer as a power-loop return path directly underneath the top layer to create a low-area switching power loop. This loop area, and hence parasitic inductance, must be as small as possible to minimize EMI as well as switch-node voltage overshoot and ringing.

The high-frequency power loop current flows through MOSFETs, through the power ground plane on the inner layer, and back to VIN through the 0603/1210 ceramic capacitors .

Six 0603 case size capacitors are placed in parallel very close to the drain of the high-side MOSFET. The low equivalent series inductance (ESL) and high self-resonant frequency (SRF) of the small footprint capacitors yield excellent high-frequency performance. The negative terminals of these capacitors are connected to the inner layer ground plane with multiple vias, further minimizing parasitic loop inductance.

Additional guidelines to improve noise immunity and reduce EMI are as follows:

- Connect PGND directly to the low-side MOSFET and power ground. Connect AGND directly to an analog ground plane for sensitive analog components. The analog ground plane for AGND and the power ground plane for PGND must be connected at a single point directly under the device at the exposed pad.
- Connect the MOSFETs directly to the inductor terminal with short copper connections (without vias) as this net has high dv/dt and contributes to radiated EMI. The single-layer routing of the switch-node connection means that switch-node vias with high dv/dt do not appear on the bottom side of the PCB. This avoids e-field coupling to the reference ground plane during the EMI test. VIN and PGND plane copper pours shield the polygon connecting the MOSFETs to the inductor terminal, further reducing the radiated EMI signature.
- Place the *EMI filter* components on the bottom side of the PCB so that the components are shielded from the power stage components on the top side.

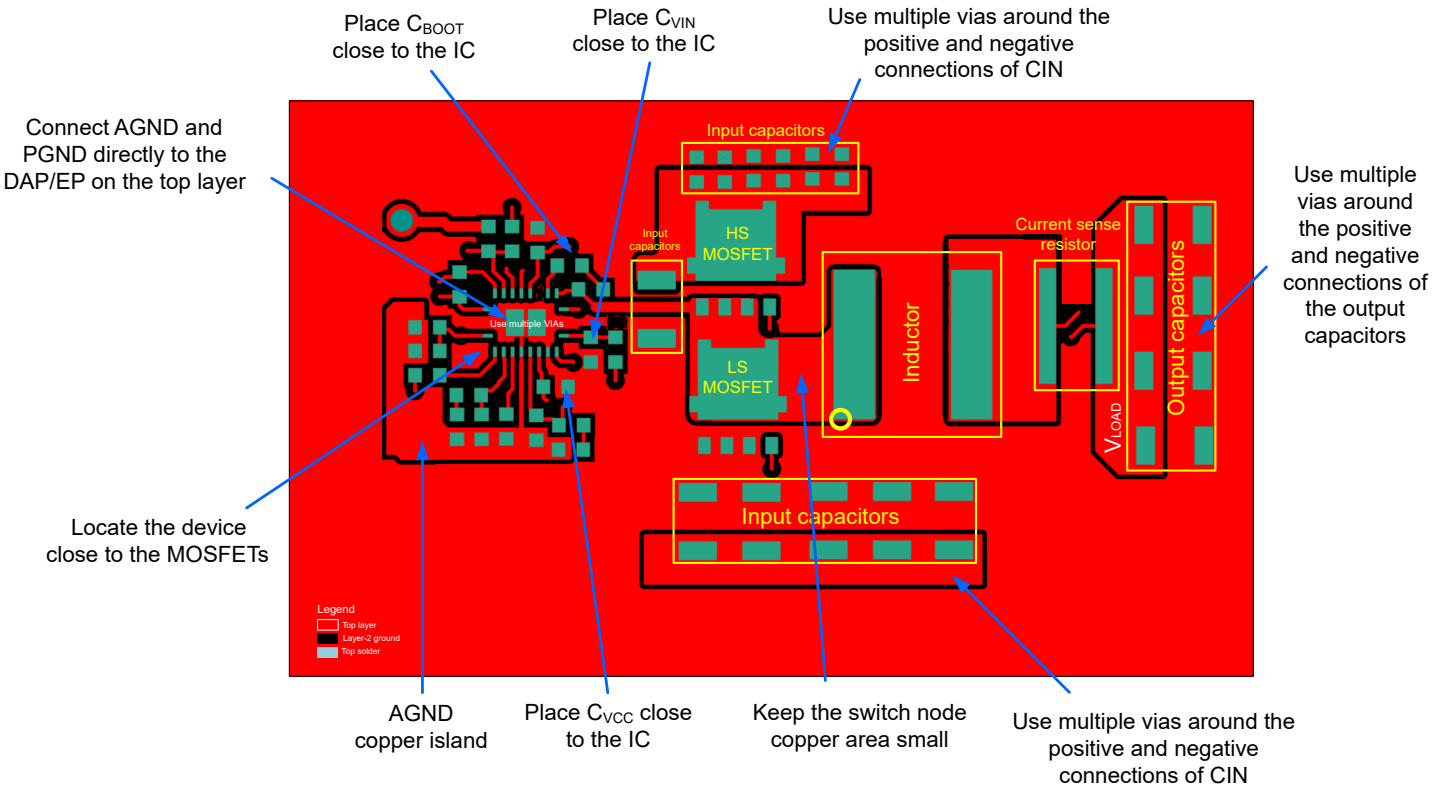

図 7-16. PCB Top Layer

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

For development support, see the following:

- For TI's reference design library, visit TI Designs
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center
- Technical articles:
  - *High-Density PCB Layout of DC/DC Converters*
  - *Synchronous Buck Controller Solutions Support Wide V_{IN} Performance and Flexibility*
  - *How to Use Slew Rate for EMI Control*

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- User's guides:
  - *LM5190-Q1 CCCV Buck Controller Evaluation Module User's Guide*
- Application reports:
  - *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout Application Report*
  - *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*
- Analog design journal:
  - *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics*
- White papers:
  - *An Overview of Conducted EMI Specifications for Power Supplies*
  - *An Overview of Radiated EMI Specifications for Power Supplies*
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*

8.2.1.1 PCB Layout Resources

- Application reports:
  - *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
  - *AN-1149 Layout Guidelines for Switching Power Supplies*
  - *AN-1229 Simple Switcher PCB Layout Guidelines*
  - *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Seminars:
  - *Constructing Your Power Supply – Layout Considerations*

8.2.1.2 Thermal Design Resources

- Application reports:
  - *AN-2020 Thermal Design by Insight, Not Hindsight*
  - *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - *Semiconductor and IC Package Thermal Metrics*
  - *Thermal Design Made Simple with LM43603 and LM43602*
  - *PowerPAD™ Thermally Enhanced Package*
  - *PowerPAD Made Easy*
  - *Using New Thermal Metrics*

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
July 2024	*	Initial release

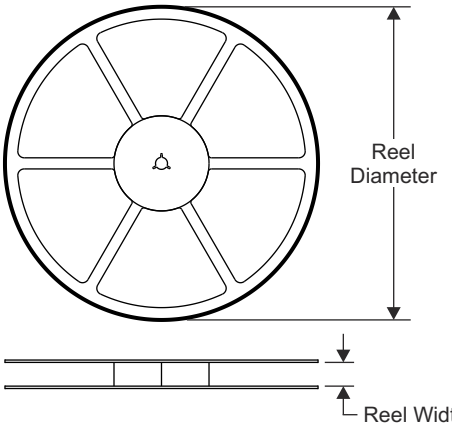
10 Mechanical, Packaging, and Orderable Information

The following pages show mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

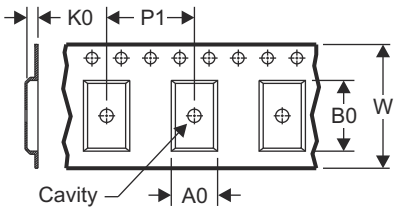
ADVANCE INFORMATION

10.1 Tape and Reel Information

REEL DIMENSIONS

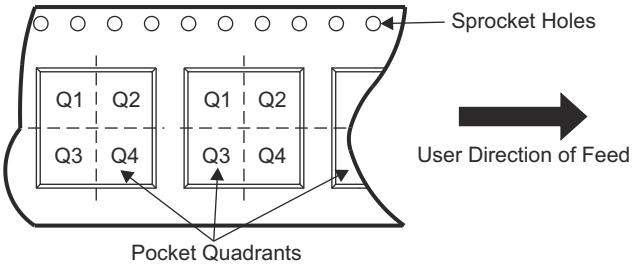


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

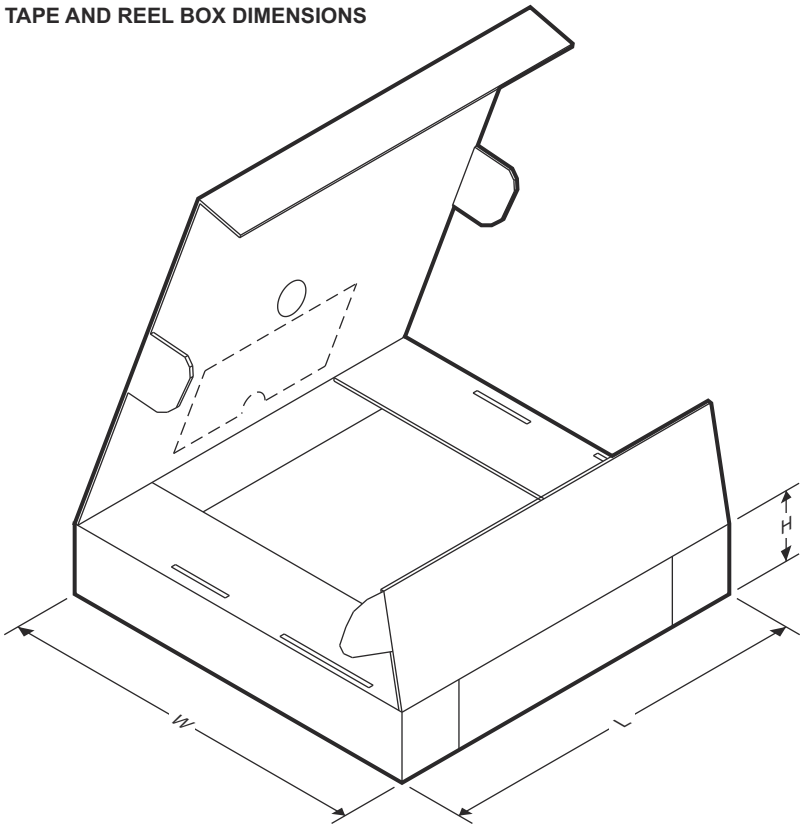
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLM5190QRGYR	VQFN	RGY	19	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



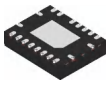
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLM5190QRGYR	VQFN	RGY	19	3000	367.0	367.0	35.0

ADVANCE INFORMATION

ADVANCE INFORMATION

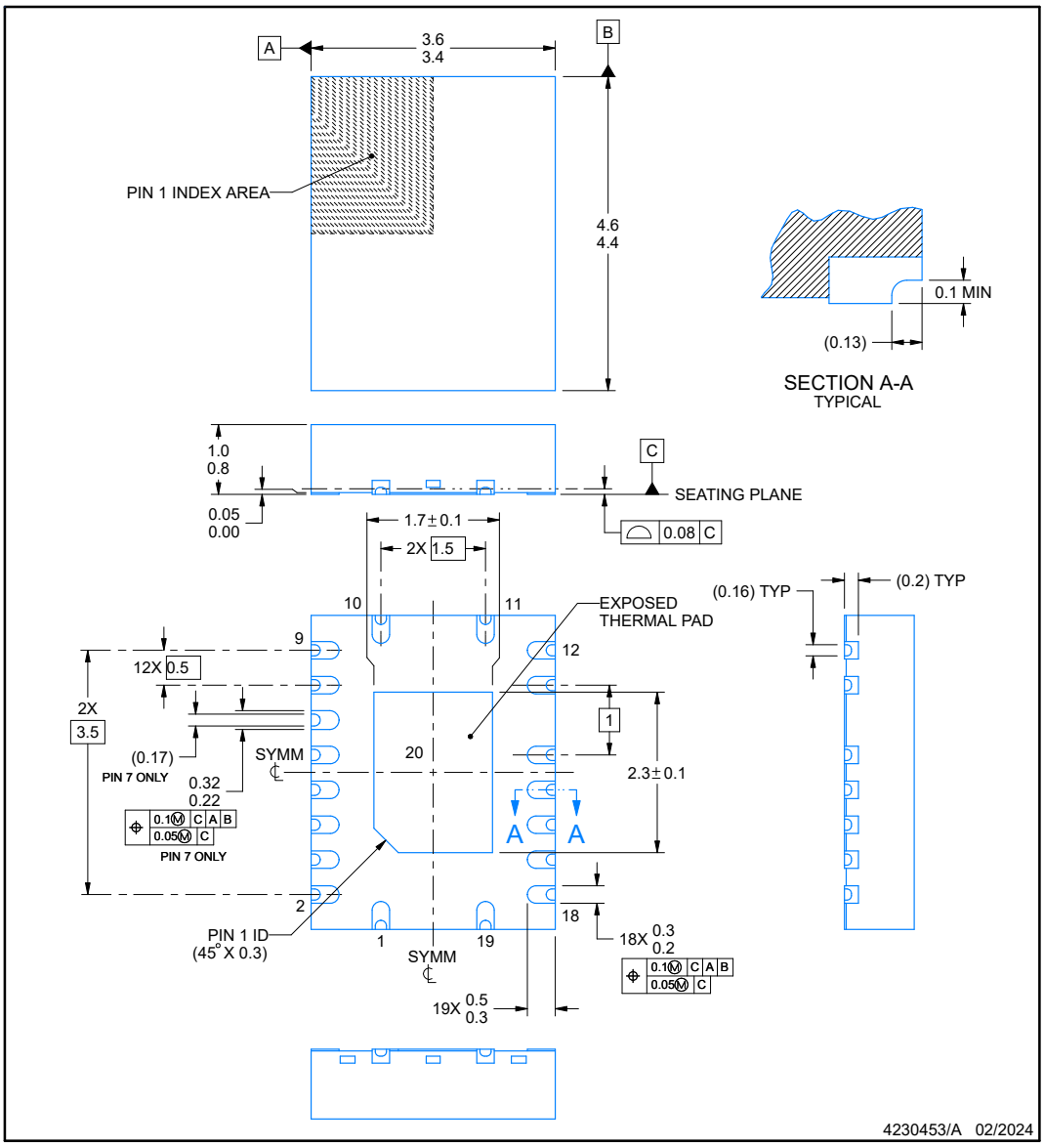
PACKAGE OUTLINE

RGY0019C



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

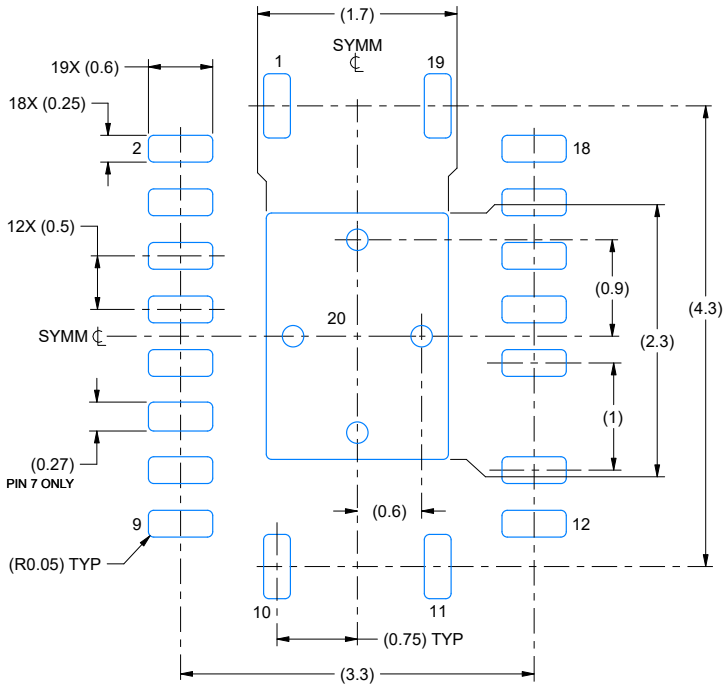
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS INSTRUMENTS
www.ti.com

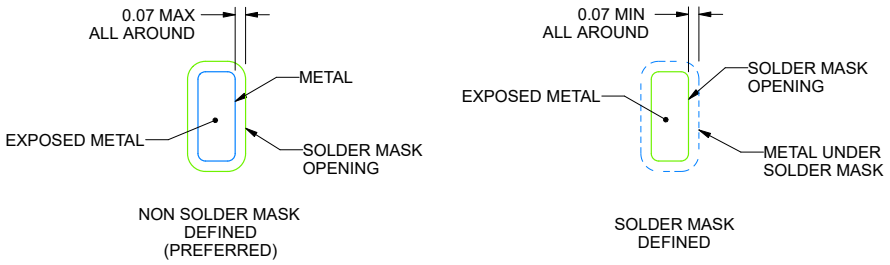
EXAMPLE BOARD LAYOUT

RGY0019C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4230453/A 02/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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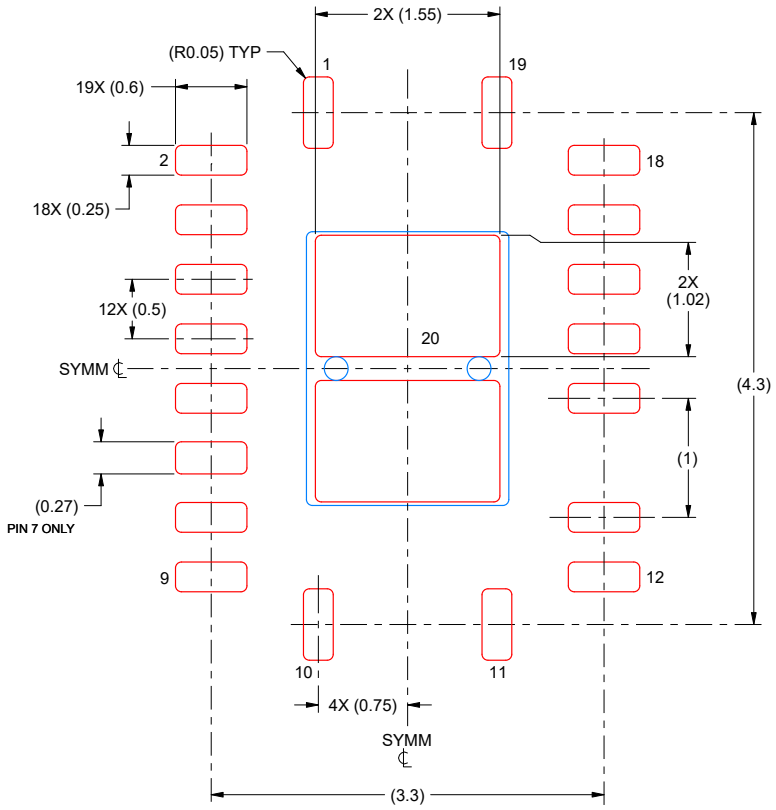
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGY0019C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4230453/A 02/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLM5190QRGYR	ACTIVE	VQFN	RGY	19	3000	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

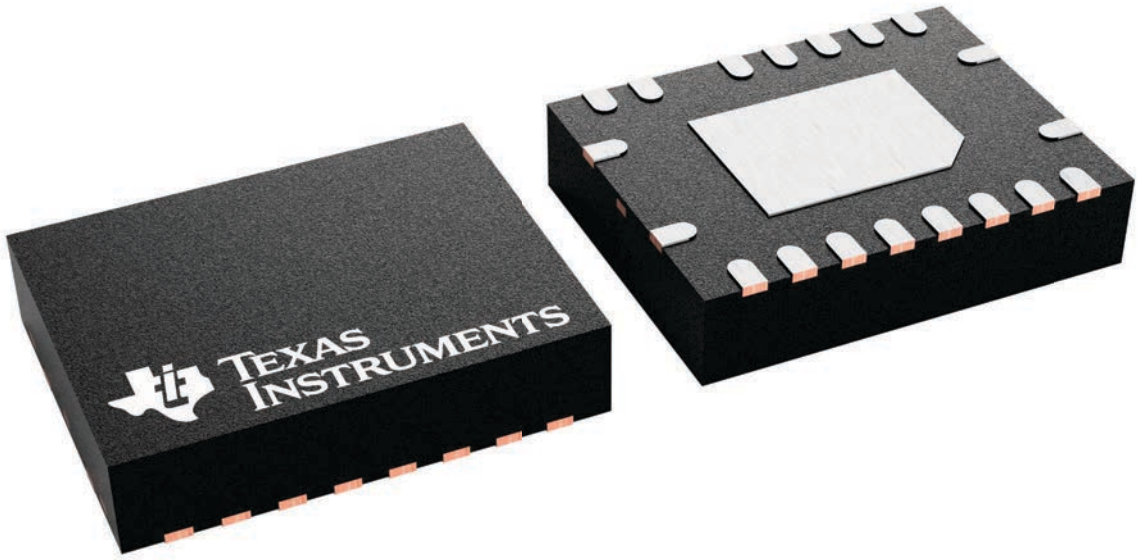
RGY 19

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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