

# LMG1210 デッドタイム調整可能な 200V、1.5A、3A ハーフ・ブリッジ MOSFET および GaN FET ドライバ、最大 50MHz のアプリケーション向け

## 1 特長

- 最大 50MHz で動作
- 10ns (標準値) の伝搬遅延
- 3.4ns のハイサイド - ローサイド間マッチング
- 最小パルス幅: 4ns
- 2つの制御入力オプション
  - デッドタイムを調整可能な1つのPWM入力
  - 独立入力モード
- 1.5A ピーク・ソースおよび 3A ピーク・シンク電流
- 外部ブートストラップ・ダイオードによる柔軟性
- 内部 LDO による電圧レールへの適応性
- 高い CMTI: 300V/ns
- HO から LO への容量が 1pF 未満
- UVLO および過熱保護
- 低インダクタンスの WQFN パッケージ

## 2 アプリケーション

- 高速 DC-DC コンバータ
- RF エンベロープ・トラッキング
- Class-D オーディオ・アンプ
- Class-E ワイヤレス充電
- 高精度のモータ制御

## 3 概要

超高周波数高効率アプリケーション用に設計された LMG1210 は、調整可能なデッドタイム機能、非常に小さい伝播遅延、3.4ns のハイサイドとローサイドのマッチングといったシステム効率を最適化する特長を備えた、200V のハーフ・ブリッジ MOSFET および窒化ガリウム電界効果トランジスタ (GaN FET) ドライバです。この製品は、電源電圧にかかわらず 5V の電圧で確実にゲートを駆動する LDO も備えています。

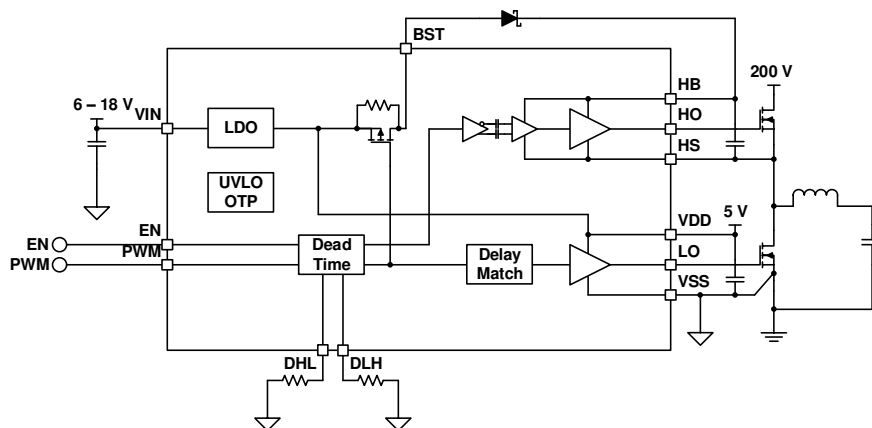
各種のアプリケーションで最高の性能を実現するため、LMG1210 では設計者が、ハイサイドのブートストラップ・コンデンサを充電するために最適なブートストラップ・ダイオードを選択できます。ローサイドがオフのときは内部スイッチによりブートストラップ・ダイオードがオフになり、ハイサイド・ブートストラップの過充電を効果的に阻止するとともに、逆方向回復充電を最小限にします。スイッチング損失の増大を抑えるため、GaN FET 両端での追加寄生容量が 1pF 未満に最小化されています。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
LMG1210	WQFN (19)	3.00mm×4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 代表的なアプリケーションの概略図



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## 4 改訂履歴

Revision C (December 2018) から Revision D に変更		Page
•	Changed Maximum High-side dynamic current from 0.61mA/MHz to 0.7mA/MHz	6

Revision B (November 2018) から Revision C に変更		Page
•	ミスマッチを 2.5ns から 3.4ns に変更	1
•	最小パルス幅を 3ns から 4ns に変更	1
•	Changed Reordered Pin Functions table in alphabetical order	4
•	追加 Figure 14 IIM Timing Diagram	11
•	追加 CMTI performance reference app note	14
•	追加 charge per cycle removed from the bootstrap due to dynamic high side current	18
•	追加 Power Consumption Calculation reference app note	20

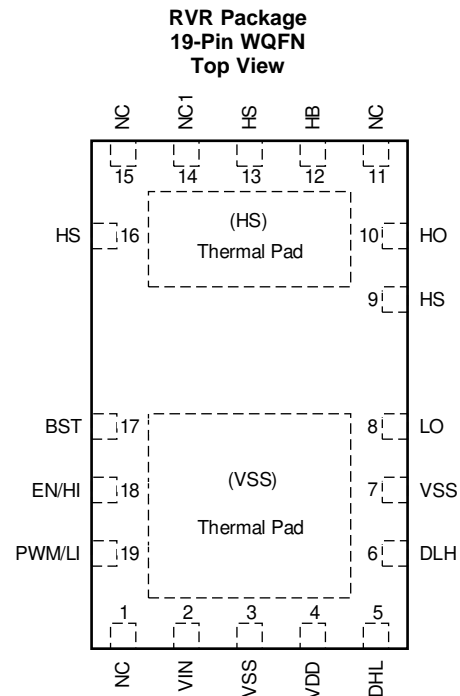
  

Revision A (May 2018) から Revision B に変更		Page
•	マーケティング・ステータスを「製品プレビュー」から「最終版」に変更	1

## 5 概要（続き）

LMG1210 には、独立入力モード (IIM) と PWM モードの 2 つの制御入力モードがあります。IIM では、各出力が専用の入力によって別に制御されます。PWM モードでは、単一の入力から 2 つの補完的な出力信号が生成され、ユーザーは各エッジについてデッド・タイムを 0 ~ 20ns の範囲で調整できます。LMG1210 は -40°C ~ 125°C の広い温度範囲で動作し、低インダクタンスの WQFN パッケージで供給されます。

## 6 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
BST	17	O	Bootstrap diode anode connection point.
DHL	5	I	Sets the dead time for a high-to-low transition in PWM mode by connecting a resistor to VSS. If using IIM this pin can be left floating, tied to GND, tied to VDD.
DLH	6	I	Sets the dead time for a low-to-high transition in PWM mode by connecting a resistor to VSS. Tie to VDD to select IIM.
EN/HI	18	I	Enable input or high-side driver control. In PWM mode this is the EN pin. In IIM mode this is the HI pin.
PWM/LI	19	I	PWM input or low-side driver control. In PWM mode this is the PWM pin. In IIM mode this is the LI pin.
HB	12	I	High-side driver supply. Bootstrap diode cathode connection point.
HO	10	O	High-side driver output.
HS	9,13,16	I	Switch node and high-side driver ground. These pins are internally connected.
LO	8	O	Low-side driver output.
NC	1,11,15	—	Not internally connected.
NC1	14	I	For proper operation, this pin should be either unconnected or tied to HS.
Thermal Pad (HS)	21	I	Connected to HS.
Thermal Pad (VSS)	20	I	Connected to VSS.
VDD	4	O	Low-side driver supply and LDO output. 5 V
VIN	2	I	6 V to 18 V input to LDO. If LDO is not required, connect to VDD.
VSS	3,7	—	Low-side ground return: all low-side signals are referenced to this ground.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{IN}$	Input Supply Voltage	-0.5	20	V
$V_{DD}$	5V Supply Voltage	-0.5	5.5	V
$V_{HS}$	High Side Voltage Without Bootstrap Diode	-300	300	V
$V_{HB}-V_{HS}$	Bootstrap supply voltage, continuous	-0.5	5.5	V
$V_{LI}/P_{WM}, V_{HI}/EN$	Input Pin Voltage on LI or HI	-0.5	10	V
$V_{DHL}, V_{DLH}$	Voltage on DLH and DHL pins	-0.5	$V_{DD} + 0.5$	V
$V_{LO}$	Low-side gate driver output	-0.5	$V_{DD} + 0.5$	V
$V_{HO}$	High-side gate driver output	$V_{HS}-0.5$	$V_{HB}+ 0.5$	V
$V_{BST}$	Bootstrap pin voltage	-0.5	$V_{DD} + 0.5$	V
$T_J$	Operating Junction Temperature Range	-40	150	°C
$T_{STG}$	Storage Temperature	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±XXX V may actually have higher performance.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±YYY V may actually have higher performance.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input Supply Voltage (if using internal LDO)	6		18	V
$V_{DD}$	5V Supply Voltage (if bypassing internal LDO)	4.75	5.00	5.25	V
$V_{HS}-V_{SS}$	High-Side Voltage Without Bootstrap diode <sup>(1)</sup>	-200		200	V
$V_{HB}-V_{HS}$	Bootstrap Supply Voltage	3.80		5.25	V
$V_{LI}, V_{HI}$	Input Pin Voltage	-0.3		10	V
$T_J$	Operating Junction Temperature Range	-40		125	°C
CMTI	High Side Slew Rate			300	V/ns
$R_{DHL}, R_{DLH}$	Dead Time Adjustment External Resistance	20		1800	kΩ
$V_{DT}$	Dead Time Voltage Range	0.8		1.8	V

- (1) If using a bootstrap diode, actual negative HS pin voltage may be more limited, see [Section 7.3.6](#) for details.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMG1210	
		RVR (QFN)	UNIT
		19 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	40.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	40	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	16.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	16.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

VDD=5V, HB-HS=4.6V, outputs unloaded over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
I <sub>DD</sub>	Quiescent Current for Low-Side Circuits Only, V <sub>in</sub> =6V, powered through LDO	LI, HI=0V, Independent Mode		300	475	μA
		EN=0V, PWM=X, PWM Input Mode, R <sub>DHL</sub> and R <sub>DLH</sub> = 1.78MΩ		380	550	μA
I <sub>HB</sub>	HB Quiescent Current	HI=0V, Independent Mode		520	850	μA
I <sub>HBS</sub>	HB to V <sub>SS</sub> Quiescent Current	V <sub>HS</sub> =100V		1		nA
I <sub>HBSO</sub>	HB to V <sub>SS</sub> Operating Current	V <sub>HS</sub> =100V, F <sub>SW</sub> =1MHz		1		nA
I <sub>LSDyn</sub>	Low-side dynamic current	Unloaded, PWM Mode		1	1.25	mA/MHz
I <sub>HSDyn</sub>	High-side dynamic current	Unloaded		0.5	0.7	mA/MHz
<b>LOW-SIDE TO HIGH-SIDE CAPACITANCE</b>						
C <sub>ISO</sub>	Capacitance from High to Low Side	Low Side Pins Shorted Together, High Side Pins Shorted Together		0.25		pF
<b>5V LDO</b>						
V <sub>5V</sub>	LDO Output	V <sub>IN</sub> =10V	4.75	5.00	5.25	V
V <sub>DO</sub>	Dropout Voltage	I <sub>O</sub> =100mA		400	750	mV
I <sub>LDOM</sub>	Maximum Current	V <sub>IN</sub> =12V	100			mA
I <sub>SC</sub>	Short Circuit Current	V <sub>IN</sub> =12V	105		250	mA
C <sub>OUT</sub>	Minimum Required Output Capacitance <sup>(1)</sup>	Effective Capacitance at Bias Voltage			0.3	μF
<b>DIGITAL INPUT PINS (LI/PWM &amp; HI/EN)</b>						
V <sub>IR</sub>	Input Rising Edge Threshold		1.70		2.45	V
V <sub>IF</sub>	Input Falling Edge Threshold		0.70		1.30	V
V <sub>IHYS</sub>	Input Hysteresis			1		V
R <sub>IPD</sub>	Input Pull-Down Resistance	V <sub>LI</sub> , V <sub>HI</sub> =1V	100	200	300	kΩ
<b>UNDERVOLTAGE LOCKOUT</b>						
V <sub>DDR</sub>	V <sub>DD</sub> Rising Threshold		4.00	4.25	4.50	V
V <sub>DDF</sub>	V <sub>DD</sub> Falling Threshold		3.8	4.05	4.3	V
V <sub>DDH</sub>	V <sub>DD</sub> Hysteresis			200		mV
V <sub>HBR</sub>	HB-HS Rising Threshold		3.40	3.55	3.8	V
V <sub>HBF</sub>	HB-HS Falling Threshold		3.30	3.45	3.65	V
V <sub>HBH</sub>	HB-HS Hysteresis			130		mV
<b>BOOTSTRAP DIODE SWITCH</b>						
R <sub>SW</sub>	Diode Switch On Resistance	I <sub>D</sub> =100mA		0.4		Ω
<b>GATE DRIVER</b>						
V <sub>OL</sub>	Low-Level Output Voltage	I <sub>OL</sub> =100mA			0.16	V

(1) Ensured by design

**Electrical Characteristics (continued)**

VDD=5V, HB-HS=4.6V, outputs unloaded over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>DD</sub> -V <sub>OH</sub>	High-Level Output Voltage	I <sub>OH</sub> = -100mA			0.30	V
I <sub>OL</sub>	Peak Sink Current	V <sub>LO</sub> ,V <sub>HO</sub> =5V	2.0	3.1	4.3	A
I <sub>OH</sub>	Peak Source Current	V <sub>LO</sub> ,V <sub>HO</sub> =0V	0.85	1.58	2.4	A
V <sub>CLAMP</sub>	Unpowered Gate Clamp Voltage	V <sub>DD</sub> , V <sub>HB</sub> Floating, 1 mA pull-up applied to LO/HO		0.55	0.8	V
<b>THERMAL SHUTDOWN</b>						
T <sub>SD</sub>	Thermal Shutdown Switching, Rising Edge <sup>(2)</sup>		150			°C
T <sub>SD_LDO</sub>	Thermal Shut Down LDO, Rising Edge <sup>(2)</sup>		160			°C
T <sub>HYS_SD</sub>	Thermal Hysteresis, LDO & Switching <sup>(2)</sup>		3	10		°C
T <sub>SD_HS</sub>	Thermal Shutdown for High-Side, Rising Edge <sup>(2)</sup>		160			°C
<b>DEADTIME CONTROL RESISTORS</b>						
R <sub>PU</sub>	Internal Pullup Resistor		23.5	25	27	kΩ

(2) Ensured by design

## 7.6 Switching Characteristics

 $V_{DD}=5V$ ,  $V_{HB-HS}=4.6V$ , outputs unloaded over operating junction temperature range (unless otherwise noted)

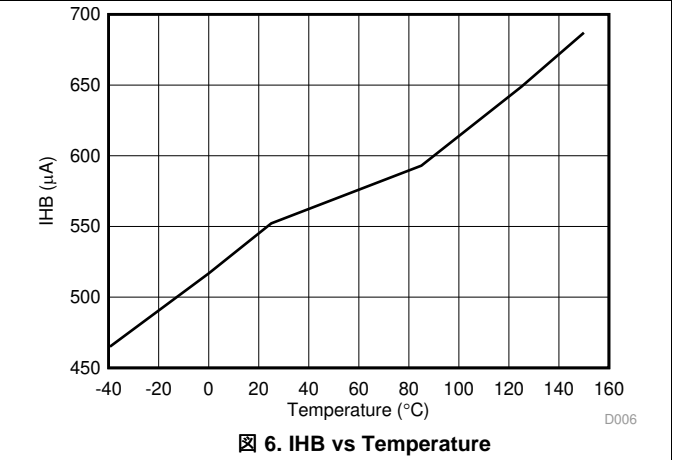
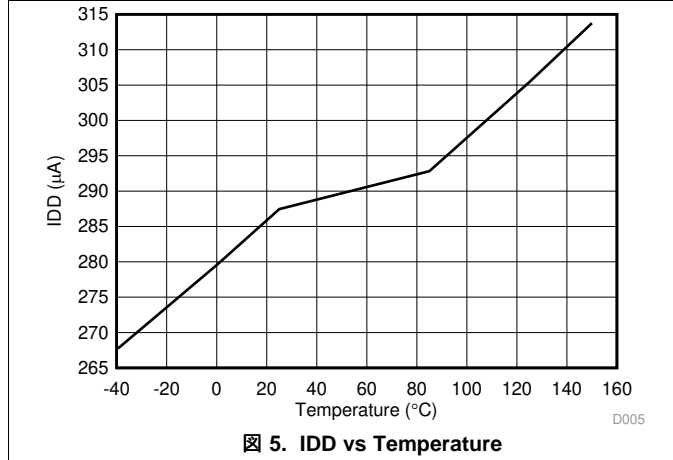
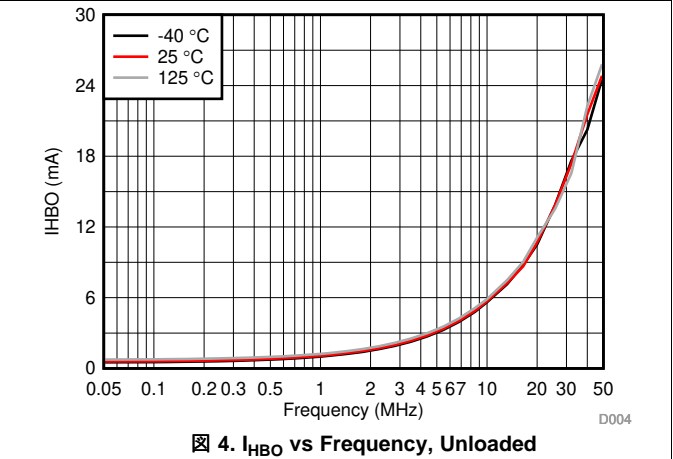
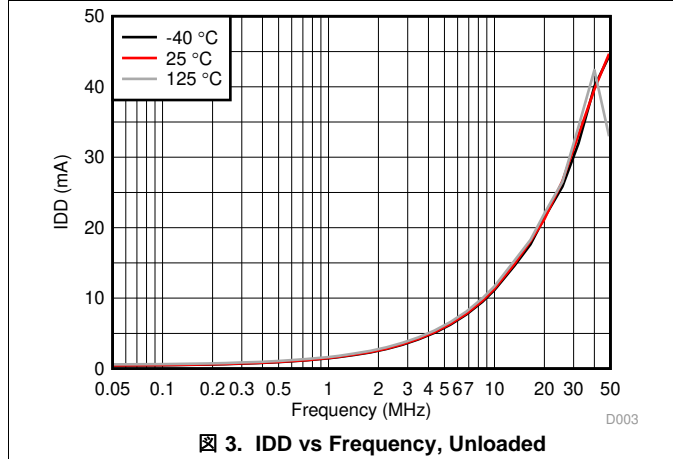
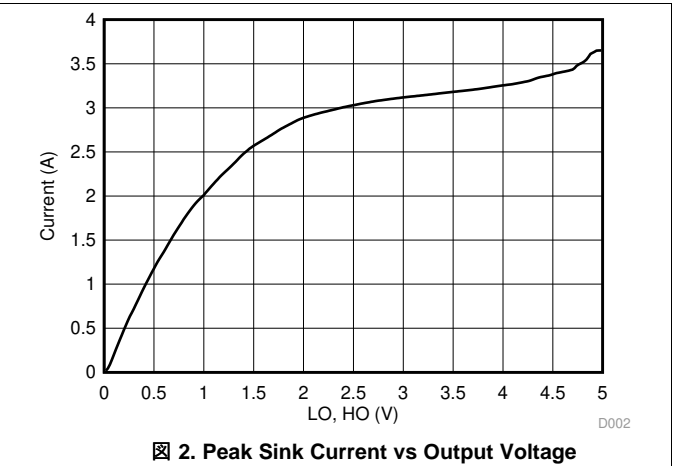
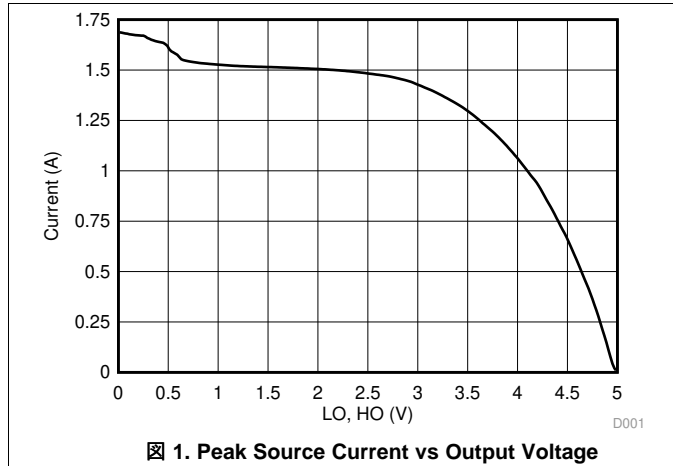
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INDEPENDENT INPUT MODE</b>						
$t_{PHL}$	Turn-Off Delay			10	18	ns
$t_{PLH}$	Turn-On Delay			10	18	ns
$t_{MTCH}$	High-Off to Low-On and Low-Off to High-On Delay Mismatch	Over temperature, $T_{jHI}=T_{jLO}$		1	3.4	ns
<b>PWM INPUT MODE</b>						
$t_{PHL}$	Turn-Off Delay	PWM rising to LO falling and PWM falling to HO falling		11	21	ns
$t_{DEAD\_MIN}$	Minimum Dead Time	$R_{ext}=1.78\text{ M}\Omega$	-0.55	0.8	3.1	ns
$t_{DEAD\_MAX}$	Maximum Dead Time	$R_{ext}=20\text{ k}\Omega$	16	20	26	ns
$t_{EN}$	Enable Propagation Time			11	20	ns
<b>OTHER CHARACTERISTICS</b>						
$t_{OR}$	Output Rise Time, Unloaded	10%-90%		0.5		ns
$t_{OF}$	Output Fall Time, Unloaded	90%-10%		0.5		ns
$t_{ORL}$	Output Rise Time, Loaded	$C_O=1\text{ nF}$ , 10%-90%		3.5	5.6	ns
$t_{OFL}$	Output Fall Time, Loaded	$C_O=1\text{ nF}$ , 90%-10%		2.3	3.3	ns
$t_{PW}$	Minimum Input Pulse Width <sup>(1)</sup>	Minimum input pulse width which changes the output		1.8	4.0	ns
$t_{PW,ext}$	H-L-H Pulse extender width <sup>(1)</sup>	Unloaded <sup>(2)</sup>		4.5	10	ns
$t_{STLS}$	Start-Up Time of low side after VDD-GND goes over UVLO threshold.	Independent Control Mode		25	60	$\mu\text{s}$
		PWM Control Mode		100	150	$\mu\text{s}$
$t_{STHS}$	Start-Up Time of High-Side After $V_{HB}-V_{HS}$ Goes Above UVLO			16	28	$\mu\text{s}$
$t_{PWD}$	Pulse-Width Distortion	$ t_{PLH}-t_{PHL} $ , Independent Input Mode		1	3	ns

(1) Ensured by design

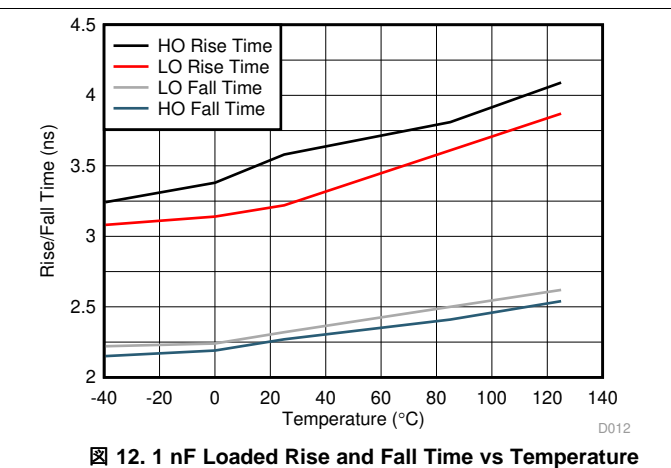
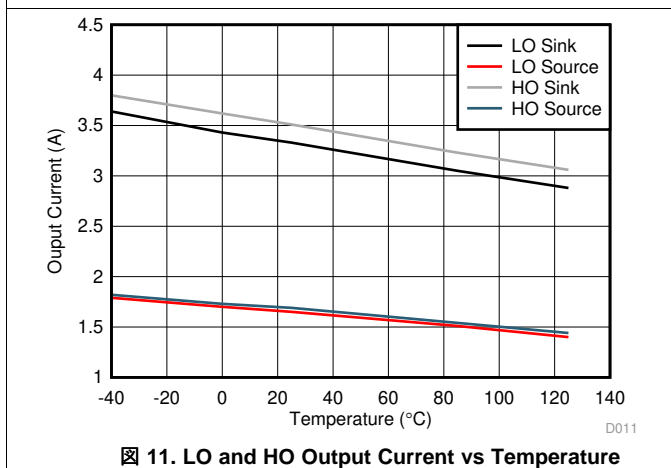
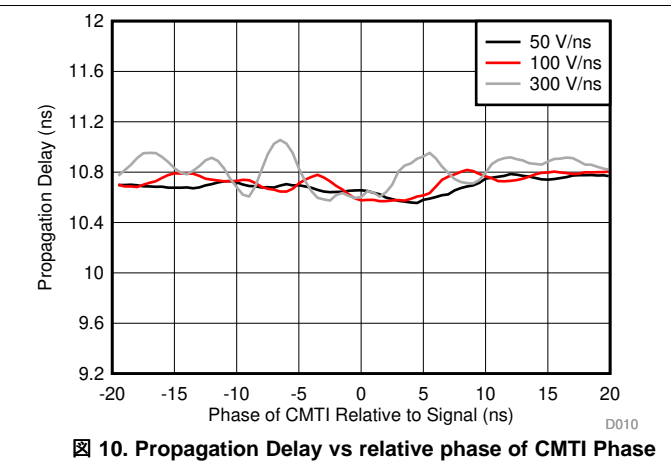
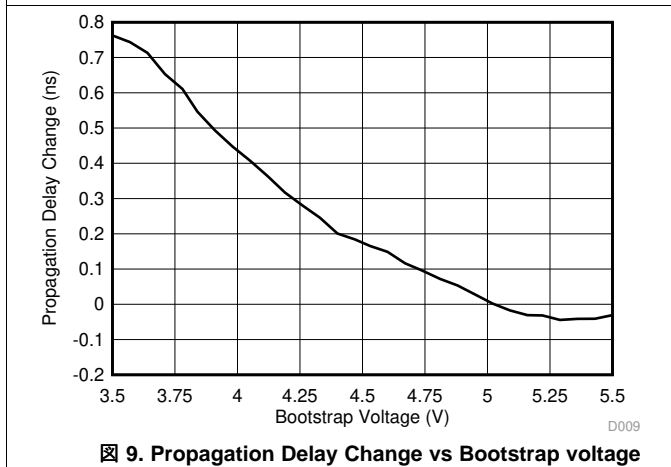
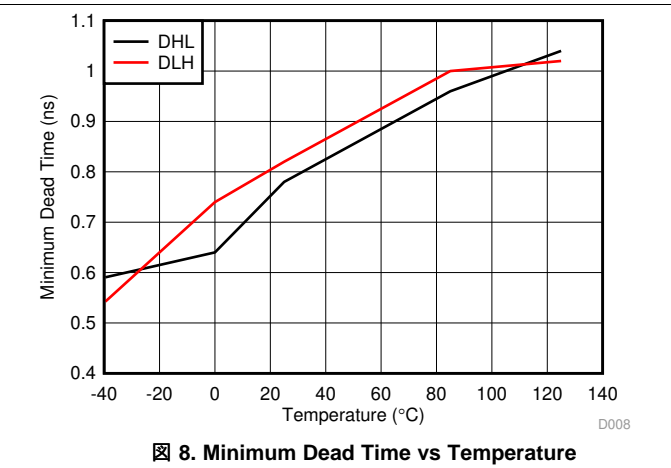
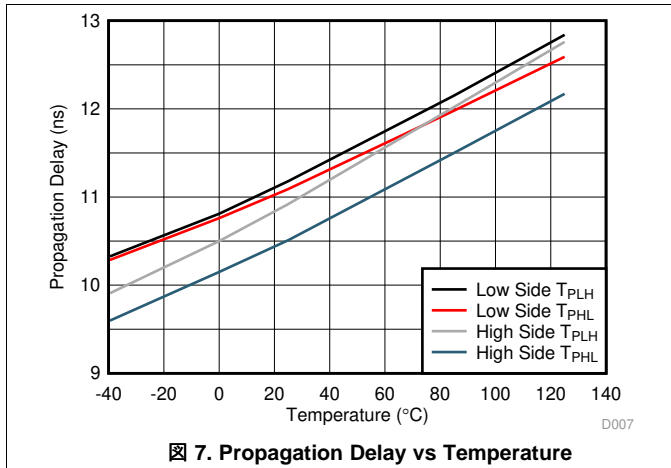
(2) Pulses longer than  $t_{PW}$ , but shorter than  $t_{PW,ext}$  get extended to  $t_{PW,ext}$



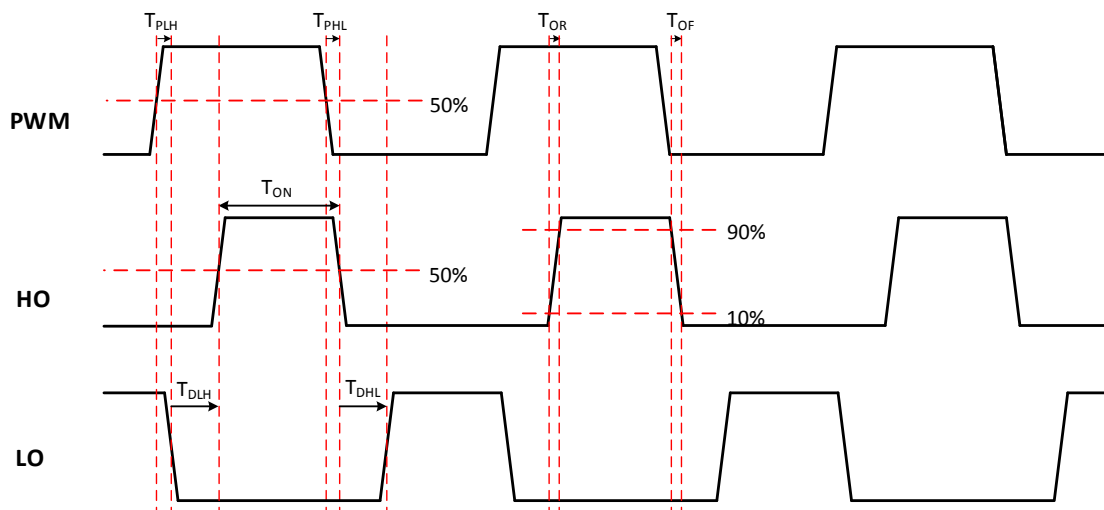
### 7.7 Typical Characteristics



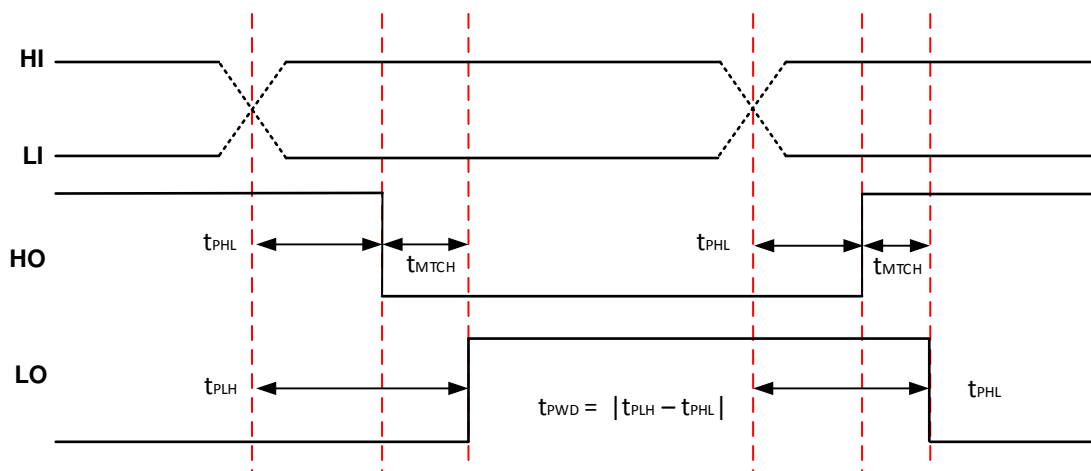
Typical Characteristics (continued)



### 7.8 Timing Diagrams



⊠ 13. Timing diagram of LMG1210 in PWM mode under no load condition



⊠ 14. Timing diagram of LMG1210 in IIM mode under no load condition

## 8 Detailed Description

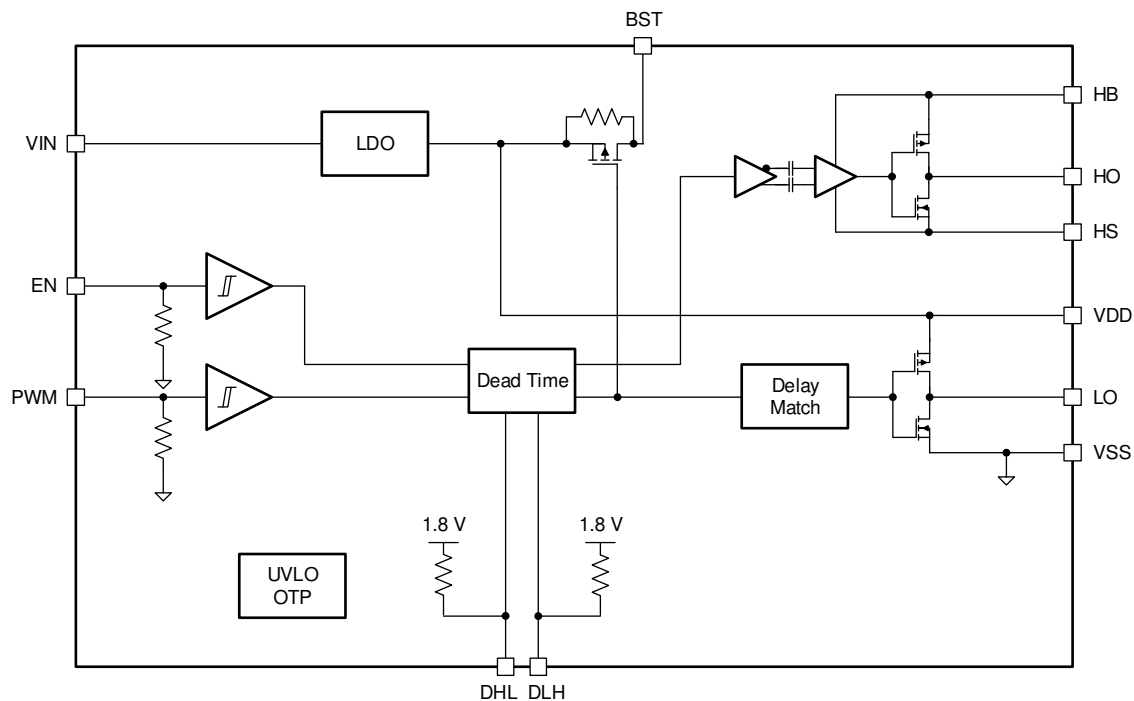
### 8.1 Overview

The LMG1210 is a high-speed half-bridge driver specifically designed to work with enhancement mode GaN FETs. Designed to operate up to 50 MHz, the LMG1210 is optimized for maximum performance and highly efficient operation. This includes reducing additional capacitance at the switch node (HS) to less than 1 pF and increased dV/dt noise immunity up to 300 V/ns on the HS pin to minimize additional switching losses. By having a 21 ns maximum propagation delay with 3.4 ns maximum mismatch, excessive dead times can be greatly reduced.

Auxiliary input voltages applied above 5 V enables an internal LDO to precisely regulate the output voltage at 5-V, preventing damage on the gate. An external bootstrap diode allows the designer to select an optimal diode. An integrated switch in series with the bootstrap diode stops overcharging of the bootstrap capacitor and decreases  $Q_{rr}$  losses in the diode.

The LMG1210 comes in a low-inductance WQFN package designed for small gate drive loops with minimal voltage overshoot.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The LMG1210 provides numerous features optimized for driving external GaN FETs.

#### 8.3.1 Bootstrap Diode Operation

An internal low impedance switch enables the bootstrap only when the low-side GaN FET is on. If used in a converter where the low-side FET operates in third quadrant conduction during the dead times, this provides two main benefits. First, it stops the bootstrap diode from overcharging the high-side bootstrap rail. Second, if using a p-n junction diode with  $Q_{rr}$  as the bootstrap diode, it decreases the  $Q_{rr}$  losses of the diode. There is a 1 k $\Omega$  resistor connected between the drain and source of this internal bootstrap switch to allow the bootstrap capacitor to slowly charge at start-up before the low-side FET is turned on.

## Feature Description (continued)

The part does not have an actual clamp on the high-side bootstrap supply. The bootstrap switch disables conduction during the dead times, and the actual bootstrap capacitor voltage is set by the operating conditions of the circuit during the low-side on-time. The bootstrap voltage can be approximately calculated in 式 1 through 式 3.

The bootstrap voltage is given by 式 1:

$$V_{\text{BST}} = V_{\text{DD}} - V_{\text{F}} - V_{\text{HS}}$$

where

- $V_{\text{F}}$  is the forward voltage drop of the bootstrap diode and series bootstrap switch. (1)

$V_{\text{HS}}$  is calculated in 式 2:

$$V_{\text{HS}} = -I_{\text{L}} \times R_{\text{DSON}}$$

where

- $I_{\text{L}}$  is the inductor current defined as flowing out of the half-bridge
- and  $R_{\text{DSON}}$  is the FET on resistance. (2)

Substituting (2) into (1) gives the expression for the bootstrap voltage as 式 3:

$$V_{\text{BST}} = V_{\text{DD}} - V_{\text{F}} + I_{\text{L}} \times R_{\text{DSON}} \quad (3)$$

From (3) one can determine that in an application where the current flows out of the half-bridge ( $I_{\text{L}}$  is positive) the bootstrap voltage can be charged up to a voltage higher than  $V_{\text{DD}}$  if  $I_{\text{L}} \times R_{\text{DSON}}$  is greater than  $V_{\text{F}}$ . Take care not to overcharge the bootstrap too much in this application by choosing a diode with a larger  $V_{\text{F}}$  or limiting the  $I_{\text{L}} \times R_{\text{DSON}}$  product.

In an application where  $I_{\text{L}}$  is negative, the  $I_{\text{L}} \times R_{\text{DSON}}$  product subtracts from the available bootstrap cap voltage. In this case using a smaller  $V_{\text{F}}$  diode is recommended if  $I_{\text{L}} \times R_{\text{DSON}}$  is large.

### 8.3.2 LDO Operation

An internal LDO allows the driver to run off higher voltages from 6 V to 18 V and regulates the supply to 5 V, so the LMG1210 can run off of higher input voltages with wide tolerances. To maintain stability of the internal LDO, care must be taken to make sure a capacitor of at least 0.3  $\mu\text{F}$  from  $V_{\text{DD}}$  to  $V_{\text{SS}}$  with an ESR below 500 m $\Omega$  is used. A high-quality ceramic capacitor with an X7R dielectric is recommended. There is no maximum limit on the capacitance allowed on the output of the LDO.

If the input supply is already 5 V  $\pm 5\%$ , then the LDO can be bypassed. This is achieved by connecting the 5 V supply directly to the  $V_{\text{DD}}$  pin. The  $V_{\text{IN}}$  pin should be tied to the  $V_{\text{DD}}$  pin, and the capacitor on the  $V_{\text{IN}}$  pin can be removed. Do not ground the  $V_{\text{IN}}$  pin.

## Feature Description (continued)

### 8.3.3 Dead Time Selection

In PWM mode the dead time can be set with a resistor placed between DHL/DLH and  $V_{SS}$ . For a desired dead time ( $t_{dt}$ ), the corresponding required resistance can be calculated in [式 4](#) with  $t_{dt}$  in ns and  $R_{ext}$  in  $k\Omega$ .

$$R_{ext} = (900/t_{dt}) - 25 \quad (4)$$

The maximum dead time is 20 ns, which gives a minimum resistor value of 20  $k\Omega$ . The minimum dead time is 0.5ns, which gives a maximum resistor value of 1.8  $M\Omega$ . There is an internal pull-up resistor at DHL/DLH pin, which forms a voltage divider with the external resistor. This voltage decides the final dead time. The calculation between dead time  $t_{DT}$  in ns and  $V_{DT}$  is shown in [式 5](#).

$$t_{dt} = (1.8 - V_{DT}) \times 20 \quad (5)$$

Before being used to generate the dead times, the voltages on the DHL and DLH pins are first filtered through an internal RC filter with a nominal corner frequency of 10 kHz to attenuate switching noise.

The pulse widths of the HO and LO outputs are decreased from the PWM input by the chosen dead-times. The timing diagram under no load condition is shown in [图 13](#) and [图 14](#). PWM mode and Independent mode configurations can be found in [图 16](#).

### 8.3.4 Overtemperature Protection

The LMG1210 has three separate overtemperature thresholds: two on the low-side and one on the high-side. The lowest overtemperature threshold is the low-side *switching* threshold at 150 degrees minimum. When exceeded, this disables switching on both the low and high sides. However, the 5 V LDO continues to operate.

If the low-side temperature continues to rise, due to a short or external load on the 5 V LDO, then at 10 degrees higher, the low-side shuts down the 5 V LDO.

The high-side has an independent overtemperature threshold at 160 minimum. When triggered, it only shuts off the high-side while the low-side may continue to operate.

If it is undesirable in an application to have only the high side shut off and not the low side, TI recommends designing the thermal cooling of the board in a way to make the low-side die hotter. This can be achieved by controlling the size of the thermal planes connected to each thermal pad.

### 8.3.5 High-Performance Level Shifter

The LMG1210 uses a high-performance level shifter to translate the signal from the low side to the high side. The level shifter is built using TI's proprietary high-voltage capacitor technology, which showcases best-in-class CMTI (common-mode transient immunity), or  $dV/dt$  on the HS pin. The level shifter can handle very high CMT (common-mode transient) rates while simultaneously providing low propagation time which does not vary depending on CMT rate. For more information on LMG1210 CMTI performance refer to [section 2.4 from Design Considerations for LMG1205 Advanced GaN FET Driver During High-Frequency Operation](#).

### 8.3.6 Negative HS Voltage Handling

The LMG1210 by itself can operate with -200V on the HS pin as stated in the recommended operating conditions table. However, if using a bootstrap diode, the system will be more limited based on the potential of high-currents flowing through the bootstrap diode.

HS goes most negative during the dead times when the low-side FET is off. This also means the bootstrap switch is off so the BST pin is relatively high impedance. Therefore as HS goes negative, the bootstrap diode becomes forward biased and pulls the voltage at BST down with it. Because the bootstrap switch is off, very little current will flow until the bootstrap diode attempts to pull the BST pin below ground at which point the ESD diode on the BST pin will clamp the voltage at a diode drop below ground. The point where significant current begins to flow through the bootstrap diode is given in [式 6](#)

$$V_{HS} = -V_{BST} - V_{ESD} - (V_{HB} - V_{HS}) \quad (6)$$

Where  $V_{BST}$  is the forward voltage drop of the selected bootstrap diode and  $V_{ESD}$  is the forward voltage drop of the ESD diode of the BST pin which is typically 0.7V at room temp. [图 15](#) shows a schematic of this current path.

## Feature Description (continued)

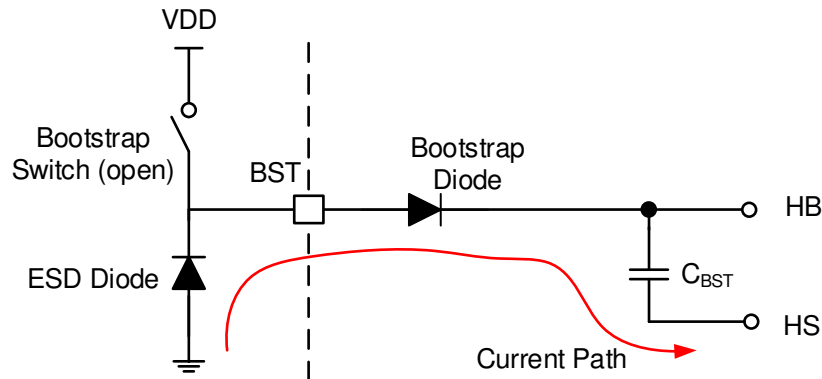


图 15. Current Path Across Bootstrap Diode

Once this negative voltage is exceeded, large currents will begin to flow out of the BST pin and through the bootstrap diode. The currents may be limited by the following: resistance of the BST ESD diode, resistance of the bootstrap diode, inductance of the bootstrap loop, or additional resistance purposely added in series with the bootstrap diode. If this current is too high, damage to the bootstrap diode or the LMG1210 can result. If this current delivers significant enough total charge, this can over-charge the bootstrap rail as well.

The BST pin ESD diode has been specifically designed to be robust to carry up to a couple amps surge current without damage.

### 8.4 Device Functional Modes

The mode of operation is determined by the state of DHL and DLH pins during power up. The state of the pins is sampled at power up and cannot be changed during operation. There are two different modes: independent operation where separate HI and LI signals are required, and PWM mode where one PWM input signal is required and the LMG1210 generates the complementary HI and LI signals. For PWM input, the dead time for the low-to-high and high-to-low switch-node transition is independently set by an external resistor at DHL and DLH. For independent input mode, DLH is tied to  $V_{DD}$  and DHL is internally set to high-impedance and can be tied to  $V_{DD}$ , tied to ground or left floating.




Operating Mode	DHL	DLH
PWM		
Independent Input Mode	Leave Floating or Tie to VSS	$V_{DD}$ 

图 16. Operation Mode Selection

表 1 lists the functional modes for the LMG1210.

表 1. LMG1210 Truth Table

INPUTS		PWM MODE		INDEPENDENT MODE	
EN/HI	PWM/LI	HO	LO	HO	LO
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	1	1	0
1	1	1	0	1	1



## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LMG1210 is designed to optimally drive GaN FETs in half-bridge configurations, such as synchronous buck and boost converters, as well as more complex topologies. By integrating the level shifting and bootstrap operation the complexities of driving the high-side device are solved for the designer.

The list below shows some sample values for a typical 48 V to 12 V application synchronous buck.

- Input Voltage: 48 V
- Output Voltage: 12 V
- Output Current: 10 A
- Bias Voltage: 6 V
- Duty Cycle: 25 %
- Switching Frequency: 1 MHz
- Inductor: 4.7  $\mu$ H

### 9.2 Typical Application

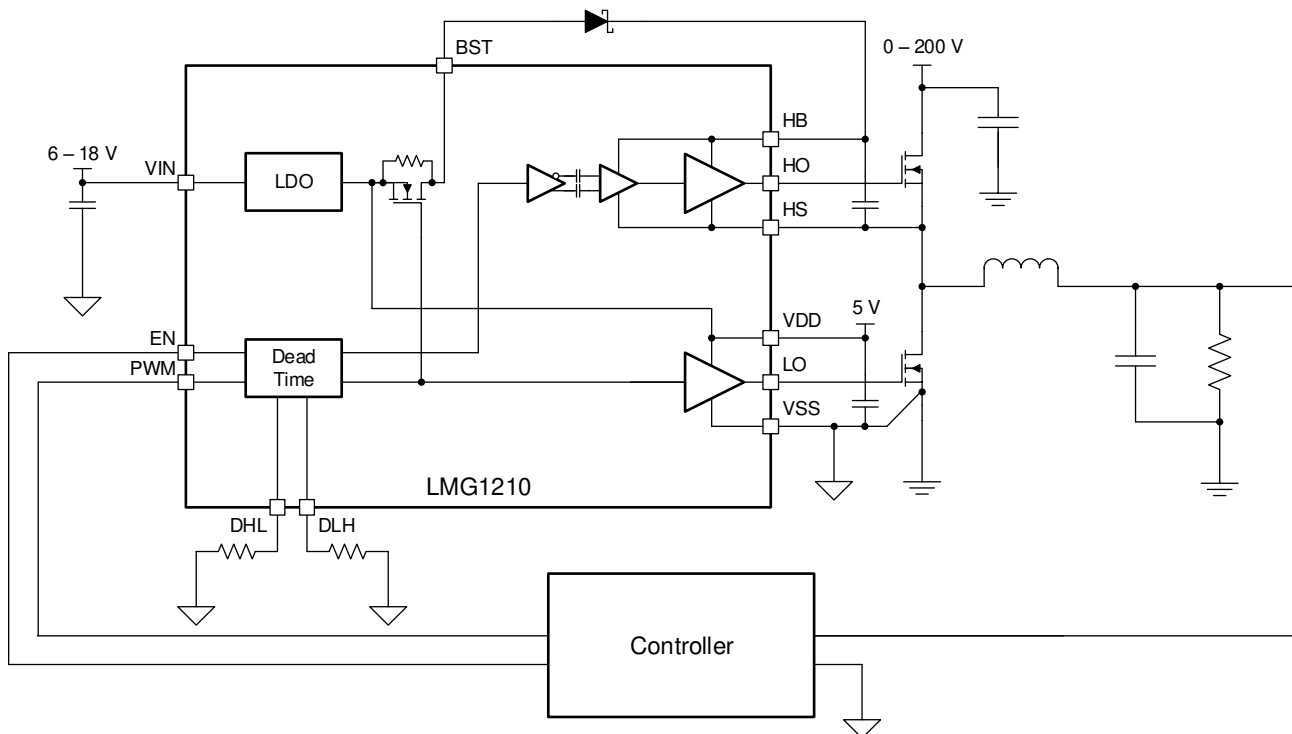


图 17. Simplified LMG1210 Configured as Synchronous Buck Converter

## Typical Application (continued)

### 9.2.1 Design Requirements

When designing a multi-MHz application that incorporates the LMG1210 gate driver and GaN power FETs, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are layout optimization, circuit voltages, passive components, operating frequency, and controller selection.

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Bypass Capacitor

To properly drive the GaN FETs, TI recommends placing high-quality ceramic bypass capacitors as close as possible between the HB to HS and  $V_{DD}$  to  $V_{SS}$ . If using the LDO, the  $V_{DD}$ - $V_{SS}$  capacitor is required to be at least 0.3  $\mu\text{F}$  at bias for stability. However, a larger capacitor may be required for many applications.

The bootstrap capacitor must be large enough to support charging the high-side FET and supplying the high-side quiescent current when the high-side FET is on. The required capacitance can be calculated as 式 7:

$$(0.5 \text{ nC} + Q_{rr} + Q_{gH} + I_{HB} \times t_{on}) / \Delta V = C_{BST, \min}$$

where

- $Q_{gH}$  is the gate charge of the high-side GaN FET,
- $I_{HB}$  is the quiescent current of the high-side driver,
- $t_{ON}$  is the maximum on time period of the high side,
- $Q_{rr}$  is the reverse recovery of the bootstrap diode,
- 0.5 nC is the additional charge per cycle removed from the bootstrap due to high side dynamic current,
- and  $\Delta V$  is the acceptable droop on the bootstrap capacitor voltage. (7)

When using larger bootstrap capacitors, TI recommends that the  $V_{DD}$ - $V_{SS}$  capacitor also be increased to keep the ratio at least 5 to 1. If this is not maintained, the charging of the bootstrap capacitor can pull the  $V_{DD}$ - $V_{SS}$  rail down sufficiently to cause UVLO conditions and potentially unwanted behavior.

#### 9.2.2.2 Bootstrap Diode Selection

The bootstrap diode blocks the high voltage from the gate drive circuitry when the switch node swings high, with the rated blocking voltage equal to the maximum  $V_{ds}$  of the GaN FET. For low or moderate frequency operation ultra-fast recovery diodes (<50 ns) are recommended. The internal low voltage switch in the LMG1210 acts to reduce the reverse recovery. For high-frequency operation a Schottky diode is recommended. To minimize switching losses and improve performance, it is important to select a diode with low capacitance.

For extreme cases, where the low-side FET on time is less than 20 ns, TI recommends using a small GaN FET as synchronous bootstrap instead of a diode. In this case, TI recommends leaving the BST pin floating or connected to  $V_{DD}$ , and to connect the source of the synchronous bootstrap directly to  $V_{DD}$ .

#### 9.2.2.3 Handling Ground Bounce

For the best switching performance, it is important to connect the  $V_{SS}$  gate return to the source of the low-side FET with a very low-inductance path.

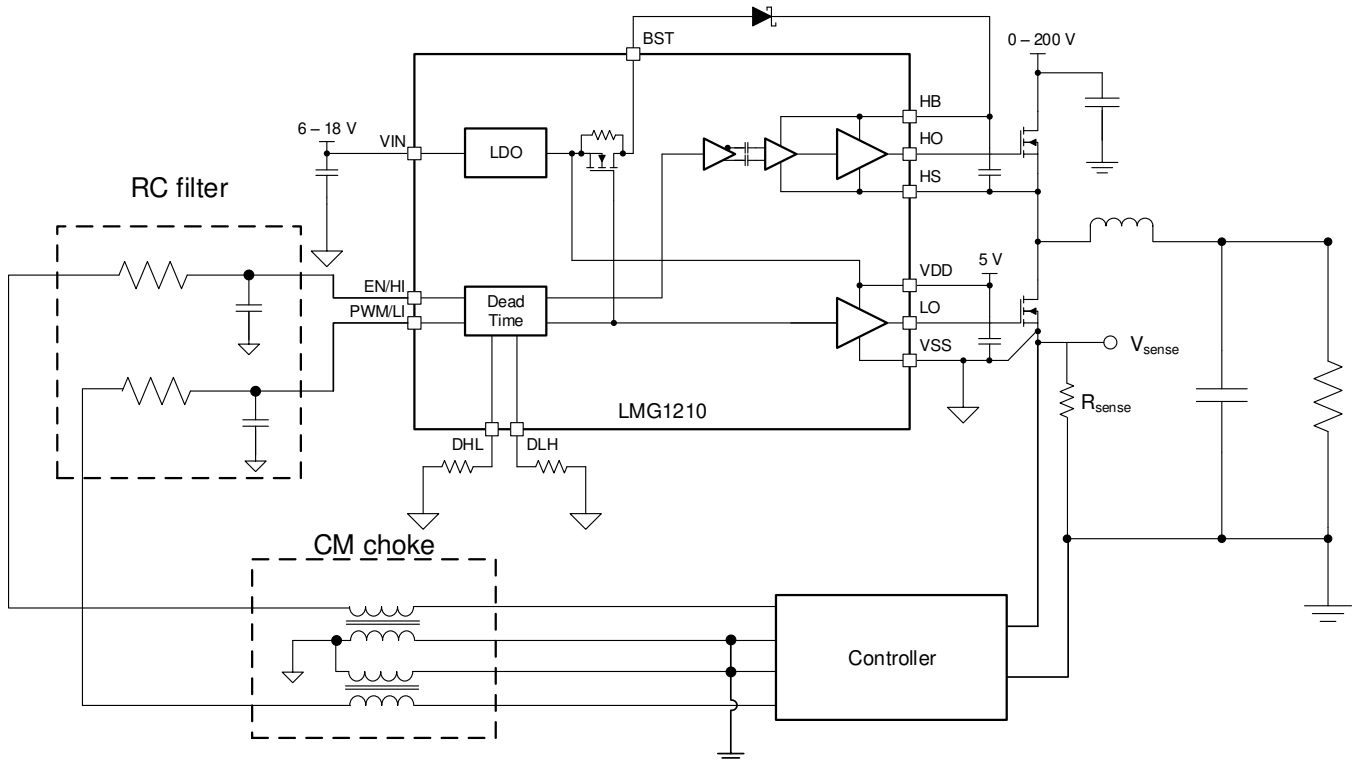
However, doing so can cause the ground of the LMG1210 to bounce relative to the system or controller ground and cause erroneous switching transitions on the inputs. Multiple strategies can be employed to eliminate these undesired transitions.

The LMG1210 has input hysteresis built into the input buffers to help counteract this effect, but this alone may not be sufficient in all applications. The simplest option is to tie the system ground together and the power ground only at the LMG1210 (single-point connection). This gives the cleanest solution but may not always be possible depending on system grounding requirements.

For moderate ground-bounce cases, a simple R-C filter can be built with a simple resistor in series with the inputs. The resistor should be close to the inputs of the LMG1210. The input capacitance of the LMG1210 produces an RC filter which can help decrease ringing at the inputs. The addition of a small C on the inputs to supplement the LMG1210 input capacitance can also be helpful. This solution is acceptable for moderate cases in applications where the extra delay is acceptable.

## Typical Application (continued)

For more extreme cases or where no delay is tolerable, using a common-mode choke provides the best results. One example application where the ground bounce is particularly challenging is when using a current sense resistor. In this application, the LMG1210 ground is connected to the GaN source, while the controller ground is connected to the other side of the current sense resistor as shown in [Figure 18](#).



**Figure 18. LMG1210 Configured With Current Sense Resistor Using a CMC as Filter**

The combination of high  $di/dt$  experienced through the sense resistor inductance will cause severe ground noise that could cause false triggering or even damage the part. To prevent this, a common-mode choke (CMC) can be used. Each signal requires its own CMC. Also, to provide additional RC filtering, a  $100\ \Omega$  resistor should be added to the signal output line before the LMG1210.

### 9.2.2.4 Independent Input Mode

In independent input mode, the signals LI and HI will propagate to the outputs LO and HO maintaining the same phase shift, varied only by the timing mismatch.

In this mode, the dead time-generating circuit will be inoperative, and the correct dead time value would have to be generated by the controller.

LI and HI cannot be high at the same time. The controller is responsible for assuring that the LI and HI on-times do not overlap and cause shoot-through.

### 9.2.2.5 Computing Power Dissipation

The power dissipation of the LMG1210 can be divided up into three parts. One is the quiescent current which is defined in the [Electrical Characteristics](#) table. This is the current consumed when no switching is taking place.

The second is the dynamic power consumed in the internal circuits of the driver at each switching transition regardless of the load on the output. This can be measured by switching the driver with no output load.

The third component is the power used to switch the load capacitance presented by the external FET.

### Typical Application (continued)

If operating in PWM mode, there is an additional quiescent current consumed in the dead time resistors. The additional current consumed in each dead time pin can be calculated as 式 8.

$$I_{qdx} = 1.8 / (25k + R_{ext}) \tag{8}$$

The first component, the quiescent power, is given in the *Electrical Characteristics* table. The second component, the dynamic power dissipation can be calculated as 式 9.

$$I_{INT} = I_{DYN} \times F_{sw}$$

where

- $I_{DYN}$  is the dynamic current consumption found in the *Electrical Characteristics* table
- and  $F_{sw}$  is the switching frequency in MHz. (9)

The third component of the power dissipation is the gate driver power. The current associated to this loss can be calculated given the  $Q_g$  of the FET as 式 10:

$$I_{FET,g} = Q_g \times F_{sw} \tag{10}$$

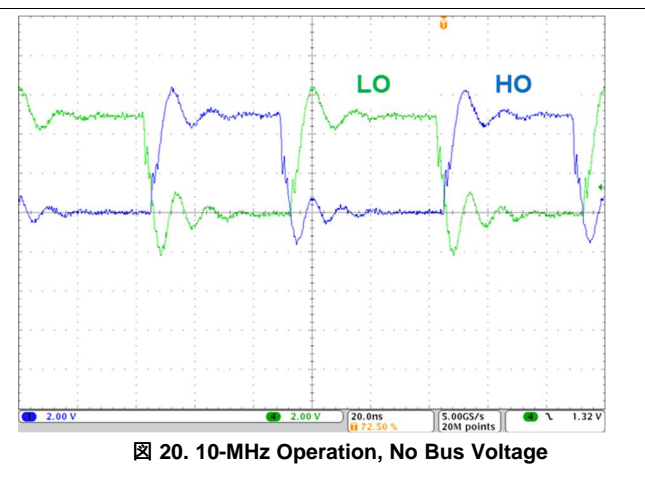
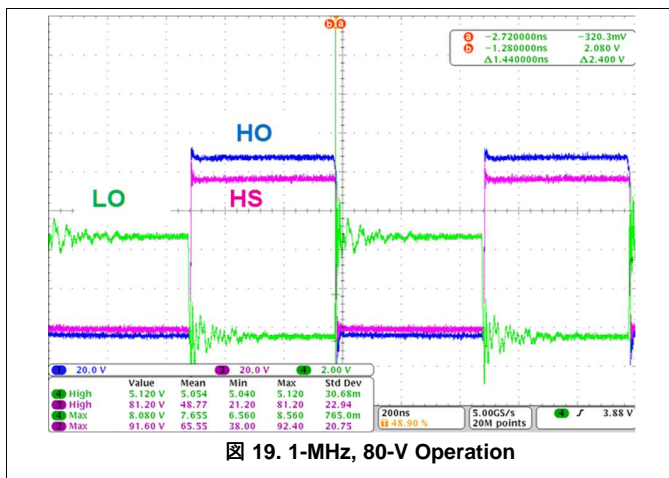
or alternatively in terms of  $C_{iss}$  as 式 11:

$$I_{FET,g} = C_{iss} \times V_{sup} \times F_{sw} \tag{11}$$

These current consumption numbers should be calculated for both the high side and low side separately and added together. When a total current consumption is computed, multiplying it by the input supply voltage gives a worst-case approximation for the total power dissipation of the LMG1210. If using a non-zero external gate resistor of value  $R_{g,ext}$ , some of this power will be dissipated in this external resistor, and can be subtracted from the power consumed inside the IC. For further details when calculating total driver power loss see [section 2 from Design Considerations for LMG1205 Advanced GaN FET Driver During High-Frequency Operation](#).

The WQFN package has two thermal pads: one for the low-side die and another for the high-side die. Though there is good thermal coupling between the die and the associated thermal pad, there is very limited thermal coupling between a die and the opposite thermal pad. This means that if power dissipation calculations indicate a die needs improved cooling, the cooling must be focused on cooling the correct thermal pad.

### 9.2.3 Application Curves



### 9.3 Do's and Don'ts

When using the LMG1210, DO:

1. Read and fully understand the data sheet, including the application notes and layout recommendations.
2. Use a four-layer board and place the return power path on an inner layer to minimize power-loop inductance.
3. Use small, surface-mount bypass and bus capacitors to minimize parasitic inductance.
4. Use the proper size decoupling capacitors and place them close to the IC as described in the [Layout Guidelines](#) section.
5. Use common-mode chokes for the input signals to reduce ground bounce noise. If not, ensure the signal source is connected to the signal  $V_{SS}$  plane which is tied to the power source only at the LMG1210 IC.

To avoid issues in your system when using the LMG1210, DON'T:

1. Use a single-layer or two-layer PCB for the LMG1210 as the power-loop and bypass capacitor inductances will be excessive and prevent proper operation of the IC.
2. Reduce the bypass capacitor values below the recommended values.
3. Allow the device to experience pin transients above 200 V as they may damage the device.
4. Drive the IC from a controller with a separate ground connection than the  $V_{SS}$  pin of the IC, unless connecting through a CMC.

## 10 Power Supply Recommendations

The power to the LMG1210 can be supplied either through the LDO or the LDO can be bypassed and 5 V can be supplied directly. The maximum input voltage to the LDO of the LMG1210 is specified in the electrical characteristics table. The minimum input voltage of the LDO is set by the minimum drop-out of the LDO at the operational current. The dropout at max current is specified in the electrical characteristics table, but a lower dropout can be used in a lower-current application. A local bypass capacitor must be placed between the  $V_{IN}$  and  $V_{SS}$  pins, and the  $V_{DD}$  and  $V_{SS}$  pins. This capacitor must be placed as close as possible to the device. TI recommends a low-ESR, ceramic, surface-mount capacitor. TI also recommends using 2 capacitors across  $V_{DD}$  and  $V_{SS}$  pin: a 100 nF ceramic surface-mount capacitor for high frequency filtering placed very close to  $V_{DD}$  and  $V_{SS}$  pin, and another surface-mount capacitor, 220 nF to 10  $\mu$ F, for IC bias requirement. The  $V_{IN}$  and  $V_{SS}$  capacitor can be removed if the LDO is bypassed.

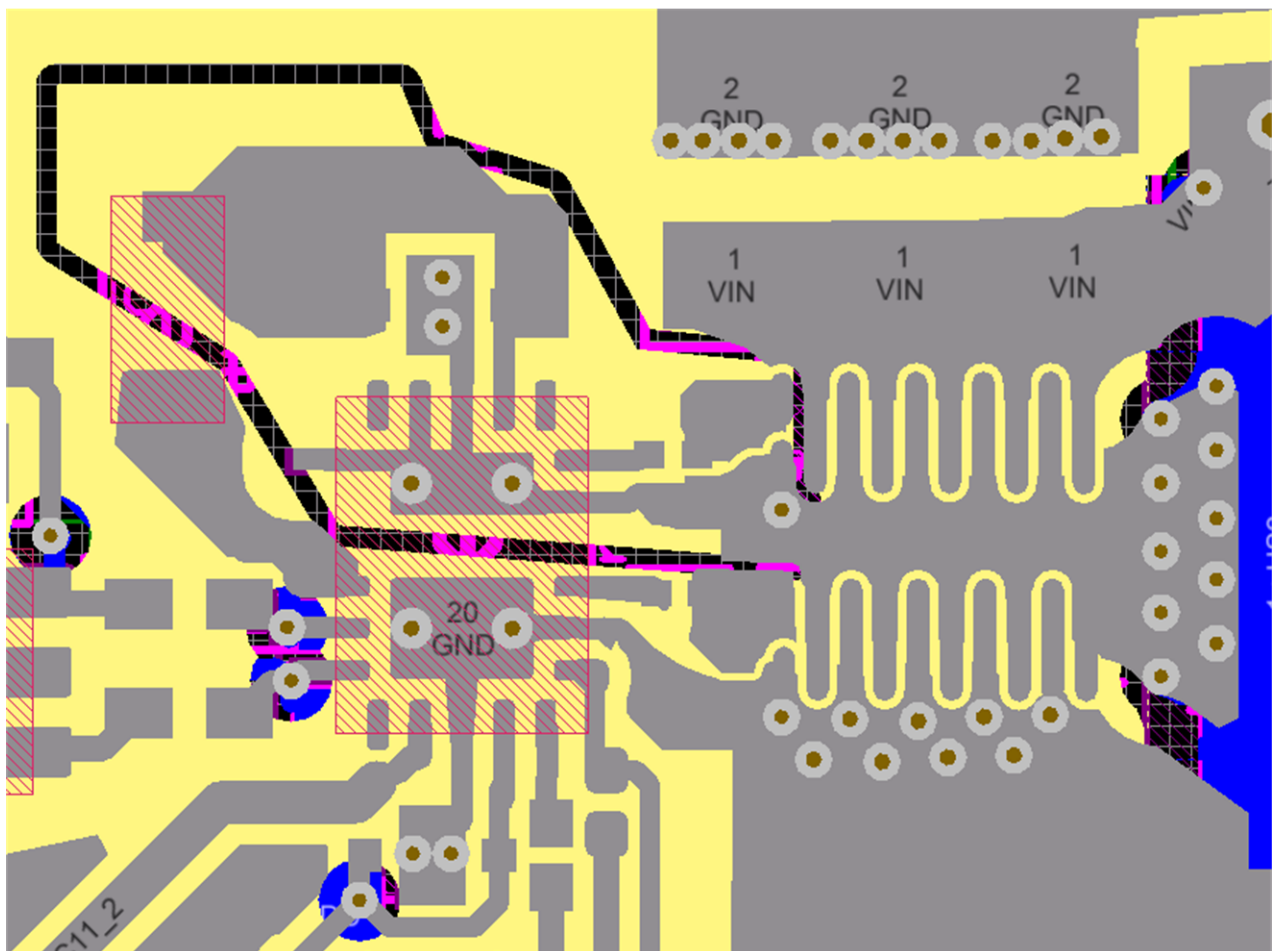
## 11 Layout

### 11.1 Layout Guidelines

The layout of the LMG1210 is critical for performance and functionality. The low inductance WQFN package helps mitigate many of the problems associated with board level parasitics, but take care with layout and placement with components to ensure proper operation. The following design rules are recommended.

- Place LMG1210 as close to the GaN FETs as possible to minimize the length of high-current traces between the HO/LO and the Gate of the GaN FETs
- Place bootstrap diode as close as possible to the LMG1210 to minimize the inductance of the BST to HB loop.
- Place the bypass capacitors across  $V_{IN}$  to  $V_{SS}$ ,  $V_{DD}$  to  $V_{SS}$ , and HB to HS as close to the LMG1210 pins as possible. The  $V_{DD}$  to  $V_{SS}$  cap is a higher priority than the  $V_{IN}$  to  $V_{SS}$  cap.
- Separate power traces and signal traces, such as output and input signals, and minimize any overlaps between layers
- Minimize capacitance from the high-side pins to the input pins to minimize noise injection.

### 11.2 Layout Example



⊗ 21. LMG1210 Layout Example

## 12 デバイスおよびドキュメントのサポート

### 12.1 ドキュメントのサポート

#### 12.1.1 関連資料

関連資料については、以下を参照してください。

- 『LMG1210 ハーフ・ブリッジ GaN ドライバのデッド・タイム最適化』(SNVA815)
- 『高周波数動作時の LMG1205 高性能 GaN FET ドライバに関する設計上の考慮事項』(SNVA723)
- 『LMG1210 TINA-TI リファレンス・デザイン』(SNOM617)
- 『LMG1210 TINA-TI 過渡 Spice モデル』(SNOM616)
- 『LMG1210 PSpice 過渡モデル』(SNOM615)

#### 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

#### 12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.4 商標

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

#### 12.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

#### 12.6 Glossary

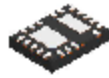
**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

LMG1210はMSL3としてリリースされます。耐用年数を超過した製品は、内部の湿気を追い出すベーキング処理によって再生可能です。IPC/JEDEC J-STD-033C には、ベーキング手順と、その処理の温度にプラスチックの筐体 (トレイ、テープ、およびリールやチューブ) が耐えられることを保証するため、どの部分に注意すべきかについてのガイドがあります。

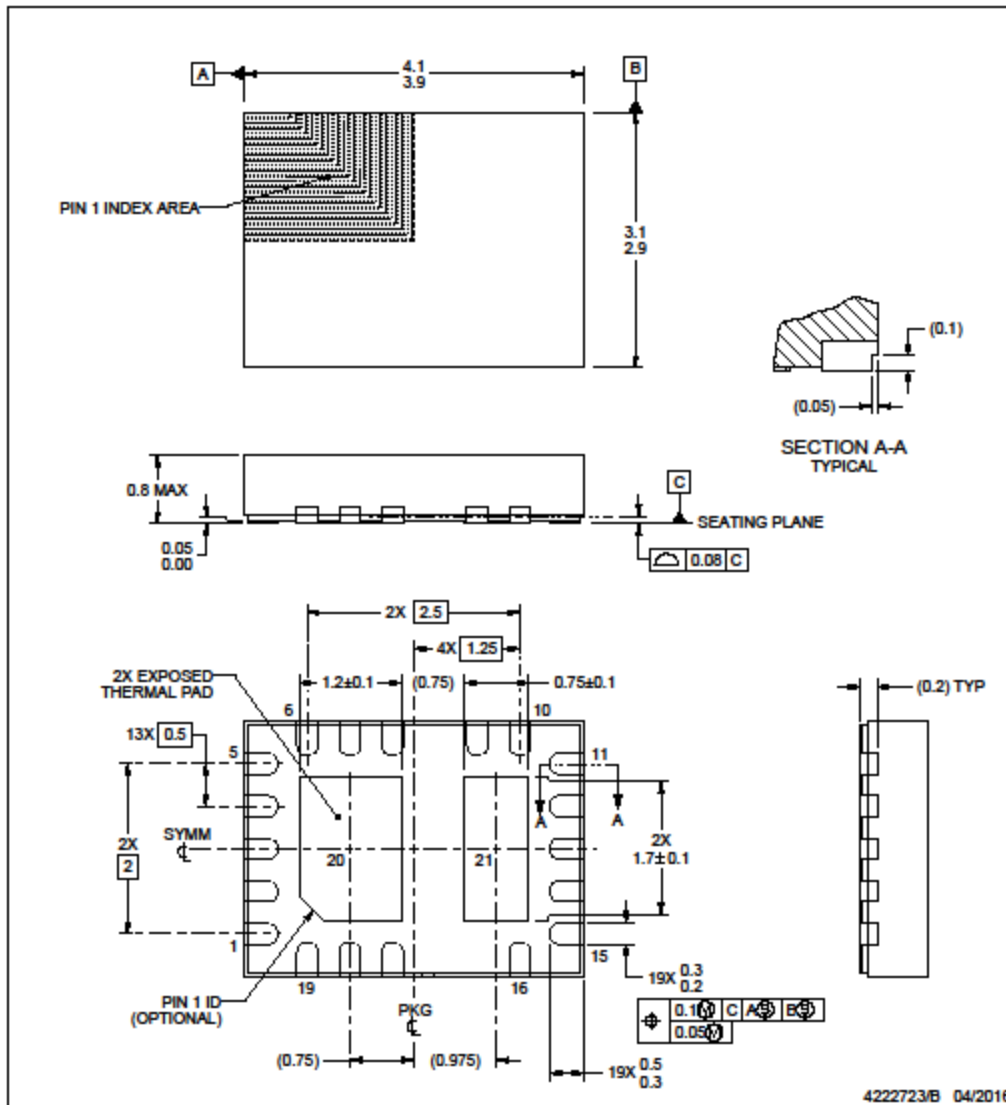


**RVR0019A**

**PACKAGE OUTLINE**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

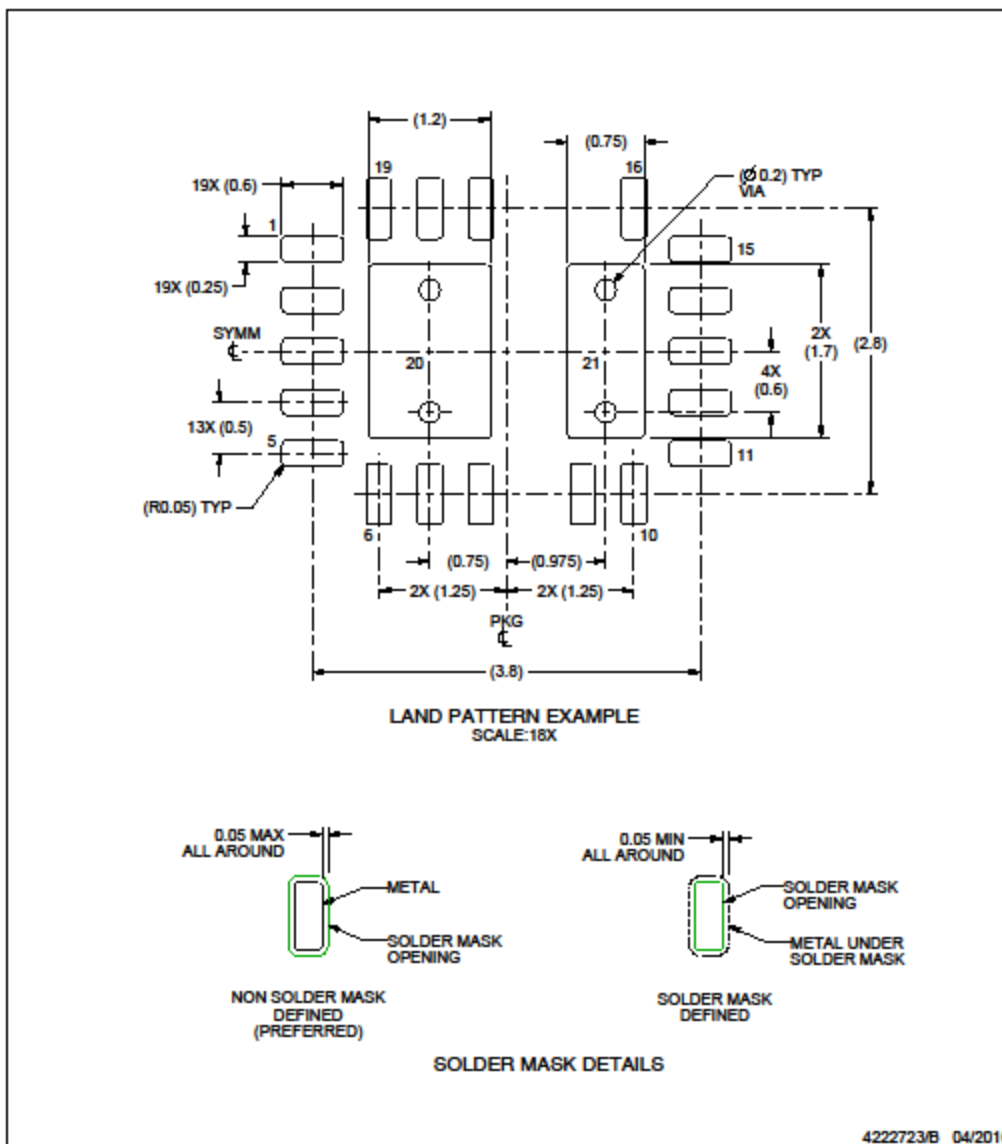


EXAMPLE BOARD LAYOUT

RVR0019A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

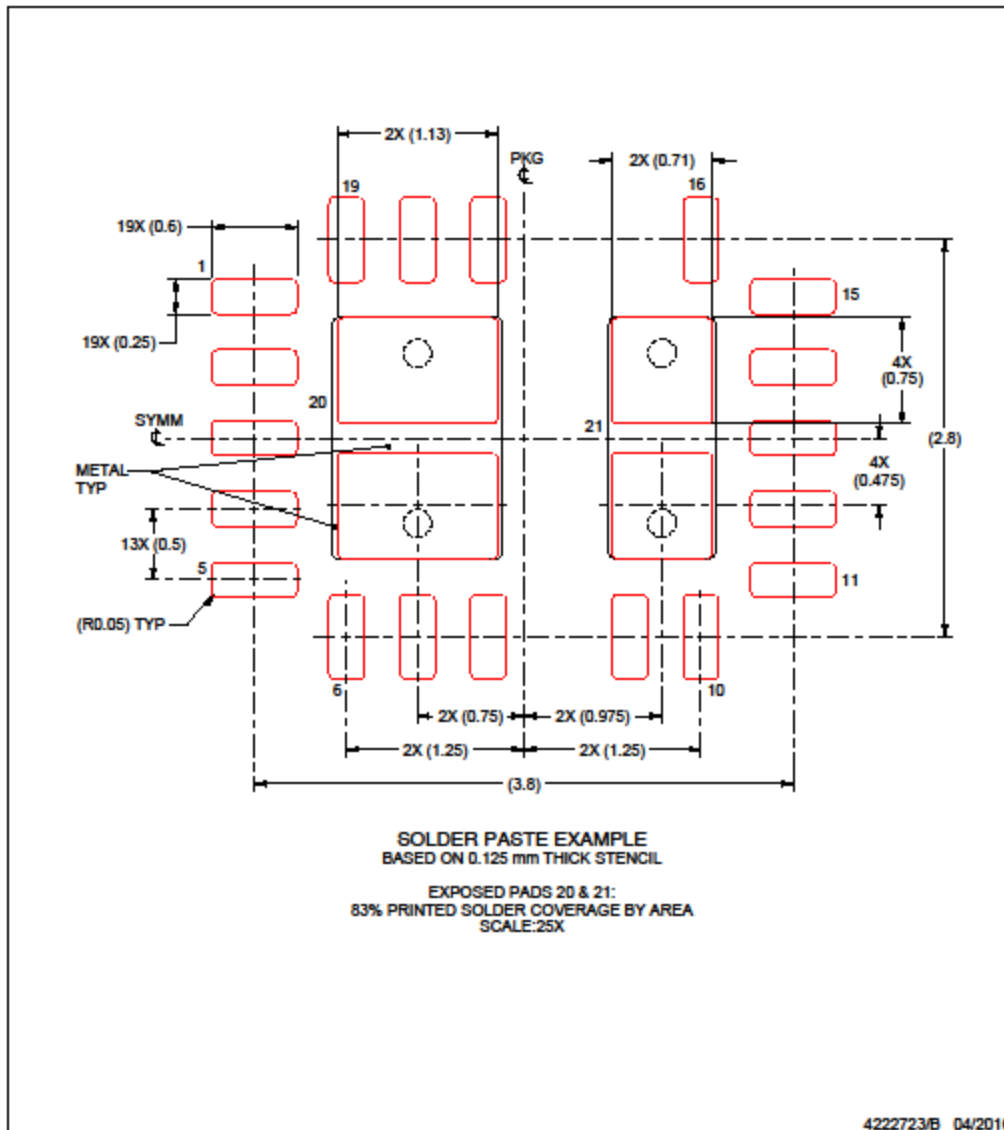
- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**EXAMPLE STENCIL DESIGN**

**RVR0019A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">LMG1210RVRR</a>	Active	Production	WQFN (RVR)   19	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LMG1210
LMG1210RVRR.A	Active	Production	WQFN (RVR)   19	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LMG1210
<a href="#">LMG1210RVRT</a>	Active	Production	WQFN (RVR)   19	250   SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LMG1210
LMG1210RVRT.A	Active	Production	WQFN (RVR)   19	250   SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LMG1210

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG1210RVRR	WQFN	RVR	19	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
LMG1210RVRT	WQFN	RVR	19	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG1210RVRR	WQFN	RVR	19	3000	367.0	367.0	38.0
LMG1210RVRT	WQFN	RVR	19	250	213.0	191.0	35.0

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