

LMG3612 650V 120mΩ GaN FET、ドライバを内蔵

1 特長

- 650V 120mΩ GaN パワー FET
- 伝搬遅延が小さく、ターンオン スルーレート制御を調整可能な内蔵ゲート ドライバ
- FLT ピン通知付きの過熱保護
- AUX 静止電流：55μA
- 電源および入力ロジック ピン最大電圧：26V
- サーマル パッド付き 8mm × 5.3mm QFN パッケージ

2 アプリケーション

- AC/DC アダプタおよびチャージャ
- AC/DC USB 壁コンセント電源
- AC/DC 補助電源
- テレビの電源
- モバイル向け充電器の設計
- USB 電源コンセント
- 補助電源
- テレビ向け SMPS 電源
- LED の電源

3 概要

LMG3612 は、スイッチ モード電源アプリケーション向けの 650V 120mΩ GaN パワー FET です。LMG3612 は、8mm × 5.3mm の QFN パッケージに GaN FET とゲート ドライバを内蔵することで、設計の簡素化と部品点数の削減を実現しています。

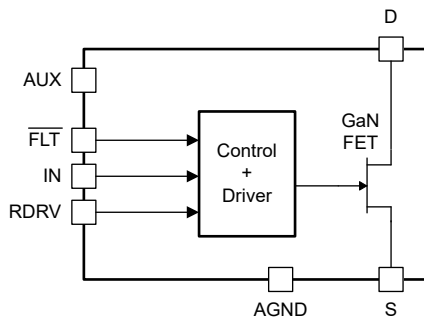
プログラマブルなターンオン スルーレートにより、EMI とリンギングを制御できます。

LMG3612 は、小さい静止電流と高速な起動時間によって、コンバータの軽負荷効率要件とバースト モード動作に対応しています。保護機能として、低電圧誤動作防止 (UVLO)、過熱保護が搭載されています。過熱保護は、オープン ドレインの FLT ピンで通知されます。

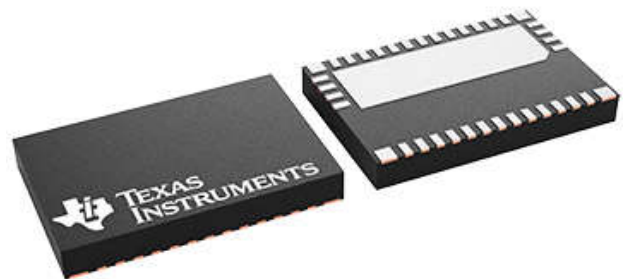
パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージサイズ ⁽²⁾
LMG3612	REQ (VQFN, 38)	8mm × 5.3mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略ブロック図



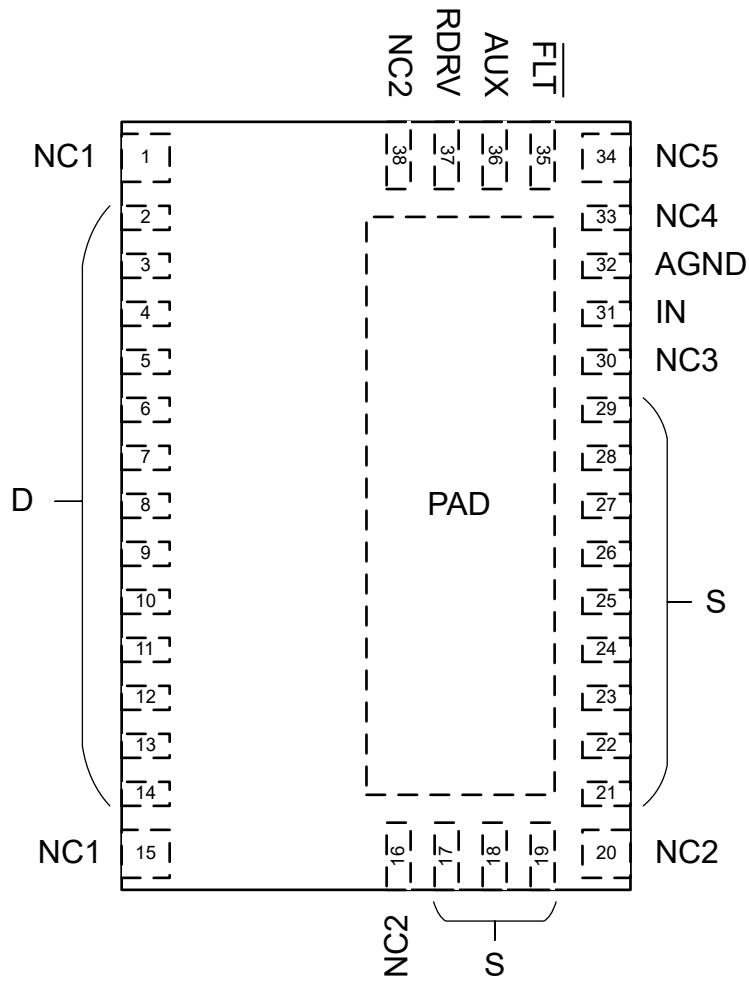
38 ピン VQFN



Table of Contents

1 特長	1	7.3 Feature Description.....	15
2 アプリケーション	1	7.4 Device Functional Modes.....	17
3 概要	1	8 Application and Implementation	18
4 Pin Configuration and Functions	3	8.1 Application Information.....	18
5 Specifications	5	8.2 Typical Application.....	19
5.1 Absolute Maximum Ratings.....	5	8.3 Power Supply Recommendations.....	20
5.2 ESD Ratings.....	5	8.4 Layout.....	20
5.3 Recommended Operating Conditions.....	6	9 Device and Documentation Support	23
5.4 Thermal Information.....	6	9.1 Documentation Support.....	23
5.5 Electrical Characteristics.....	7	9.2 ドキュメントの更新通知を受け取る方法.....	23
5.6 Switching Characteristics.....	9	9.3 サポート・リソース.....	23
5.7 Typical Characteristics.....	10	9.4 Trademarks.....	23
6 Parameter Measurement Information	11	9.5 静電気放電に関する注意事項.....	23
6.1 GaN Power FET Switching Parameters.....	11	9.6 用語集.....	23
7 Detailed Description	13	10 Revision History	23
7.1 Overview.....	13	11 Mechanical, Packaging, and Orderable Information	23
7.2 Functional Block Diagram.....	14		

4 Pin Configuration and Functions





4-1. REQ Package, 38-Pin VQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
NC1	1, 15	NC	Used to anchor QFN package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally connected to D.
D	2-14	P	GaN FET drain. Internally connected to NC1.
NC2	16, 20, 38	NC	Used to anchor QFN package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally connected to AGND, S and, PAD.
S	17-19, 21-29	P	GaN FET source. Internally connected to AGND, PAD, and NC2.
NC3	30	NC	Pin is not functional. Do not connect PCB landing pad to other metal. Internally connected to AGND through active impedance.
IN	31	I	Gate-drive control input. There is a forward based ESD diode from IN to AUX so avoid driving IN higher than AUX.
AGND	32	GND	Analog ground. Internally connected to S, PAD, and NC2.
NC4	33	NC	Pin is not functional. Do not connect PCB landing pad to other metal. Internally connected to AGND through active impedance.
NC5	34	NC	Used to anchor QFN package to PCB. Pin must be soldered to a PCB landing pad. The PCB landing pad is non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Pin not connected internally.
FLT	35	O	Active-low fault output. Open-drain output that asserts during overtemperature protection.
AUX	36	P	Auxiliary voltage rail. Device supply voltage. Connect a local bypass capacitor between AUX and AGND.
RDRV	37	I	Drive strength control resistor. Set a resistance between RDRV and AGND to program the GaN FET turn-on slew rate.
PAD	—	—	Thermal pad. Internally connected to S, AGND, and NC2. All the S current may be conducted with PAD (PAD = S).

(1) I = input, O = output, I/O = input or output, GND = ground, P = power, NC = no connect.

5 Specifications

5.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to AGND⁽¹⁾

		MIN	MAX	UNIT	
V_{DS}	Drain-source (D to S) voltage, FET off		650	V	
$V_{DS(surge)}$	Drain-source (D to S) voltage, surge condition, FET off ⁽²⁾		720	V	
$V_{DS(tr)(surge)}$	Drain-source (D to S) transient ringing peak voltage, surge condition, FET off ⁽²⁾		800	V	
	Pin voltage	AUX	-0.3	30	V
		IN, \overline{FLT}	-0.3	$V_{AUX} + 0.3$	V
		RDRV	-0.3	4	V
$I_{D(cnts)}$	Drain (D to S) continuous current, FET on	-9.3	9.3	A	
$I_{D(pulse)}$	Drain (D to S) pulsed current, $t_p < 10 \mu s$, FET on ⁽³⁾		22.7	A	
$I_{S(cnts)}$	Source (S to D) continuous current, FET off		9.3	A	
	Positive sink current	\overline{FLT} (while asserted)	Internally limited	mA	
T_J	Operating junction temperature	-40	150	°C	
T_{stg}	Storage temperature	-40	150	°C	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) See [GaN Power FET Switching Capability](#) for more information on the GaN power FET switching capability.
- (3) GaN power FET may self-limit below this value if it enters saturation.

5.2 ESD Ratings

			VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Pins 1 through 15	±1000	V
			Pins 16 through 38	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾		±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Unless otherwise noted: voltages are respect to AGND

			MIN	NOM	MAX	UNIT
	Supply voltage	AUX	10		26	V
	Input voltage	IN	0		V_{AUX}	V
	Pull-up voltage on open-drain output	FLT	0		V_{AUX}	V
V_{IH}	High-level input voltage	IN	2.5			V
V_{IL}	Low-level input voltage				0.6	V
$I_{D(cnts)}$	Drain (D to S) continuous current, FET on		-7.7		7.7	A
C_{AUX}	AUX to AGND capacitance from external bypass capacitor		0.030			μ F
R_{RDRV}	RDRV to AGND resistance from external slew-rate control resistor to configure below slew rate settings					
	slew rate setting 0 (slowest)		90	120	open	k Ω
	slew rate setting 1		42.5	47	51.5	k Ω
	slew rate setting 2		20	22	24	k Ω
	slew rate setting 3 (fastest)		0	5.6	11	k Ω

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMG3612	UNIT
		REQ (VQFN)	
		38 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.2	$^{\circ}$ C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.31	$^{\circ}$ C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

1) Symbol definitions: I_D = D to S current; I_S = S to D current; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$; $10\text{ V} \leq V_{\text{AUX}} \leq 26\text{ V}$; $V_{\text{IN}} = 0\text{ V}$; $R_{\text{RDRV}} = 0\ \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER FET						
$R_{\text{DS(on)}}$	Drain-source (D to S) on resistance	$V_{\text{IN}} = 5\text{ V}$, $I_D = 4.2\text{ A}$, $T_J = 25^\circ\text{C}$		120		m Ω
		$V_{\text{IN}} = 5\text{ V}$, $I_D = 4.2\text{ A}$, $T_J = 125^\circ\text{C}$		214		
I_{DSS}	Drain (D to S) leakage current	$V_{\text{DS}} = 650\text{ V}$, $T_J = 25^\circ\text{C}$		3		μA
		$V_{\text{DS}} = 650\text{ V}$, $T_J = 125^\circ\text{C}$		15		
Q_{OSS}	Output (D to S) charge	$V_{\text{DS}} = 400\text{ V}$		28.3		nC
C_{OSS}	Output (D to S) capacitance			43.9		pF
E_{OSS}	Output (D to S) capacitance stored energy			3.74		μJ
$C_{\text{OSS,er}}$	Energy related effective output (D to S) capacitance			46.7		pF
$C_{\text{OSS,tr}}$	Time related effective output (D to S) capacitance	$V_{\text{DS}} = 0\text{ V to }400\text{ V}$		70.2		pF
Q_{RR}	Reverse recovery charge			0		nC
IN						
$V_{\text{IT+}}$	Positive-going input threshold voltage		1.7		2.45	V
$V_{\text{IT-}}$	Negative-going input threshold voltage		0.7		1.3	V
	Input threshold voltage hysteresis			1		V
	Pull-down input resistance	$0\text{ V} \leq V_{\text{PIN}} \leq 3\text{ V}$	200	400	600	k Ω
	Pull-down input current	$10\text{ V} \leq V_{\text{PIN}} \leq 26\text{ V}$; $V_{\text{AUX}} = 26\text{ V}$		10		μA

5.5 Electrical Characteristics (続き)

1) Symbol definitions: I_D = D to S current; I_S = S to D current; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$; $10\text{ V} \leq V_{AUX} \leq 26\text{ V}$; $V_{IN} = 0\text{ V}$; $R_{RDRV} = 0\ \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERTEMPERATURE PROTECTION						
	Temperature fault – positive-going threshold temperature			165		$^\circ\text{C}$
	Temperature fault – negative-going threshold temperature			145		$^\circ\text{C}$
	Temperature fault – threshold temperature hysteresis			20		$^\circ\text{C}$
FLT						
	Low-level output voltage	$\overline{\text{FLT}}$ sinking 1 mA while asserted			200	mV
	Off-state sink current	$V_{\text{FLT}} = V_{\text{AUX}}$ while de-asserted			1	μA
AUX						
$V_{\text{AUX,T+}}$ (UVLO)	UVLO – positive-going threshold voltage		8.9	9.3	9.7	V
	UVLO – negative-going threshold voltage		8.6	9.0	9.4	V
	UVLO – threshold voltage hysteresis			250		mV
	Quiescent current			55	120	μA
	Operating current	$V_{\text{IN}} = 0\text{ V}$ or 5 V , $V_{\text{DS}} = 0\text{ V}$, $f_{\text{IN}} = 500\text{ kHz}$		2.2		mA

5.6 Switching Characteristics

1) Symbol definitions: I_D = D to S current; I_S = S to D current; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; $10\text{ V} \leq V_{\text{AUX}} \leq 26\text{ V}$; $V_{\text{IN}} = 0\text{ V}$; $R_{\text{RDRV}} = 0\ \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER FET						
$t_{\text{d(on)}}$ (I _{drain})	Drain current turn-on delay time	From $V_{\text{IN}} > V_{\text{IN,IT+}}$ to $I_D > 50\text{ mA}$, $V_{\text{BUS}} = 400\text{ V}$, L_{HB} current = 2 A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		75		ns
		slew rate setting 1		34		
		slew rate setting 2		28		
slew rate setting 3 (fastest)		23				
$t_{\text{d(on)}}$	Turn-on delay time	From $V_{\text{IN}} > V_{\text{IN,IT+}}$ to $V_{\text{DS}} < 320\text{ V}$, $V_{\text{BUS}} = 400\text{ V}$, L_{HB} current = 2 A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		107		ns
		slew rate setting 1		47		
		slew rate setting 2		37		
slew rate setting 3 (fastest)		28				
$t_{\text{d(off)}}$	Turn-off delay time	From $V_{\text{IN}} < V_{\text{IN,IT-}}$ to $V_{\text{DS}} > 80\text{ V}$, $V_{\text{BUS}} = 400\text{ V}$, L_{HB} current = 2 A, (independent of slew rate setting), see GaN Power FET Switching Parameters		33		ns
$t_{\text{f(off)}}$	Turn-off fall time	From $V_{\text{DS}} > 80\text{ V}$ to $V_{\text{DS}} > 320\text{ V}$, $V_{\text{BUS}} = 400\text{ V}$, L_{HB} current = 2 A, (independent of slew rate setting), see GaN Power FET Switching Parameters		21		ns
	Turn-on slew rate	From $V_{\text{DS}} < 250\text{ V}$ to $V_{\text{DS}} < 150\text{ V}$, $T_J = 25^{\circ}\text{C}$, $V_{\text{BUS}} = 400\text{ V}$, L_{HB} current = 2 A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		17		V/ns
		slew rate setting 1		42		
		slew rate setting 2		65		
slew rate setting 3 (fastest)		125				

5.7 Typical Characteristics

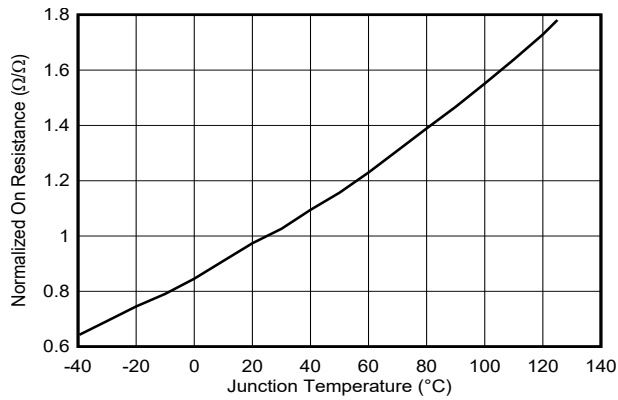
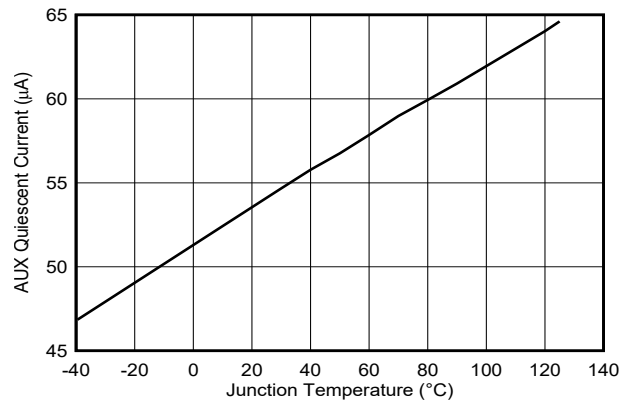


图 5-1. Normalized On-Resistance vs Junction Temperature



$V_{IN} = 0\text{ V}$

图 5-2. AUX Quiescent Current vs Junction Temperature

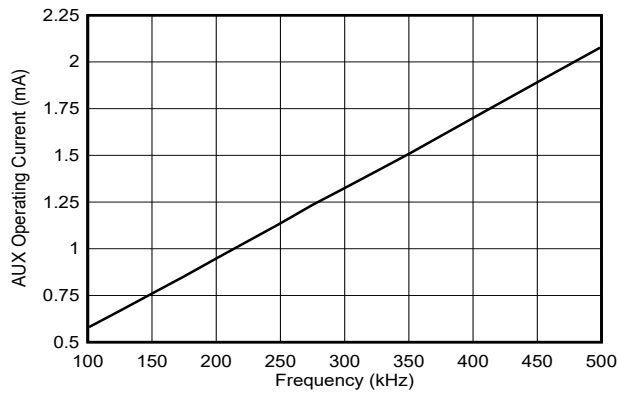


图 5-3. AUX Operating Current vs Frequency

6 Parameter Measurement Information

6.1 GaN Power FET Switching Parameters

図 6-1 shows the circuit used to measure the GaN power FET switching parameters. The circuit is operated as a double-pulse tester. Consult external references for double-pulse tester details. The circuit operates in the boost configuration with the low-side LMG3612 being the device under test (DUT). The high-side LMG3612 acts as the double-pulse tester diode and circulates the inductor current in the off-state, third-quadrant conduction mode.

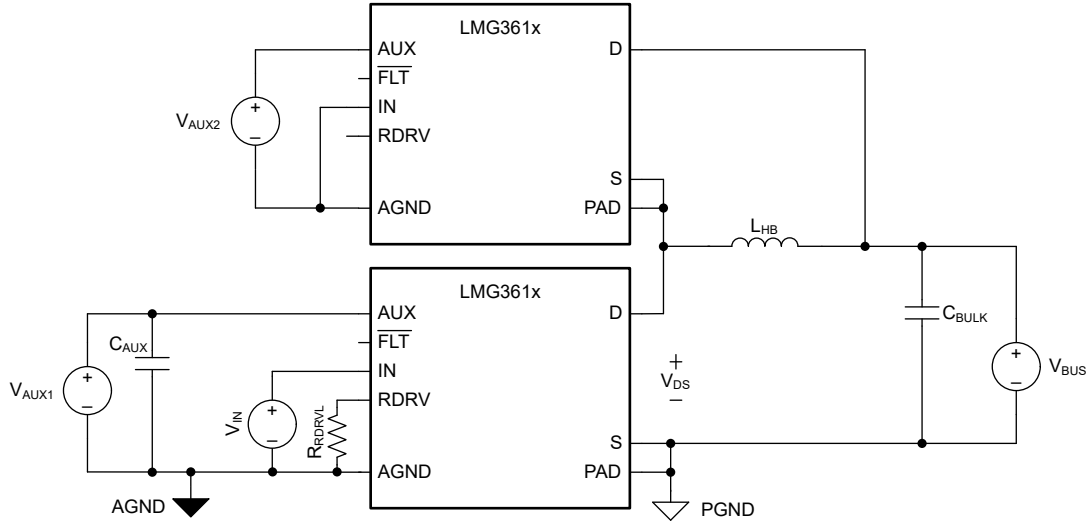


図 6-1. GaN Power FET Switching Parameters Test Circuit

Figure 6-2 shows the GaN power FET switching parameters.

The GaN power FET turn-on transition has three timing components: drain-current turn-on delay time, turn-on delay time, and turn-on rise time. Note that the turn-on rise time is the same as the V_{DS} 80% to 20% fall time. All three turn-on timing components are a function of the RDRV pin setting.

The GaN power FET turn-off transition has two timing components: turn-off delay time, and turn-off fall time. Note that the turn-off fall time is the same as the V_{DS} 20% to 80% rise time. The turn-off timing components are independent of the RDRV pin setting, but heavily dependent on the L_{HB} current.

The turn-on slew rate is measured over a smaller voltage delta (100 V) compared to the turn-on rise time voltage delta (240 V) to obtain a faster slew rate which is useful for EMI design. The RDRV pin is used to program the slew rate.

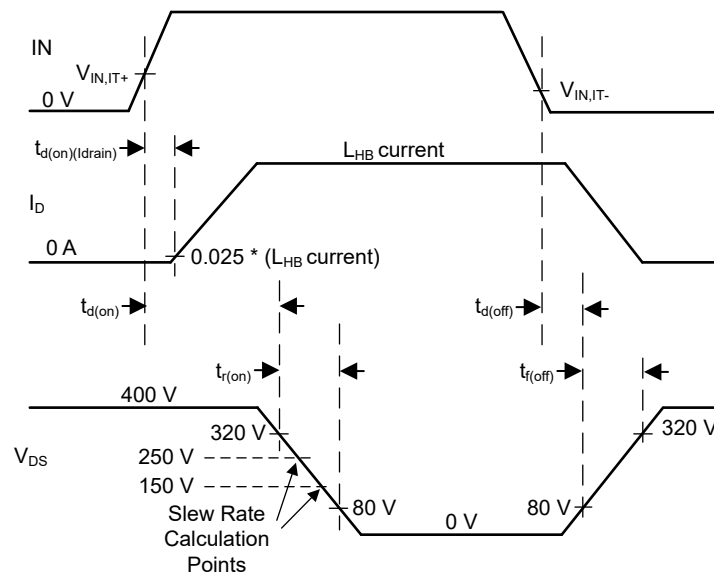


Figure 6-2. GaN Power FET Switching Parameters

7 Detailed Description

7.1 Overview

The LMG3612 is an integrated 650-V 120-m Ω GaN power FET intended for use in switching-power converters. The LMG3612 combines the GaN FET, gate driver, and protection features in a 8-mm by 5.3-mm QFN package.

The 650-V rated GaN FET supports the high voltages encountered in off-line power switching applications. The GaN FET low output-capacitive charge reduces both the time and energy needed for power converter switching and is the key characteristic needed to create small, efficient power converters.

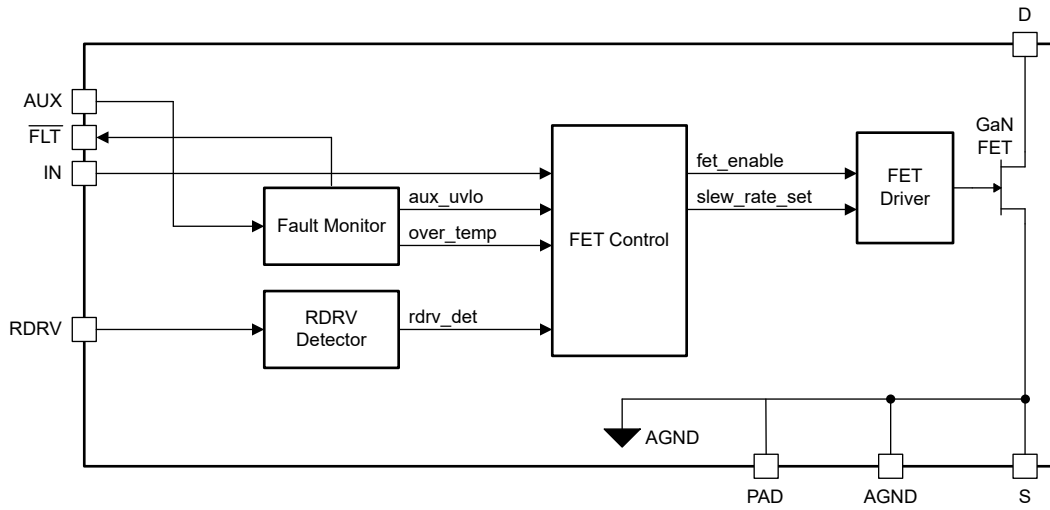
The LMG3612 internal gate driver regulates the drive voltage for optimum GaN FET on-resistance. The internal driver reduces total gate inductance and GaN FET common-source inductance for improved switching performance, including common-mode transient immunity (CMTI). The GaN FET turn-on slew rate can be individually programmed to one of four discrete settings for design flexibility with respect to power loss, switching-induced ringing, and EMI.

The AUX input supply wide voltage range is compatible with the corresponding wide range supply rail created by power supply controllers. Low AUX quiescent currents support converter burst-mode operation critical for meeting government light-load efficiency mandates. Further AUX quiescent current reduction is obtained by placing the device in standby mode with the EN pin.

The IN control pin has high input impedance, low input threshold voltage and maximum input voltage equal to the AUX voltage. This allows the pin to support both low voltage and high voltage input signals and be driven with low-power outputs.

The LMG3612 protection features are under-voltage lockout (UVLO) and overtemperature protection. The overtemperature protection is reported on the open drain $\overline{\text{FLT}}$ output.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 GaN Power FET Switching Capability

Due to the silicon FET's long reign as the dominant power-switch technology, many designers are unaware that the nameplate drain-source voltage cannot be used as an equivalent point to compare devices across technologies. The nameplate drain-source voltage of a silicon FET is set by the avalanche breakdown voltage. The nameplate drain-source voltage of a GaN FET is set by the long term compliance to data sheet specifications.

Exceeding the nameplate drain-source voltage of a silicon FET can lead to immediate and permanent damage. Meanwhile, the breakdown voltage of a GaN FET is much higher than the nameplate drain-source voltage. For example, the breakdown drain-source voltage of the LMG3612 GaN power FET is more than 800 V which allows the LMG3612 to operate at conditions beyond an identically nameplate rated silicon FET.

The LMG3612 GaN power FET switching capability is explained with the assistance of [Figure 7-1](#). The figure shows the drain-source voltage versus time for the LMG3612 GaN power FET for four distinct switch cycles in a switching application. No claim is made about the switching frequency or duty cycle. The first two cycles show normal operation and the second two cycles show operation during a rare input voltage surge. The LMG3612 GaN power FETs are intended to be turned on in either zero-voltage switching (ZVS) or discontinuous-conduction mode (DCM) switching conditions.

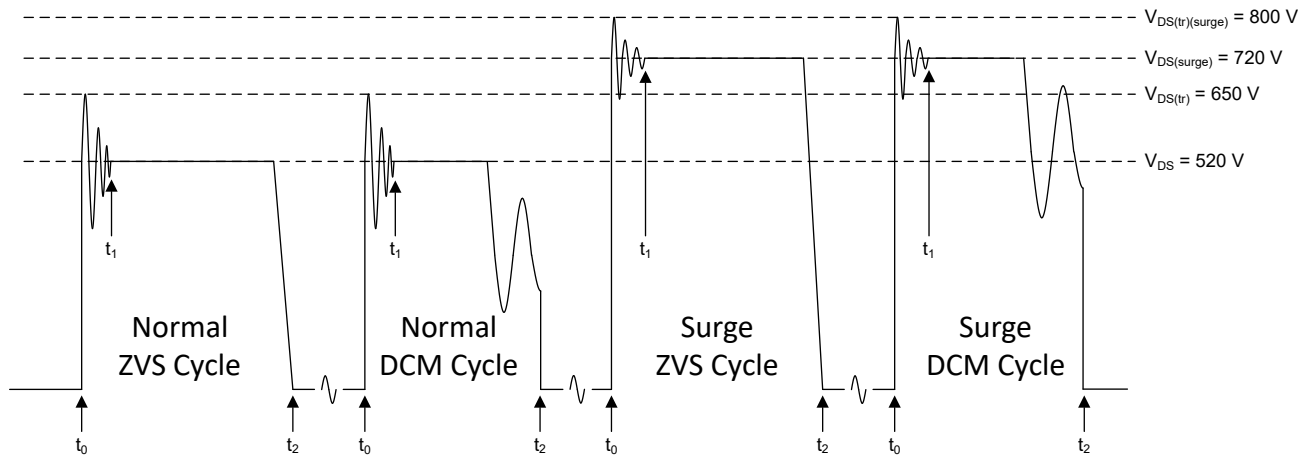


図 7-1. GaN Power FET Switching Capability

Each cycle starts before t_0 with the FET in the on state. At t_0 the GaN FET turns off and parasitic elements cause the drain-source voltage to ring at a high frequency. The high frequency ringing has damped out by t_1 . Between t_1 and t_2 the FET drain-source voltage is set by the characteristic response of the switching application. The characteristic is shown as a flat line (plateau), but other responses are possible. At t_2 the GaN FET turns on. For normal operation, the transient ring voltage is limited to 650 V and the plateau voltage is limited to 520 V. For rare surge events, the transient ring voltage is limited to 800 V and the plateau voltage is limited to 720 V.

7.3.2 Turn-On Slew-Rate Control

The turn-on slew rate of the GaN power FET is programmed to one of four discrete settings by the resistance between the RDRV and AGND pins. The slew-rate setting is determined one time during AUX power up when the AUX voltage goes above the AUX power-on reset voltage. The slew-rate setting determination time is not specified but is around 0.4 μ s.

表 7-1 shows the recommended typical resistance programming value for the four slew rate settings and the typical turn-on slew rate at each setting. As noted in the table, an open-circuit connection is acceptable for programming slew-rate setting 0 and a short-circuit connection (RDRV shorted to AGND) is acceptable for programming slew-rate setting 3.

表 7-1. Slew-Rate Setting

TURN-ON SLEW RATE SETTING	RECOMMENDED TYPICAL PROGRAMMING RESISTANCE (k Ω)	TYPICAL TURN-ON SLEW RATE (V/ns)	COMMENT
0 (slowest)	120	17	Open-circuit connection for programming resistance is acceptable.
1	47	42	
2	22	65	
3 (fastest)	5.6	125	Short-circuit connection for programming resistance (RDRV shorted to AGND) is acceptable.

7.3.3 Input Control Pin (IN)

The IN pin is used to turn the GaN power FET on and off.

The IN pin has a typical 1-V input-voltage-threshold hysteresis for noise immunity. The pin also has a typical 400-k Ω pull-down resistance to protect against floating inputs. The 400 k Ω saturates for nominal input voltages above 4 V to limit the maximum input pull-down current to a typical 10 μ A.

The IN turn-on action is blocked by the following conditions:

- AUX UVLO
- Overtemperature protection

The AUX UVLO and overtemperature protection are independent of the IN logic state. 図 7-2 shows the IN independent blocking condition operation.

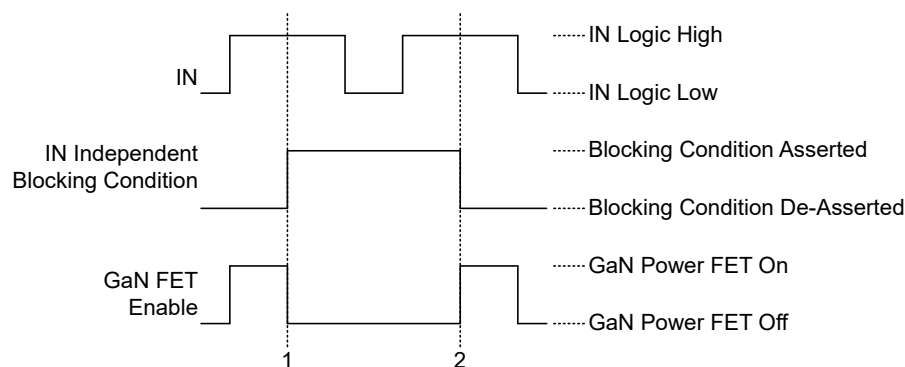


図 7-2. IN Independent Blocking Condition Operation

7.3.4 AUX Supply Pin

The AUX pin is the input supply for the internal circuits.

7.3.4.1 AUX Power-On Reset

The AUX power-on reset disables all low-side functionality if the AUX voltage is below the AUX power-on reset voltage. The AUX power-on reset voltage is not specified but is around 5 V. The AUX power-on reset initiates the one-time determination of the low-side slew-rate setting programmed on the RDRV pin when the AUX voltage goes above the AUX power-on reset voltage. The AUX power-on reset enables the overtemperature protection function if the AUX voltage is above the AUX power-on reset voltage.

7.3.4.2 AUX Under-Voltage Lockout (UVLO)

The AUX UVLO holds off the GaN power FET if the AUX voltage is below the AUX UVLO voltage. [Figure 7-2](#) shows the AUX UVLO hold-off (blocking) operation. The AUX UVLO voltage hysteresis prevents on-off chatter near the UVLO voltage trip point.

7.3.5 Overtemperature Protection

The overtemperature protection holds off the GaN power FET if the LMG3612 temperature is above the overtemperature protection temperature. [Figure 7-2](#) shows the overtemperature protection hold-off (blocking) operation. The overtemperature protection hysteresis avoids erratic thermal cycling.

An overtemperature fault is reported on the $\overline{\text{FLT}}$ pin when the overtemperature protection is asserted. This is the only fault event reported on the $\overline{\text{FLT}}$ pin. The overtemperature protection is enabled when the AUX voltage is above the AUX power-on reset voltage. The low AUX power-on reset voltage helps the overtemperature protection remain operational when the AUX rail droops during the application cool-down phase.

7.3.6 Fault Reporting

The LMG3612 only reports an overtemperature fault. An overtemperature fault is reported on the $\overline{\text{FLT}}$ pin when the Overtemperature Protection function is asserted. The $\overline{\text{FLT}}$ pin is an active low open-drain output so the pin pulls low when there is an overtemperature fault.

7.4 Device Functional Modes

The LMG3612 has one mode of operation that applies when operated within the recommended operating conditions.

8 Application and Implementation

注

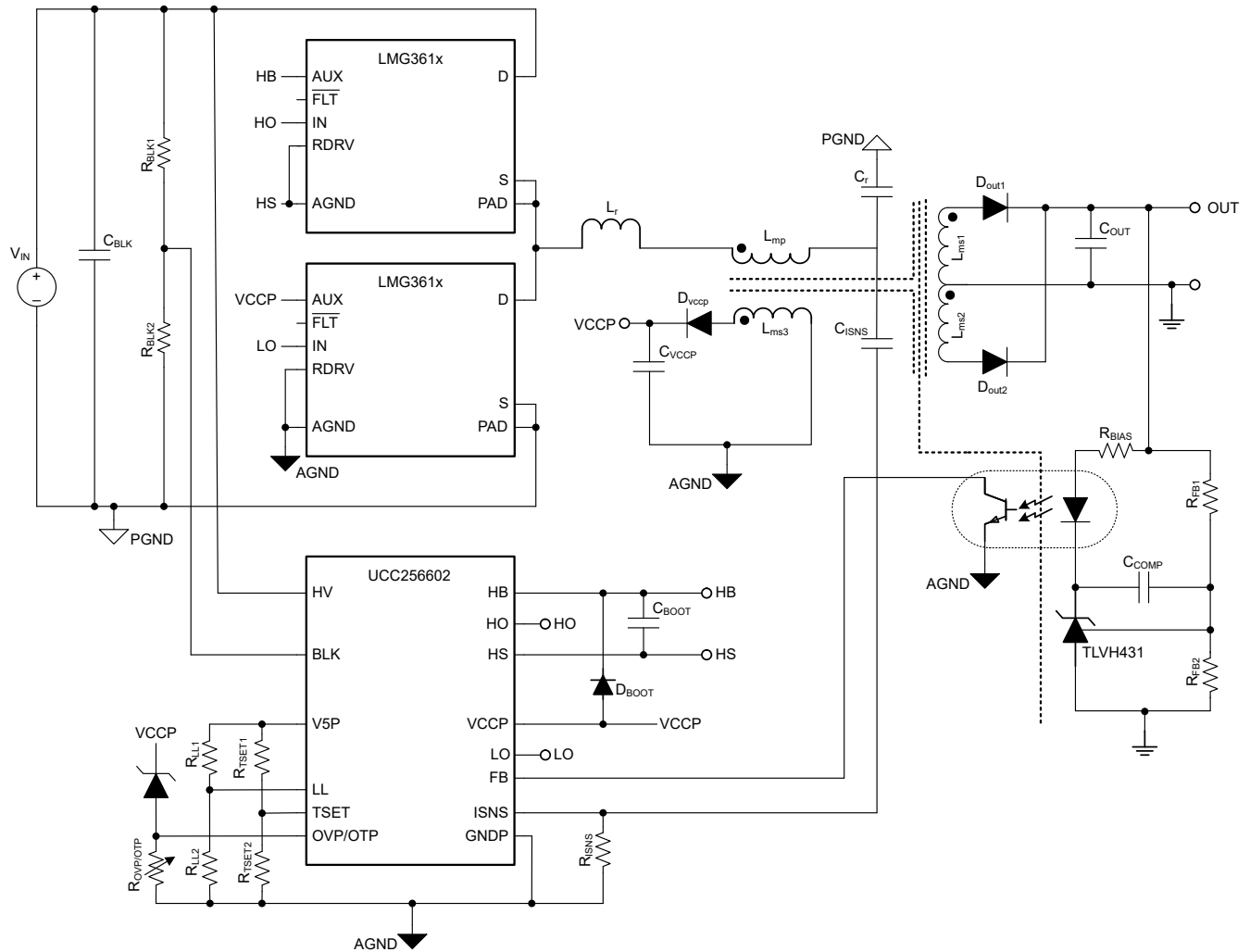
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMG3612 enables the simple adoption of GaN FET technology in switch-mode power-supply applications. The integrated gate driver, low IN input threshold voltage, and wide AUX input-supply voltage allows the LMG3612 to seamlessly pair with common industry power-supply controllers.

Using the LMG3612 only requires setting the desired turn-on slew rate with a programming resistor.

8.2 Typical Application



8-1. 280-W LLC Converter Application

8.2.1 Design Requirements

表 8-1. Design Specification

SPECIFICATION	VALUE
Input DC voltage range	365 VDC to 410 VDC
Output DC voltage	12 V
Output rated current	23.34 A
Output voltage ripple at 390 VDC	120 mVpp
Peak efficiency at 390 VDC	93%

8.2.2 Detailed Design Procedure

The typical application shows the LMG3612 pairing seamlessly with the Texas Instruments [UCC25660](#) LLC controller to create a high-power-density, high-efficiency, 280-W, LLC converter. The 280-W LLC converter application is adapted from the typical application found in the UCC25660 data sheet. The UCC25660 data sheet typical application design procedure is not repeated here. Refer to the UCC25660 data sheet for the details in designing the LLC primary power stage and in using the UCC25660 controller. This detailed design procedure focuses on the specifics of using the LMG3612 in the application.

8.2.2.1 Turn-On Slew-Rate Design

The LMG3612 turn-on slew rates are programmed as discussed in the *Turn-On Slew-Rate Control* section. The design consideration is the trade-off between power supply efficiency and EMI / transient ringing. Slower turn-on slew-rates lessen EMI and ringing problems but can increase switching losses and vice versa.

The UCC256602 controller used in the typical application provides for ZVS in all expected converter operation. Since EMI and ringing issues are not seen in ZVS, the turn-on slew rate is programmed to the fastest setting to minimize third-quadrant losses at the beginning of the turn-on event. Third-quadrant losses are not impacted by the slew rate. However, third-quadrant losses are effected by the switch turn-on delay which is also a function of the programmed slew rate. The RDRV pins are shorted to the AGND pin to program the fastest slew rate settings.

8.3 Power Supply Recommendations

The LMG3612 operates from a single input supply connected to the AUX pin. The LMG3612 supports being operated from the same supply managed and used by the power supply controller. The wide recommended AUX voltage range of 10 V to 26 V overlaps common-controller supply-pin turn-on and UVLO voltage limits.

The AUX external capacitance is recommended to be a ceramic capacitor that is at least 0.03 μ F over operating conditions.

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 Solder-Joint Stress Relief

Large QFN packages can experience high solder-joint stress. Several best practices are recommended to provide solder-joint stress relief. First, the instructions for the NC1, NC2, and NC3 anchor pins found in [表 4-1](#) must be followed. Second, all the board solder pads must be non-solder-mask defined (NSMD) as shown in the land pattern example in the *Mechanical, Packaging, and Orderable Information* section. Finally, any board trace connected to an NSMD pad must be less than two thirds the width of the pad on the pad side where it is connected. The trace must maintain this two-thirds width limit for as long as it is not covered by solder mask. After the trace is under solder mask, there are no limits on the trace dimensions. All these recommendations are followed in the *Layout Example* section.

8.4.1.2 Signal-Ground Connection

Design the power supply with separate signal and power grounds that only connect in one location. Connect the LMG3612 AGND pin to signal ground. Connect the LMG3612 SL pin and PAD thermal pad to power ground.

This serves as the single connection point between the signal and power grounds since the AGND pin, S pin, and PAD thermal pad are connected internally. Do not connect the signal and power grounds anywhere else on the board except as recommended in the next sentence. To facilitate board debug with the LMG3612 not installed, connect the AGND pad to the PAD thermal pad as shown in the *Layout Example* section.

8.4.2 Layout Example

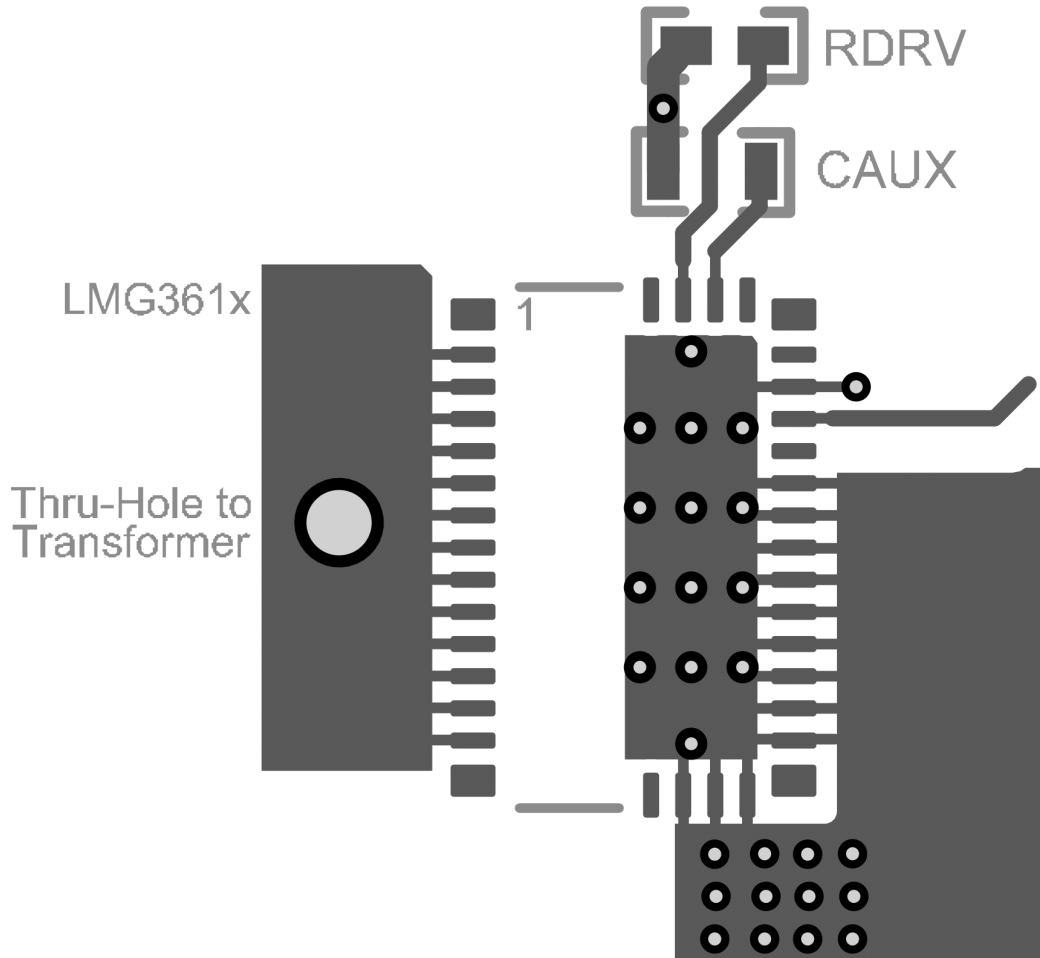


図 8-2. PCB Top Layer (First Layer)

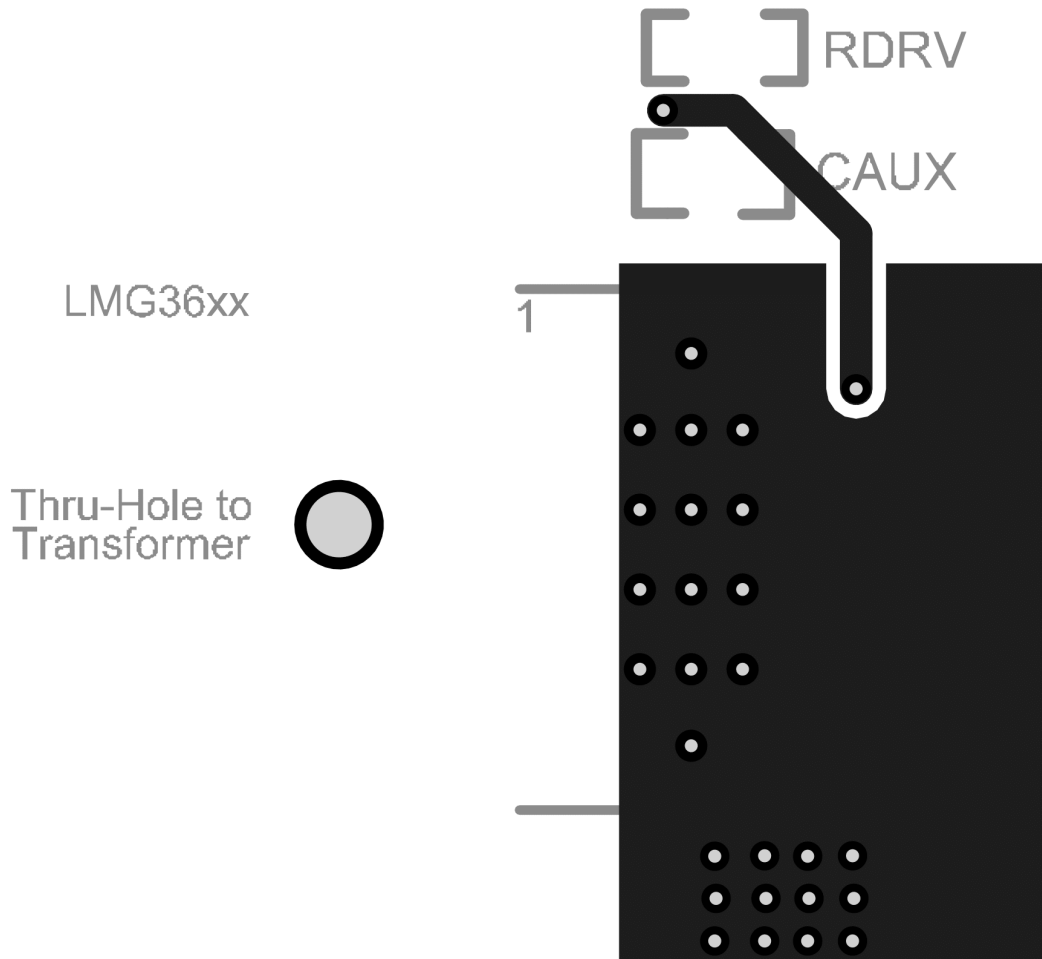


図 8-3. PCB Bottom Layer (Second Layer)

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

The [UCC25660X Design Calculator](#) is an Excel-based calculation tool for LLC converter design using the UCC25660 controller.

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[\[通知\]](#) をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

[テキサス・インスツルメンツ E2E™ サポート・フォーラム](#) は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2023	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMG3612REQR	ACTIVE	VQFN	REQ	38	2000	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	LMG3612 NNNNC	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

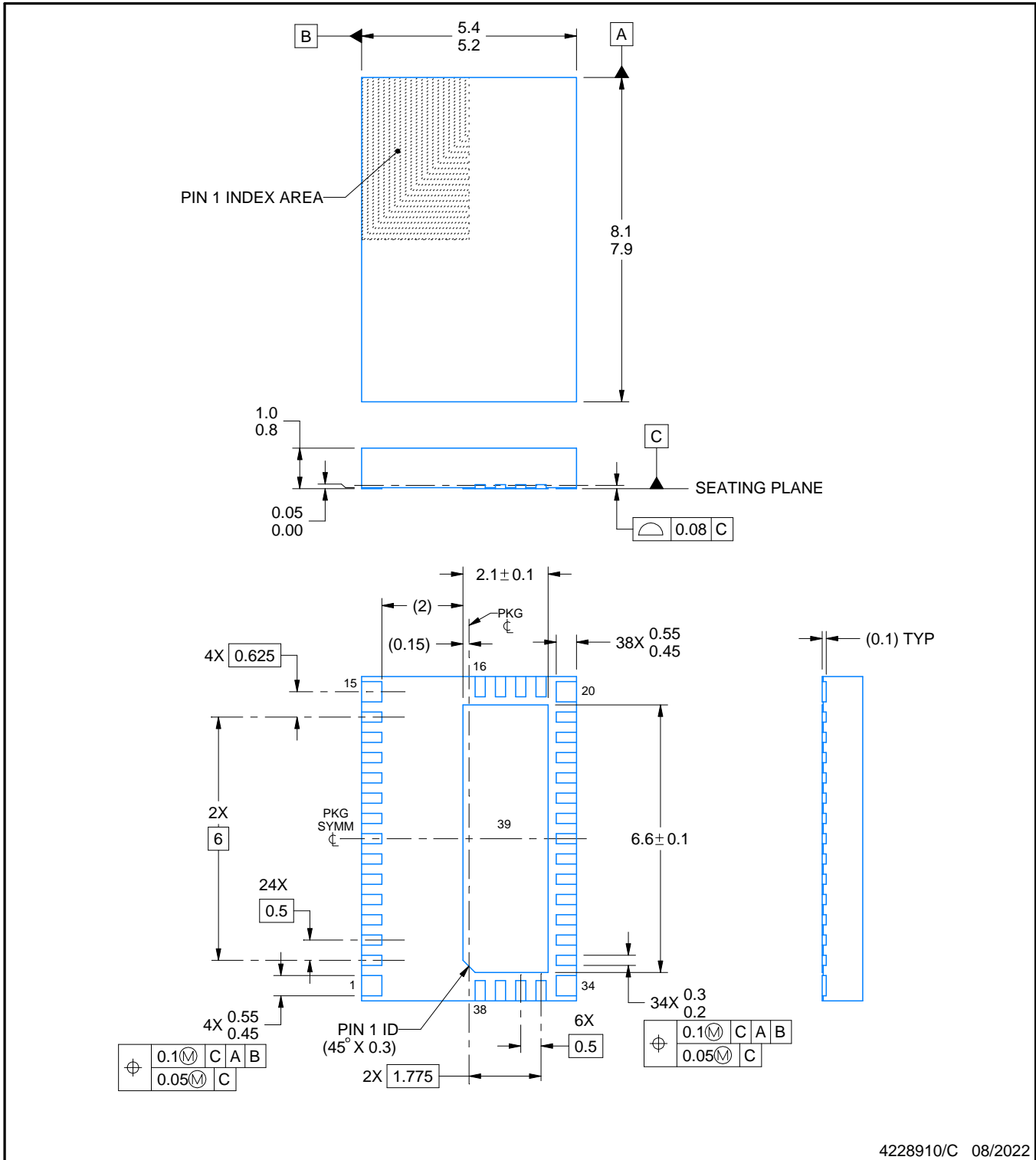
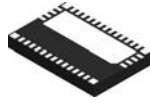
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



4228910/C 08/2022

NOTES:

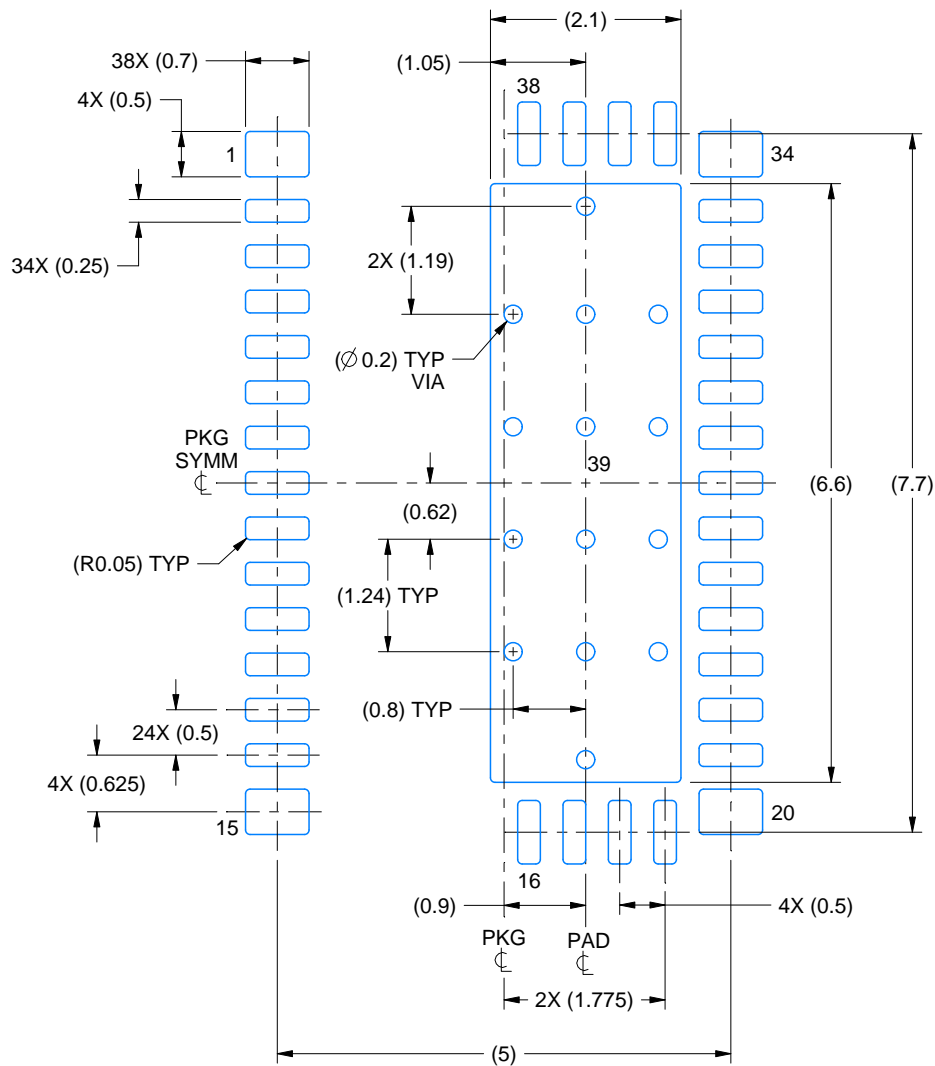
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

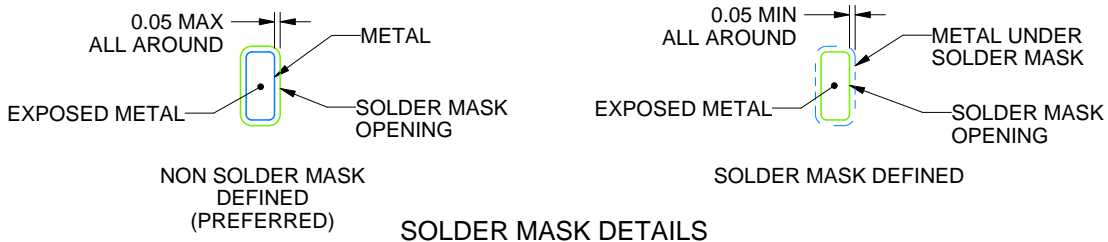
REQ0038A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



4228910/C 08/2022

NOTES: (continued)

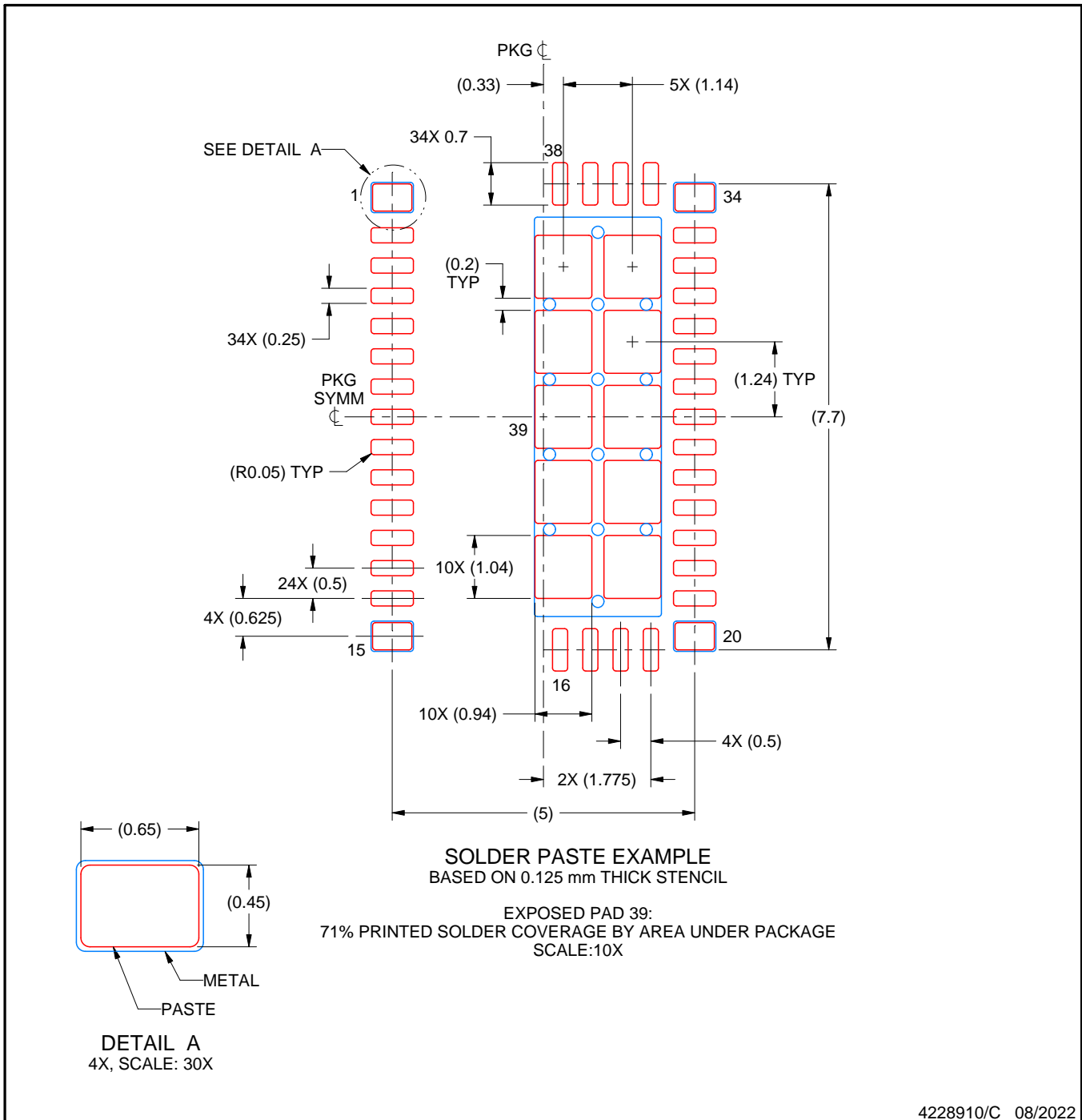
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

REQ0038A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated