TEXAS INSTRUMENTS
LMH32401
JAJSI19D – OCTOBER 2019 – REVISED JANUARY 2023

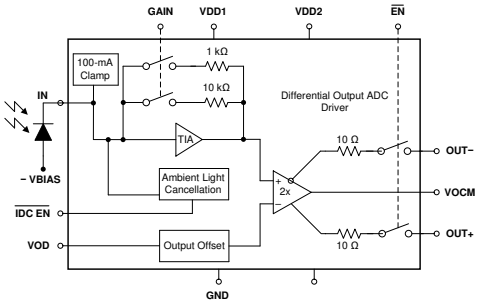
LMH32401 450-MHz、プログラマブル・ゲイン、差動出力のトランスインピーダンス・アンプ

1 特長

- 内蔵のプログラム・ゲイン：2kΩ～20kΩ
- 性能 (ゲイン = 2kΩ、C_{PD} = 1pF)
  - 帯域幅：450MHz
  - 入力換算ノイズ：250nA$_{RMS}$
  - 立ち上がり / 立ち下がり時間：0.8ns
- 性能 (ゲイン = 20kΩ、C_{PD} = 1pF)
  - 帯域幅：275MHz
  - 入力換算ノイズ：49nA$_{RMS}$
  - 立ち上がり / 立ち下がり時間：1.3ns
- 環境光キャンセル機能内蔵
- 内蔵の 100mA 保護クランプ
- 内蔵の出力マルチプレクサ
- 大きな出力振幅：1.5V$_{pp}$
- 静止電流：30mA
- パッケージ：16 ピン VQFN と ベア・ダイ
- 温度範囲：-40～+125℃

2 アプリケーション

- 機械式スキャン LIDAR
- ソリッド・ステート・スキャン LIDAR
- レーザー距離計
- 光学 ToF 位置センサ
- ドローン・ビジョン
- 産業用ロボットの LIDAR
- 移動型ロボットの LIDAR
- 掃除ロボットの LIDAR



概略ブロック図

3 概要

LMH32401 デバイスは、LIDAR (光検出と測距) アプリケーションとレーザー距離測定システムのための、プログラマブル・ゲイン、シングルエンド入力、差動出力のトランスインピーダンス・アンプです。LMH32401 デバイスは、2kΩ または 20kΩ のゲインに構成できます。LMH32401 デバイスは 1.5V$_{PP}$ の出力スイングを持ち、100Ω の負荷を駆動するように設計されています。

LMH32401 デバイスは、過負荷入力状態からアンプを保護し迅速にデバイスを回復させることができる 100mA のクランプを内蔵しています。LMH32401 は、フォトダイオードとアンプとの AC 結合の代わりに使用できる環境光キャンセル回路も内蔵しているため、システム・コストの低減に加えて、基板面積を削減できます。DC 結合が必要な場合は、環境光キャンセル回路を無効にできます。

LMH32401 デバイスは $\overline{EN}$ ピンを使用して低消費電力モードに移行させることができ、アンプを使用していないときに電力を節約できます。アンプを低消費電力モードに移行させると、出力ピンは高インピーダンス状態になります。この機能により、複数の LMH32401 アンプを 1 つの ADC に多重化し、$\overline{EN}$ 制御ピンをマルチプレクサ選択機能として使用できます。

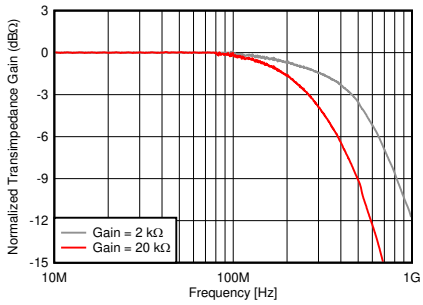
パッケージ情報(1)

部品番号	パッケージ	本体サイズ (公称)
LMH32401	VQFN (16)	3.00mm × 3.00mm

製品情報 (1)

部品番号	パッケージ	ダイ・サイズ (公称)
LMH32401	ベア・ダイ	1.025mm × 1.060mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



クローズド・ループのトランスインピーダンス帯域幅

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (August 2022) to Revision D (January 2023) — **Page**

- Updated the *backside potential* information for *bare die package* information in the *Pin Configuration and Functions* section ... 3

Changes from Revision B (February 2022) to Revision C (August 2022) — **Page**

- ベア・ダイのステータスをプレビューから *アクティブに変更* ... 1
- Updated the *bare die package* information in the *Pin Configuration and Functions* section ... 3

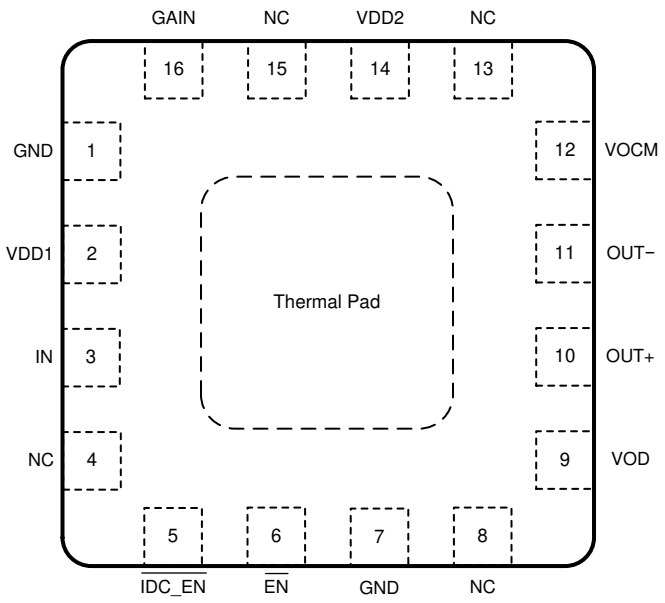
Changes from Revision A (September 2020) to Revision B (February 2022) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「特長」セクションと「製品情報」表にベア・ダイ・プレビュー・パッケージを追加 ... 1
- Added the *bare die preview package* to the *Pin Configuration and Functions* section ... 3

Changes from Revision * (October 2019) to Revision A (June 2020) — **Page**

- ステータスを「事前情報」から「量産データ」に変更 ... 1

5 Pin Configuration and Functions



Not to scale

図 5-1. RGT Package, 16-Pin VQFN with Exposed Thermal Pad (Top View)

表 5-1. Pin Functions

PIN		TYPE[2]	DESCRIPTION
NAME	NO.		
$\overline{EN}$	6	I	Device enable pin. $\overline{EN}$ = logic low = normal operation (default)[1]; $\overline{EN}$ = logic high = power off mode.
GAIN	16	I	Gain setting. GAIN = low = 2 kΩ (default)[1]; GAIN = high = 20 kΩ.
GND	1, 7	I	Amplifier ground.
$\overline{IDC\_EN}$	5	I	Ambient light cancellation (ALC) loop enable. $\overline{IDC\_EN}$ = logic low = enable DC current cancellation (default)[1]; $\overline{IDC\_EN}$ = logc high = disable DC current cancellation.
IN	3	I	Transimpedance amplifier input.
NC	4, 8, 13, 15	—	No connection.
OUT–	11	O	Inverting amplifier output. When light is incident on the photodiode the output pin transitions in a negative direction from the no light condition (APD anode connected to negative bias).
OUT+	10	O	Noninverting amplifier output. When light is incident on the photodiode the output pin transitions in a positive direction from the no light condition (APD anode connected to negative bias).
VDD1	2	I	Positive power supply for the transimpedance amplifier stage.
VDD2	14	I	Positive power supply for the differential amplifier stage. Tie VDD1 and VDD2 to the same power supply with independent power-supply bypassing.
VOCM	12	I	Differential amplifier common-mode output setting.
VOD	9	I	Differential amplifier differential output offset setting.
Thermal pad		—	Connect the thermal pad to GND or the most negative power supply of the device under test (DUT).

(1) TI recommends driving a digital pin with a low-impedance source rather than leaving the pin floating because fast-moving transients can couple into the pin and inadvertently change the logic level.
(2) I = input, O = output

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION
381 µm	Silicon with backgrind	Wafer backside is not electrically isolated and should be held at the same potential as the most negative power supply connected to the die (GND)	AlCu

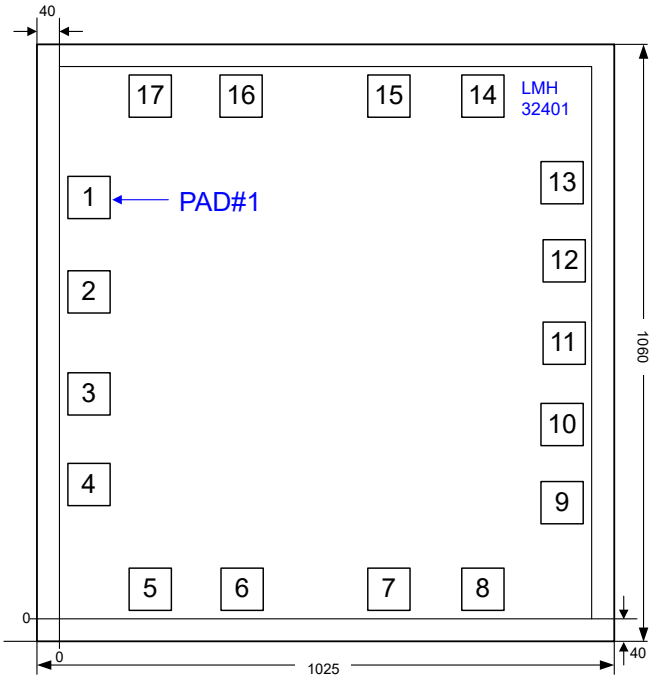


図 5-2. Bare Die Package

表 5-2. Bond Pad Coordinates of Bare Die Version in Microns

PAD NUMBER	PAD NAME	X-MIN	Y-MIN	X-MAX	Y-MAX
1	GND	15	711.4	90	786.4
2	VDD1	15	543	90	618
3	IN	15	362	90	437
4	NC	15	201	90	276
5	$\overline{\text{IDC\_EN}}$	124.675	15	199.675	90
6	$\overline{\text{EN}}$	286.675	15	361.675	90
7	GND	547.7	15	622.7	90
8	NC	713.675	15	788.675	90
9	VOD	855	169.075	930	244.075
10	OUT+	855	307.6	930	382.6
11	NC	855	452.5	930	527.5
12	OUT-	855	597.325	930	672.325
13	VOCM	855	736.05	930	811.05
14	NC	713.65	890	788.65	965
15	VDD2	547.675	890	622.675	965
16	NC	286.675	890	361.675	965
17	GAIN	124.675	890	199.675	965

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD1}, V_{DD2}	Total supply voltage, V_{DD} (2)		3.65	V
	Voltage at output pins	0	V_{DD}	V
	Voltage at logic pins	–0.25	V_{DD}	V
I_{IN}	Continuous current into IN		25	mA
I_{OUT}	Continuous output current		35	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VDD1 and VDD2 should always be tied to the same supply and have separate power-supply bypass capacitors.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Total supply voltage	3	3.3	3.45	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH32401(2) RGT (VQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Thermal information is applicable to packaged parts only.

6.5 Electrical Characteristics: Gain = 2 kΩ

V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, GAIN = 0 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		450		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		450		MHz
t_R, t_F	Rise and fall time	V_{OUT} = 100 mV_{PP}, pulse width = 10 ns		0.8		ns
	Slew rate(2)	V_{OUT} = 1 V_{PP}, pulse width = 10 ns		1100		V/µs
	Overload pulse extention (3)	I_{IN} = 10 mA, pulse width = 10 ns		4		ns
i_N	Integrated input current noise	f = 500 MHz		250		nA_{RMS}
DC PERFORMANCE						
Z_{21}	Small-signal transimpedance gain(4)		1.75	2	2.25	kΩ
V_{OD}	Differential output offset voltage (V_{OUT-} – V_{OUT+})		–12	3.5	12	mV
$\Delta V_{OD}/\Delta T_A$	Differential output offset voltage drift			±5.5		µV/°C
INPUT PERFORMANCE						
R_{IN}	Input Resistance		60	100	120	Ω
V_{IN}	Default input bias voltage	Input pin floating	2.42	2.47	2.52	V
$\Delta V_{IN}/\Delta T_A$	Default input bias voltage drift	Input pin floating		1.1		mV/°C
I_{IN}	DC input current range	Z_{21} < 3-dB degradation from I_{IN} = 50 µA	600	705		µA

(1) Input capacitance of photodiode.
(2) Average of rising and falling slew rate.
(3) Pulse width extension measured at 50% of pulse height of a square wave.
(4) Gain measured at the amplifier output pins when driving a 100-Ω resistive load. At higher resistor loads the gain increases.

6.6 Electrical Characteristics: Gain = 20 kΩ

V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, GAIN = 3.3 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		275		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		275		MHz
t_R, t_F	Rise and fall time	V_{OUT} = 100 mV_{PP}, pulse width = 10 ns		1.3		ns
	Slew rate(2)	V_{OUT} = 1 V_{PP}, pulse width = 10 ns		700		V/µs
	Overload pulse extension (4)	I_{IN} = 10 mA, pulse width = 10 ns		4		ns
i_N	Integrated input current noise	f = 250 MHz		49		nA_{RMS}
DC PERFORMANCE						
Z_{21}	Small-signal transimpedance gain(3)		17	20	22.5	kΩ
V_{OD}	Differential output offset voltage (V_{OUT-} – V_{OUT+})		–20	5	20	mV
$\Delta V_{OD}/\Delta T_A$	Differential output offset voltage			±17.5		µV/°C
INPUT PERFORMANCE						
R_{IN}	Input Resistance		270	350	410	Ω
V_{IN}	Default input bias voltage	Input pin floating	2.42	2.47	2.52	V
$\Delta V_{IN}/\Delta T_A$	Default input bias voltage drift	Input pin floating		1.1		mV/°C
I_{IN}	DC input current range	Z_{21} < 3-dB degradation from I_{IN} = 5 µA	60	72		µA

(1) Input capacitance of photodiode.
(2) Average of rising and falling slew rate.
(3) Gain measured at the amplifier output pins when driving a 100-Ω resistive load. At higher resistor loads the gain increases.
(4) Pulse width extension measured at 50% of pulse height of a square wave.

6.7 Electrical Characteristics: Both Gains

V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, GAIN = 0 V / 3.3 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT PERFORMANCE						
V_{OH}	Single-sided output voltage swing (high) (2)	T_A = 25°C	2.87	2.9		V
V_{OL}	Single-sided output voltage swing (low)(2)	T_A = 25°C		0.36	0.39	V
I_{OUT}	Linear output drive (sink and source)	T_A = 25°C, I_{IN} = 500 µA, gain = 2 kΩ, R_L = 25 Ω	24	26.6	32	mA
		T_A = –40°C, I_{IN} = 500 µA, gain = 2 kΩ, R_L = 25 Ω		27.1		
		T_A = 125°C, I_{IN} = 500 µA, gain = 2 kΩ, R_L = 25 Ω		25.1		
I_{SC}	Output short-circuit current (differential) (3)			70		mA
Z_{OUT}	DC output impedance (amplifier enabled)	Differential impedance	18	21	24	Ω
Z_{OUT}	DC output impedance in shutdown	Differential impedance	2.8	3.3		kΩ
OUTPUT COMMON-MODE CONTROL (V_{OCM}) PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OCM} = 100 mV_{PP} at VOCM pin		285		MHz
LSBW	Large-signal bandwidth	V_{OCM} = 1 V_{PP} at VOCM pin		85		MHz
e_N	Output common-mode noise	f = 10 MHz, 1-nF capacitor to GND on VOCM pin		17.8		nV/√Hz
A_V	Gain, ($\Delta V_{OCM}/\Delta$VOCM)	IN floating, VOCM = 1.1 V (driven)		1		V/V
	Gain error	T_A = 25°C, VOCM = 0.7 V to 2.3 V	–2%	0.5%	2%	
		T_A = –40°C to 125°C, VOCM = 0.7 V to 2.3 V		±1%		
	Input impedance			17		kΩ
$VOCM_{OS}$	VOCM pin default offset from 1.1 V	VOCM floating, (VOCM measured - 1.1 V)	0	10	20	mV
$\Delta V_{OCM}/\Delta I_{IN}$	V_{OCM} error vs Input current	Gain = 20 kΩ, VOCM driven to 1.1 V		–15		µV/µA
V_{OCM}	Output common-mode voltage, (V_{OUT+} + V_{OUT-})/2	T_A = 25°C, VOCM pin floating	1.05	1.1	1.15	V
	Output common-mode voltage drift, ($\Delta V_{OCM}/\Delta T_A$)	T_A = –40°C to 125°C, VOCM pin floating		75		µV/°C
V_{OCM}	Output common-mode voltage, (V_{OUT+} + V_{OUT-})/2	T_A = 25°C, VOCM pin driven to 1.1 V	1.05	1.1	1.15	V
	Output common-mode voltage drift, ($\Delta V_{OCM}/\Delta T_A$)	T_A = –40°C to 125°C, VOCM pin driven to 1.1 V		–14		µV/°C

V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, GAIN = 0 V / 3.3 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DIFFERENTIAL OFFSET (V_{OD}) PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OD} = 100 mV_{PP} at VOD pin		45		MHz
LSBW	Large-signal bandwidth	V_{OD} = 1 V_{PP}		14		MHz
V_{OS_D}	Differential output offset, V_{OUT} = (V_{OUT-} –V_{OUT+})	IN floating, VOD = 0.5 V	490	510	530	mV
	Differential output offset drift, $\Delta V_{OS\_D}/\Delta T_A$	IN floating, VOD = 0.5 V		0.03		mV/°C
V_{OS_D}	Differential output offset, V_{OUT} = (V_{OUT-} –V_{OUT+})	IN floating, VOD floating	490	510	530	mV
	Differential output offset drift, $\Delta V_{OS\_D}/\Delta T_A$	IN floating, VOD floating		0.04		mV/°C
A_V	Gain, ($\Delta V_{OUT}/\Delta VOD$), where V_{OUT} = (V_{OUT-} –V_{OUT+})	IN floating, VOCM = 1.1 V (driven)		1.01		V/V
	Gain error	T_A = 25°C, VOD = 0 V to 1.2 V	–5%	–1%	5%	
		T_A = –40°C to 125°C, VOD = 0 V to 1.2 V		±1.5%		
	Input impedance			2.5		kΩ
AMBIENT LIGHT CANCELLATION PERFORMANCE ($\overline{IDC\_EN}$ = 0 V) (4)						
	Settling time (within V_{OD} limit)	I_{IN} = 0 µA → 100 µA, GAIN = 2 kΩ		18		µs
		I_{IN} = 0 µA → 10 µA, GAIN = 20 kΩ		2.5		
		I_{IN} = 100 µA → 0 µA, GAIN= 2 kΩ		35		
		I_{IN} = 10 µA → 0 µA, GAIN = 20 kΩ		13		
	Ambient light current cancellation range	Differential output offset (V_{OUT-} – V_{OUT+}) shift from I_{DC} = 10 µA < ±10 mV	2	3		mA
POWER SUPPLY						
I_Q	Quiescent current, total	T_A = 25°C	24	30	33.5	mA
		T_A = 125°C		32		
		T_A = –40°C		27		
PSRR+	Positive power-supply rejection ratio, VDD1 = VDD2		54	66		dB
SHUTDOWN						
I_Q	Disabled quiescent current ($\overline{EN}$ = V_{DD})	T_A = 25°C	2.4	3.3	4.2	mA
		T_A = –40°C		2.75		
		T_A = 125°C		5.2		
	Enable pin input bias current	T_A = 25°C		75	120	µA

(1) Input capacitance of photodiode.
(2) Output levels achieved by adjusting VOCM, VOD, and input current.
(3) Device cannot withstand continuous short-circuit between the differential outputs.
(4) Enabling the ambient light cancellation loop adds noise to the system.

6.8 Electrical Characteristics: Logic Threshold and Switching Characteristics

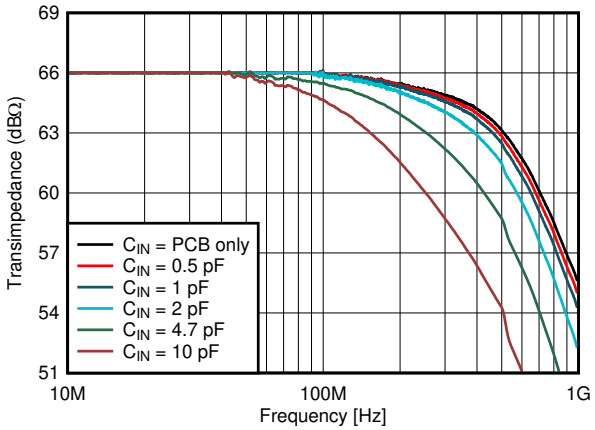
V_{DD} = 3.3 V, V_{OCM} = Open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, GAIN = 0 V / 3.3 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω, and T_A = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD PERFORMANCE						
	High gain enable, threshold voltage	Amplifier in high gain above this voltage		1.8	2	V
	Low gain enable, threshold voltage	Amplifier in low gain below this voltage	0.8	1		V
	$\overline{EN}$ control, disable threshold voltage	Amplifier disabled above this voltage		1.8	2	V
	$\overline{EN}$ control, enable threshold voltage	Amplifier enabled below this voltage	0.8	1		V
	$\overline{IDC\_EN}$ control, disable threshold voltage	Ambient light cancellation loop disabled above this voltage		1.8	2	V
	$\overline{IDC\_EN}$ control, enable threshold voltage	Ambient light cancellation loop enabled below this voltage	0.8	1		V
GAIN CONTROL TRANSIENT PERFORMANCE						
	High gain to low gain transition-time, (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP} (Initial condition), I_{DC} = 0 µA		90		ns
	Low gain to high gain transition-time, (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP} (Final condition), I_{DC} = 0 µA		750		ns
	High gain to low gain transition-time, (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP} (Initial condition), I_{DC} = 100 µA		4		µs
	Low gain to high gain transition-time, (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP} (Final condition), I_{DC} = 100 µA		4		µs
$\overline{EN}$ CONTROL TRANSIENT PERFORMANCE						
	Enable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA, GAIN = 2 kΩ		125		ns
	Disable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA, GAIN = 2 kΩ		3		ns
	Enable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA, GAIN = 20 kΩ		850		ns
	Disable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA, GAIN = 20 kΩ		3		ns
	Enable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA, GAIN = 2 kΩ		10		µs
	Disable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA, GAIN = 20 kΩ		3.5		ns
	Enable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA, GAIN = 20 kΩ		4		µs
	Disable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA, GAIN = 2 kΩ		3		ns

(1) Input capacitance of photodiode.

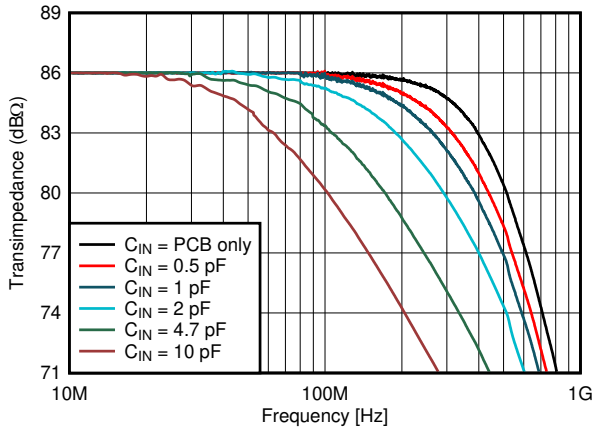
6.9 Typical Characteristics

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted).



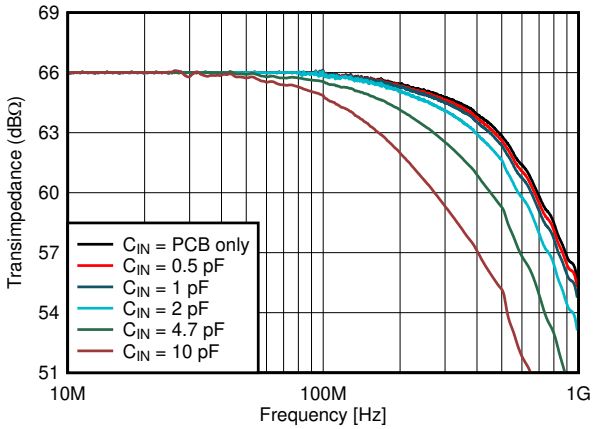
Gain = 2 kΩ, V_{OUT} = 100 mV_{PP}

図 6-1. Small Signal Response vs Input Capacitance



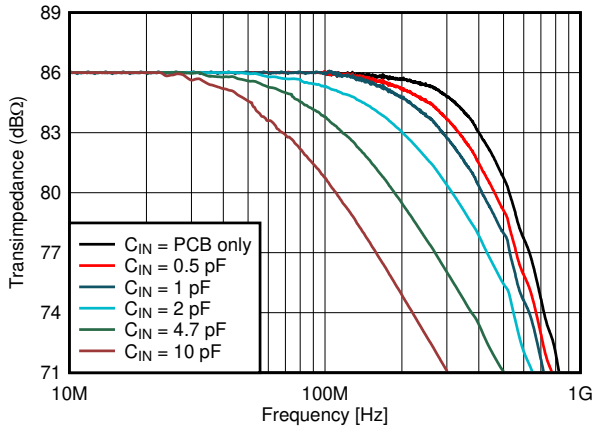
Gain = 20 kΩ, V_{OUT} = 100 mV_{PP}

図 6-2. Small Signal Response vs Input Capacitance



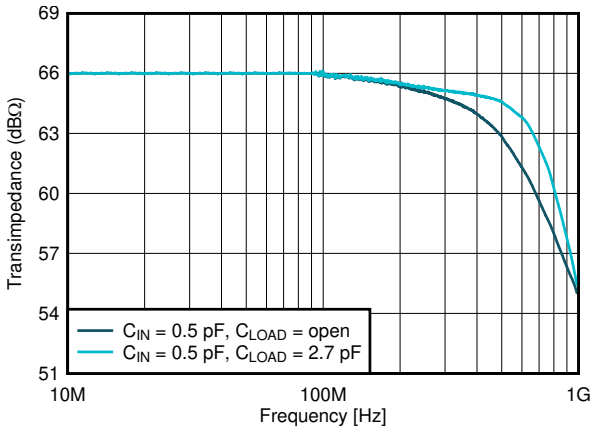
Gain = 2 kΩ, V_{OUT} = 1 V_{PP}

図 6-3. Large Signal Response vs Input Capacitance



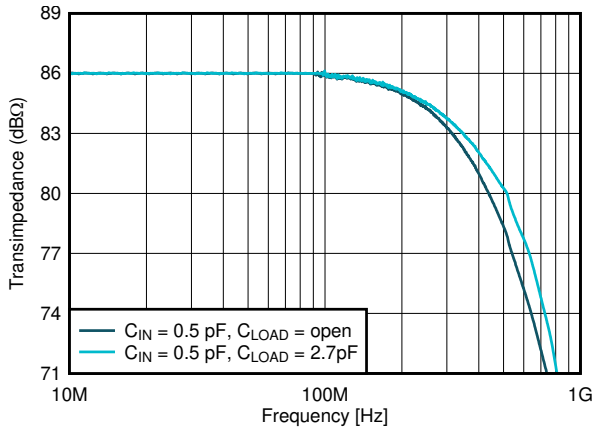
Gain = 20 kΩ, V_{OUT} = 1 V_{PP}

図 6-4. Large Signal Response vs Input Capacitance



Gain = 2 kΩ, V_{OUT} = 100 mV_{PP}

図 6-5. Small Signal Response vs Load Capacitance

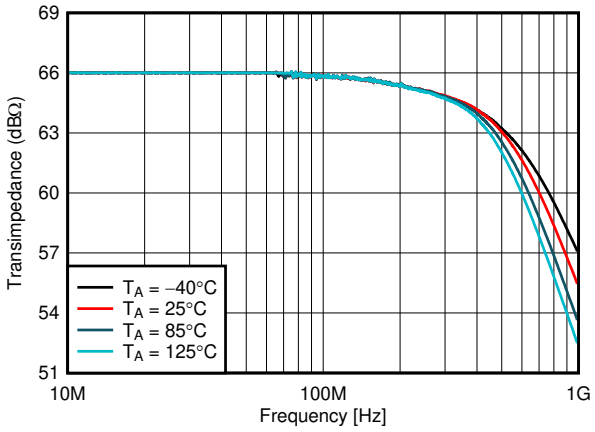


Gain = 20 kΩ, V_{OUT} = 100 mV_{PP}

図 6-6. Small Signal Response vs Load Capacitance

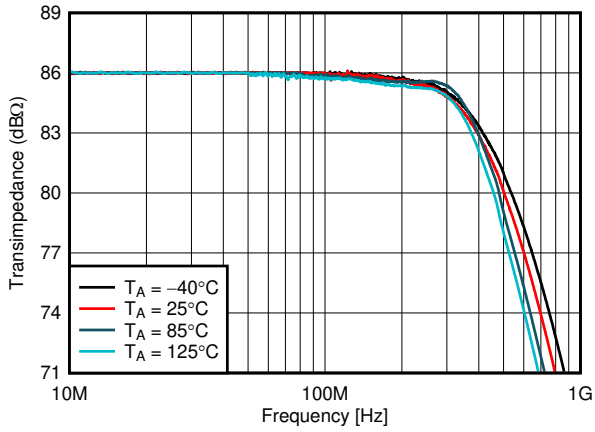
6.9 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted).



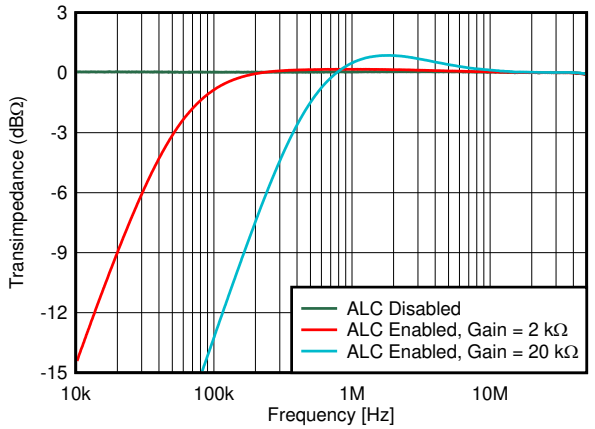
Gain = 2 kΩ, C_{IN} = PCB

図 6-7. Small Signal Response vs Ambient Temperature



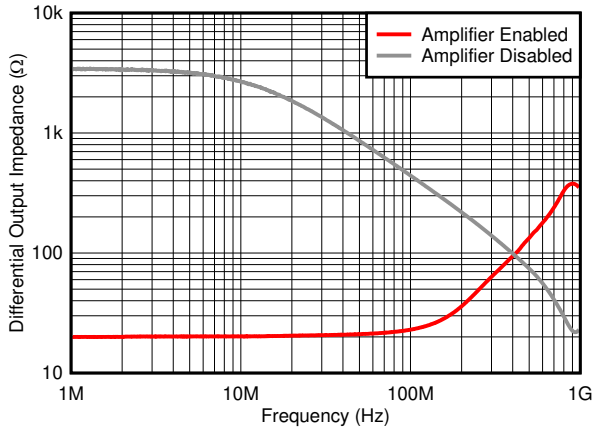
Gain = 20 kΩ, C_{IN} = PCB

図 6-8. Small Signal Response vs Ambient Temperature



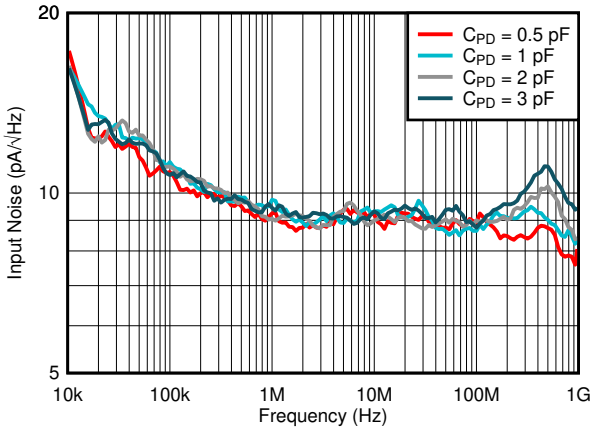
I_{DC_IN} = 100 µA

図 6-9. Low-side Frequency Response vs Ambient Light Cancellation



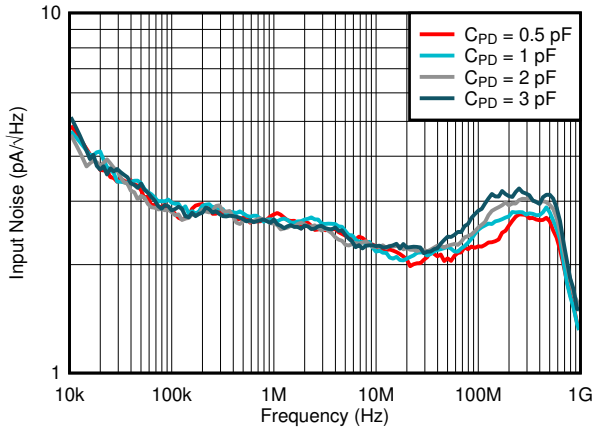
Gain = 2 kΩ

図 6-10. Closed-loop Output Impedance vs Frequency



Gain = 2 kΩ

図 6-11. Input Noise Density vs Input Capacitance



Gain = 20 kΩ

図 6-12. Input Noise Density vs Input Capacitance

6.9 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted).

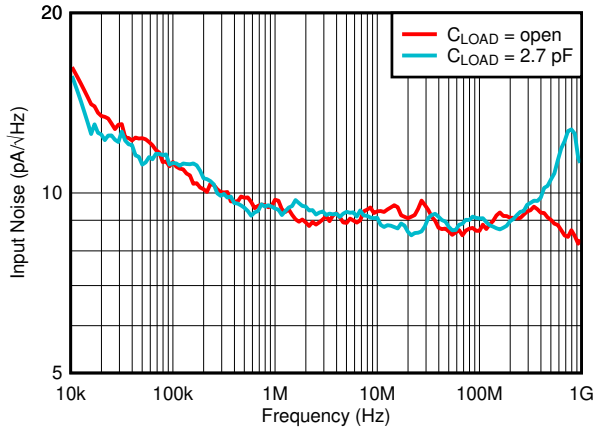


図 6-13. Input Noise Density vs Load Capacitance

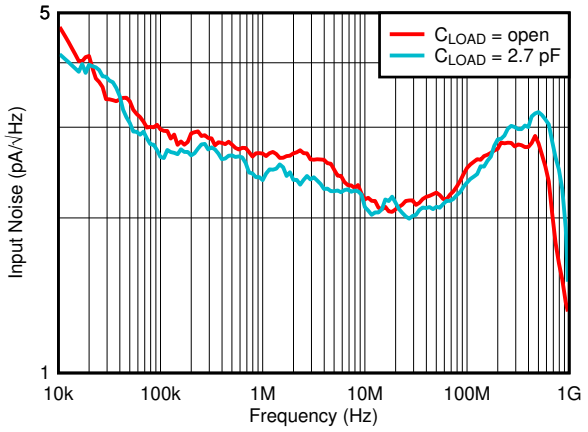


図 6-14. Input Noise Density vs Load Capacitance

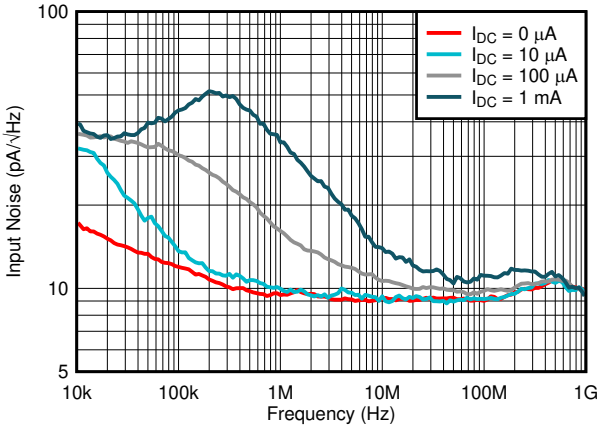


図 6-15. Input Noise Density vs Ambient Light DC Current

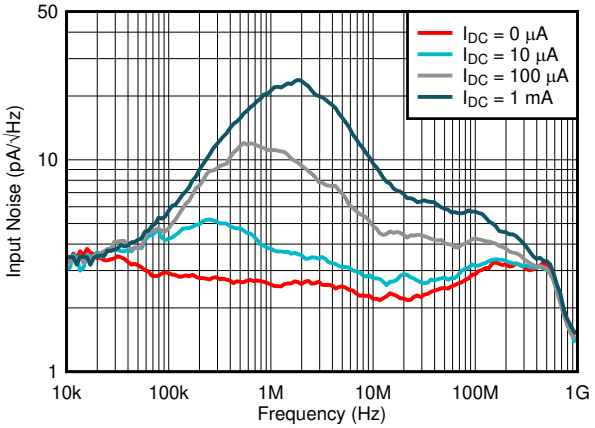


図 6-16. Input Noise Density vs Ambient Light DC Current

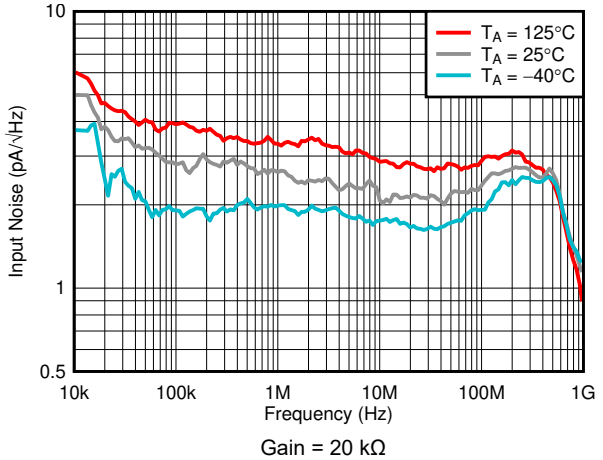


図 6-17. Input Noise Density vs Ambient Temperature

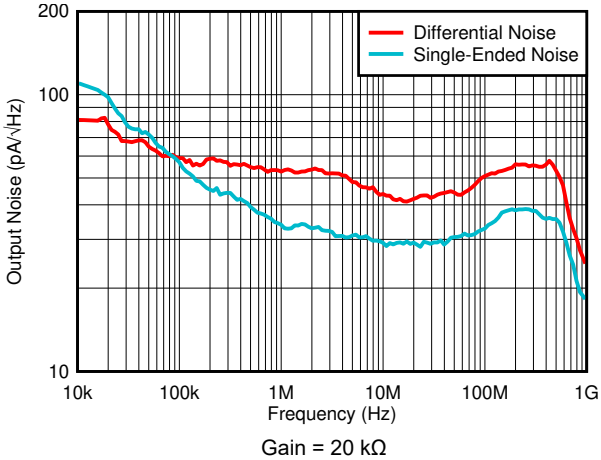
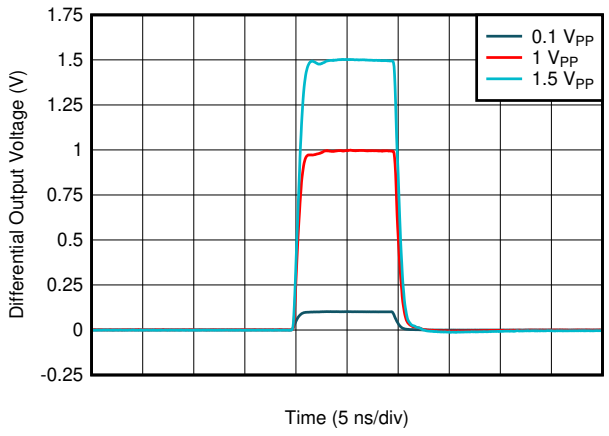


図 6-18. Output Noise Density vs Output Configuration

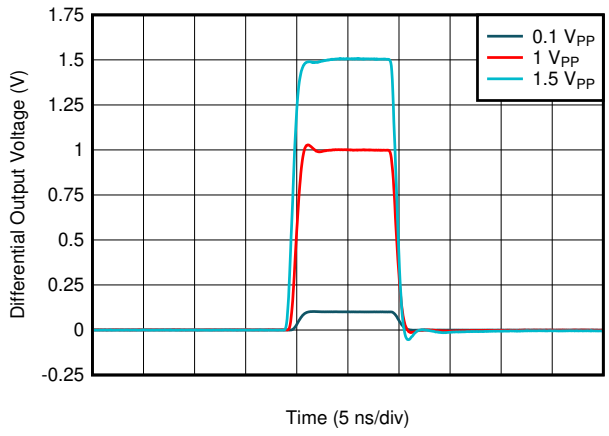
6.9 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted).



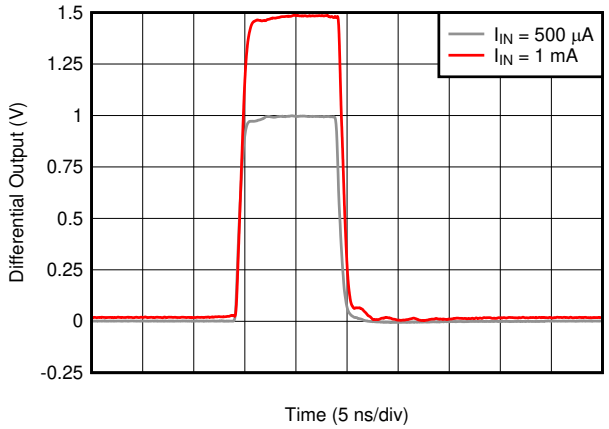
Gain = 2 kΩ

図 6-19. Pulse Response vs Output Swing



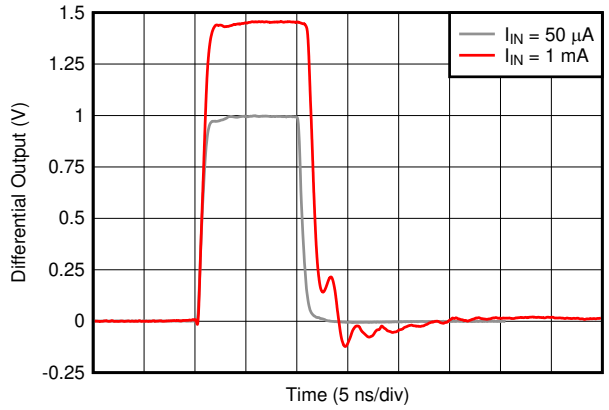
Gain = 20 kΩ

図 6-20. Pulse Response vs Output Swing



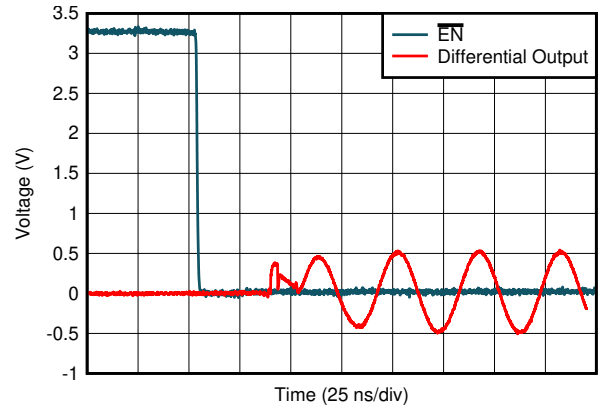
Gain = 2 kΩ

図 6-21. Overloaded Pulse Response



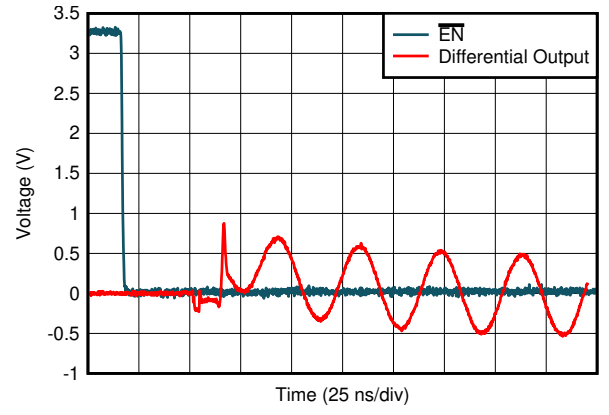
Gain = 20 kΩ

図 6-22. Overloaded Pulse Response



Gain = 2 kΩ

図 6-23. Turn-On Time

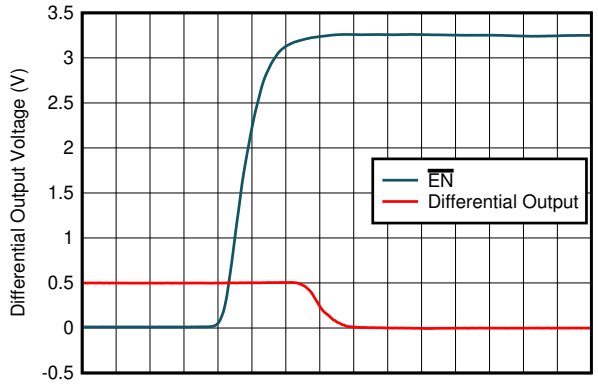


Gain = 20 kΩ

図 6-24. Turn-On Time

6.9 Typical Characteristics (continued)

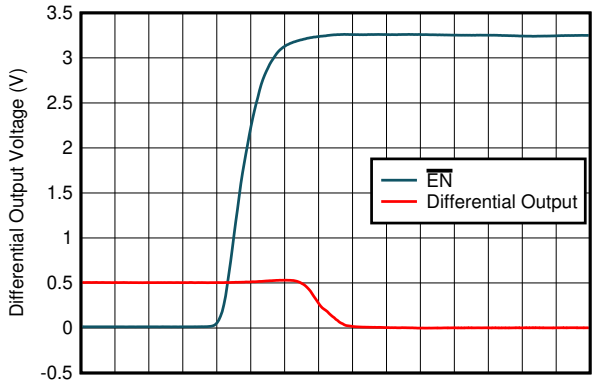
At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted).



Time (1 ns/div)

Gain = 2 kΩ, VOD = 0.5 V

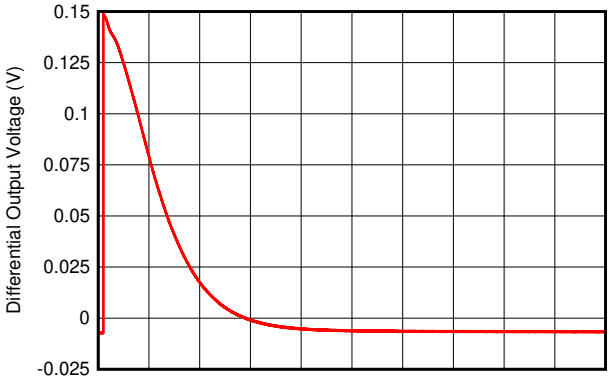
図 6-25. Turn-Off Time



Time (1 ns/div)

Gain = 20 kΩ, VOD = 0.5 V

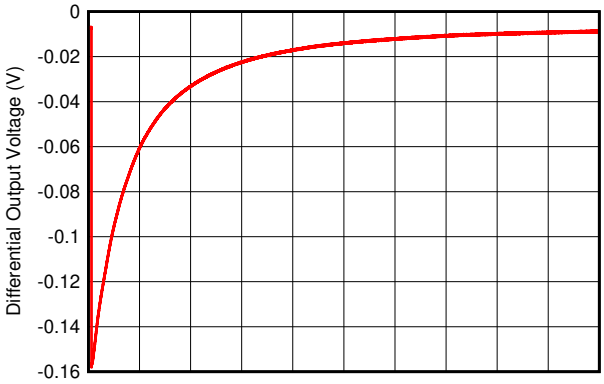
図 6-26. Turn-Off Time



Time (5 µs/div)

Gain = 2 kΩ, I_{DC_IN} = 0 µA → 100 µA [1]

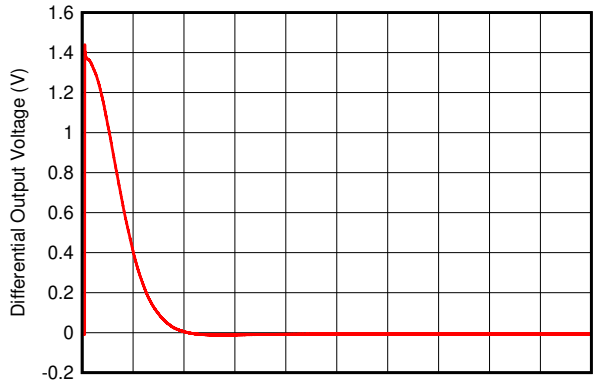
図 6-27. Ambient Loop Cancellation Settling Time



Time (5 µs/div)

Gain = 2 kΩ, I_{DC_IN} = 100 µA → 0 µA[1]

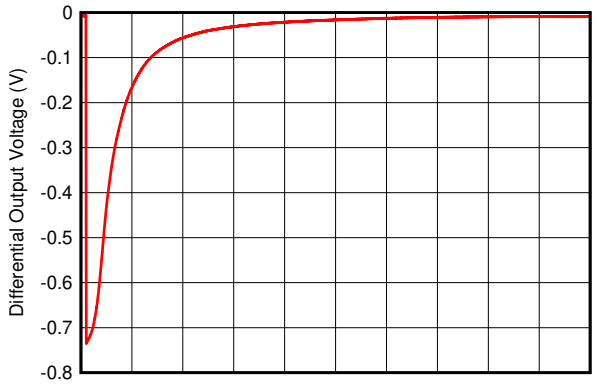
図 6-28. Ambient Loop Cancellation Settling Time



Time (1 µs/div)

Gain = 20 kΩ, I_{DC_IN} = 0 µA → 100 µA[1]

図 6-29. Ambient Loop Cancellation Settling Time



Time (2 µs/div)

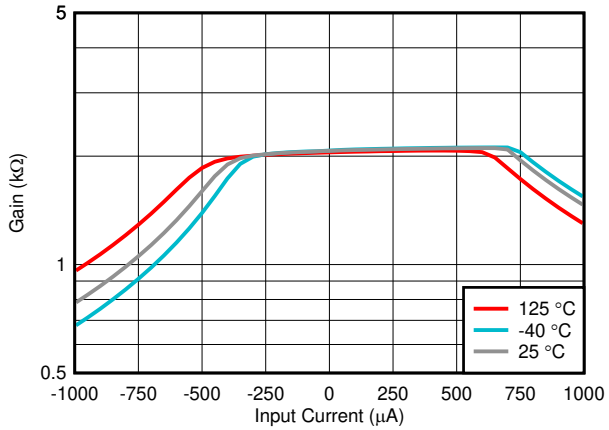
Gain = 20 kΩ, I_{DC_IN} = 100 µA → 0 µA[1]

図 6-30. Ambient Loop Cancellation Settling Time

[1] Current due to ambient light transitions at t = 0 in.

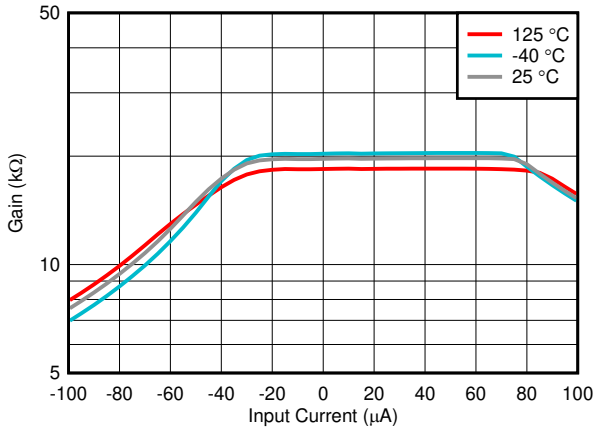
6.9 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted).



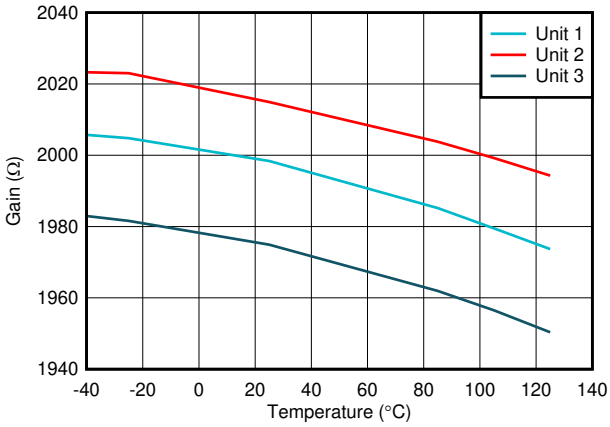
Gain = 2 kΩ, positive current is sinking current into the photodiode's cathode

図 6-31. Transimpedance Gain vs Input Current



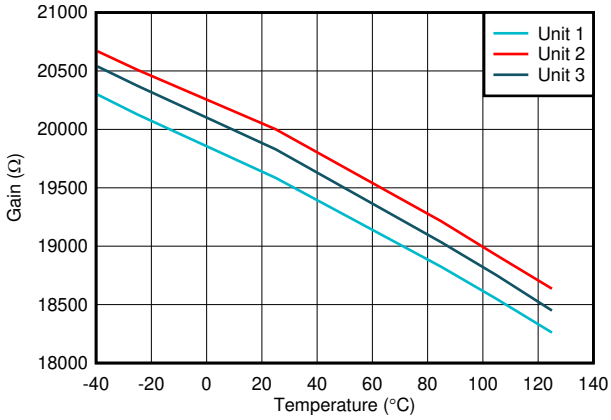
Gain = 20 kΩ, positive current is sinking current into the photodiode's cathode

図 6-32. Transimpedance Gain vs Input Current



Gain = 2 kΩ

図 6-33. Transimpedance Gain vs Ambient Temperature



Gain = 20 kΩ

図 6-34. Transimpedance Gain vs Ambient Temperature

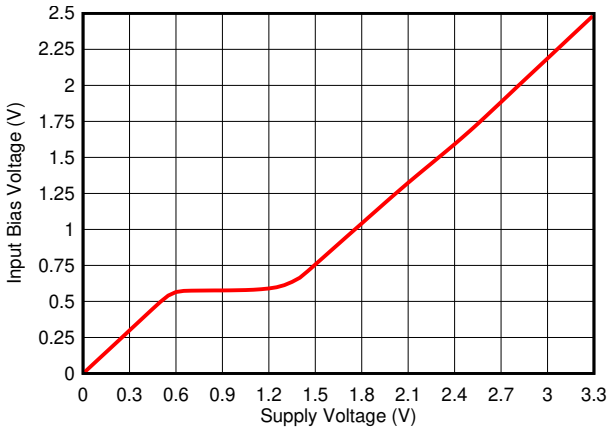
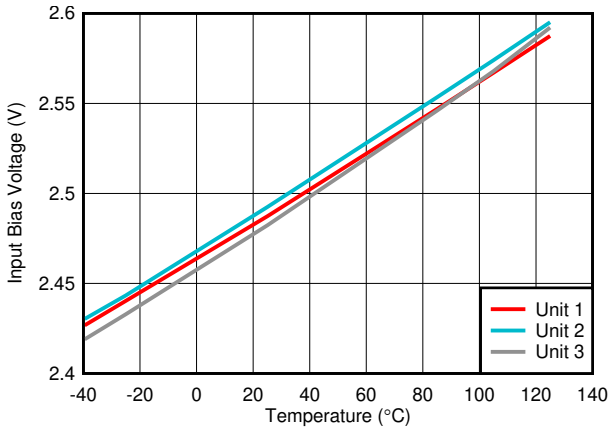


図 6-35. Input Bias Voltage vs Supply Voltage



Gain = 20 kΩ

図 6-36. Input Bias Voltage vs Ambient Temperature

6.9 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted).

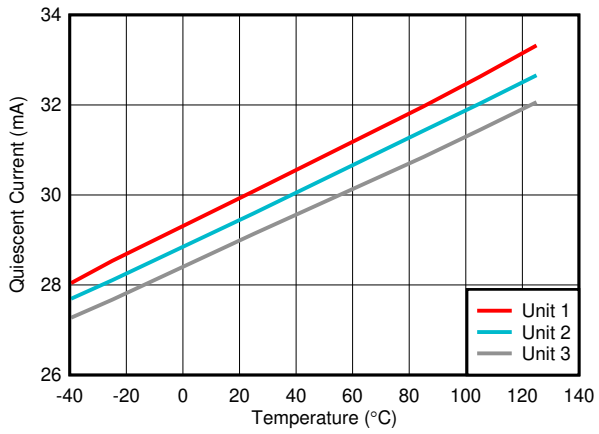


図 6-37. Quiescent Current vs Ambient Temperature

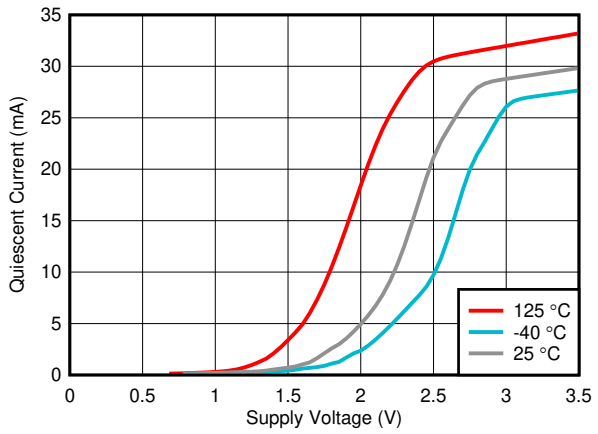
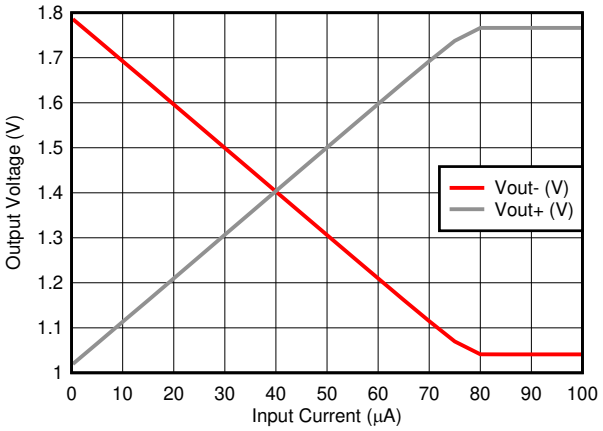
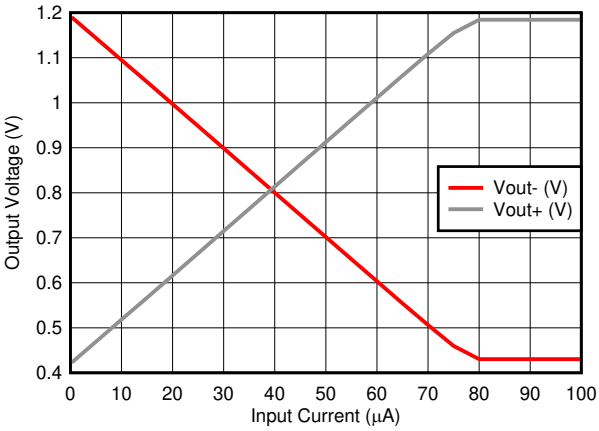


図 6-38. Quiescent Current vs Supply Voltage



VOD = 0.75 V, VOCM = 1.4 V

図 6-39. High-side Swing vs Input Current



VOD = 0.75 V, VOCM = 0.8 V

図 6-40. Low-side Swing vs Input Current

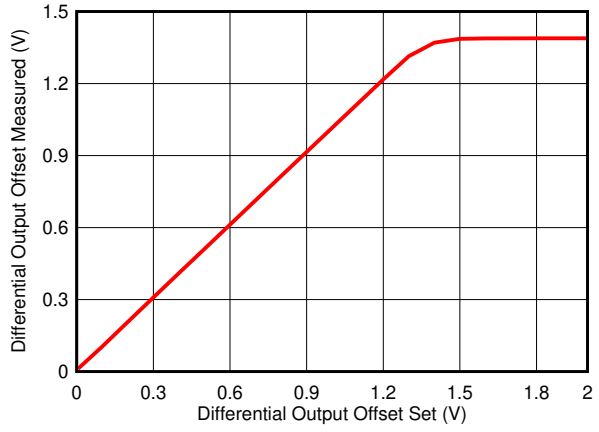


図 6-41. Differential Output Offset Gain

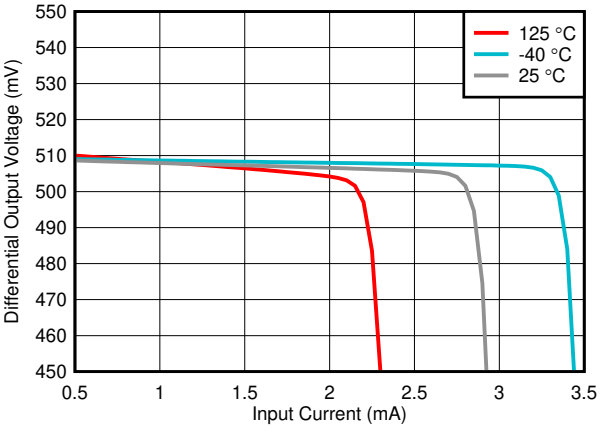
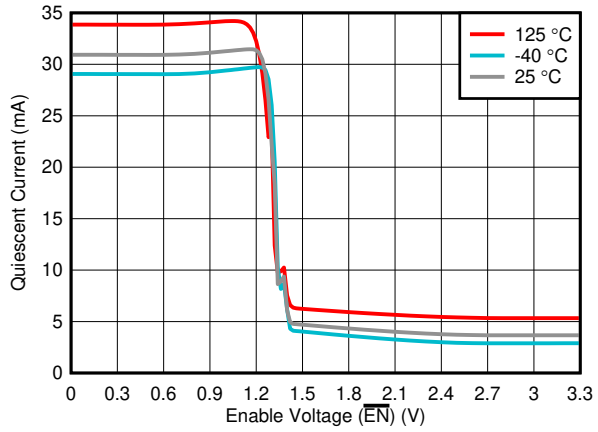


図 6-42. Ambient Light Cancellation Range vs Ambient Temperature

6.9 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted).



Logic switching demonstrated using $\overline{EN}$ pin. $\overline{IDC\_EN}$ and gain pins behave similarly.

図 6-43. Logic Threshold vs Ambient Temperature

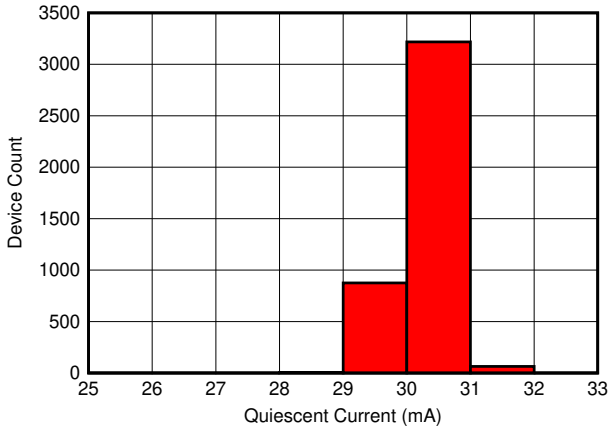


図 6-44. Quiescent Current Distribution

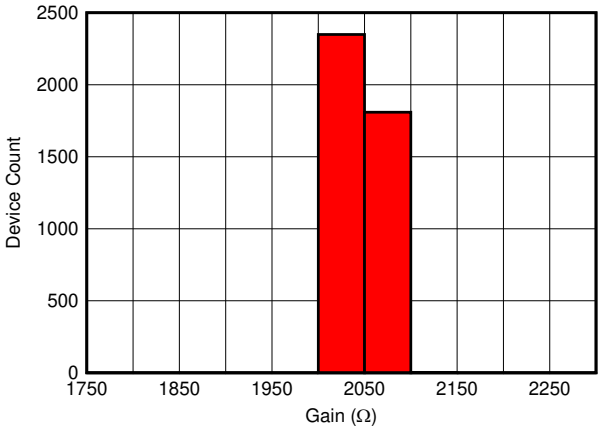
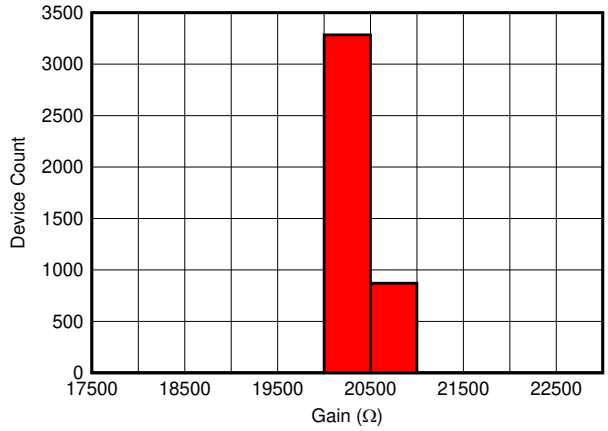


図 6-45. Transimpedance Gain (Low) Distribution



Gain = 20 kΩ

図 6-46. Transimpedance Gain (High) Distribution

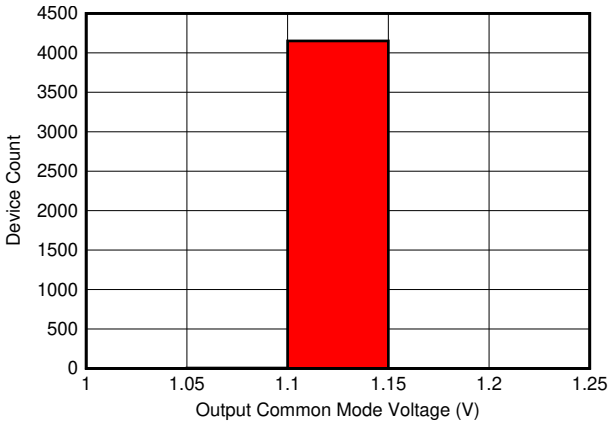


図 6-47. Output Common-Mode Voltage (V_{OCM}) Distribution

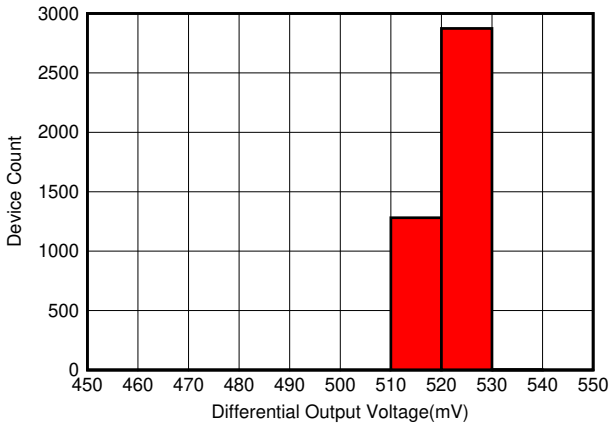


図 6-48. Differential Output Offset Voltage (V_{OD}) Distribution

6.9 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted).

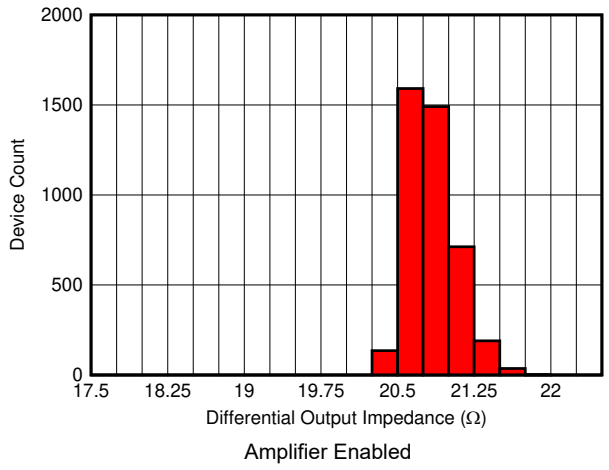


図 6-49. Differential Output Impedance (Z_{OUT}) Distribution

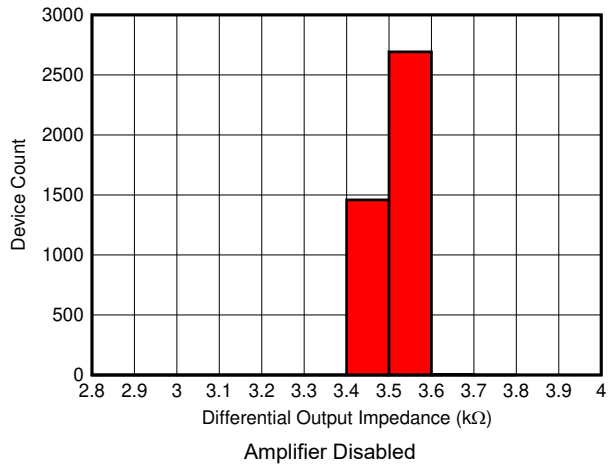


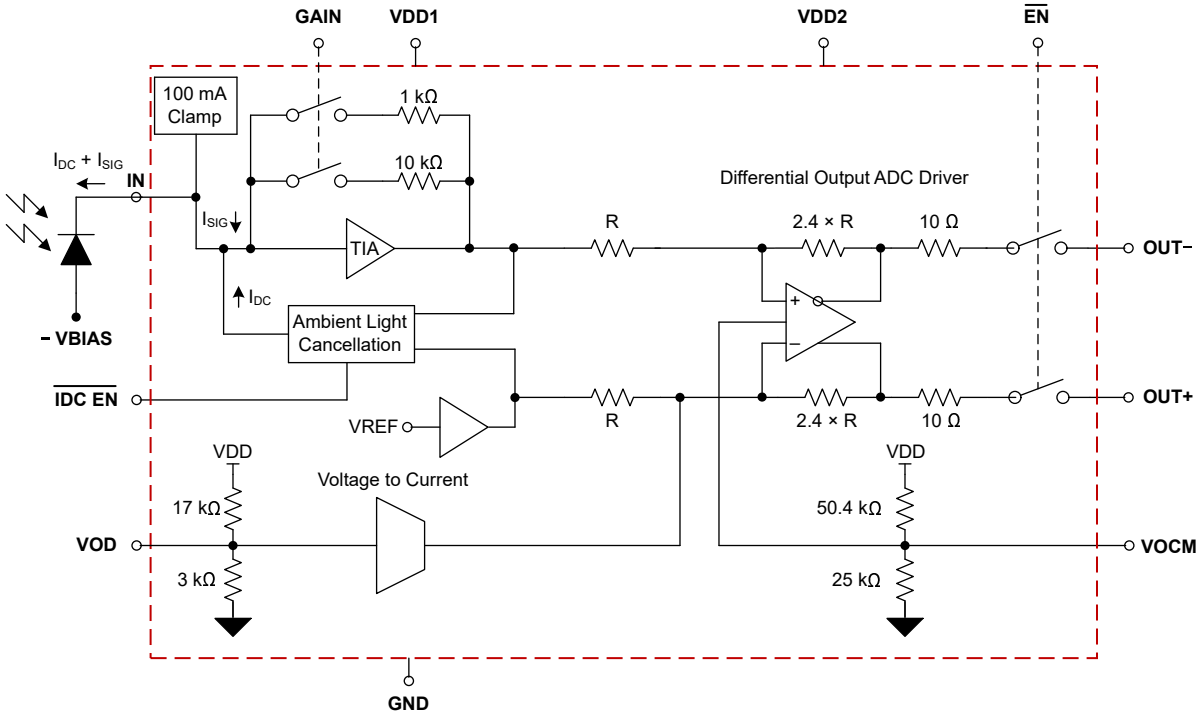
図 6-50. Differential Output Impedance (Z_{OUT}) Distribution

7 Detailed Description

7.1 Overview

The LMH32401 device is a single-channel, differential output, high-speed transimpedance amplifier (TIA) that features several integrated functions geared towards light detection and ranging (LIDAR) and pulsed time-of-flight (ToF) systems. The LMH32401 device is designed to work with photodiode (PD) configurations that can source or sink the current. When the photodiode sinks the photocurrent (anode is biased to a negative voltage and cathode is tied to the amplifier input) the fast recovery clamp activates when the amplifier input is overloaded. When the photodiode sources the photocurrent (cathode is biased to a positive voltage and anode is tied to the amplifier input) a soft clamp activates when the amplifier input is overloaded. When the soft clamp activates, the amplifier takes longer to recover. The recovery time depends on the level of input overload. The LMH32401 device is offered in a space-saving 3-mm × 3-mm, 16-pin VQFN package and is rated over a temperature range from –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Switched Gain Transimpedance Amplifier

The LMH32401 device features a programmable gain transimpedance amplifier (TIA) stage followed by a fixed-gain, single-ended input to differential output amplifier stage. The closed-loop bandwidth and noise of a TIA are affected by the transimpedance gain and photodiode capacitance. For a given value of photodiode capacitance, the LMH32401 device has higher bandwidth in its low-gain configuration compared to the high-gain configuration. Increasing the gain of the TIA stage by a factor of X increases the output signal by a factor X, but the noise contribution from the resistor only increases by $\sqrt{X}$. The input-referred noise density of the low-gain configuration is therefore higher than the input-referred noise density of the high-gain configuration.

The gain of the TIA stage is controlled by the GAIN pin. Setting this pin low places the TIA in its low-gain configuration, whereas setting the pin high places the TIA in a high-gain configuration. The LMH32401 device defaults to its low-gain configuration when the GAIN pin is left floating.

7.3.2 Clamping and Input Protection

The LMH32401 device is designed to work with photodiode (PD) configurations that can source or sink current; however, the LMH32401 is optimized for a sinking current configuration. It is assumed that the LMH32401 device is being used with a PD that is configured with its cathode tied to the amplifier input and the anode tied to a negative supply voltage, unless stated otherwise.

The LMH32401 features two internal clamps, a fast recovery clamp and a soft clamp. The fast recovery clamp is the active clamp when the photodiode is sinking a photocurrent. The soft clamp is the active clamp when the photodiode is sourcing a photocurrent. Stray reflections from nearby objects with high reflectivity can produce large output current pulses from the PD. The linear input range of the LMH32401 device is approximately 65 µA in the high-gain configuration and 650 µA in the low-gain configuration (PD sinking the photocurrent).

Input currents in excess of the linear current range cause the internal nodes of the amplifier to saturate, which increases the amplifier recovery time. The end result is a broadening of the output pulse leading to blind zones in the system response. To protect against this condition, the LMH32401 features an integrated clamp that absorbs and diverts the excess current to the positive supply (V_{DD1}) when the amplifier detects its nodes entering a saturated condition. The integrated clamp minimizes the pulse extension to less than a few ns for input pulses up to 100 mA. The power-supply pins (VDD1 and VDD2) must each have their own bypass capacitors to prevent large input pulses from affecting the differential output stage. When the amplifier is in low-power mode, the clamp circuitry is still active, thereby protecting the TIA input.

7.3.3 ESD Protection

All LMH32401 pins have an internal electrostatic discharge (ESD) protection diode to the positive and negative supply rails to protect the amplifier from ESD events.

7.3.4 Differential Output Stage

The differential output stage of the LMH32401 device performs the following two functions, which are common across all differential amplifiers:

1. Converts the single-ended output from the TIA stage to a differential output.
2. Performs a common-mode output shift to match the specified ADC input common-mode voltage.

The differential output stage has two 10-Ω series resistors on its output to isolate the amplifier output stage transistors from the package bond-wire inductance and printed circuit board (PCB) capacitance. The net gain of the LMH32401 device (TIA + output stage) is 2 kΩ (low gain) and 20 kΩ (high gain) when driving an external 100-Ω resistor. When the external load resistor is increased above 100 Ω, the effective gain from the IN pin to the differential output pin increases. Conversely, when the external load resistor is decreased to less than 100 Ω, the effective gain from the IN pin to the differential output pin decreases as a result of the larger voltage drop across the two internal 10-Ω resistors. When there is no load resistor between the OUT+ and OUT– pins, the effective gain of the LMH32401 is 2.4 kΩ and 24 kΩ in the low-gain and high-gain configurations, respectively.

The output common-mode voltage of the LMH32401 device can be set externally through the VOCM pin. A resistor divider internal to the amplifier, between VDD2 and ground sets the default voltage to 1.1 V. The internal resistors generate common-mode noise that is typically rejected by the CMRR of the subsequent ADC stage. To maximize the amplifier signal-to-noise ratio (SNR), place an external noise bypass capacitor to ground on the VOCM pin. In single-ended signal chains, such as ToF systems that use time-to-digital converters (TDCs), only a single output of the LMH32401 device is needed. In such situations, terminate the unused differential output in the same manner as the used output to maintain balance and symmetry. The signal swing of the single-ended output is half the available differential output swing. Additionally, the common-mode noise of the output stage, which is typically rejected by the differential input ADC, is now added to the total noise, further degrading SNR.

The output stage of the LMH32401 device has an additional VOD input that sets the differential output between OUT– and OUT+. 図 7-1 shows how each output pin of the LMH32401 device is at the voltage set by the VOCM pin (default = 1.1 V) when the photodiode output current is zero and the VOD input is set to 0 V. When the VOD pin is driven to a voltage of *X* volts, the two output pins are separated by *X* volts when the photodiode current is zero. The average voltage is still equal to VOCM. For example, 図 7-2 shows if VOCM is set to 1.1 V and VOD is set to 0.4 V, then OUT– = 1.1 V + 0.2 V = 1.3 V and OUT+ = 1.1 V – 0.2 V = 0.9 V.

The VOD pin is functional only when the LMH32401 device is used with a PD that sinks the photocurrent. Set VOD = 0 V when the LMH32401 device is interfaced with a PD that sources the photocurrent. The VOD output offset feature is included in the LMH32401 device because the output current of a photodiode is unipolar. Depending on the reverse bias configuration, the photodiode can either sink or source current, but cannot do both at the same time. With the anode connected to a negative bias and the cathode connected to the TIA stage input, the photodiode can only sink current, which implies that the TIA stage output swings in a positive direction above its default input bias voltage (2.47 V). Subsequently, OUT– only swings below VOCM and OUT+ only swings above VOCM. 図 7-1 shows how the LMH32401 device only uses half of its output swing range (V_{OUT} = V_{OUT+} – $V_{OUT–}$) when VOD = 0 V, because one output never swings below VOCM and the other output never goes above VOCM. The signal dynamic range in this case is 0.4 V_{PP} – 0 V = 0.4 V_{PP}.

図 7-2 shows how the VOD pin voltage allows OUT– to be level-shifted above VOCM and OUT+ to be level-shifted below VOCM to maximize the output swing capabilities of the amplifier. The signal dynamic range in this case is 0.4 V_{PP} – (–0.4 V_{PP}) = 0.8 V_{PP}.

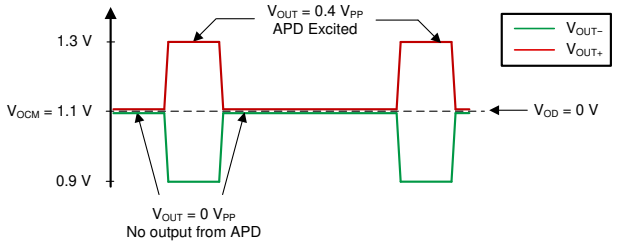


図 7-1. Individual Single-Ended Outputs With VOD = 0 V

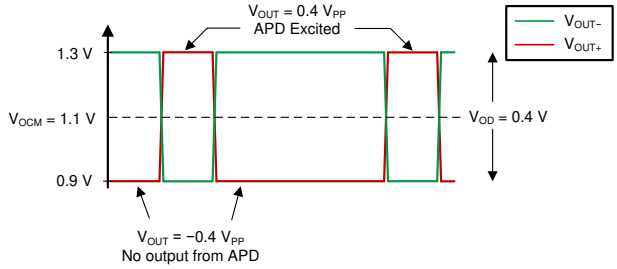


図 7-2. Individual Single-Ended Outputs With VOD = 0.4 V

When the LMH32401 device drives a 100-Ω load, the voltage set at the VOD pin is equal to the differential output offset (V_{OUT} = V_{OUT+} – $V_{OUT–}$) when the input signal current is zero. Use 式 1 to calculate the differential output offset under other load conditions.

$$V_{OD} = 1.2 \times VOD \times \frac{R_L}{\left(R_L \times 20\ \Omega\right)} \quad (1)$$

Where:

- VOD = Voltage applied at pin 9
- V_{OD} = ($V_{OUT–}$ – V_{OUT+})
- R_L = External load resistance

7.4 Device Functional Modes

7.4.1 Ambient Light Cancellation (ALC) Mode

The LMH32401 device has an integrated DC cancellation loop that cancels and voltage offsets from incidental ambient light. The ALC mode only works when the PD is sinking the photocurrent. The DC cancellation loop is enabled by setting $\overline{IDC\_EN}$ low. Incident ambient light on a photodiode produces a DC current resulting in an offset voltage at the output of the LMH32401's TIA stage. The *Functional Block Diagram* shows how the ALC loop senses the low-frequency DC offset at the output of the TIA stage and compares it against an internal reference voltage (V_{REF}). The ALC loop then outputs an opposing DC current (I_{DC}) to compensate for the differential offset voltage at its input. The loop has a high-pass cutoff frequency of 100 kHz. The ambient light cancellation loop is disabled when the amplifier is placed in power-down mode.

The shot noise current introduced by the DC cancellation loop increases the overall amplifier noise; so, if the ambient light level is negligible, then disable the loop to improve SNR. The cancellation loop helps save PCB space and system costs by eliminating the need for external AC coupling passive components. Additionally, the extra trace inductance and PCB capacitance introduced by using external AC coupling components degrades the LMH32401 device dynamic performance.

7.4.2 Power-Down Mode (Multiplexer Mode)

The LMH32401 device can be placed in low-power mode by setting $\overline{EN}$ high, which helps in saving system power. Enabling low-power mode puts the outputs of the internal amplifiers in the LMH32401 device, including the differential outputs, in a high-impedance state. 図 7-3 shows how this device feature can further save board space and cost by eliminating the need for a discrete high-speed multiplexer, if a system consists of several photodiode and amplifier channels multiplexed to a single ADC channel. The disabled channel outputs are not an ideal open circuit so as the number of multiplexed channels increases the disabled channels begin to load the enabled channel. Multiplexing more than four channels in parallel degrades the performance of the enabled channel. When the amplifier is in its low-power mode, the clamp circuitry is still active thereby protecting the TIA input. The ambient light cancellation loop is disabled when the amplifier is placed in power-down mode. When the LMH32401 device is brought out of power-down operation the ambient light cancellation loop requires several time constants to settle. 図 6-9 shows the low-frequency loop response which in turn determines the time constant needed for the loop to settle.

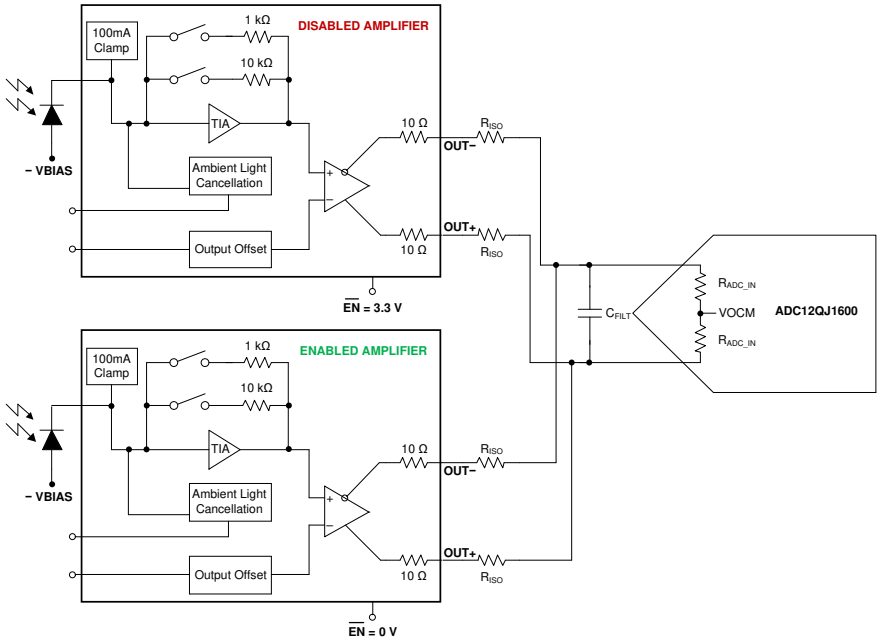


図 7-3. Configuring Two LMH32401 Devices in Multiplexer Mode to Drive a Single ADC

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The differential outputs of the LMH32401 device can directly drive a high-speed differential input ADC. 図 8-1 shows the LMH32401 differential outputs directly driving the ADC12QJ1600. The effective signal gain between the TIA input and the ADC input is 2 kΩ or 20 kΩ when driving an ADC with a 100-Ω differential input impedance (R_{ADC_IN} = 50 Ω). 式 2 gives the effective signal gain between the TIA input and the ADC input when driving an ADC with any other value of differential input impedance (R_{ADC_IN} ≠ 50 Ω).

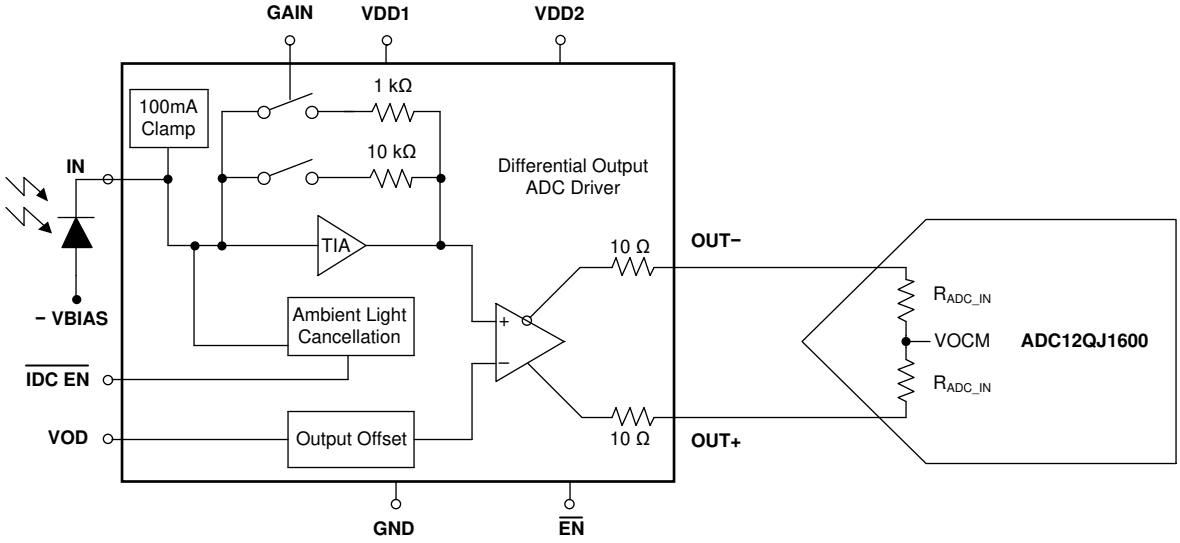


図 8-1. LMH32401 to ADC Interface

$$A_V = 2\ k\Omega\ (\text{or } 20\ k\Omega) \times 1.2 \times \frac{2 \times R_{ADC\_IN}}{(2 \times R_{ADC\_IN} + 20\ \Omega)} \quad (2)$$

Where:

- A_V = Differential gain from the TIA input to the ADC input
- R_{ADC_IN} = Input resistance of the ADC

図 8-2 shows a matching resistor network between the LMH32401 output and the ADC12QJ1600 input. The matching network is needed to prevent signal reflections when the signal path between the LMH32401 and ADC is very long. 式 3 gives the effective gain from the TIA input to the ADC input when using a matching resistor network.

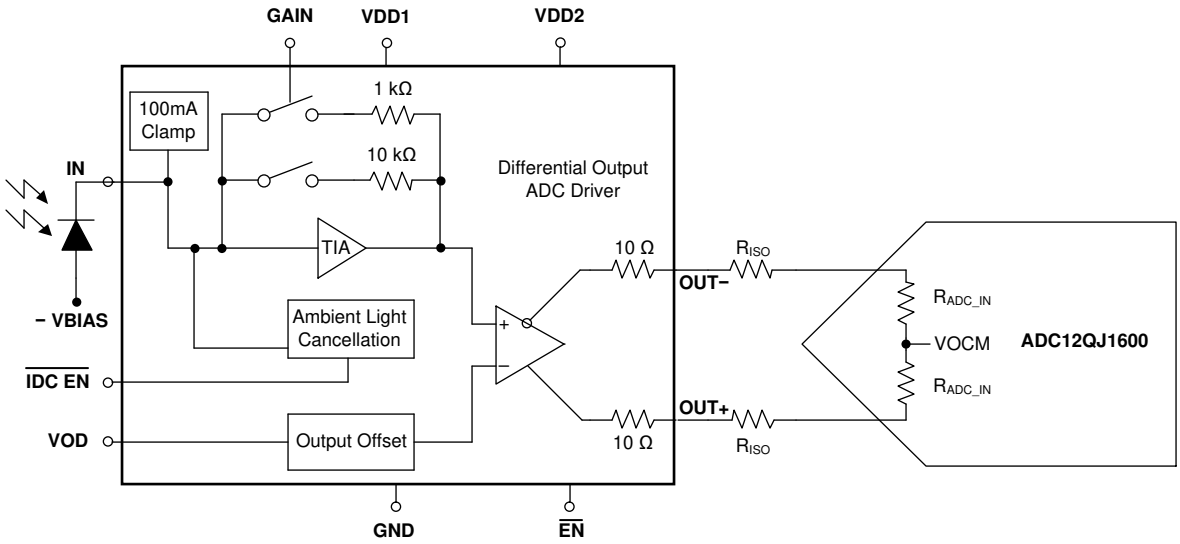


図 8-2. LMH32401 to ADC Interface with a Matching Resistor Network

$$A_V = 2\ k\Omega\ (\text{or } 20\ k\Omega) \times 1.2 \times \frac{2 \times R_{ADC\_IN}}{\left(2 \times R_{ADC\_IN} + 2 \times R_{ISO} + 20\ \Omega\right)} \quad (3)$$

Where:

- A_V = Gain from the TIA input to the ADC input
- R_{ADC_IN} = Differential input resistance of the ADC
- R_{ISO} = Series resistance between the TIA and ADC

式 4 gives the voltage to be applied at the VOD pin (pin 9) if a certain differential offset voltage (V_{OD}) is needed at the ADC input for the circuit in 図 8-2.

$$VOD = V_{OD} \times \left(\frac{1}{1.2}\right) \times \frac{\left(2 \times R_{ADC\_IN} + 2 \times RISO + 20\ \Omega\right)}{\left(2 \times R_{ADC\_IN}\right)} \quad (4)$$

Where:

- VOD = Voltage applied at pin 9
- V_{OD} = Desired differential offset voltage at the ADC input
- R_{ADC_IN} = Differential input resistance of the ADC
- R_{ISO} = Series resistance between the TIA and ADC

8.2 Typical Application

This section demonstrates the performance of the LMH32401 device when the input current flows into the IN pin. 図 8-3 shows the circuit used to test the LMH32401 device with a voltage source. This configuration demonstrates the use case when the photodiode's anode is tied to the amplifier input and its cathode is tied to a positive voltage greater than 2.47 V.

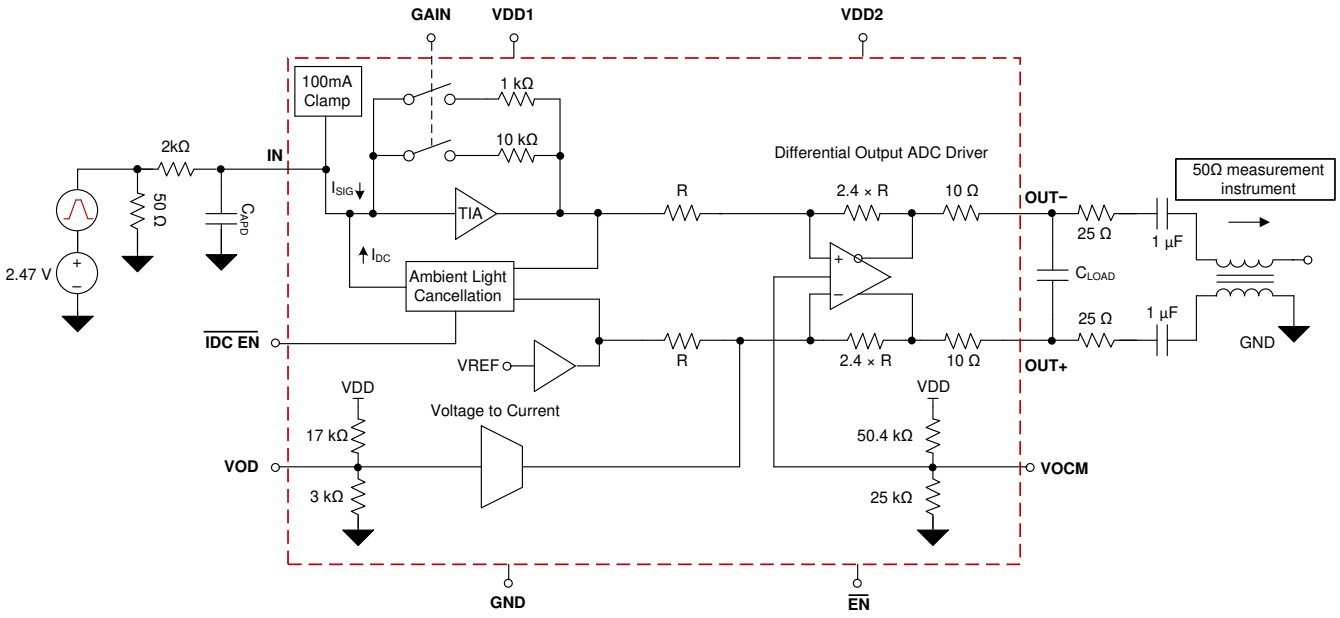


図 8-3. LMH32401 Test Circuit

8.2.1 Design Requirements

The objective is to design a low-noise, wideband differential output transimpedance amplifier. The design requirements are as follows:

- Amplifier supply voltage: 3.3 V
- Transimpedance gain: 2 kΩ and 20 kΩ
- Input capacitance: C_{PCB} ≅ 1 pF
- Target bandwidth: > 250 MHz
- Differential output offset (VOD): 0 V
- Ambient light cancellation ($\overline{IDC\_EN}$): 3.3 V (disabled)

8.2.2 Detailed Design Procedure

図 8-3 shows the LMH32401 device test circuit used to measure its bandwidth and transient pulse response. The voltage source is DC biased close to the input bias voltage of the LMH32401 device (approximately 2.47 V). The internal design of the LMH32401 device is optimized to only source current out of the input pin (pin 3), and all the data shown previously is with the current flowing out of the pin. When the voltage input from the source exceeds 2.47 V, the LMH32401 device input will sink the current. Set VOD = 0 V when the input has to sink the current from the photodiode, or in this case the voltage source. Set the DC bias so that sum of the input AC and DC component is always greater than the input voltage (2.47 V) when testing the LMH32401 device with a network analyzer or sinusoidal source.

図 8-4 and 図 8-5 shows the bandwidth of the LMH32401 device when its input is sinking the current. The input current range of the LMH32401 device is reduced when it is sinking the current. This effect is seen by the decrease in bandwidth as the output swing increases and is more pronounced in a gain configuration of 20 kΩ. Compare 図 8-4 with 図 6-1 and 図 6-3 to see the effect of current direction and input range in a 2 kΩ gain configuration. In a similar way, compare 図 8-5 with 図 6-2 and 図 6-4 to see the effect of current direction and input range in a gain of 20 kΩ.

図 8-6 and 図 8-7 show the pulsed output response of the LMH32401 device when the input current is increased past the amplifier linear input range. When the input is sinking current, a soft clamp will aid in fast recovery; however, the pulse will stretch slightly as the input current overrange increases. Compare 図 8-6 with 図 6-21 to see the pulse extension effect in a gain of 2 kΩ. Compare 図 8-7 with 図 6-22 to see the pulse extension effect in a gain of 20 kΩ. Knowledge of the pulse extension can be used to determine the approximate input current even under overrange situations that can occur due to the presence of retro-reflectors in the environment. As shown in 図 7-1, each half of the differential output pulse will only swing above or below the VOCM voltage and the resulting maximum differential output swing is 0.75 V_{PP} since VOD is set to 0 V. Consequently only half of the total ADC range is utilized in this photodiode configuration.

8.2.3 Application Curves

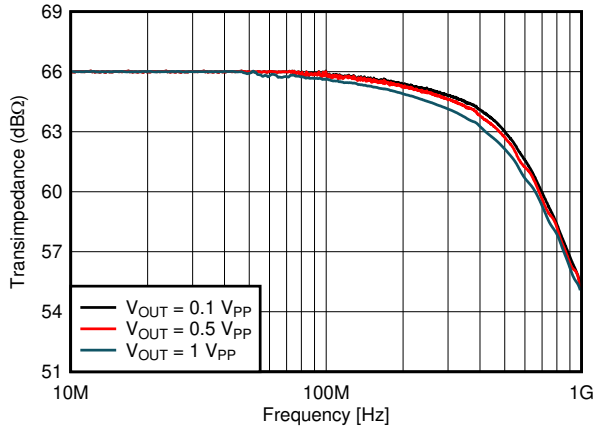


図 8-4. Bandwidth vs Output Swing (Gain = 2 kΩ)

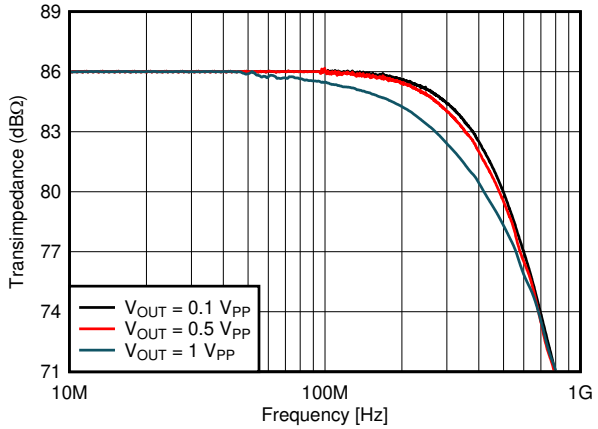


図 8-5. Bandwidth vs Output Swing (Gain = 20 kΩ)

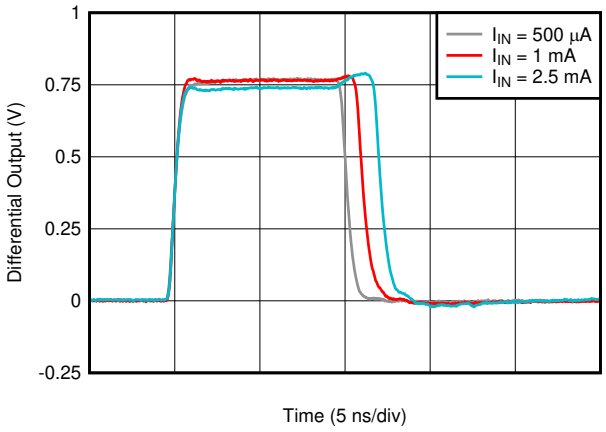


図 8-6. Pulse Response vs Input Current (Gain = 2 kΩ)

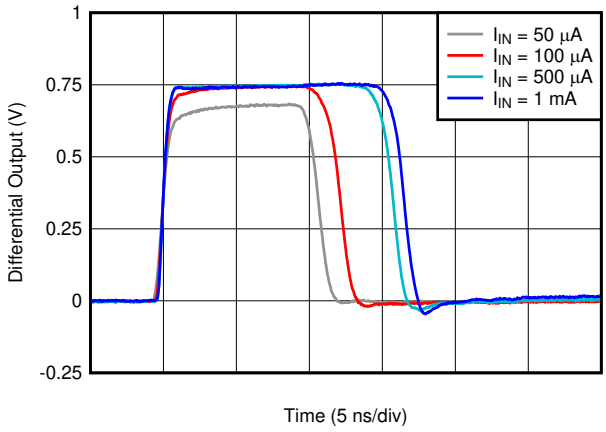


図 8-7. Pulse Response vs Input Current (Gain = 20 kΩ)

9 Power Supply Recommendations

The LMH32401 device operates on 3.3-V supplies. The VDD1 and VDD2 pins must always be driven from the same supply source and individually bypassed. A low power-supply source impedance must be maintained across frequency. So use multiple bypass capacitors in parallel. Place the bypass capacitors as close to the supply pins as possible. Place the smallest capacitor on the same side of the PCB as the LMH32401 device. Placing the larger valued bypass capacitors on the same side of the PCB is preferable as well. However, if there are space constraints, then the capacitors can be moved to the opposite side of the PCB using multiple vias to reduce the series inductance resulting from the vias. The LMH32401 device can operate on bipolar supplies by connecting pins 1 and 7 to the negative supply. The thermal pad must always be connected to the most negative supply. The digital pin threshold voltages must be appropriately level shifted as they are connected to voltages at pins 1 and 7.

10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the LMH32401 device requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include the following:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output pins can cause instability whereas parasitic capacitance on the input pin reduces the amplifier bandwidth. To reduce unwanted capacitance, cut out the power and ground traces under the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
- **Minimize the distance from the power-supply pins to high-frequency bypass capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. Place the smallest value capacitors on the same side as the DUT. If space constraints force the larger value bypass capacitors to be placed on the opposite side of the PCB, then use multiple vias on the supply and ground side of the capacitors. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).

10.2 Layout Example

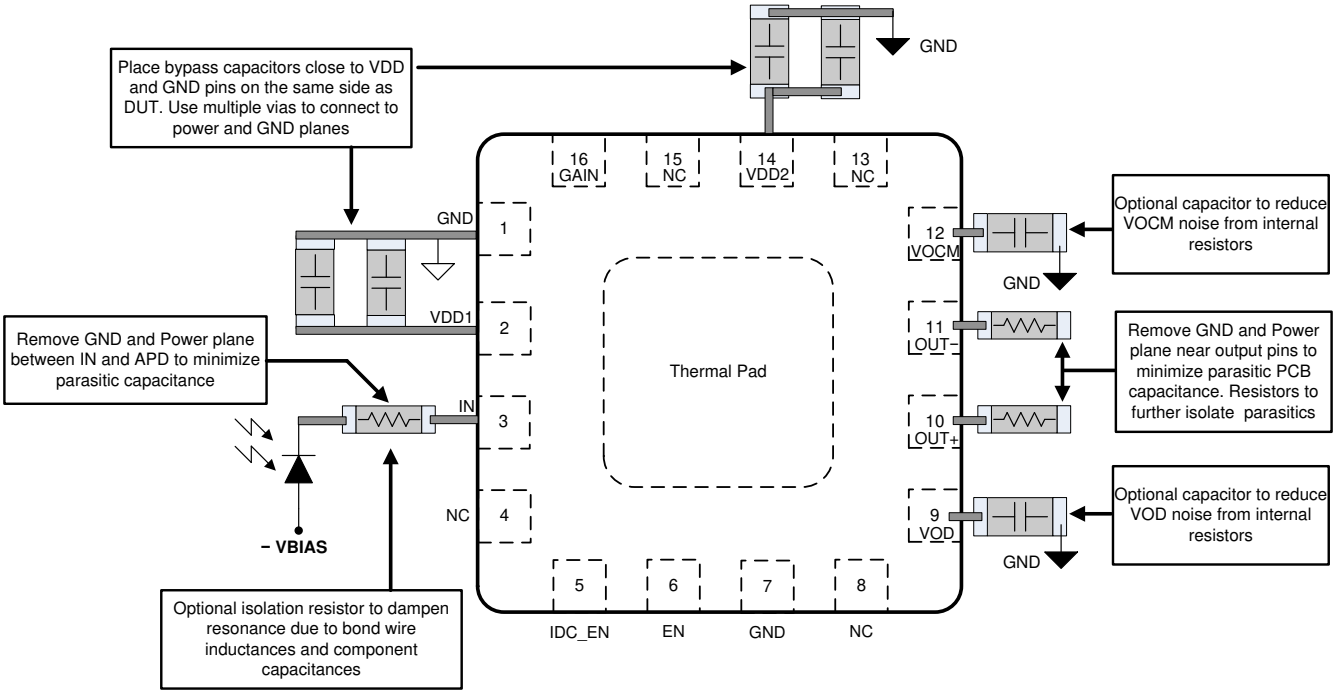


図 10-1. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

- Texas Instruments, *LMH32401 Transimpedance Amplifier Evaluation Module*.
- Texas Instruments, *Optical Front-End System Reference Design* design guide.
- Texas Instruments, *LIDAR-Pulsed Time-of-Flight Reference Design Using High-Speed Data Converters* design guide.
- Texas Instruments, *LIDAR Pulsed Time of Flight Reference Design* design guide.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *LMH32401IRGT Evaluation Module* user's guide.
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report.
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1* blog.
- Texas Instruments, *An Introduction to Automotive LIDAR*.
- Texas Instruments, *Maximizing the Dynamic Range of Analog Front Ends Having a Transimpedance Amplifier*.
- Texas Instruments, *Time of Flight and LIDAR – Optical Front End Design*.
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2* blog.
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*.
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*.
- Texas Instruments, *Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model*.

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

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11.5 Trademarks

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11.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH32401IRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L32401	Samples
LMH32401IRGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L32401	Samples
LMH32401YR	ACTIVE	DIESALE	Y	0	3000	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

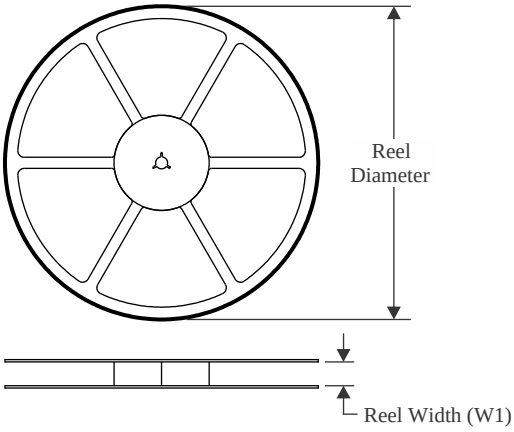
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

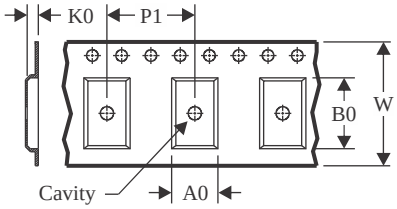
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

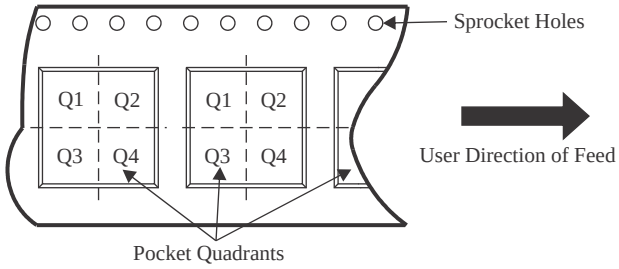


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

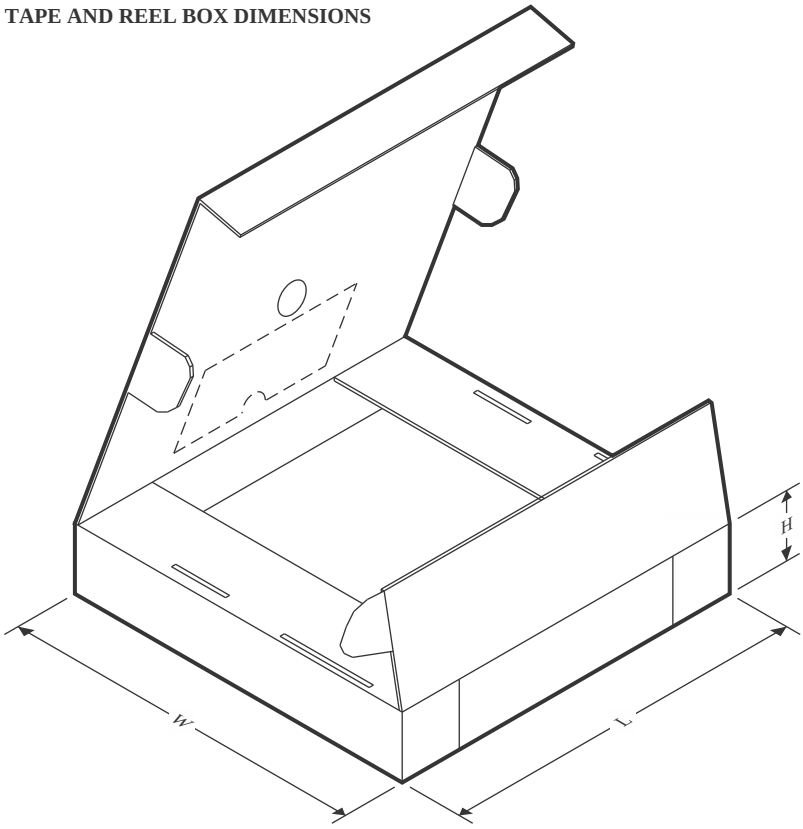
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH32401IRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMH32401IRGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMH32401YR	DIESALE	Y	0	3000	180.0	8.4	1.1	1.1	0.4	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

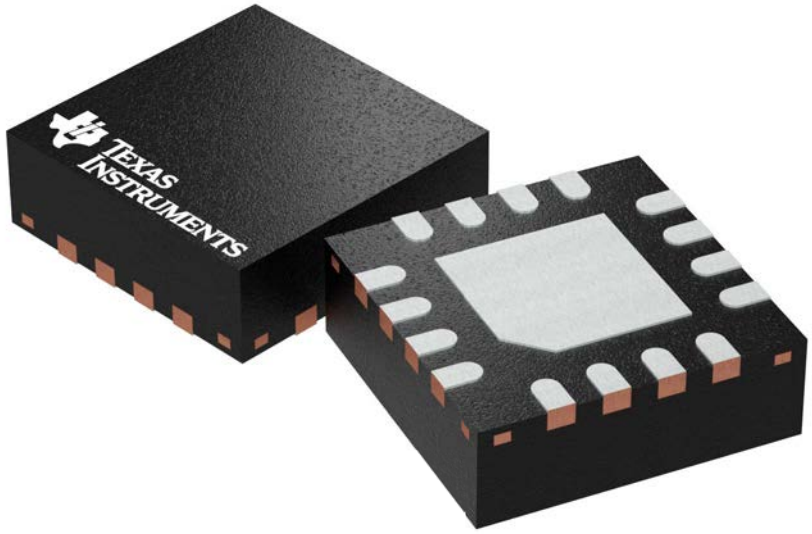


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH32401IRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
LMH32401IRGTT	VQFN	RGT	16	250	210.0	185.0	35.0
LMH32401YR	DIESALE	Y	0	3000	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



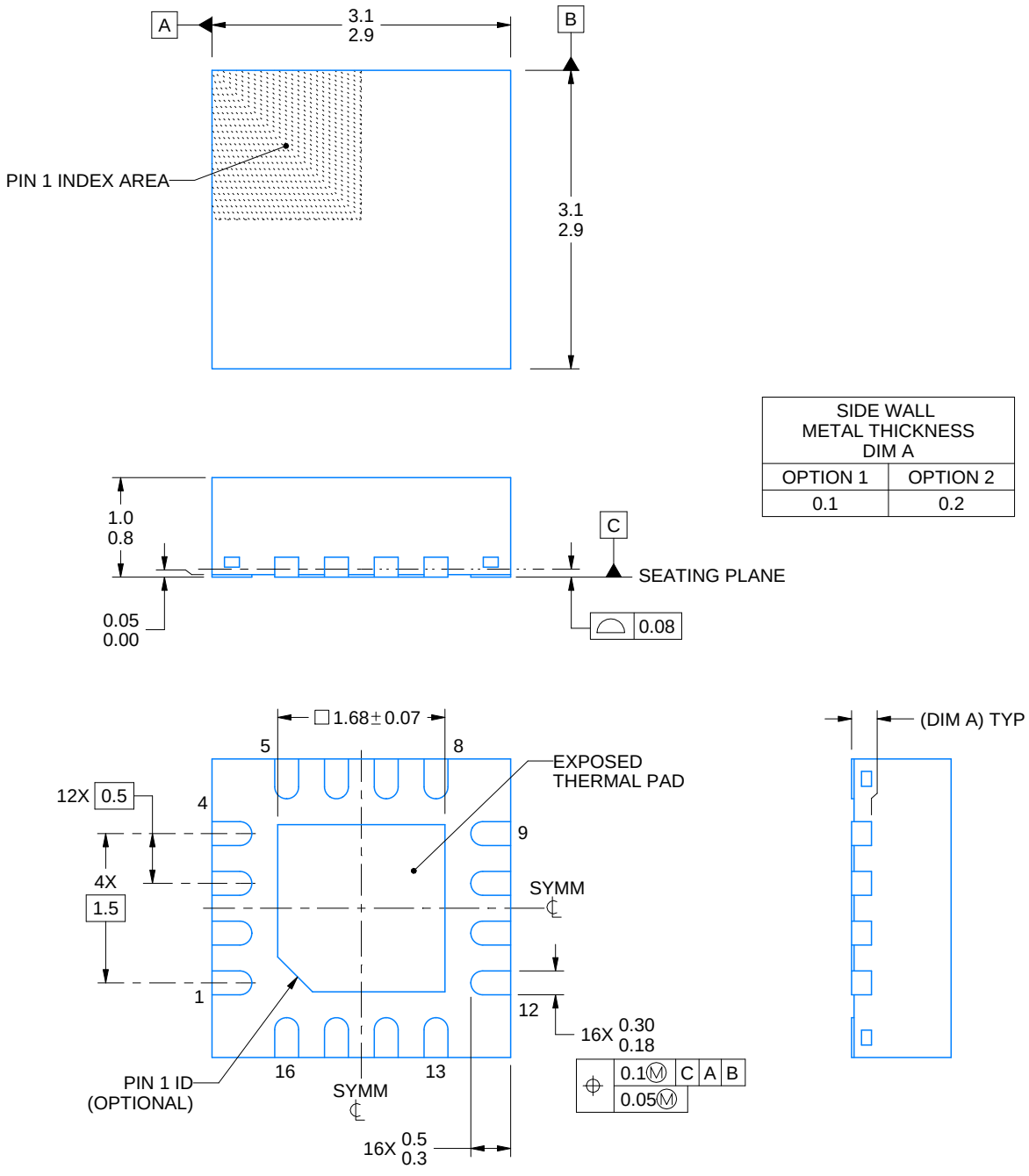
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

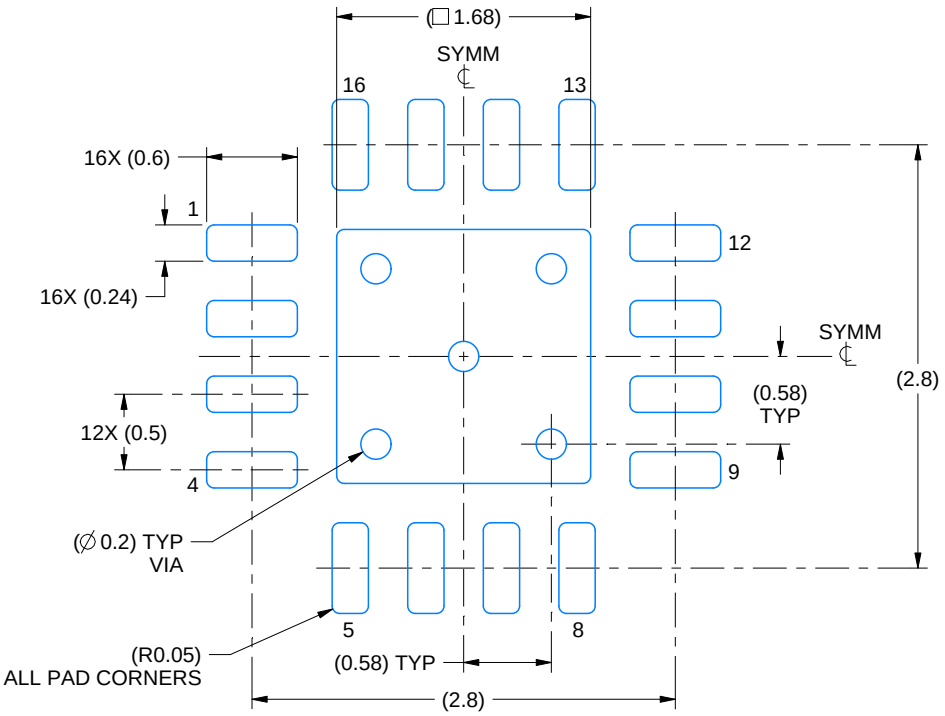
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

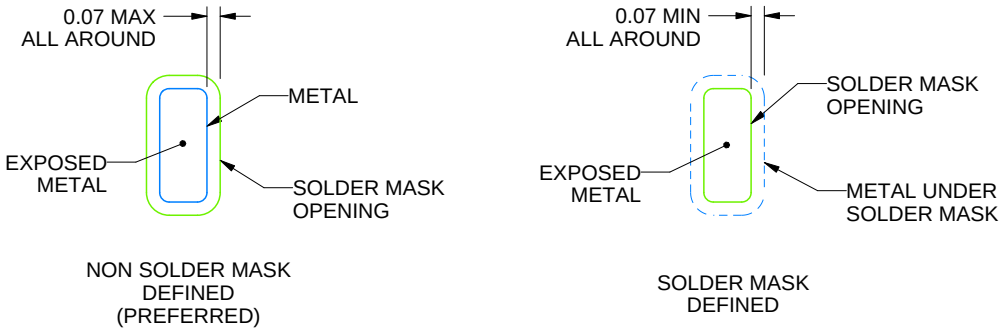


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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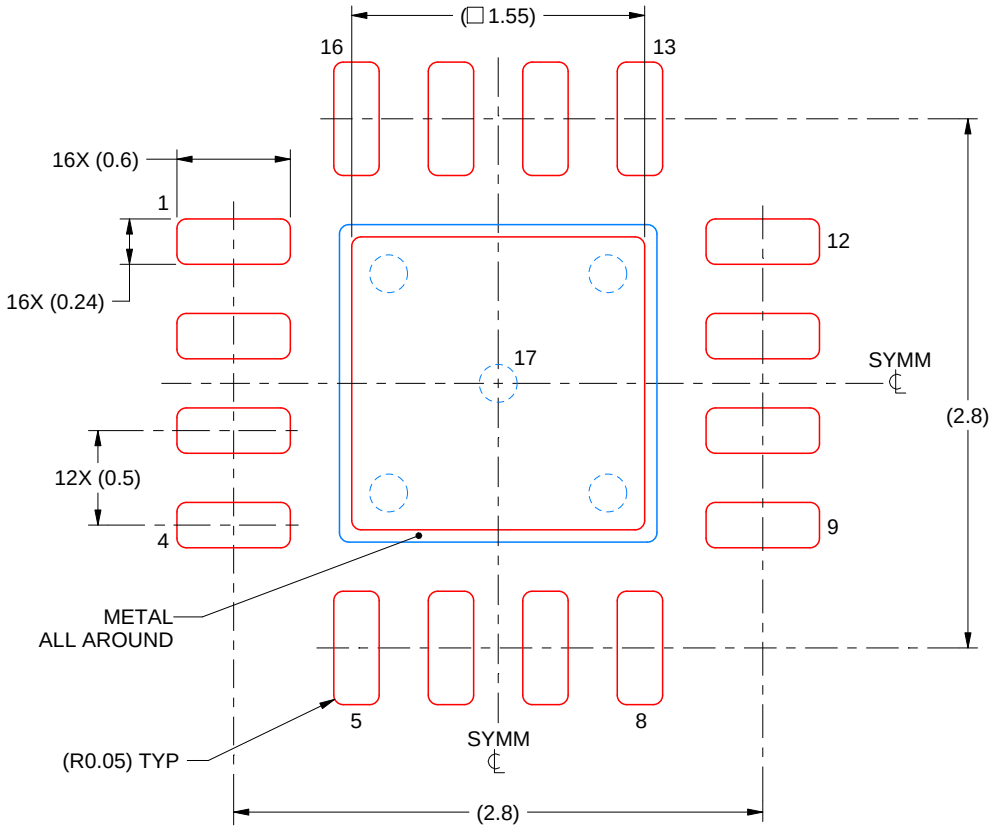
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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