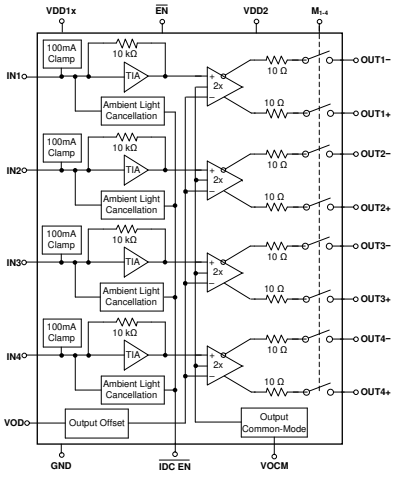
LMH32404 クランプ機能および環境光キャンセル機能内蔵、4 チャネル、差動出力、マルチプレクシング・トランスインピーダンス・アンプ

1 特長

- ゲイン:20kΩ
- 性能、C_{PD} = 1pF:
  - 帯域幅:350MHz
  - 入力換算ノイズ:56nA$_{RMS}$
  - 立ち上がり / 立ち下がり時間:1.25ns
- 静止電流:28mA/チャネル
- スタンバイ・モード:10mA/チャネル
- 低消費電力モード:2.5mA (4 チャネル)
- チャネル・スイッチング時間:10ns
- 環境光キャンセル機能内蔵
- 100mA 保護クランプ内蔵
- 4 個の入力チャネルと 4 個の差動出力チャネル
- 内蔵マルチプレクサにより、光センサと ADC/TDC の間でフレキシブルな構成が可能
- 複数の LMH32404 を並列に組み合わせて、より広い視野角 (FOV) を実現可能
- パッケージ:28 ピン VQFN
  - ベア・ダイ
- 温度範囲:-40℃～+125℃

2 アプリケーション

- 機械式スキャン LIDAR
- ソリッド・ステート・スキャン LIDAR
- レーザー距離計
- 安全エリア・スキャナ



ブロック概略図

3 概要

LMH32404 は、LIDAR (光検出と測距) アプリケーションとレーザー距離測定システムのための、クワッド・チャネル、シングルエンド入力、差動出力のトランスインピーダンス・アンプ (TIA) です。

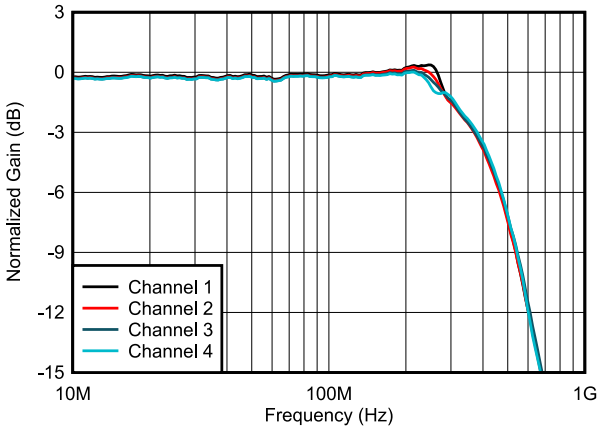
LMH32404 は、過負荷入力状態からアンプを保護し、迅速にデバイスを回復させることができる 100mA のクランプを各チャネルに内蔵しています。LMH32404 は、フォトダイオードとアンプの間の AC 結合の代わりに使用できる環境光キャンセル (ALC) 回路も各チャネルに内蔵しているため、基板面積とシステム・コストを削減できます。DC および低周波数成分を測定するときは、ALC ループを無効にしてください。

各 LMH32404 チャネルの出力にはスイッチが内蔵されており、このスイッチにより、差動出力アンプは出力ピンから切断され、チャネルはスタンバイ・モードに移行します。異なるチャネル間で切り替える場合の遷移時間はわずか 10ns です。LMH32404 は $\overline{EN}$ ピンを使って低消費電力モードに移行させることができ、アンプを使用していないときに電力を節約できます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
LMH32404	VQFN (28)	5.00mm × 4.00mm
	ベア・ダイ	1.346mm × 2.455mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (February 2022) to Revision C (November 2022) — **Page**

- ベア・ダイ・パッケージのステータスをプレビューからアクティブに変更 ... 1

Changes from Revision A (November 2021) to Revision B (February 2022) — **Page**

- 「特長」セクションと「製品情報」表にベア・ダイ・プレビュー・パッケージを追加 ... 1
- Added the *bare die preview package* to the *Pin Configuration and Functions* section ... 3

Changes from Revision * (August 2021) to Revision A (November 2021) — **Page**

- Updated the JEDEC reference in the *ESD Ratings* table from *JESD22-C101* to *JEDEC JS-002* ... 7
- Updated the *Overview* section ... 18
- Updated the *Clamping and Input Protection* section ... 20
- Updated the *Differential Output Stage* section ... 20
- Updated the *Ambient Light Cancellation (ALC) Mode* section ... 22

5 Pin Configuration and Functions

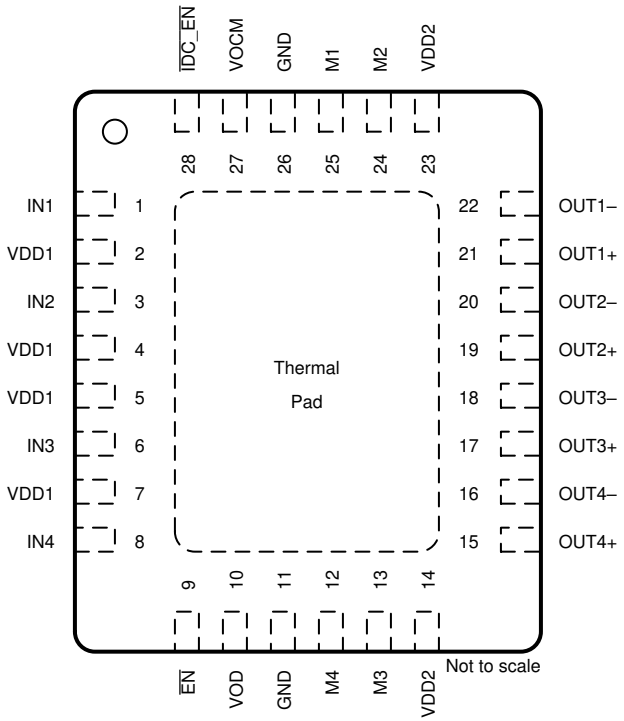


図 5-1. RHF Package, 28-Pin VQFN, (Top View)

表 5-1. Pin Functions

PIN		TYPE[2]	DESCRIPTION
NAME	NO.		
$\overline{EN}$	9	I	Device enable pin. $\overline{EN}$ = logic low = normal operation (default); $\overline{EN}$ = logic high = low power mode.[1]
GND	11, 26	I	Amplifier ground.
$\overline{IDC\_EN}$	28	I	Ambient light cancellation loop enable. $\overline{IDC\_EN}$ = logic low = enable DC cancellation (default); $\overline{IDC\_EN}$ = logic high = disable DC cancellation.[1]
IN1	1	I	Transimpedance amplifier input – Channel 1.
IN2	3	I	Transimpedance amplifier input – Channel 2.
IN3	6	I	Transimpedance amplifier input – Channel 3.
IN4	8	I	Transimpedance amplifier input – Channel 4.
M1	25	I	Select Channel 1. M1 = logic high = Channel 1 operational and output switches closed. M1 = logic low (default) = Channel 1 in standby power mode and output switches open. [1]
M2	24	I	Select Channel 2. M2 = logic high = Channel 2 operational and output switches closed. M2 = logic low (default) = Channel 2 in standby power mode and output switches open. [1]
M3	13	I	Select Channel 3. M3 = logic high = Channel 3 operational and output switches closed. M3 = logic low (default) = Channel 3 in standby power mode and output switches open. [1]
M4	12	I	Select Channel 4. M4 = logic high = Channel 4 operational and output switches closed. M4 = logic low (default) = Channel 4 in standby power mode and output switches open. [1]
OUT1–	22	O	Channel 1 inverting amplifier output. When light is incident on the photodiode the output pin transitions in a negative direction from the no light condition.
OUT1+	21	O	Channel 1 noninverting amplifier output. When light is incident on the photodiode the output pin transitions in a positive direction from the no light condition.
OUT2–	20	O	Channel 2 inverting amplifier output. When light is incident on the photodiode the output pin transitions in a negative direction from the no light condition.
OUT2+	19	O	Channel 2 noninverting amplifier output. When light is incident on the photodiode the output pin transitions in a positive direction from the no light condition.

表 5-1. Pin Functions (continued)

PIN		TYPE[2]	DESCRIPTION
NAME	NO.		
OUT3–	18	O	Channel 3 inverting amplifier output. When light is incident on the photodiode the output pin transitions in a negative direction from the no light condition.
OUT3+	17	O	Channel 3 noninverting amplifier output. When light is incident on the photodiode the output pin transitions in a positive direction from the no light condition.
OUT4–	16	O	Channel 4 inverting amplifier output. When light is incident on the photodiode the output pin transitions in a negative direction from the no light condition.
OUT4+	15	O	Channel 4 noninverting amplifier output. When light is incident on the photodiode the output pin transitions in a positive direction from the no light condition.
VDD1	2, 4, 5, 7	I	Positive power supply for the transimpedance amplifier stage. Each pin should be tied to the same power supply with independent power-supply bypassing.
VDD2	14, 23	I	Positive power supply for the differential amplifier stage. Tie VDD1 and VDD2 to the same power supply with independent power-supply bypassing.
VOCM	27	I	Differential amplifier common-mode output control.
VOD	10	I	Differential amplifier differential output offset control.
Thermal pad		—	Connect the thermal pad to the same potential as pin 11 and 26 (GND).

(1) TI recommends driving a digital pin with a low-impedance source rather than leaving the pin floating because fast-moving transients can couple into the pin and inadvertently change the logic level.
(2) I = input, O = output

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION
381 µm	Silicon with backgrind	Wafer backside is not electrically isolated and should be held at the same potential as the most negative power supply connected to the die (GND)	AlCu

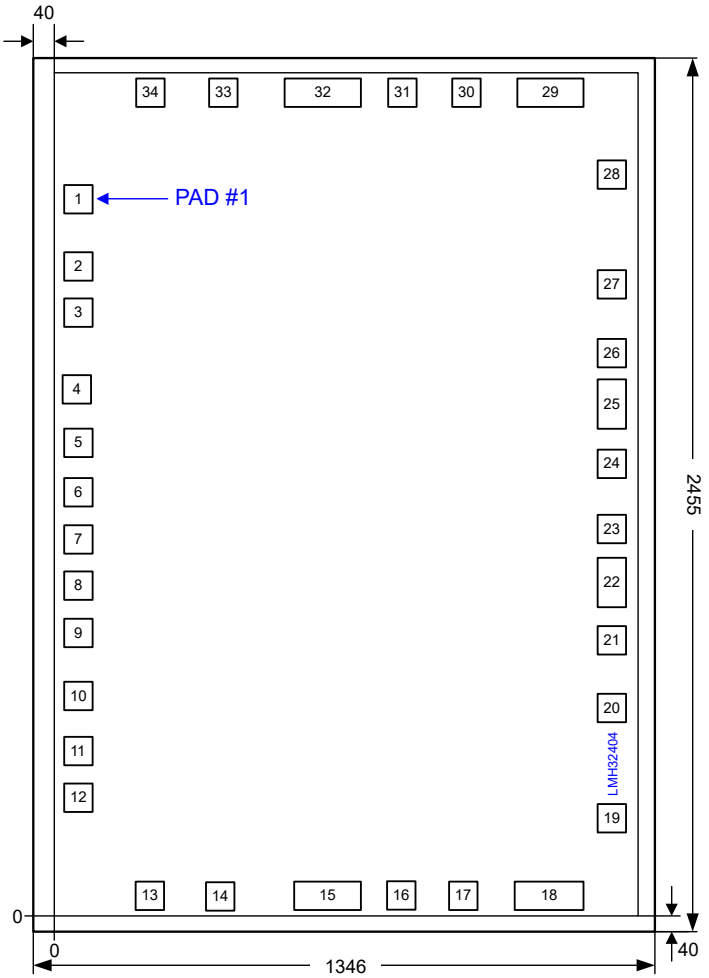


図 5-2. Bare Die Package

表 5-2. Bond Pad Coordinates of Bare Die Version in Microns

PAD NUMBER	PAD NAME	X-MIN	Y-MIN	X-MAX	Y-MAX
1	IN1	15	1981.075	90	2056.075
2	VDD1	15	1795.225	90	1870.225
3	GND	15	1663.3	90	1738.3
4	IN2	15	1450.675	90	1525.675
5	VDD1	15	1295.225	90	1370.225
6	GND	15	1163.3	90	1238.3
7	VDD1	15	1026.65	90	1101.65
8	IN3	15	898.55	90	973.55
9	GND	15	766.475	90	841.475
10	GND	15	590.775	90	665.775
11	VDD1	15	435.325	90	510.325
12	IN4	15	301.75	90	376.75

表 5-2. Bond Pad Coordinates of Bare Die Version in Microns (continued)

PAD NUMBER	PAD NAME	X-MIN	Y-MIN	X-MAX	Y-MAX
13	$\overline{EN}$	172.675	15	247.675	90
14	VOD	329.35	15	404.35	90
15	GND	522.85	15	672.85	90
16	M4	718.525	15	793.525	90
17	M3	857.95	15	932.95	90
18	VDD2	1001.725	15	1151.725	90
19	OUT4+	1176	244.2	1251	319.2
20	OUT4–	1176	552.2	1251	627.2
21	OUT3+	1176	744.2	1251	819.2
22	GND	1176	864.45	1251	1014.45
23	OUT3–	1176	1052.2	1251	1127.2
24	OUT2+	1176	1244.2	1251	1319.2
25	GND	1176	1364.45	1251	1514.45
26	OUT2–	1176	1552.2	1251	1627.2
27	OUT1+	1176	1744.2	1251	1819.2
28	OUT1–	1176	2052.2	1251	2127.2
29	VDD2	1001.725	2285	1151.725	2360
30	M2	857.95	2285	932.95	2360
31	M1	718.525	2285	793.525	2360
32	GND	497.85	2285	672.85	2360
33	VOCM	329.35	2285	404.35	2360
34	$\overline{IDC\_EN}$	172.675	2285	247.675	2360

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD1}, V_{DD2}	Total supply voltage, (V_{DD})(2)		3.65	V
	Voltage at Output pins	0	V_{DD}	V
	Voltage at Logic pins	–0.2	V_{DD}	V
I_{IN}	Continuous current into IN		25	mA
I_{OUT}	Continuous output current		35	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VDD1 and VDD2 should always be tied to the same supply and have separate power-supply bypass capacitors.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Total supply voltage	3	3.3	3.45	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH32404 RHF (VQFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

V_{DD} = 3.3 V, V_{OCM} = Open, V_{OD} = 0 V, C_{PD} [1] = 1 pF, $\overline{EN}$ = 0 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω (differential load between OUT+ and OUT-), and T_A = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		350		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		300		MHz
t_R, t_F	Rise and fall time	V_{OUT} = 100 mV_{PP}, Pulse width = 10 ns		1.25		ns
	Slew Rate[4]	V_{OUT} = 1 V_{PP}, Pulse width = 10 ns		750		V/µs
	Overload recovery time (1% settling)	I_{IN} = 100 mA, Pulse width = 10 ns		12		ns
	Overload pulse width extension[5]	I_{IN} = 100 mA, Pulse width = 10 ns		5		ns
i_N	Integrated input current noise	f = 250 MHz		56		nA_{RMS}
	Adjacent channel crosstalk	f = 100 MHz		-49		dBc
	Non adjacent channel crosstalk	f = 100 MHz		-58		dBc
	All hostile channels crosstalk	f = 100 MHz		-39		dBc
DC PERFORMANCE						
Z_{21}	Small-signal transimpedance gain[6]		17	20	23	kΩ
V_{OD}	Differential output offset voltage ($V_{OUT-} - V_{OUT+}$)		–20	±5	20	mV
	Differential output offset voltage drift, $\Delta V_{OD}/\Delta T_A$			±20		µV/°C
INPUT PERFORMANCE						
V_{IN}	Default input bias voltage[8]	Input pin floating	2.42	2.47	2.52	V
	Default input bias voltage drift, $\Delta V_{IN}/\Delta T_A$	Input pin floating		1.1		mV/°C
I_{IN}	DC Input current range	Z_{21} < 3-dB degradation from I_{IN} = 5 µA	60	72		µA
OUTPUT PERFORMANCE						
V_{OH}	Single-sided output voltage swing(high)[2] [8]		2.85	2.9		V
V_{OL}	Single-sided output voltage swing (low)[2] [8]			0.36	0.39	V
I_{OUT}	Linear output drive (sink and source)	T_A = 25°C, I_{IN} = 50 µA , R_L = 25 Ω	24	26.6	32	mA
		T_A = –40°C, I_{IN} = 50 µA , R_L = 25 Ω		27.1		
		T_A = 125°C, I_{IN} = 50 µA , R_L = 25 Ω		25.1		
I_{SC}	Output short-circuit current (differential) [3]			70		mA
Z_{OUT}	DC differential output impedance[8]	M_X = high	18	21	24	Ω
		M_X = low		1		MΩ
OUTPUT COMMON-MODE CONTROL (V_{OCM}) PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OCM} = 100 mV_{PP} at VOCM pin		375		MHz
LSBW	Large-signal bandwidth	V_{OCM} = 1 V_{PP} at VOCM pin		120		MHz
e_N	Output common-mode noise	f = 10 MHz, 1 nF capacitor to GND on VOCM pin		15		nV/√Hz
A_V	Gain, ($\Delta V_{OCM}/\Delta$VOCM)	IN floating, VOCM = 1.1 V (driven)		1		V/V
	Gain Error[8]	T_A = 25°C, VOCM = 0.7 V to 2.3 V	–2%	0.5%	2%	
		T_A = –40°C to 125°C, VOCM = 0.7 V to 2.3 V		±1%		
	Input impedance			17		kΩ
VOCM	VOCM pin default offset from 1.1 V	VOCM floating, (VOCM - 1.1 V)	–25	8	45	mV
	V_{OCM} error vs Input current, $\Delta V_{OCM}/\Delta I_{IN}$	VOCM driven to 1.1 V		10		V/A
V_{OCM}	Output common-mode voltage, (V_{OUT+} + V_{OUT-})/2	T_A = 25°C, VOCM floating	1	1.1	1.2	V

6.5 Electrical Characteristics (continued)

V_{DD} = 3.3 V, V_{OCM} = Open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω (differential load between OUT+ and OUT-), and T_A = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output common-mode voltage drift, ($\Delta V_{OCM}/\Delta T_A$)	T_A = –40°C to 125°C, VOCM floating		300		µV/°C
V_{OCM}	Output common-mode voltage, (V_{OUT+} + V_{OUT-})/2	T_A = 25°C, VOCM driven to 1.1V	1.05	1.1	1.15	V
	Output common-mode voltage drift, ($\Delta V_{OCM}/\Delta T_A$)	T_A = –40°C to 125°C, VOCM driven to 1.1V		–10		µV/°C
	VOCM headroom to positive supply voltage	T_A = 25°C, V_{OCM} offset shift from VOCM = 1.1 V (driven) < 10-mV		1.2	1.3	V
		T_A = –40°C to 125°C, V_{OCM} offset shift from VOCM = 1.1 V (driven) < 10-mV		1		V
	VOCM headroom to negative supply voltage	T_A = 25°C, V_{OCM} offset shift from VOCM = 1.1 V (driven) < 10-mV		0.2	0.65	V
		T_A = –40°C to 125°C, V_{OCM} offset shift from VOCM = 1.1 V (driven) < 10-mV		0.25		V
OUTPUT DIFFERENTIAL OFFSET (V_{OD}) PERFORMANCE						
SSBW	Small-signal bandwidth	VOD = 100 mV_{PP}		45		MHz
LSBW	Large-signal bandwidth	VOD = 1 V_{PP}		17		MHz
V_{OD}	Default VOD pin voltage			0.5		V
V_{OS_D}	Differential output offset,(8) V_{OUT} = (V_{OUT-} –V_{OUT+})	IN floating, VOD = 0.5 V	470	500	530	mV
	Differential output offset drift, $\Delta V_{OS\_D}/\Delta T_A$	IN floating, VOD = 0.5 V		0.03		mV/°C
V_{OS_D}	Differential output offset,(8) V_{OUT} = (V_{OUT-} –V_{OUT+})	IN floating, VOD floating	470	500	530	mV
	Differential output offset drift, $\Delta V_{OS\_D}/\Delta T_A$	IN floating, VOD floating		0.05		mV/°C
A_V	Gain, ($\Delta V_{OUT}/\Delta VOD$), where V_{OUT} = (V_{OUT-} –V_{OUT+})	IN floating, VOCM = 1.1 V (driven)		-1.01		V/V
	Gain Error	T_A = 25°C, VOD = 0.3 V to 1.2 V	–5%	±0.8%	5%	
		T_A = –40°C to 125°C, VOD = 0.3 V to 1.2 V		±1.5%		
	Input impedance			2.5		kΩ
AMBIENT LIGHT CANCELLATION PERFORMANCE ($\overline{IDC\_EN}$ = 0 V) (7)						
	Settling time, 1% (2 mV) of settled V_{OS}	I_{IN} = 0 µA → 10 µA		20		µs
		I_{IN} = 10 µA → 0 µA		60		
	Ambient light current cancellation range	Differential output offset (V_{OUT-} – V_{OUT+}) shift from I_{DC} = 10 µA < 10 mV	1.8	2.5		mA
POWER SUPPLY						
I_Q	Quiescent current, per channel, (VDD1 + VDD2)	M_X = 3.3 V, T_A = 25°C	22.8	27.7	32.5	mA
		M_X = 0 V, T_A = 25°C	8.5	10.4	13.4	
PSRR+	Positive power-supply rejection ratio	VDD1 = VDD2	54	74		dB
SHUTDOWN						
I_Q	Total disabled quiescent current ($\overline{EN}$ = V_{DD})	T_A = 25°C		2.35	3	mA
		T_A = –40°C		2.25		
		T_A = 125°C		2.55		

(1) Input capacitance of photodiode.
(2) Output slammed to the rail and V_{OCM} adjusted to achieve output swing.
(3) Device cannot withstand continuous short-circuit between the differential outputs.
(4) Average of rising and falling slew rate.
(5) Pulse width extension measured at 50% of pulse height of a square wave.
(6) Gain measured at the amplifier output pins when driving a 100-Ω resistive load. At higher resistor loads the gain will increase.

(7) Enabling the ambient light cancellation loop will add noise to the system.
(8) Min and Max limits apply to VQFN package only.

6.6 Electrical Characteristics: Logic Threshold and Switching Characteristics

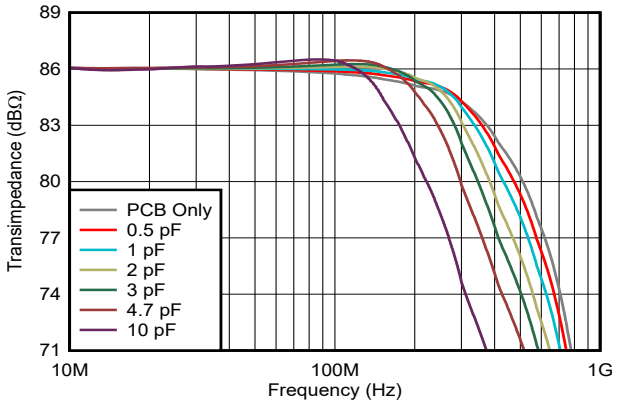
V_{DD} = 3.3 V, V_{OCM} = Open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, $\overline{IDC\_EN}$ = 3.3 V, R_L = 100 Ω (differential load between OUT+ and OUT-), and T_A = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD PERFORMANCE						
	Logic pin bias current			75	120	µA
	$\overline{EN}$, $\overline{IDC\_EN}$, disable threshold voltage	Disabled above this voltage		1.5	2	V
	$\overline{EN}$, $\overline{IDC\_EN}$, enable threshold voltage	Enabled below this voltage	0.8	1		V
	M_X control, enable threshold voltage	Switch closed above this voltage		1.5	2	V
	M_X control, disable threshold voltage	Switch open below this voltage	0.8	1.0		V
$\overline{EN}$ CONTROL TRANSIENT PERFORMANCE						
	Enable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA		250		ns
	Disable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA		8		ns
	Enable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA		4		µs
	Disable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA		3		ns
MULTIPLEXER CONTROL TRANSIENT PERFORMANCE						
	Channel to Channel transition-time (1% settling)	Ambient loop disabled, 0 → 0.5V transition at V_{OUT}.		10		ns
	Disable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA		8		ns

(1) Input capacitance of photodiode.

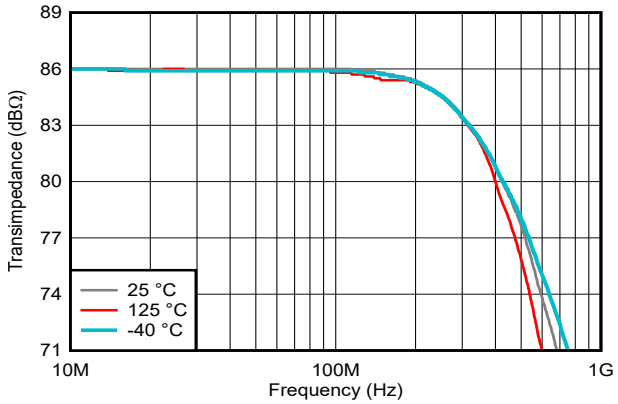
6.7 Typical Characteristics

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted)



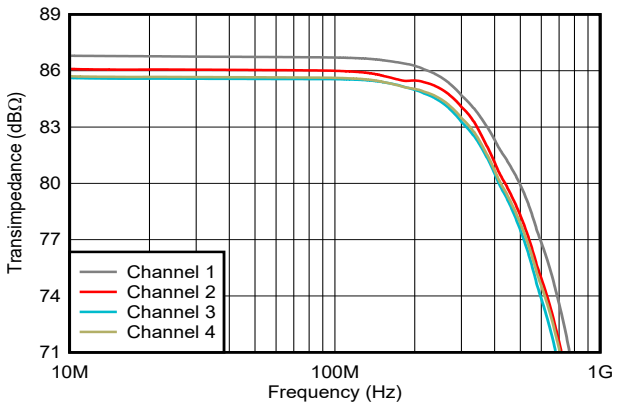
V_{OUT} = 100 mV_{PP}

図 6-1. Small Signal Response vs Input Capacitance



V_{OUT} = 100 mV_{PP}

図 6-2. Small Signal Response vs Ambient Temperature



V_{OUT} = 100 mV_{PP}

図 6-3. Small Signal Response vs Channels

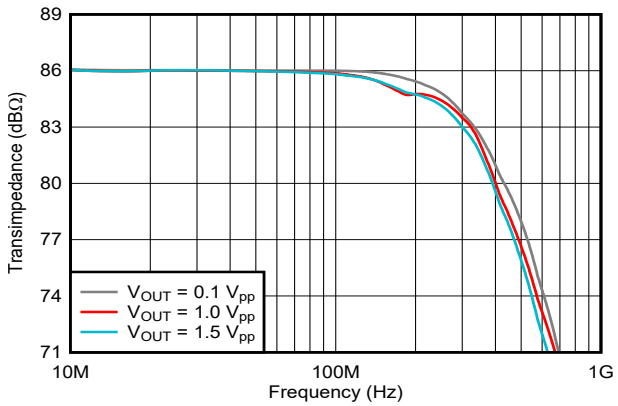
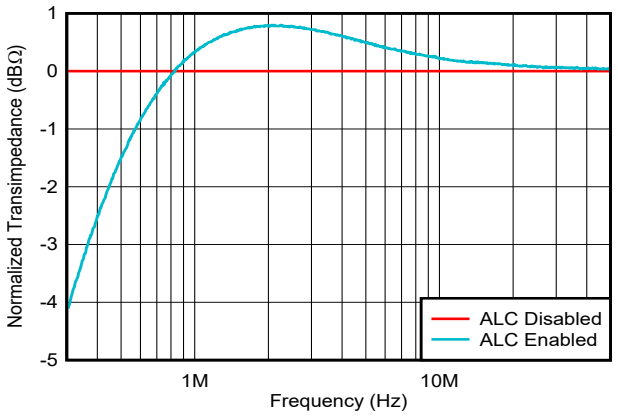
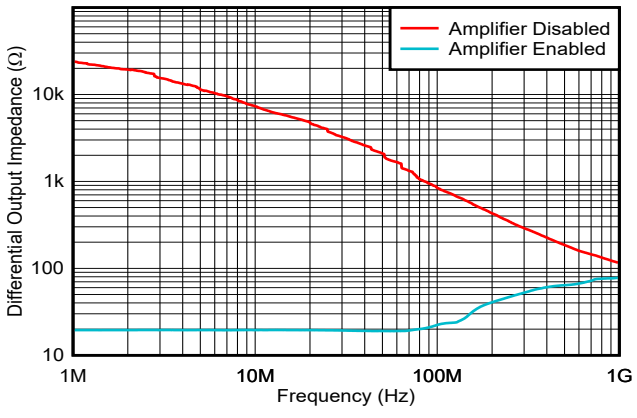


図 6-4. Frequency Response vs Output Swing



I_{DC_IN} = 100 µA

図 6-5. Low-Side Frequency Response vs Ambient Light Cancellation



I_{DC_IN} = 100 µA

図 6-6. Closed-Loop Output Impedance vs Frequency

6.7 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted)

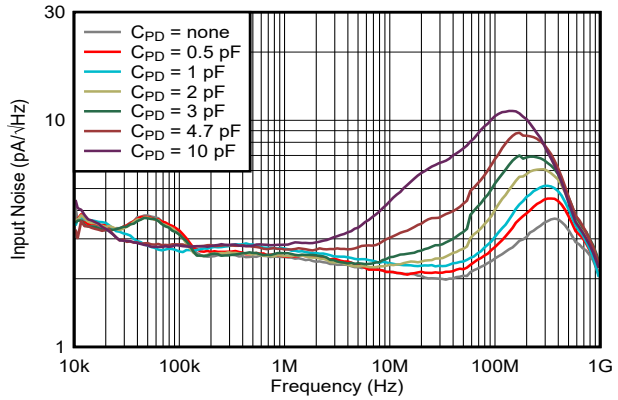


図 6-7. Input Noise Density vs Input Capacitance

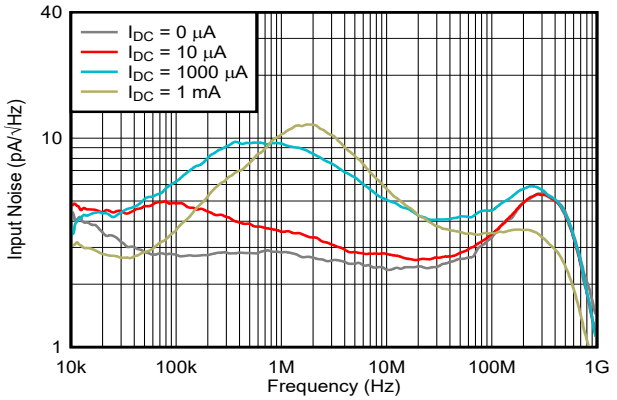


図 6-8. Input Noise Density vs Ambient Light DC Current

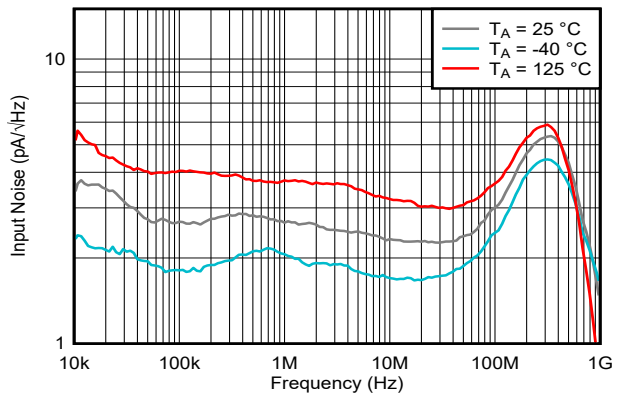


図 6-9. Input Noise Density vs Ambient Temperature

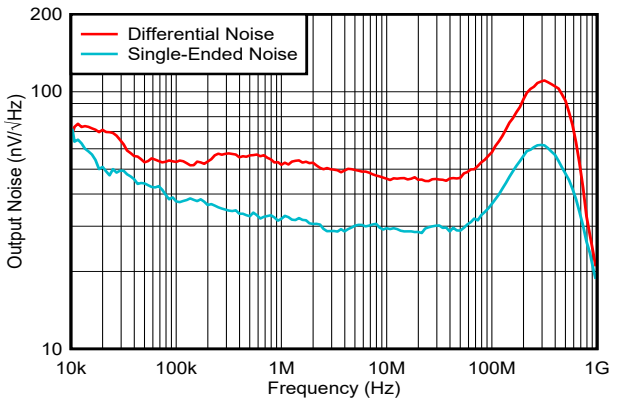


図 6-10. Output Noise Density vs Output Configuration

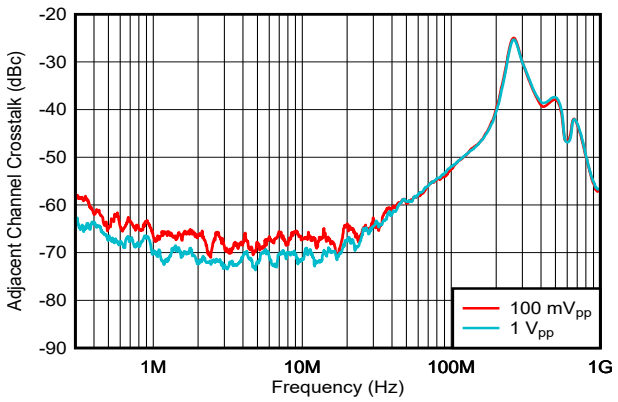


図 6-11. Adjacent Channel Crosstalk

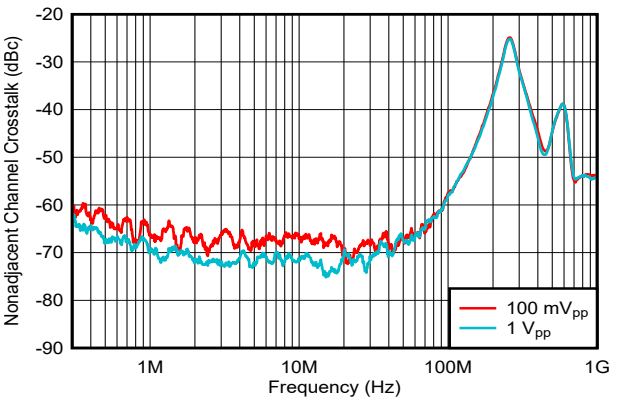


図 6-12. Non-Adjacent Channel Crosstalk

6.7 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted)

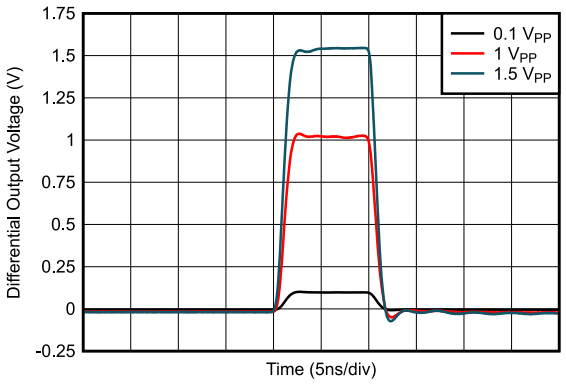


図 6-13. Pulse Response vs Output Swing

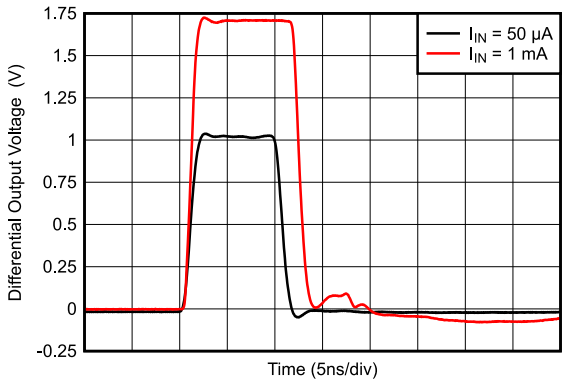


図 6-14. Overloaded Pulse Response

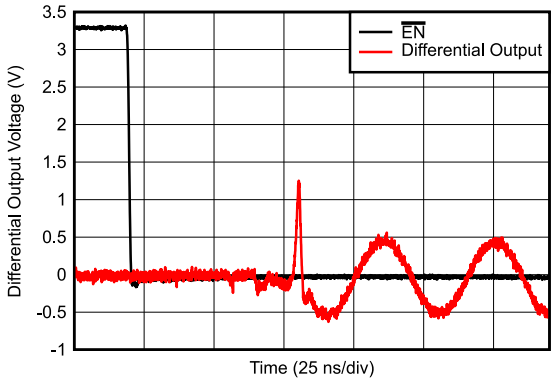


図 6-15. Turn-On Time

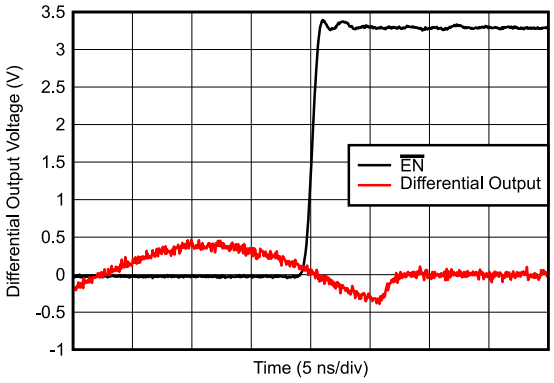
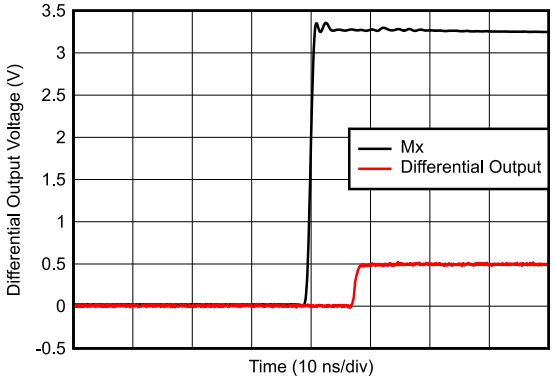


図 6-16. Turn-Off Time



0 → 0.5V transition at VOUT (1% settling)

図 6-17. Channel Turn-On Response

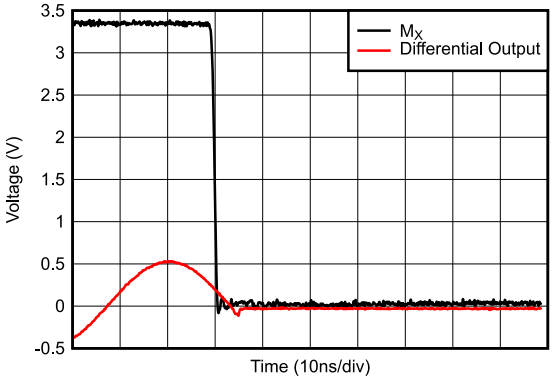
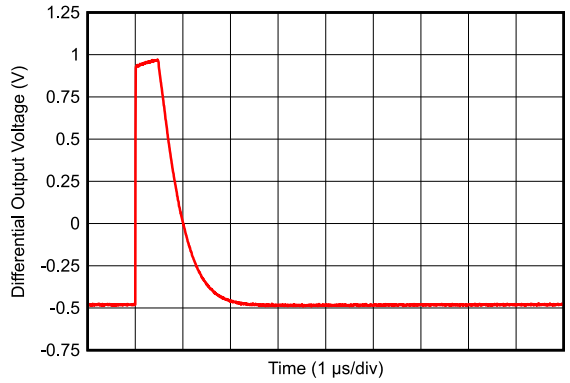


図 6-18. Channel Turn-Off Response

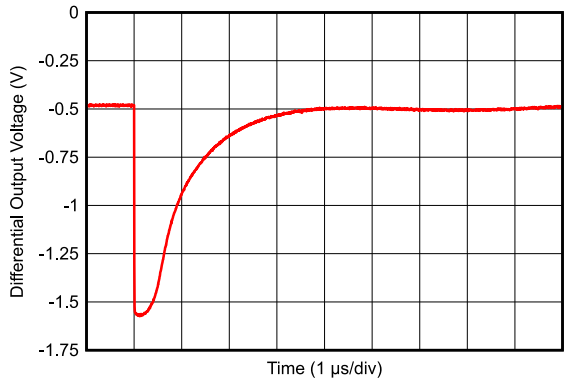
6.7 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted)



I_{DC_IN} = 0 µA → 100 µA, VOD = 0.5 V

図 6-19. Ambient Loop Cancellation Settling Time (1)



I_{DC_IN} = 100 µA → 0 µA, VOD = 0.5 V

図 6-20. Ambient Loop Cancellation Settling Time (1)

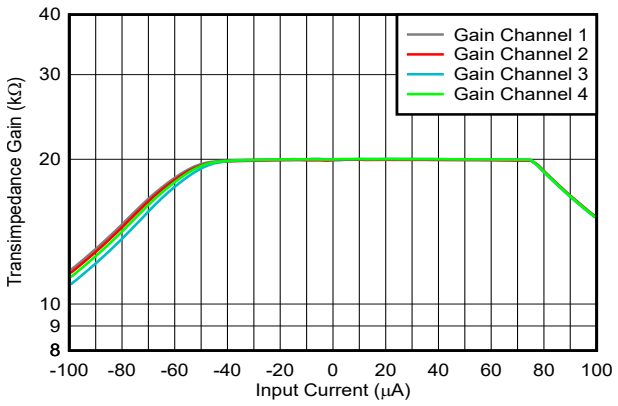


図 6-21. Transimpedance Gain vs Input Current

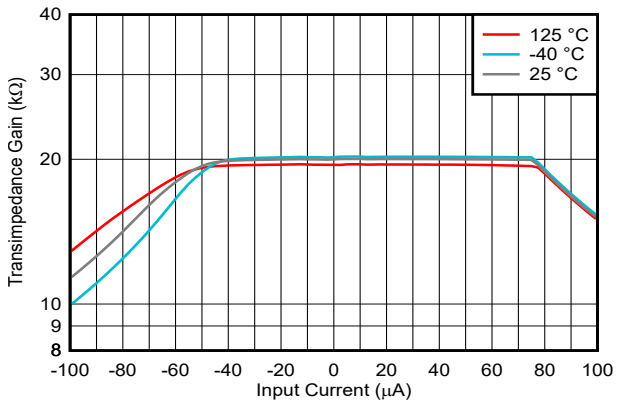


図 6-22. Transimpedance Gain vs Ambient Temperature

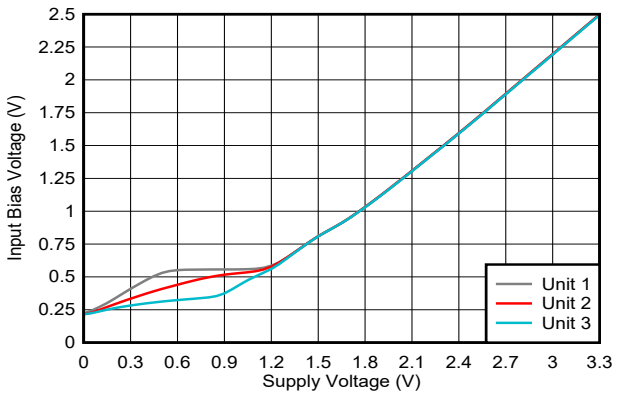


図 6-23. Input Bias Voltage vs Supply Voltage (2)

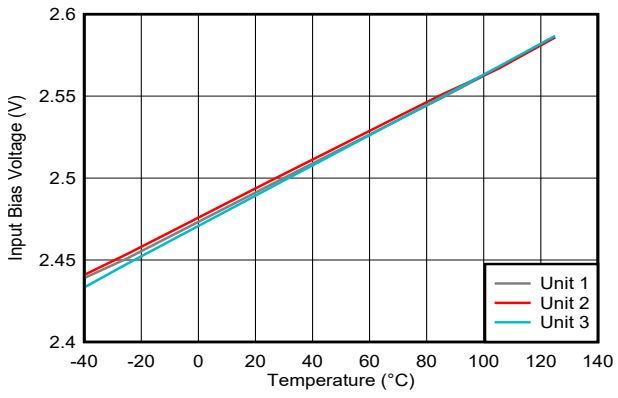


図 6-24. Input Bias Voltage vs Ambient Temperature (2)

1 Differential Output Voltage = (Vout+ - Vout-).
2 Typical units from different lots.

6.7 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted)

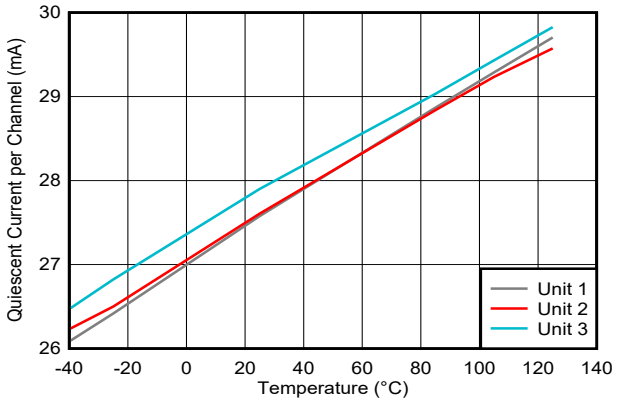


図 6-25. Quiescent Current (Per Channel) vs Ambient Temperature (2)

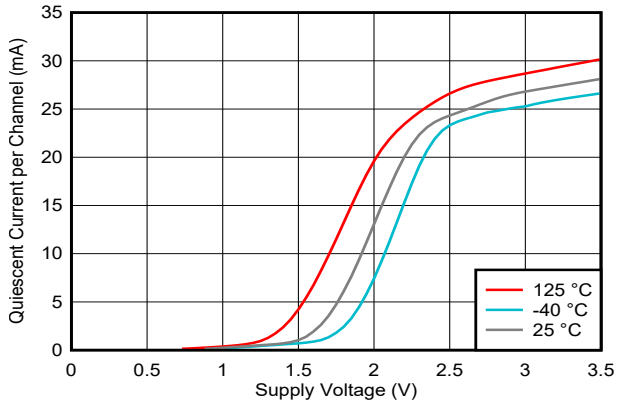
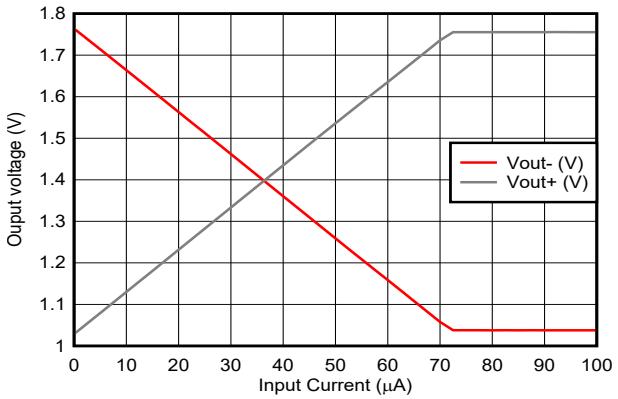
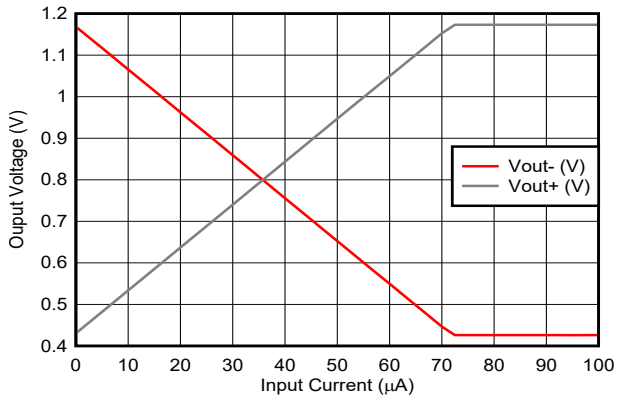


図 6-26. Quiescent Current (Per Channel) vs Supply Voltage



VOD = 0.75 V, VOCM = 1.4 V

図 6-27. High-Side Swing vs Input Current



VOD = 0.75 V, VOCM = 0.8 V

図 6-28. Low-Side Swing vs Input Current

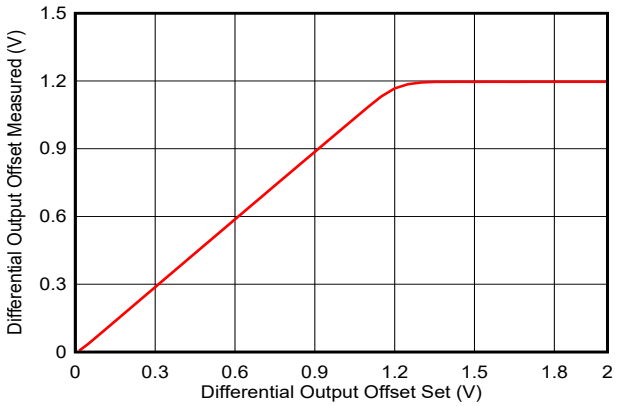
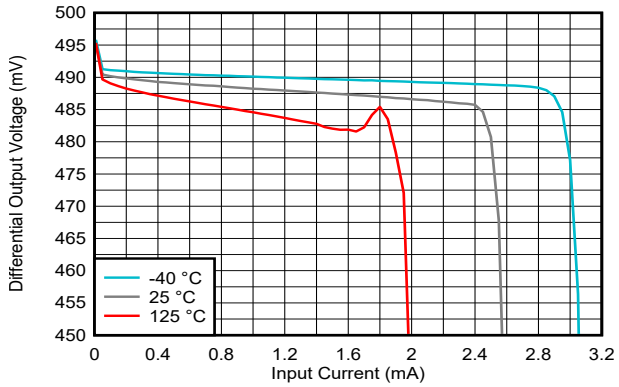


図 6-29. Differential Output Offset Gain



VOD = open

図 6-30. Ambient Light Cancellation Range vs Ambient Temperature

6.7 Typical Characteristics (continued)

At V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC\_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted)

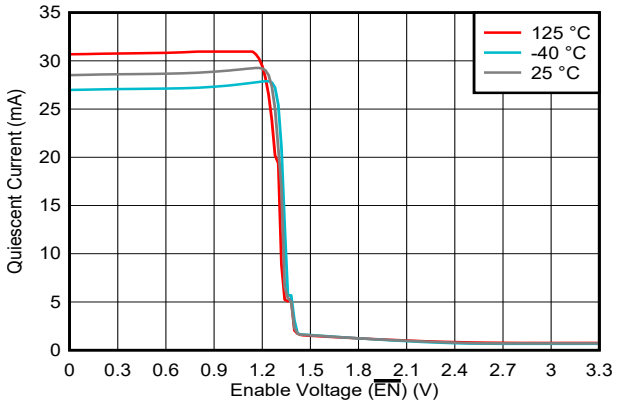
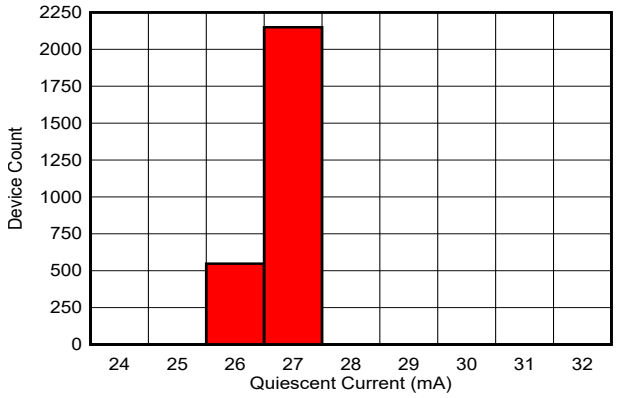
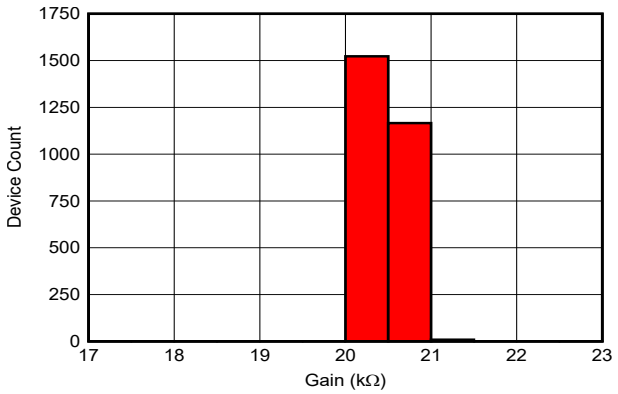


図 6-31. Logic Threshold vs Ambient Temperature



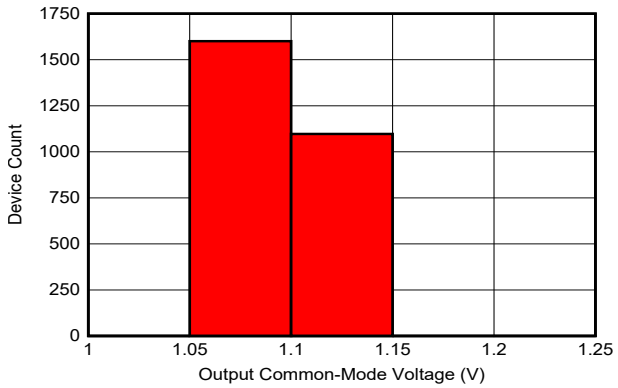
μ = 27.2 mA, σ = 0.27 mA

図 6-32. Quiescent Current Distribution



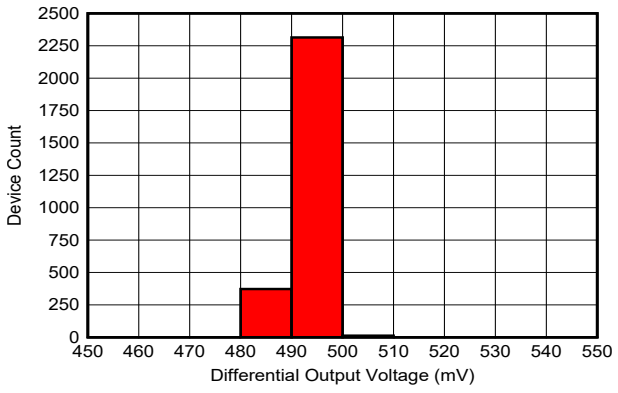
μ = 20.5 kΩ, σ = 0.2 kΩ

図 6-33. Transimpedance Gain Distribution



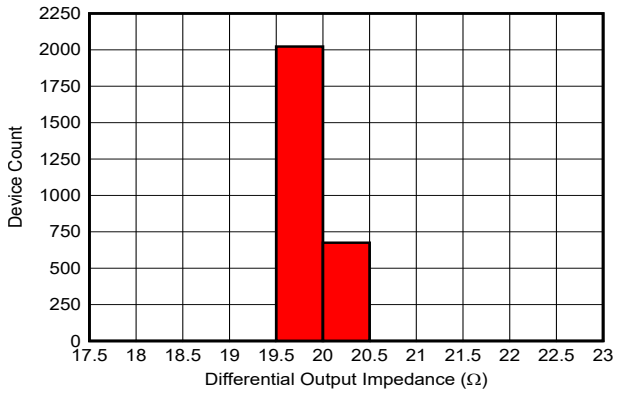
μ = 1.1 V, σ = 2 mV

図 6-34. Output Common-Mode Voltage (V_{OCM}) Distribution



μ = 493 mV, σ = 2.8 mV

図 6-35. Differential Output Offset Voltage (V_{OD}) Distribution



μ = 19.9 Ω , σ = 0.14 Ω, Device Enabled

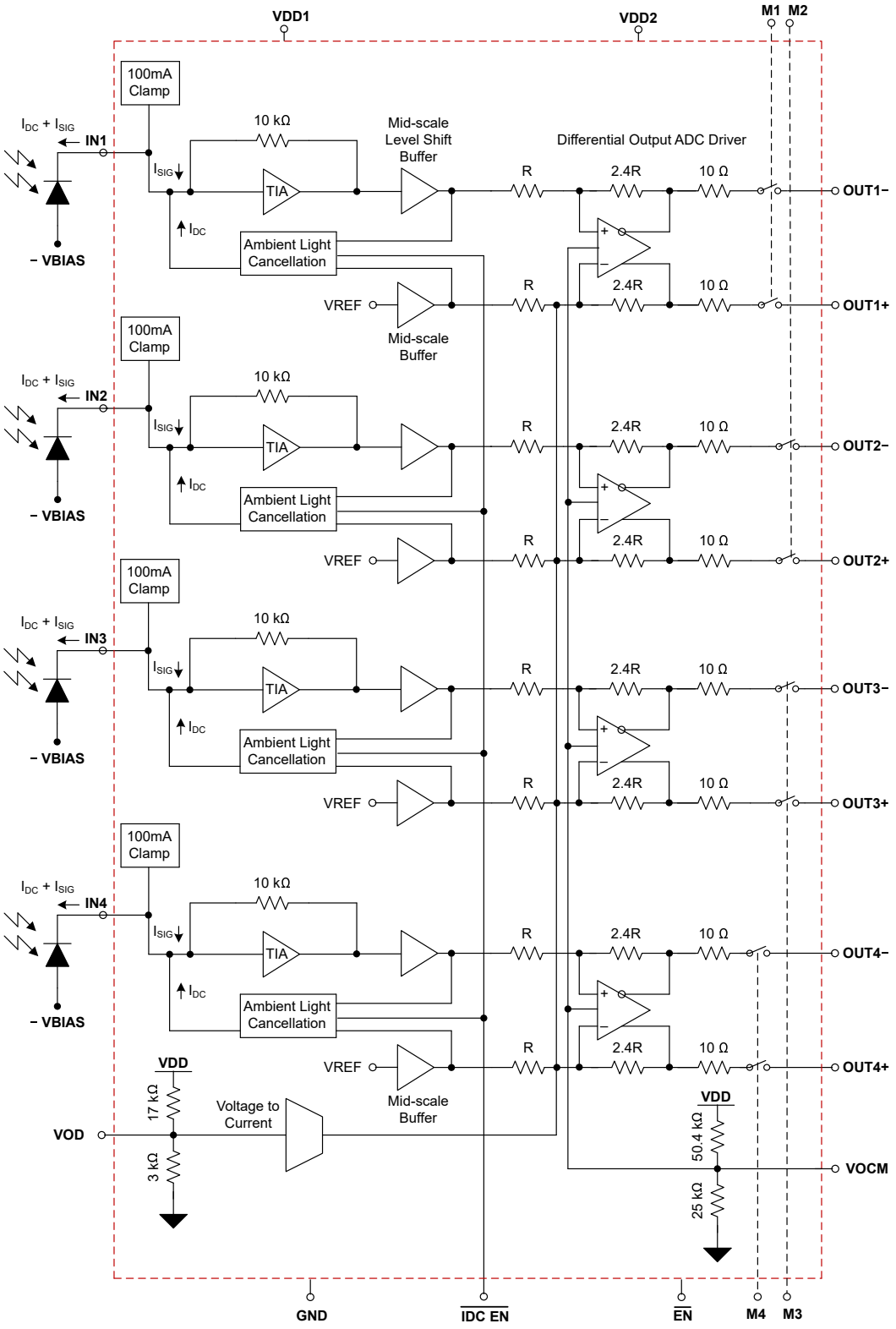
図 6-36. Differential Output Impedance (Z_{OUT}) Distribution

7 Detailed Description

7.1 Overview

The LMH32404 is a quad-channel, differential output, high-speed transimpedance amplifier (TIA) geared towards light detection and ranging (LIDAR) and laser distance measurement systems. Each LMH32404 channel has integrated switches on the output to disconnect the differential output amplifier from the output pins. This enables the LMH32404 to be highly configurable in a multi-channel LIDAR system. The LMH32404 device is designed to work with photodiodes (PDs), for example avalanche photodiodes (APDs), connected in configurations that can source or sink the current. When the photodiode sinks the photocurrent (anode is biased to a negative voltage and cathode is tied to the amplifier input) the fast recovery clamp activates when the amplifier input is overloaded. When the photodiode sources the photocurrent (cathode is biased to a positive voltage and anode is tied to the amplifier input) a soft clamp activates when the amplifier input is overloaded. When the soft clamp activates the amplifier takes longer to recover. The recovery time depends on the level of input overload. The LMH32404 is offered in a space-saving 5-mm × 4-mm, 28-pin VQFN package and is rated over a temperature range from –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Clamping and Input Protection

The LMH32404 device is optimized to work with photodiodes (PD) configurations that can source or sink current; however, the LMH32404 is optimized for a sinking current configuration. It is assumed that the LMH32404 device is being used with a PD that is configured with its cathode tied to the amplifier input and the anode tied to a negative supply voltage, unless stated otherwise.

The LMH32404 features two internal clamps, a fast recovery clamp and a soft clamp. The fast recovery clamp is the active clamp when the photodiode is sinking a photocurrent. The soft clamp is the active clamp when the photodiode is sourcing a photocurrent. Stray reflections from nearby objects with high reflectivity can produce large output current pulses from the PD. The linear input range of the LMH32404 is approximately 65 µA. Input currents in excess of the linear current range will cause the internal nodes of the amplifier to saturate, which increases the amplifier recovery time. The end result broadens the output pulse, which leads to blind zones.

To protect against this condition, the LMH32404 features an integrated fast recovery clamp that absorbs and diverts the excess current to the positive supply (V_{DD1}) when the amplifier detects its nodes entering a saturated condition. The integrated clamp minimizes the pulse extension to less than a few nanoseconds for input pulses up to 100 mA. The power-supply pins (VDD1 and VDD2) must have their own bypass capacitors to prevent large input pulses from affecting the differential output stage. The clamp circuitry is active when the amplifier is in standby mode and low-power mode, thereby protecting the TIA input.

7.3.2 ESD Protection

All LMH32404 IO pins (excluding VDD1, VDD2, and GND) have an internal electrostatic discharge (ESD) protection diode to the positive and negative supply rails to protect the amplifier from ESD events.

7.3.3 Differential Output Stage

Each channel of the LMH32404 has a differential output stage that performs two functions that are common across all differential amplifiers. This stage does the following:

1. Converts the single-ended output from the TIA stage to a differential output.
2. Performs a common-mode output shift to match the specified ADC input common-mode voltage.

The VOD pin is functional only when the LMH32404 device is used with a PD that sinks the photocurrent. Set VOD = 0 V when the LMH32404 device is interfaced with a PD that sources the photocurrent. The differential output stage has two 10-Ω series resistors on its output to isolate the amplifier output stage transistors from the package bond-wire inductance and printed circuit board (PCB) capacitance. The net gain of the LMH32404 (TIA plus the output stage) is 20 kΩ per channel when driving an external 100-Ω resistor. When the external load resistor is increased above 100 Ω, the effective gain from the IN pin to the differential output pin increases. Consequently, when the external load resistor is decreased to less than 100 Ω, the effective gain from the IN pin to the differential output pin decreases as a result of the larger voltage drop across the two internal 10-Ω resistors. The effective TIA gain is 24 kΩ when there is no load resistor between the OUT+ and OUT– pins.

The output common-mode voltage of the LMH32404 can be set externally through the VOCM pin. A resistor divider internal to the amplifier, between VDD2 and ground sets the default voltage to 1.1 V. The internal resistors generate common-mode noise that is typically rejected by the CMRR of the subsequent ADC stage. To maximize the amplifier SNR, place an external noise bypass capacitor to ground on the VOCM pin. In single-ended signal chains, such as ToF systems that use time-to-digital converters (TDCs), only a single output per channel of the LMH32404 is needed. In such situations, terminate the unused differential output in the same manner as the used output to maintain balance and symmetry. The signal swing of the single-ended output is half the available differential output swing. Additionally, the common-mode noise of the output stage, which is typically rejected by the differential input ADC, is now added to the total noise, further degrading SNR.

The output stage of the LMH32404 has an additional VOD input that sets the differential output between OUT– and OUT+. 図 7-1 shows how each output pin of the LMH32404 is at the voltage set by the VOCM pin (default = 1.1 V) when the photodiode output current is zero and the VOD input is set to 0 V. When the VOD pin is driven to a voltage of *X* volts, the two output pins are separated by *X* volts when the photodiode current is zero. The average voltage is still equal to VOCM. For example, 図 7-2 shows how if VOCM is set to 1.1 V and VOD is set to 0.4 V, then OUT– = 1.1 V + 0.2 V = 1.3 V and OUT+ = 1.1 V – 0.2 V = 0.9 V.

The VOD output offset feature is included in the LMH32404 because the output current of a photodiode is unipolar. Depending on the reverse bias configuration, a photodiode can either sink or source current, but cannot do both at the same time. With the anode connected to a negative bias and the cathode connected to the TIA stage input, the photodiode can only sink current, which implies that the TIA stage output swings in a positive direction above its default input bias voltage. Subsequently, OUT– only swings below VOCM and OUT+ only swings above VOCM. 図 7-1 shows how the with VOD = 0 V, the LMH32404 only uses half its output swing range ($V_{OUT} = V_{OUT+} – V_{OUT–}$), because one output never swings below VOCM and the other output never goes above VOCM. The signal dynamic range in this case is 0.4 V_{PP} – 0 V = 0.4 V_{PP}.

図 7-2 shows how the VOD pin voltage allows OUT– to be level-shifted above VOCM, and OUT+ to be level-shifted below VOCM to maximize the output swing capabilities of the amplifier. The signal dynamic range in this case is 0.4 V_{PP} − (-0.4 V_{PP}) = 0.8 V_{PP}.

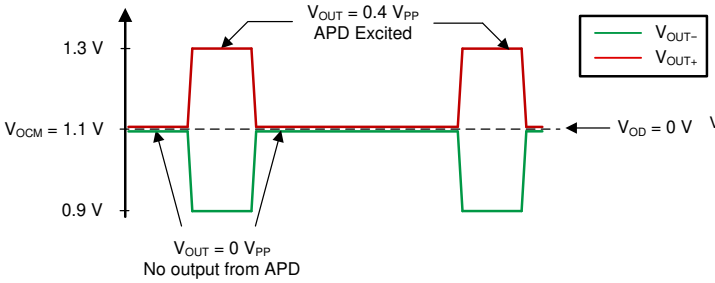


図 7-1. Single-Ended Outputs With VOD = 0 V

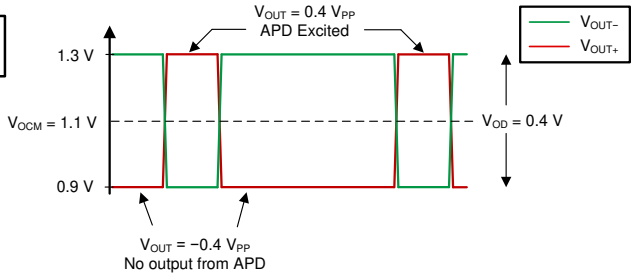


図 7-2. Single-Ended Outputs With VOD = 0.4 V

When the LMH32404 drives a 100-Ω load, the voltage set at the VOD pin is equal to the differential output offset ($V_{OUT} = V_{OUT+} – V_{OUT–}$) when the input signal current is zero. Use 式 1 to calculate the differential output offset under other load conditions.

$$V_{OD} = 1.2 \times VOD \times \frac{R_L}{\left(R_L + 20\ \Omega\right)} \quad (1)$$

where

- VOD = Voltage applied at pin 10
- $V_{OD} = (V_{OUT–} – V_{OUT+})$
- R_L = External load resistance

7.4 Device Functional Modes

7.4.1 Ambient Light Cancellation (ALC) Mode

The LMH32404 has an integrated DC cancellation loop that cancels and voltage offsets from incidental ambient light. The ALC mode only works when the PD is sinking the photocurrent. The DC cancellation loop is enabled by setting $\overline{\text{IDC\_EN}}$ low. Incident ambient light on a photodiode produces a DC current resulting in an offset voltage at the output of the TIA stage.

If the photodiode produces a DC output current resulting from ambient light, the output of the level-shift buffer stage is offset from the reference voltage V_{REF}. The ALC loop detects this offset and produces an opposing DC current to compensate for the differential offset voltage at its input. The loop has a high-pass cutoff frequency of 400 kHz. The ambient light cancellation loop is disabled when the amplifier is placed in low-power mode.

The shot noise current introduced by the DC cancellation loop increases the overall amplifier noise; so, if the ambient light level is negligible, then disable the loop to improve SNR. The cancellation loop helps save PCB space and system costs by eliminating the need for external AC coupling passive components. Additionally, the extra trace inductance and PCB capacitance introduced by using external AC coupling components degrades the LMH32404 dynamic performance.

The ambient light cancellation loop is active (depending on $\overline{\text{IDC\_EN}}$ configuration) when one or more of the channels is in standby mode. The ambient light cancellation loop is disabled when the amplifier is placed in low-power mode. When the LMH32404 is brought out of low-power operation the ambient light cancellation loop requires several time constants to settle. The time constant is based on the 400-kHz cutoff frequency of the loop. When in standby mode, the ALC loop is still active depending on IDC_EN configuration.

7.4.2 Channel Multiplexer Mode

The LMH32404 is a highly integrated transimpedance amplifier device with four independent channels. Each channel has its own single-ended input, differential output stage and multiplexing switch. The integrated switch can be used to disconnect the differential output amplifier from the output pin, thereby enabling high-impedance output for the respective channel.

図 7-4 shows how this device feature can further save board space and cost by eliminating the need for discrete high-speed multiplexer in a system that consists of several amplifier channels multiplexed to a single ADC channel. When switching between different channels, the LMH32404 has a transition time of 10 ns (typical). The disabled channel outputs are high-impedance so multiple amplifier outputs can be directly shorted to each other. If one channel is enabled and other channels are disabled, the disabled channels will not load the enabled channel. This further makes the LMH32404 easy to use in photodiode array applications.

Set Mx (M1, M2, M3, or M4) high for the corresponding channel to be enabled and output switches closed. Set Mx to logic low (default state) for the corresponding channel to be disabled (standby mode) and output switches open. When the channel is in its standby power mode, the clamp circuitry is still active thereby protecting the TIA input. Also, when in standby mode, the ALC loop is still active depending on $\overline{\text{IDC\_EN}}$ configuration.

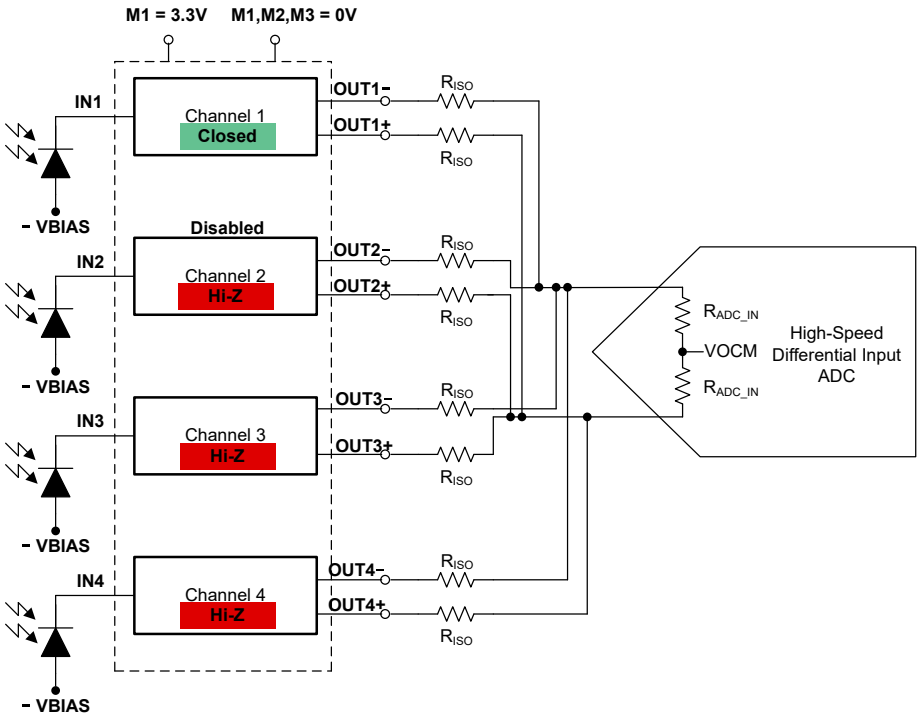


図 7-3. Configuring LMH32404 in Channel Multiplexer Mode to Drive a Single ADC

7.4.3 Low-Power Mode

The LMH32404 can be placed in low-power mode by setting $\overline{EN}$ high, which helps in saving system power. Enabling low-power mode puts the outputs of the internal amplifiers in the LMH32404, including the differential outputs, in a high-impedance state.

If a system consists of high number of amplifier channels multiplexed to a few ADC channels. 図 7-4 shows how this device feature can further save board space and cost by eliminating the need for a discrete high-speed multiplexer. The disabled LMH32404 outputs are high-impedance so multiple LMH32404 device outputs can be directly shorted to each other. If one LMH32404 device is enabled and others are disabled, the disabled devices will not load the enabled device. This further makes the LMH32404 easy to use in photodiode array applications.

When the amplifier is in its low-power mode, the clamp circuitry is still active thereby protecting the TIA input. The ambient light cancellation loop is disabled when the amplifier is placed in low-power mode. When the LMH32404 is brought out of low-power operation the ambient light cancellation loop requires several time constants to settle. The time constant is based on the 400-kHz cutoff frequency of the loop.

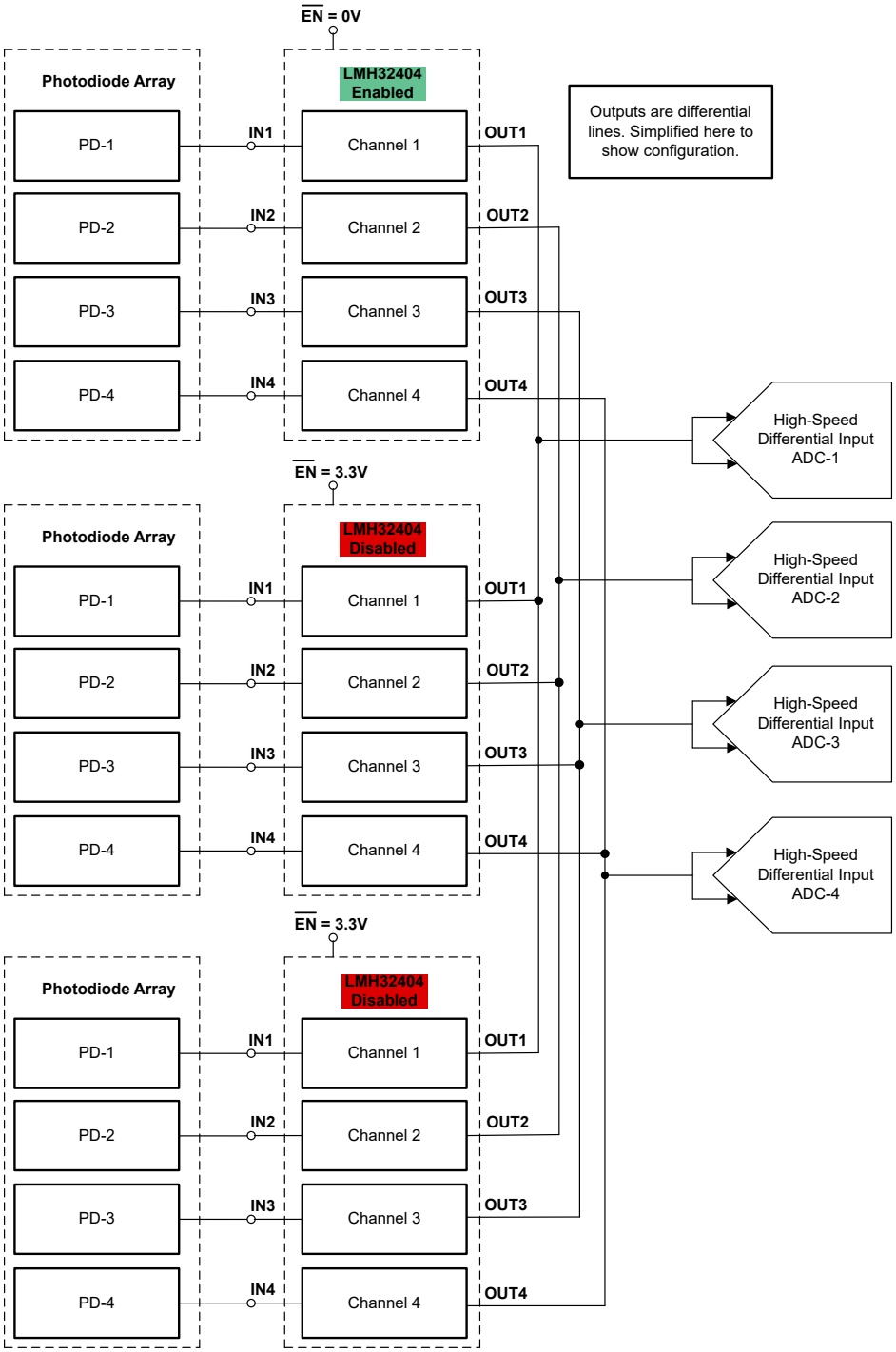


図 7-4. Configuring Three LMH32404 Devices to Drive Four ADC Channels

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

Each differential output pair of the LMH32404 can directly drive a high-speed differential input ADC. 図 8-1 shows how the effective signal the effective signal gain between the TIA input and the ADC input is 20 kΩ when driving an ADC with a 100-Ω differential input impedance (R_{ADC_IN} = 50 Ω). 式 2 gives the effective signal gain between the TIA input and the ADC input when driving an ADC with any other value of differential input impedance (R_{ADC_IN} ≠ 50 Ω).

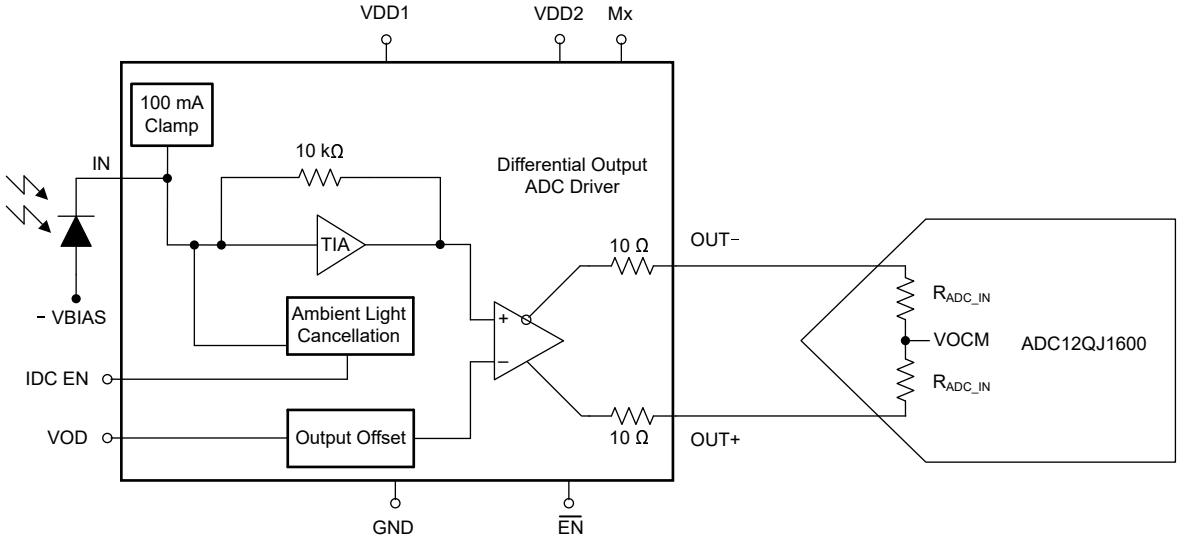


図 8-1. LMH32404 (Single Channel) to ADC Interface

$$A_V = 20\ k\Omega \times 1.2 \times \frac{2 \times R_{ADC\_IN}}{\left(2 \times R_{ADC\_IN} + 20\ \Omega\right)} \quad (2)$$

where

- A_V = Differential gain from the TIA input to the ADC input
- R_{ADC_IN} = Input resistance of the ADC

図 8-2 shows that in some designs a matching resistor network can be inserted between the LMH32404 output and the ADC inputs. 式 3 gives the effective gain from the TIA input to the ADC input when using a matching resistor network.

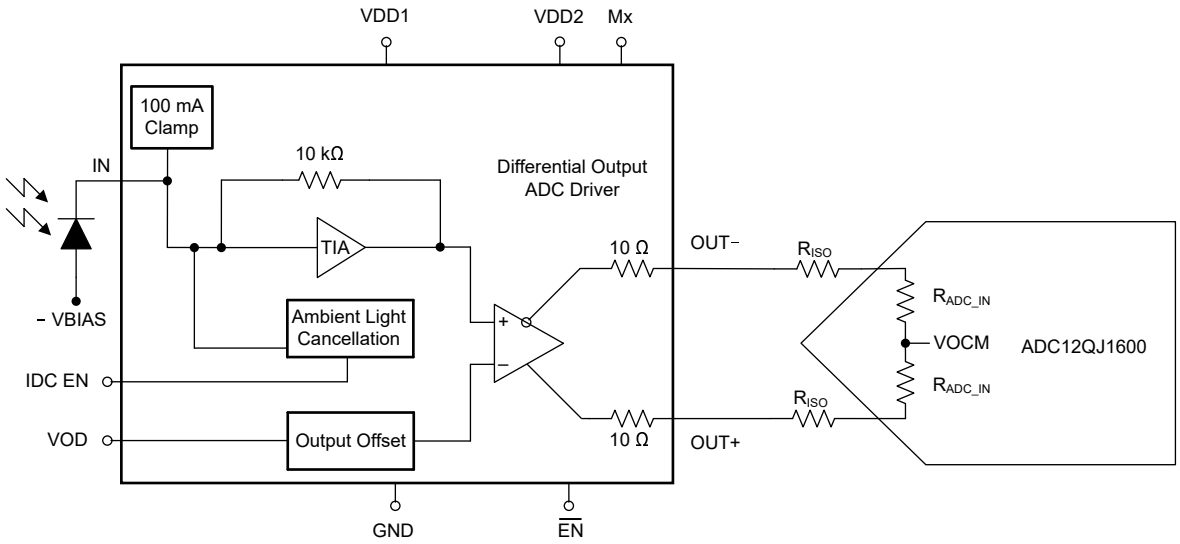


図 8-2. LMH32404 (Single Channel) to ADC Interface With a Matching Resistor Network

$$A_V = 20\,k\Omega \times 1.2 \times \frac{2 \times R_{ADC\_IN}}{\left(2 \times R_{ADC\_IN} + 2 \times R_{ISO} + 20\,\Omega\right)} \quad (3)$$

where

- A_V = Gain from the TIA input to the ADC input
- R_{ADC_IN} = Differential input resistance of the ADC
- R_{ISO} = Series resistance between the TIA and ADC

式 4 gives the voltage to be applied at the VOD pin (pin 10) if a certain differential offset voltage (V_{OD}) is needed at the ADC input for the circuit in 図 8-2.

$$VOD = V_{OD} \times \left(\frac{1}{1.2}\right) \times \frac{\left(2 \times R_{ADC\_IN} + 2 \times R_{ISO} + 20\,\Omega\right)}{\left(2 \times R_{ADC\_IN}\right)} \quad (4)$$

where

- VOD = Voltage applied at pin 10
- V_{OD} = Desired differential offset voltage at the ADC input
- R_{ADC_IN} = Differential input resistance of the ADC
- R_{ISO} = Series resistance between the TIA and ADC

8.2 Typical Application

8.2.1 Standard TIA Application

図 8-3 and 図 8-4 shows the circuit used to test the LMH32404 with a voltage source.

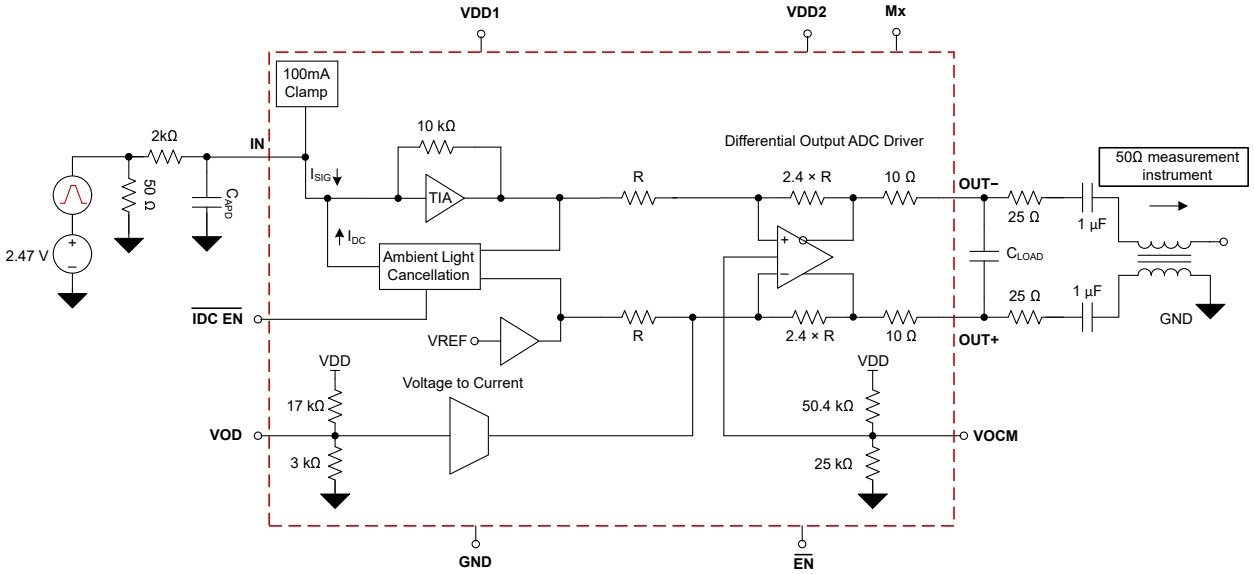


図 8-3. LMH32404 Single Channel Test Circuit for Single-Ended Measurement

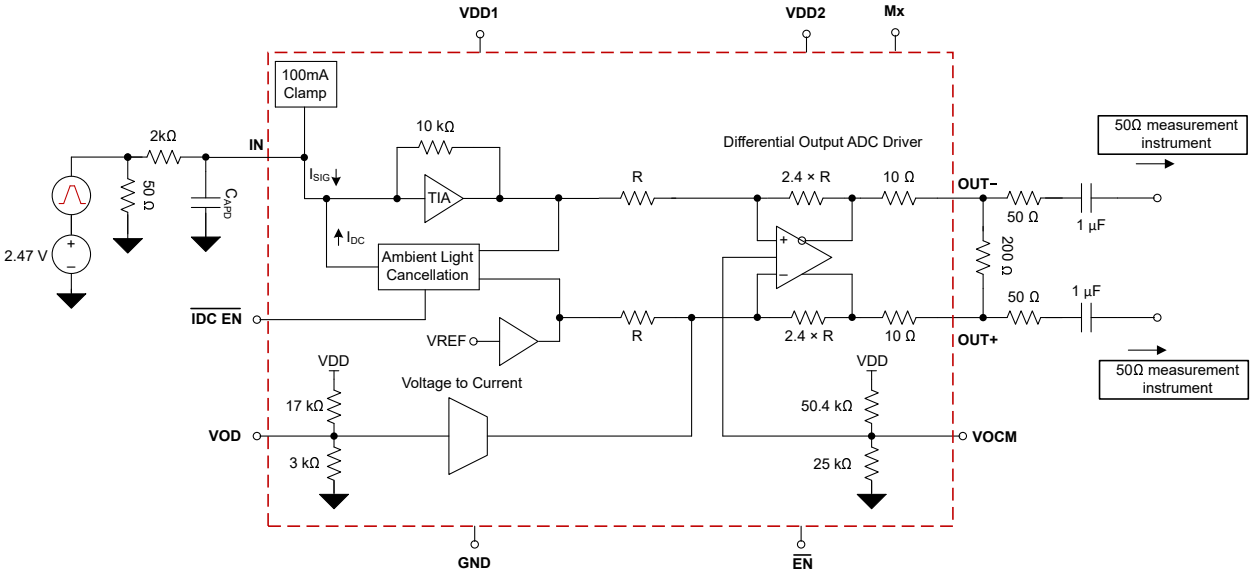


図 8-4. LMH32404 Single Channel Test Circuit for Differential Measurement

8.2.1.1 Design Requirements

The objective is to design a low-noise, wideband differential output transimpedance amplifier. The design requirements are:

- Amplifier supply voltage: 3.3 V
- Transimpedance gain: 20 kΩ
- Photodiode capacitance: C_{APD} = 1 pF
- Target bandwidth: > 300 MHz
- Multiple channels for array applications

8.2.1.2 Detailed Design Procedure

図 8-3 and 図 8-4 shows the LMH32404 test circuit used to measure its bandwidth, noise and transient response. The voltage source is DC biased close to the input bias voltage of the LMH32404. The LMH32404 internal design is optimized to only source current out of the input pin (INx). When testing the LMH32404 with a network analyzer or sinusoidal source, set the DC bias such that sum of the input AC and DC component does not result in a sourcing current into the amplifier input. Only use the LMH32404 with avalanche photodiodes (APDs) that sink current. An anode-biased APD satisfies this requirement.

図 8-5 shows the measured results for bandwidth of LMH32404 for all four channels.

図 8-6 shows the output noise spectral density of the LMH32404 with C_{APD} = 1 pF and no photodiode capacitance.

図 8-7 shows the turn-on time of the LMH32404 channel when the Mx pin is toggled from logic low to high. When the amplifier is off, the output is in a high-impedance state. When the amplifier turns on, the output settles and starts tracking the input within a few nanoseconds.

図 8-8 shows the turn-off time of the LMH32404 channel when the Mx pin is toggled from logic high to low. When the amplifier is off, the output is in a high-impedance state.

8.2.1.3 Application Curves

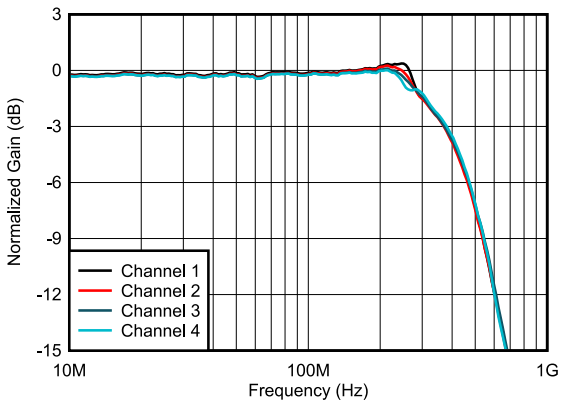


図 8-5. Transimpedance Bandwidth

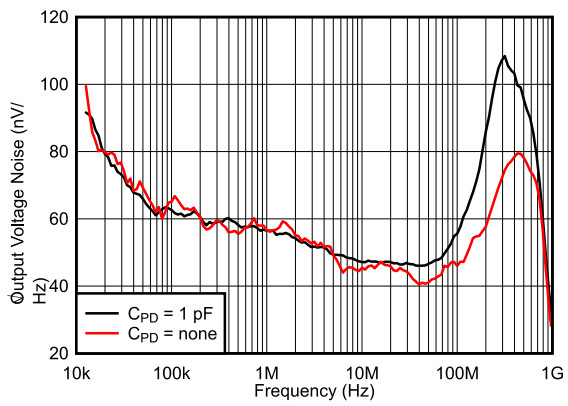


図 8-6. Output Noise Spectral Density

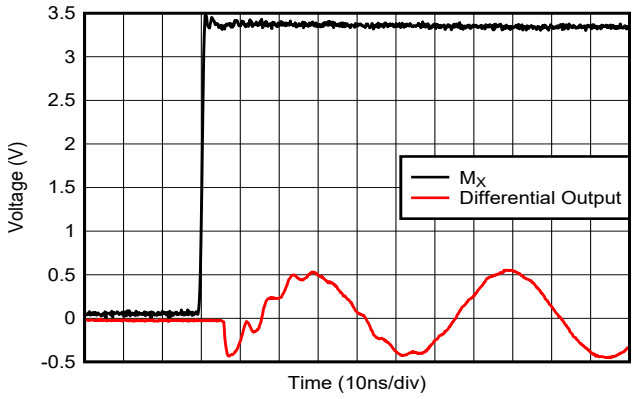


図 8-7. Channel Turn-On Response

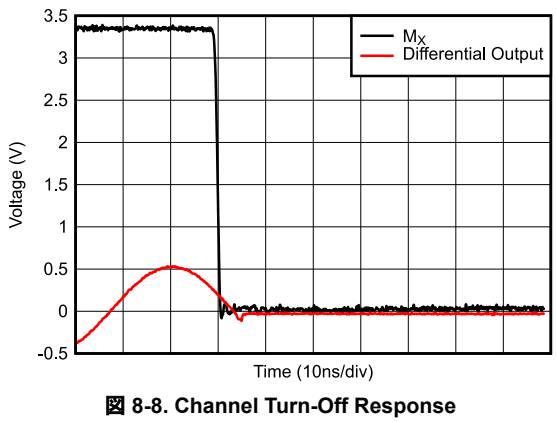


図 8-8. Channel Turn-Off Response

8.2.2 Increase Channel Density for Optical Front-End Systems

Modern LiDAR systems are moving towards solid state configurations with multi-channel photodiode arrays. For optical front-end designs it is impractical to have single transimpedance amplifiers (TIA) connected to each diode output along with additional multiplexers or other switching solutions to connect to the digitizer. This approach causes increased solution size, complexity and signal degradation.

The LMH32404 resolves this problem in two ways, by providing higher integration within the device and by allowing user configured output multiplexing for independent output control.

図 8-9 shows a comparison of a non-integrated front end using individual amplifiers, a multiplexer, and fully-differential amplifier (FDA) to connect to the differential input ADC. In comparison, the front end using the LMH32404 is able to connect four channels per amplifier to each ADC or set of ADC differential inputs. 図 8-9 shows how the LMH32404 improves solution size and system complexity compared to a non-integrated solution. With the additional features like input current clamps and ambient light cancellation, LMH32404 also improves system design and eliminates need for additional circuitry.

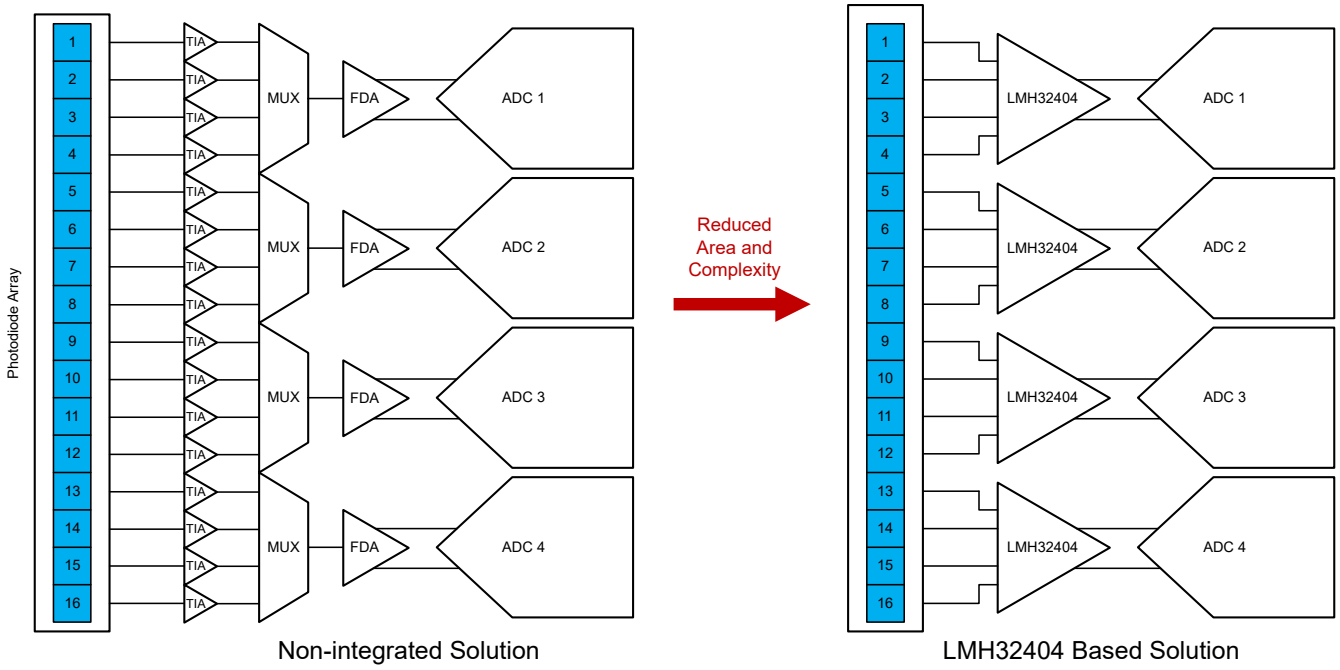


図 8-9. Solution Size Comparison

LMH32404 is a quad-channel device and each channel has an independent differential output stage and multiplexing switch. 図 8-10 shows two common output configurations. In a four-to-four configuration the LMH32404 operates with no output multiplexing with each input and corresponding differential output active. This configuration is useful when the user needs to be able to capture data from four optical sensors simultaneously. In a four-to-one configuration, the LMH32404 internally multiplexes all four differential outputs into a single differential output. The LMH32404 outputs can be configured in any permutation such as one channel operating in one-to-one mode with the other three channels multiplexed in a three-to-one configuration. This independent control and multiplexing feature significantly increases channel density for systems that do not need to record all inputs simultaneously.

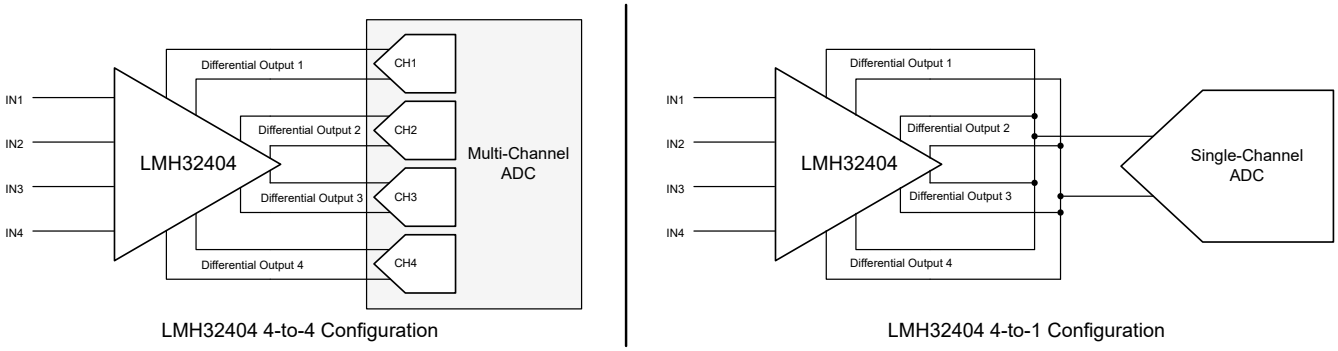


図 8-10. LMH32404 Multiplexing Configuration Examples

To show the front-end design integration and multiplexing capability, the LMH32404 performance was measured with the ADC12QJ1600-Q1 quad channel analog to digital converter. 図 8-11 shows the data measured from the ADC12QJ1600-Q1 using a 10 ns electrical input pulse on a single channel of the LMH32404. These pulses are similar to outputs seen in a typical LiDAR application. 図 8-12 shows the data from the ADC12QJ1600- Q1 when the LMH32404 outputs multiplex between different channels. The initial output shows a 10ns duration pulse train on channel 1, followed by a 20 MHz sinusoidal signal on channel 2 and then the output with all channels turned off but the input signals still present. Details on these measurements and application are discussed in the application brief, How to Increase the Channel Density of LiDAR Systems with the 4-Channel LMH32404 Transimpedance Amplifier.

8.2.2.1 Application Curves

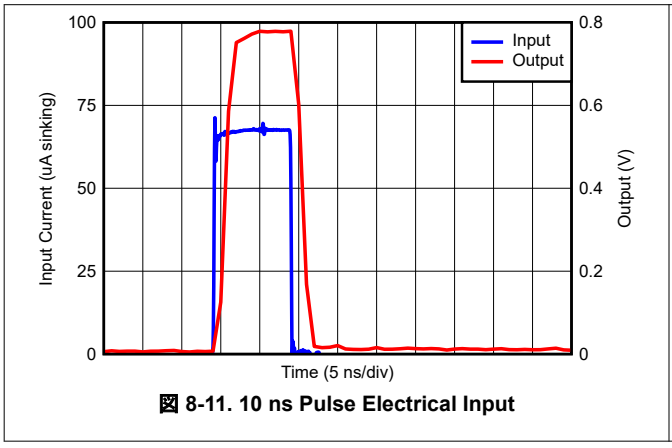


図 8-11. 10 ns Pulse Electrical Input

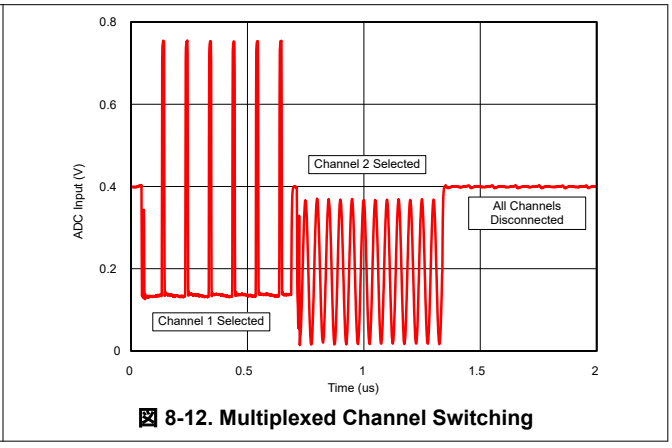


図 8-12. Multiplexed Channel Switching

9 Power Supply Recommendations

The LMH32404 operates on 3.3-V supplies. The VDD1 and VDD2 pins must always be driven from the same supply source and individually bypassed. Use multiple bypass capacitors in parallel, because a low power-supply source impedance must be maintained across frequency. Place the bypass capacitors as close to the supply pins as possible. Place the smallest capacitor on the same side of the PCB as the LMH32404. Placing the larger valued bypass capacitors on the same side of the PCB is preferable as well; if there are space constraints however, the capacitors can be moved to the opposite side of the PCB using multiple vias to reduce the series inductance resulting from the vias. The LMH32404 can be run on bipolar supplies by connecting pins 11 and 26 to the negative supply. The thermal pad must always be connected to the most negative supply. The digital pin threshold voltages must be appropriately level shifted as they are referred to voltages at pins 11 and 26.

10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the LMH32404 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output pins can cause instability, whereas parasitic capacitance on the input pin reduces the amplifier bandwidth. Cut out the power and ground traces under the signal input and output pins to reduce unwanted capacitance. Otherwise, ground and power planes must be unbroken elsewhere on the board.
- **Minimize the distance from the power-supply pins to high-frequency bypass capacitors.** Use low inductance ceramic capacitors as decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. Place a combination of 100 pf (or higher) and 33 nF (or higher) capacitors on the same side as the DUT. If space constraints force the larger value bypass capacitors to be placed on the opposite side of the PCB, use multiple vias on the supply and ground side of the capacitors. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).
- For more information on board design and layout, see the evaluation module user guide, LMH32404 Evaluation Module User's Guide.

10.2 Layout Example

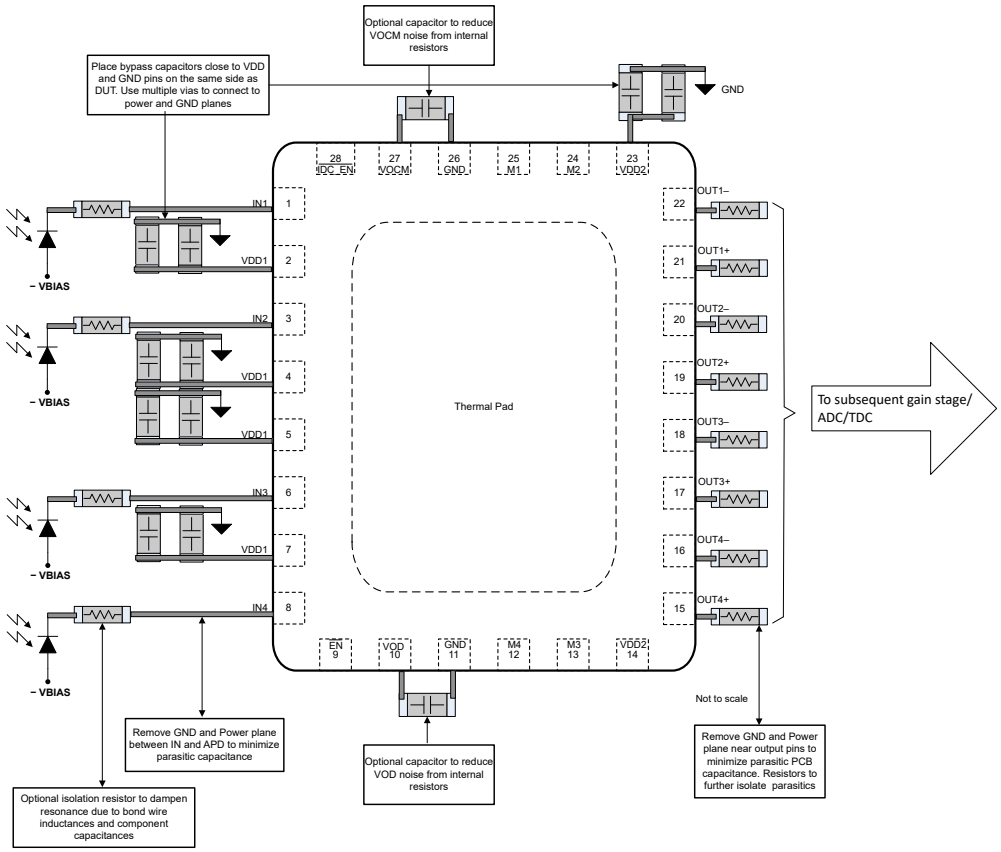


図 10-1. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

- Texas Instruments, *LIDAR-Pulsed Time-of-Flight Reference Design* design guide
- Texas Instruments, *LIDAR-Pulsed Time-of-Flight Reference Design: Using High-Speed Data Converters* design guide
- Texas Instruments, *Optical Front-End System Reference Design* design guide

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LMH32404 Evaluation Module* user's guide
- Texas Instruments, *Training Video: High speed TIAs for optical time of flight and LIDAR systems*
- Texas Instruments, *Training Video: Multi-channel optical front-end reference design overview*
- Texas Instruments, *Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1* blog
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2* blog

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH32404IRHFR	ACTIVE	VQFN	RHF	28	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	32404I	Samples
LMH32404YR	ACTIVE	DIESALE	Y	0	3000	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LMH32404 :

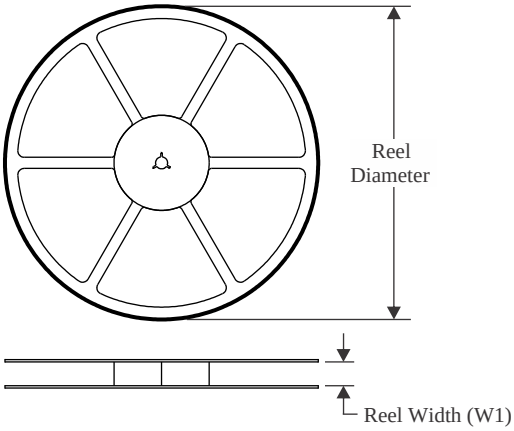
- Automotive : LMH32404-Q1

NOTE: Qualified Version Definitions:

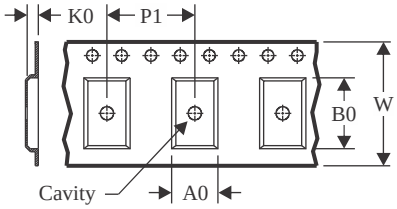
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

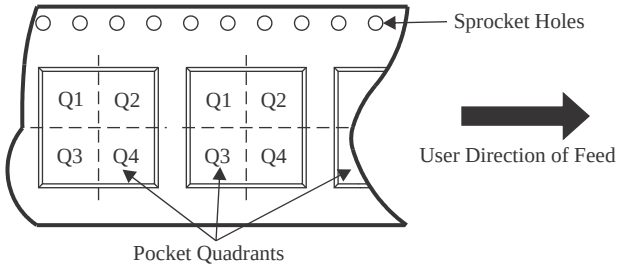


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

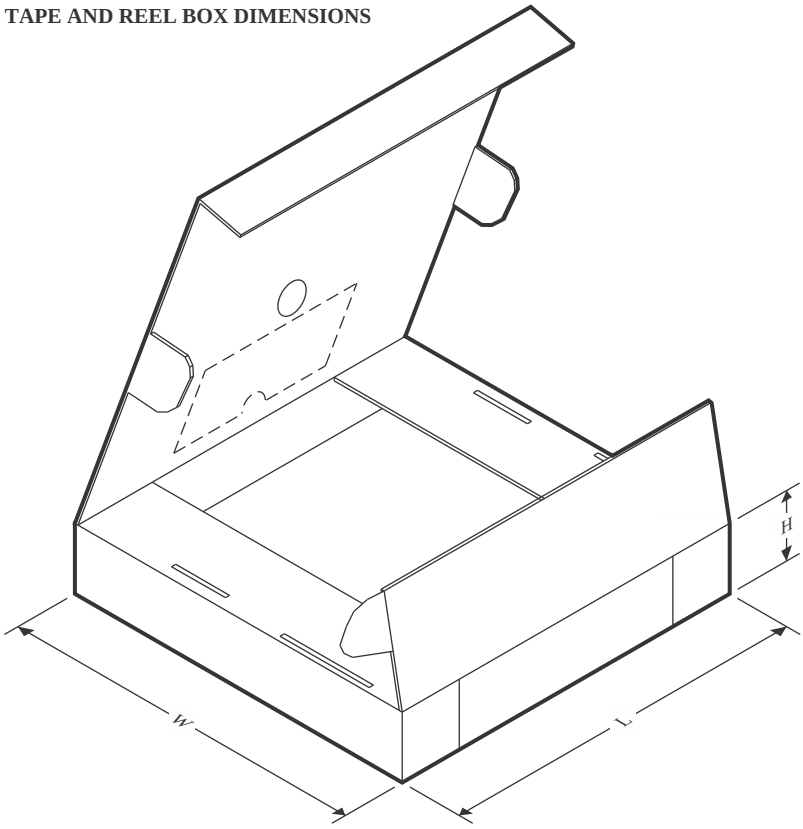
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH32404IRHFR	VQFN	RHF	28	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LMH32404YR	DIESALE	Y	0	3000	180.0	8.4	1.5	2.61	0.4	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



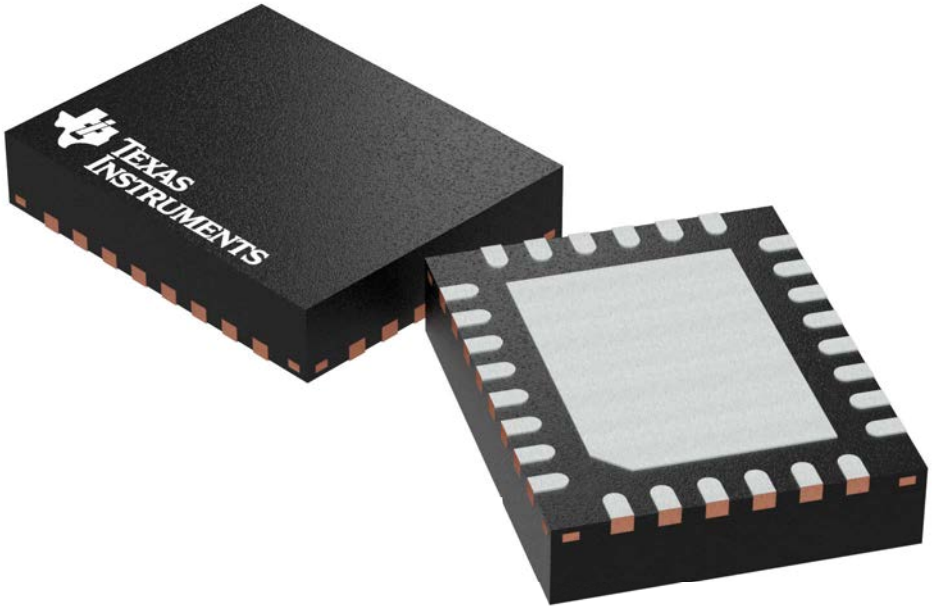
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH32404IRHFR	VQFN	RHF	28	3000	367.0	367.0	35.0
LMH32404YR	DIESALE	Y	0	3000	210.0	185.0	35.0

RHF 28

VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



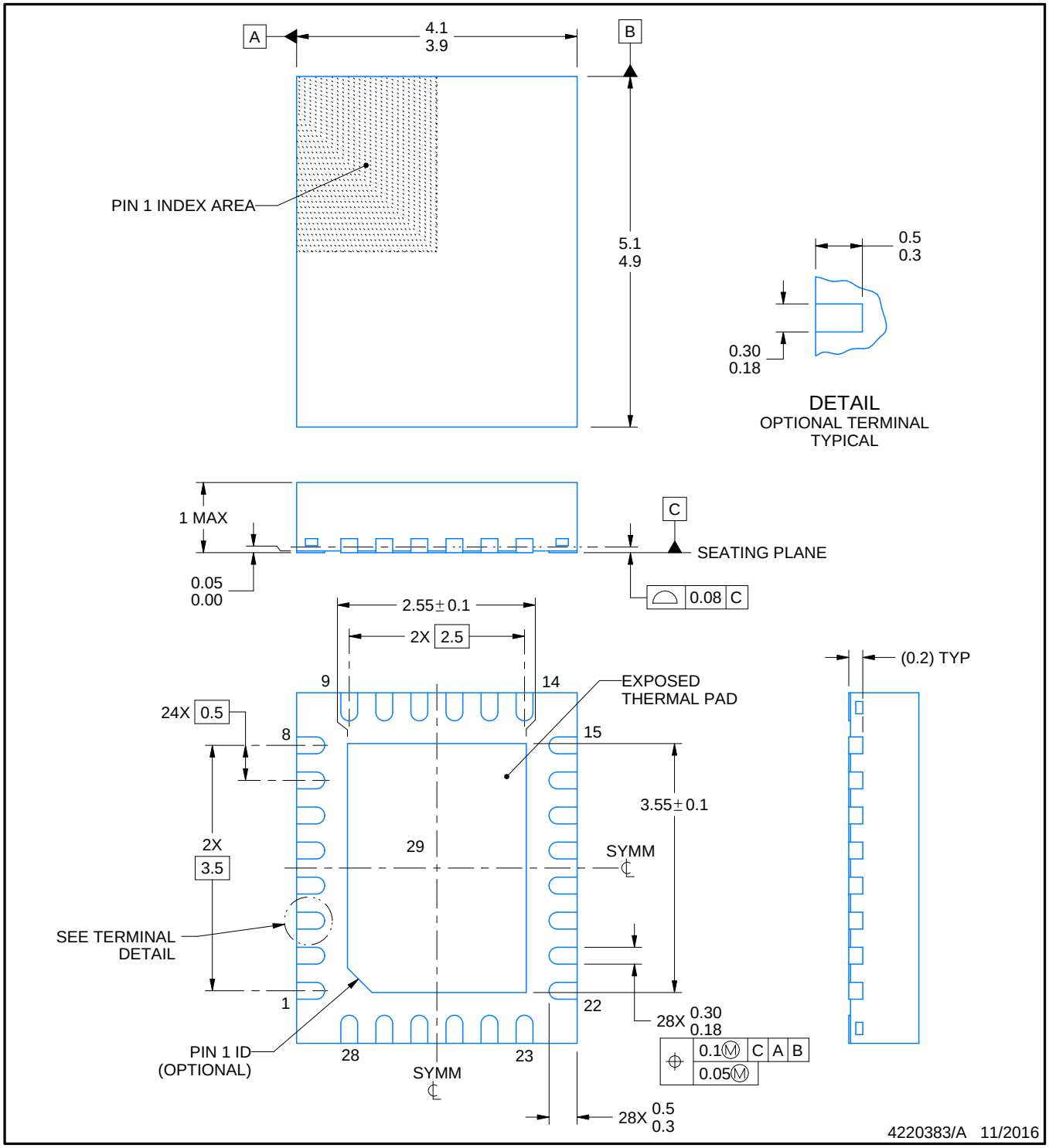
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RHF0028A

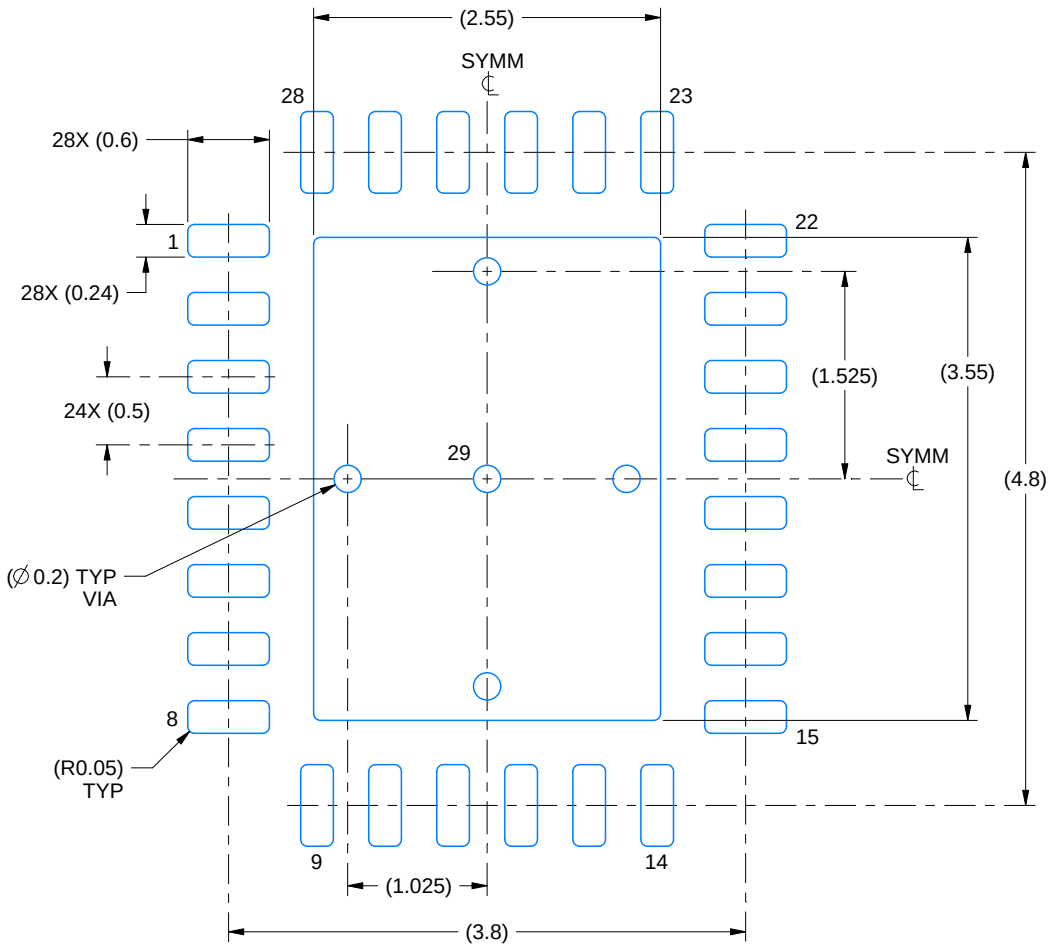
VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

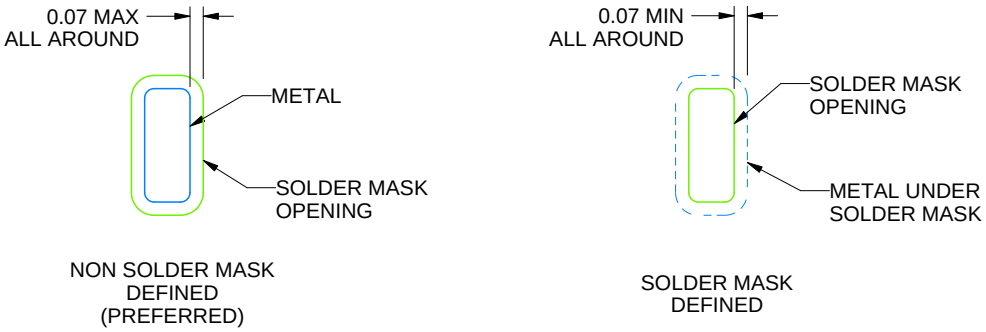


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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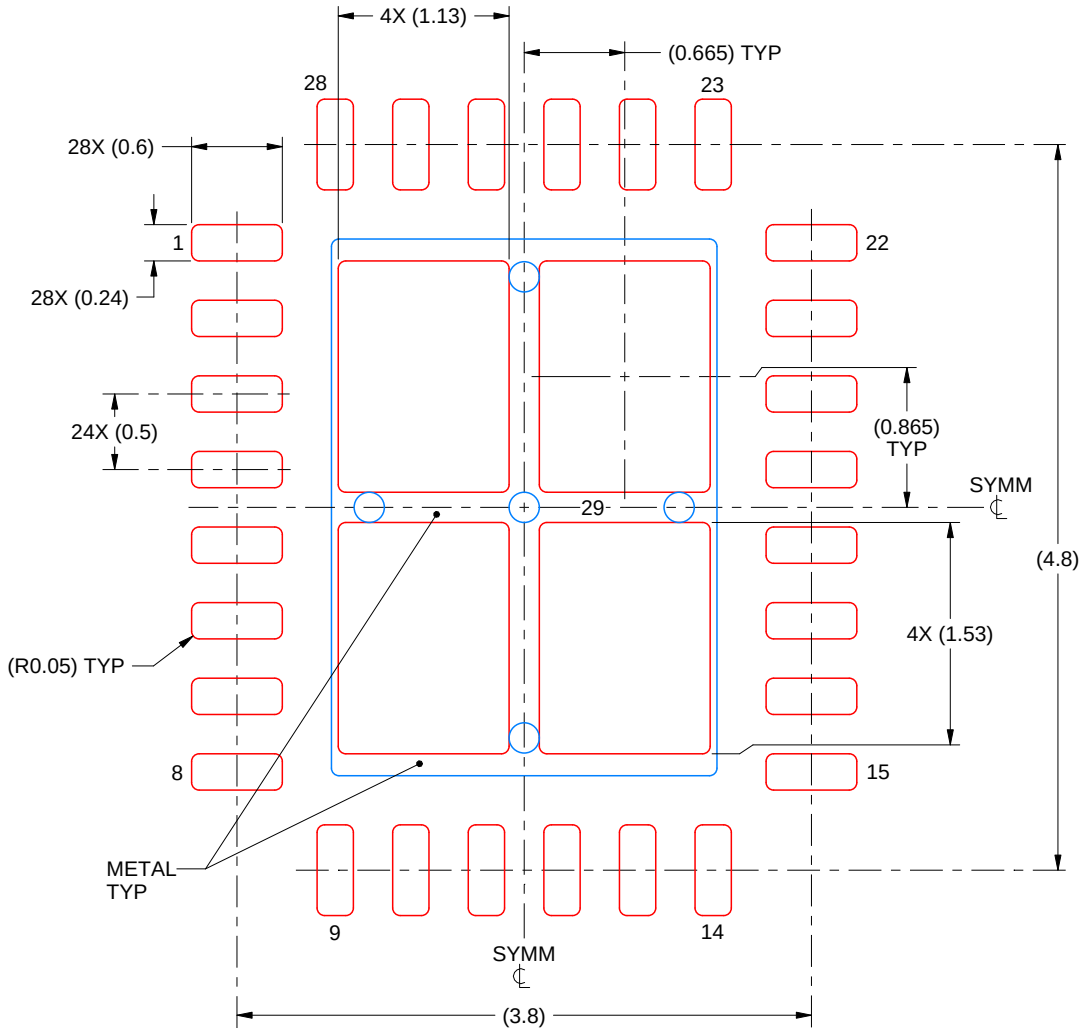
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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