

LMH6572 トリプル2:1高速ビデオ・マルチプレクサ

1 特長

- 350MHz、250mV、-3dB帯域幅
- 290MHz、2V_{pp}、-3dB帯域幅
- チャンネルのスイッチング時間: 10ns
- 5MHzにおいてチャンネル間分離90dB
- 0.02%、0.02°の差動ゲイン、位相
- ゲイン・フラットネス: 140MHzまで0.1dB
- スルー・レート: 1400V/μs
- 広い電源電圧範囲:
6V (±3V) ~ 12V (±6V)
- 10MHzにおいて-78dB HD2
- 10MHzにおいて-75dB HD3

2 アプリケーション

- RGBビデオ・ルータ
- 複数入力のビデオ・モニタ
- フォルト・トレラントのデータ・スイッチ

3 概要

LMH6572は高性能のアナログ・マルチプレクサで、プロフェッショナル・グレードのビデオや、他の高忠実度、高帯域幅のアナログ・アプリケーション用に最適化されています。LMH6572は、2V_{pp}の出力信号レベルで290MHzの帯域幅を提供します。140MHzの0.1dB帯域幅と、1500V/μsのスルー・レートから、この製品は高解像度テレビ(HDTV)および高解像度のマルチメディア・ビデオ・アプリケーションに適しています。

LMH6572は、コンポジット・ビデオ・アプリケーションをサポートし、NTSCおよびPALビデオ信号で0.02%および0.02°の差動ゲイン誤差と位相誤差を実現し、単一のバック終端の75Ω負荷を駆動します。LM6572は80mAのリニア出力電流を供給し、複数のビデオ負荷アプリケーションを駆動できます。

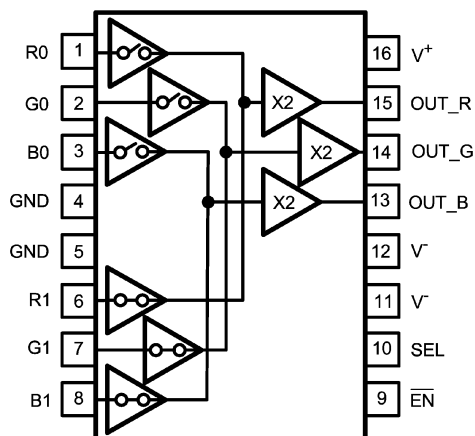
LMH6572の内部ゲインは2V/V (+6dBv)で、バック終端の伝送ラインを1V/V (0dBv)の実質ゲインで駆動します。

LMH6572はSSOPパッケージで供給されます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
LMH6572	SSOP (16)	4.90mm×3.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



目次

1	特長	1	7.1	Overview	11
2	アプリケーション	1	7.2	Feature Description	11
3	概要	1	8	Power Supply Recommendations	15
4	改訂履歴	2	8.1	Power Dissipation	15
5	Pin Configuration and Functions	3	8.2	ESD Protection	15
6	Specifications	4	9	Layout	16
	6.1 Absolute Maximum Ratings	4	9.1	Layout Guidelines	16
	6.2 ESD Ratings	4	10	デバイスおよびドキュメントのサポート	17
	6.3 Recommended Operating Conditions	4	10.1	ドキュメントの更新通知を受け取る方法	17
	6.4 Thermal Information	4	10.2	コミュニティ・リソース	17
	6.5 $\pm 5V$ Electrical Characteristics	5	10.3	商標	17
	6.6 $\pm 3.3V$ Electrical Characteristics	7	10.4	静電気放電に関する注意事項	17
	6.7 Typical Characteristics	8	10.5	Glossary	17
7	Detailed Description	11	11	メカニカル、パッケージ、および注文情報	17

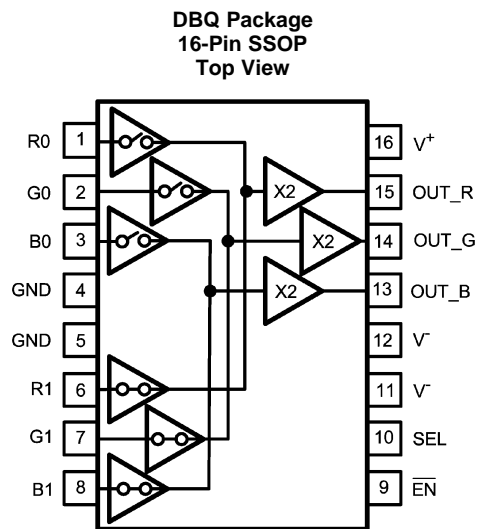
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (May 2013) から Revision G に変更	Page
• プレビュー版のウォーターマーク 削除	1
• 「製品情報」表、「ピン構成および機能」セクション、「ESD定格」表、「機能説明」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1
• Deleted bolding from Electrical Characteristics specifications, added temperature range to test conditions for clarification	5
• Changed <i>Overview</i> title from <i>General Information</i>	11
• Changed <i>Layout Considerations</i> title to <i>Layout Guidelines</i>	16

Revision E (April 2013) から Revision F に変更	Page
• Changed layout of National Semiconductor Data Sheet to TI format	16

5 Pin Configuration and Functions



Truth Table

SEL	$\overline{\text{EN}}$	OUT
0	0	CH 1
1	0	CH 0
X	1	Disable

6 Specifications

6.1 Absolute Maximum Ratings

 see ⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
Supply Voltage ($V^+ - V^-$)		13.2	V
$I_{OUT}^{(3)}$		130	mA
Input Voltage Range		$\pm(V_S)$	V
Maximum Junction Temperature ⁽⁴⁾		+150	°C
Storage temperature, T_{stg}	-65	+150	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations. See the [Power Dissipation](#) section for more details. A short circuit condition should be limited to 5 seconds or less.
- (4) Human Body Model, 1.5 k Ω in series with 100 pF. Machine Model 0 Ω in series with 200 pF.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
		Machine model (MM)	± 200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 see ⁽¹⁾

		MIN	NOM	MAX	UNIT
	Operating Temperature	-40		85	°C
	Supply Voltage Range	6		12	V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMH6572	UNIT
		DBQ (SSOP)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 ±5V Electrical Characteristics

 $V_S = \pm 5\text{ V}$ and $R_L = 100\ \Omega$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
FREQUENCY DOMAIN PERFORMANCE						
SSBW	–3 dB Bandwidth	$V_{OUT} = 0.25\ V_{PP}$		350		MHz
LSBW	–3 dB Bandwidth ⁽²⁾	$V_{OUT} = 2\ V_{PP}$	250	290		MHz
.1 dBBW	0.1 dB Bandwidth	$V_{OUT} = 0.25\ V_{PP}$		140		MHz
DG	Differential Gain	$R_L = 150\ \Omega$, $f = 4.43\ \text{MHz}$		0.02%		
DP	Differential Phase	$R_L = 150\ \Omega$, $f = 4.43\ \text{MHz}$		0.02		deg
TIME DOMAIN RESPONSE						
TRS	Channel to Channel Switching Time	Logic Transition to 90% Output		10		ns
	Enable and Disable Times	Logic Transition to 90% or 10% Output		11		ns
TRL	Rise and Fall Time	2-V Step		1.5		ns
TSS	Settling Time to 0.05%	2-V Step		17		ns
OS	Overshoot	4-V Step		5%		
SR	Slew Rate ⁽²⁾	4-V Step	1200	1400		V/ μs
DISTORTION						
HD2	2 nd Harmonic Distortion	$2\ V_{PP}$, 10 MHz		–78		dBc
HD3	3 rd Harmonic Distortion	$2\ V_{PP}$, 10 MHz		–75		dBc
IMD	3 rd Order Intermodulation Products	10 MHz, Two tones $2\ V_{PP}$ at Output		–80		dBc
EQUIVALENT INPUT NOISE						
VN	Voltage	>1 MHz, Input Referred		5		$nV\sqrt{\text{Hz}}$
ICN	Current	>1 MHz, Input Referred		5		$pA\sqrt{\text{Hz}}$
STATIC, DC PERFORMANCE						
GAIN	Voltage Gain			2.0		V/V
	Gain Error ⁽³⁾	No load, with respect to nominal gain of 2.00 V/V		±0.3%	±0.5%	
		No load, with respect to nominal gain of 2.00 V/V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		±0.3%	±0.7%	
	Gain Error	$R_L = 50\ \Omega$, with respect to nominal gain of 2.00 V/V		0.3%		
VIO	Output Offset Voltage ⁽³⁾	$V_{IN} = 0\ \text{V}$		1	±14	mV
		$V_{IN} = 0\ \text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		1	±17.5	
DVIO	Average Drift			27		$\mu\text{V}/^\circ\text{C}$
IBN	Input Bias Current ⁽³⁾⁽⁴⁾	$V_{IN} = 0\ \text{V}$		–1.4	±5.0	μA
		$V_{IN} = 0\ \text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		–1.4	±5.6	
DIBN	Average Drift			7		$\text{nA}/^\circ\text{C}$
PSRR	Power Supply Rejection Ratio ⁽³⁾	DC, Input referred	50	54		dB
		DC, Input referred, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	48	54		
ICC	Supply Current ⁽³⁾	No load	20	23	25	mA
		No load, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	20	23	28.5	
	Supply Current Disabled ⁽³⁾	No load		2.0	2.2	mA
		No load, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		2.0	2.3	
VIH	Logic High Threshold ⁽³⁾	Select and Enable Pins	2.0			V

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See the [Power Dissipation](#) section for information on temperature de-rating of this device. Minimum and maximum ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

(2) Parameters ensured by design.

(3) Parameters ensured by electrical testing at 25°C .

(4) Positive Value is current into device.

±5V Electrical Characteristics (continued)
 $V_S = \pm 5\text{ V}$ and $R_L = 100\ \Omega$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
VIL	Logic Low Threshold ⁽³⁾	Select and Enable Pins			0.8	V
IiL	Logic Pin Input Current Low ⁽⁴⁾	Logic Input = 0 V		-1	±5.0	µA
		Logic Input = 0 V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		-1	±15	
IiH	Logic Pin Input Current High ⁽⁴⁾	Logic Input = 2.0 V	112	150	200	µA
		Logic Input = 2.0 V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	100	150	210	
MISCELLANEOUS PERFORMANCE						
RF	Internal Feedback and Gain Set Resistor Values		650	800	940	Ω
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	620	800	1010	
RODIS	Disabled Output Resistance	Internal Feedback and Gain Set Resistors in Series to Ground	1.3	1.6	1.88	kΩ
RIN+	Input Resistance			100		kΩ
CIN	Input Capacitance			0.9		pF
ROUT	Output Resistance			0.26		Ω
VO	Output Voltage Range	No Load	±3.83	±3.9		V
		No Load, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	±3.80	±3.9		
VOL	Output Voltage Range	$R_L = 100\ \Omega$	±3.52	±3.53		V
		$R_L = 100\ \Omega$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	±3.5	±3.53		
CMIR	Input Voltage Range		±2	±2.5		V
IO	Linear Output Current ⁽³⁾⁽⁴⁾	$V_{IN} = 0\text{ V}$	+70	±80		mA
		$V_{IN} = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	40	±80		
ISC	Short Circuit Current ⁽⁵⁾	$V_{IN} = \pm 2\text{ V}$, Output Shorted to Ground		±230		mA
XTLK	Channel to Channel Crosstalk	$V_{IN} = 2\text{ V}_{PP}$ at 5 MHz		-90		dBc
XTLK	Channel to Channel Crosstalk	$V_{IN} = 2\text{ V}_{PP}$ at 100 MHz		-54		dBc
XTLK	All Hostile Crosstalk	In A, C, Out B, $V_{IN} = 2\text{ V}_{PP}$ at 5 MHz		-95		dBc

(5) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations. See the [Power Dissipation](#) section for more details. A short circuit condition should be limited to 5 seconds or less.

6.6 ±3.3V Electrical Characteristics

 $V_S = \pm 3.3\text{ V}$, $R_L = 100\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
FREQUENCY DOMAIN PERFORMANCE						
SSBW	-3 dB Bandwidth	$V_{OUT} = 0.25\ V_{PP}$		360		MHz
LSBW	-3 dB Bandwidth	$V_{OUT} = 2.0\ V_{PP}$		270		MHz
0.1 dBBW	0.1 dB Bandwidth	$V_{OUT} = 0.5\ V_{PP}$		80		MHz
GFP	Peaking	DC to 200 MHz		0.3		dB
DG	Differential Gain	$R_L = 150\ \Omega$, $f = 4.43\ \text{MHz}$		0.02%		
DP	Differential Phase	$R_L = 150\ \Omega$, $f = 4.43\ \text{MHz}$		0.03		deg
TIME DOMAIN RESPONSE						
TRL	Rise and Fall Time	2-V Step		2.0		ns
TSS	Settling Time to 0.05%	2-V Step		15		ns
OS	Overshoot	2-V Step		5%		
SR	Slew Rate	2-V Step		1000		V/ μs
DISTORTION						
HD2	2 nd Harmonic Distortion	2 V_{PP} , 10 MHz		-70		dBc
HD3	3 rd Harmonic Distortion	2 V_{PP} , 10 MHz		-74		dBc
IMD	3 rd Order Intermodulation Products	10 MHz, Two tones 2 V_{PP} at Output		-79		dBc
STATIC, DC PERFORMANCE						
GAIN	Voltage Gain			2.0		V/V
VIO	Output Offset Voltage	$V_{IN} = 0\ \text{V}$		1		mV
DVIO	Average Drift			36		$\mu\text{V}/^\circ\text{C}$
IBN	Input Bias Current ⁽²⁾	$V_{IN} = 0\ \text{V}$		2		μA
DIBN	Average Drift			24		nA/ $^\circ\text{C}$
PSRR	Power Supply Rejection Ratio	DC, Input Referred		54		dB
ICC	Supply Current	$R_L = \infty$		20		mA
VIH	Logic High Threshold	Select and Enable Pins			1.3	V
VIL	Logic Low Threshold	Select and Enable Pins	0.4			V
MISCELLANEOUS PERFORMANCE						
RIN+	Input Resistance			100		k Ω
CIN	Input Capacitance			0.9		pF
ROUT	Output Resistance			0.27		Ω
VO	Output Voltage Range	No Load		± 2.5		V
VOL		$R_L = 100\ \Omega$		± 2.2		V
CMIR	Input Voltage Range			± 1.2		V
IO	Linear Output Current	$V_{IN} = 0\ \text{V}$		± 60		mA
ISC	Short Circuit Current	$V_{IN} = \pm 1\ \text{V}$, Output Shorted to Ground		± 150		mA
XTLK	Channel to Channel Crosstalk	5 MHz		-90		dBc

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See the [Power Dissipation](#) section for information on temperature de-rating of this device. Minimum and maximum ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

(2) Positive Value is current into device.

6.7 Typical Characteristics

$V_S = \pm 5\text{ V}$ and $R_L = 100\ \Omega$ (unless otherwise noted)

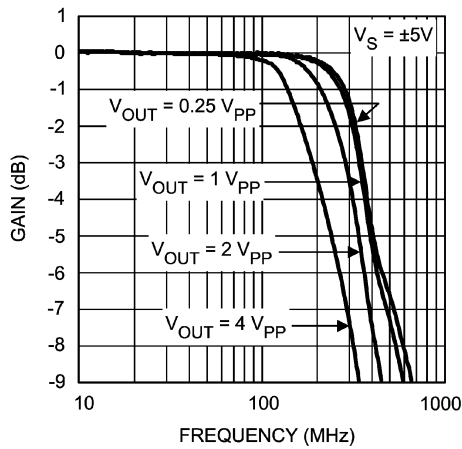


Figure 1. Frequency Response vs V_{OUT}

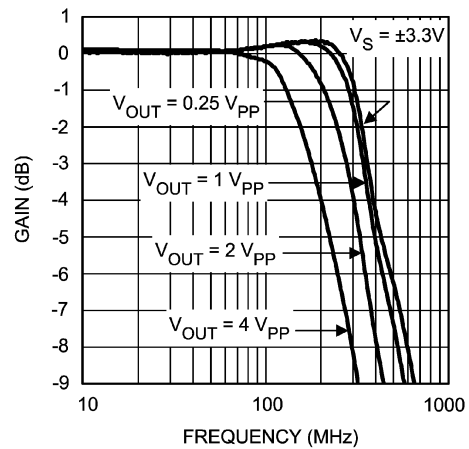


Figure 2. Frequency Response vs V_{OUT}

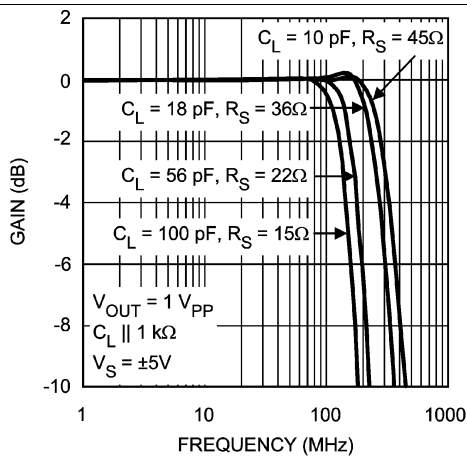


Figure 3. Frequency Response vs Capacitive Load

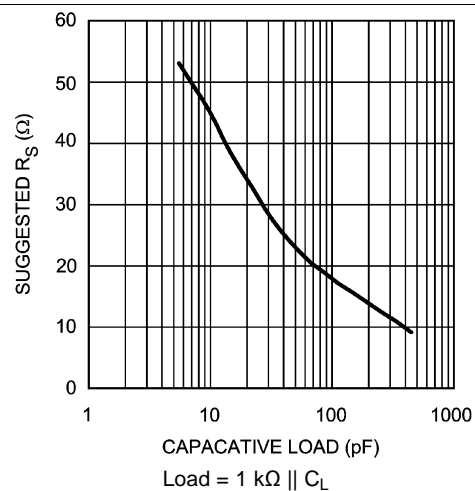


Figure 4. Suggested R_S vs Capacitive Load

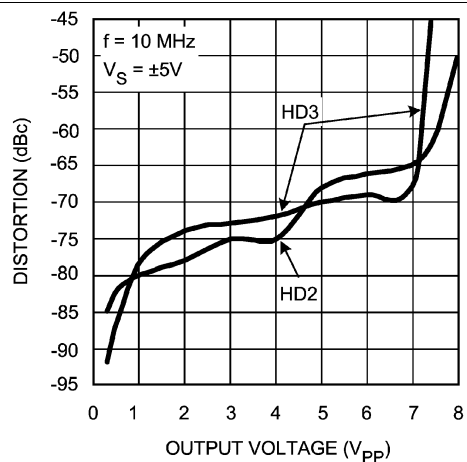


Figure 5. Harmonic Distortion vs Output Voltage

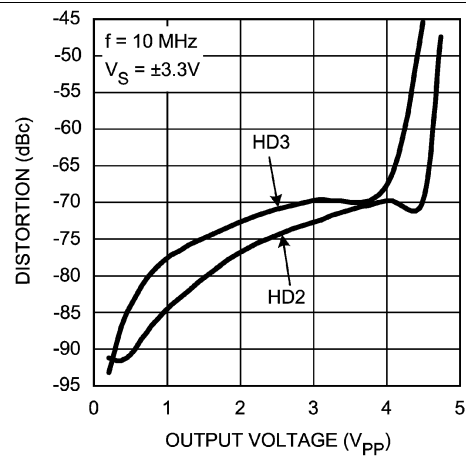


Figure 6. Harmonic Distortion vs Output Voltage

Typical Characteristics (continued)

$V_S = \pm 5\text{ V}$ and $R_L = 100\ \Omega$ (unless otherwise noted)

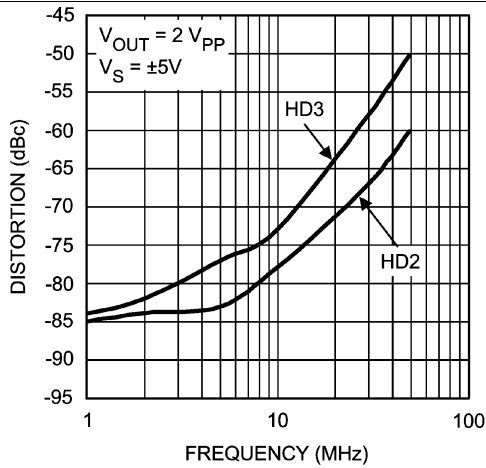


Figure 7. Harmonic Distortion vs Frequency

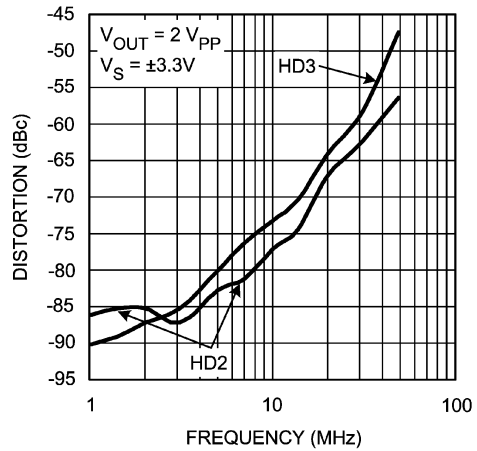


Figure 8. Harmonic Distortion vs Frequency

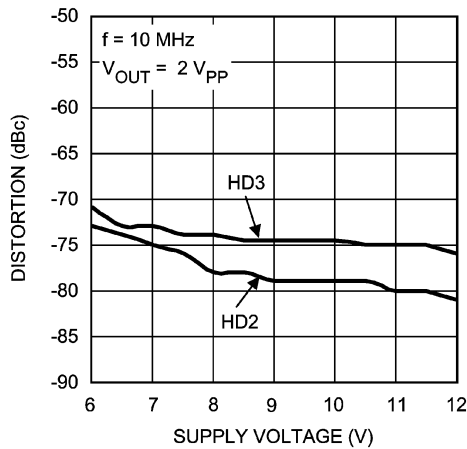


Figure 9. Harmonic Distortion vs Supply Voltage

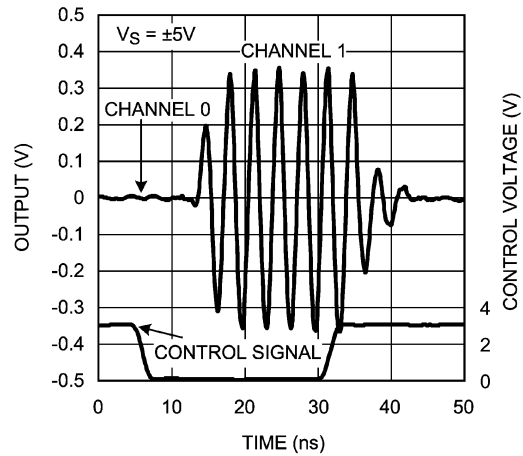


Figure 10. Channel Switching Time

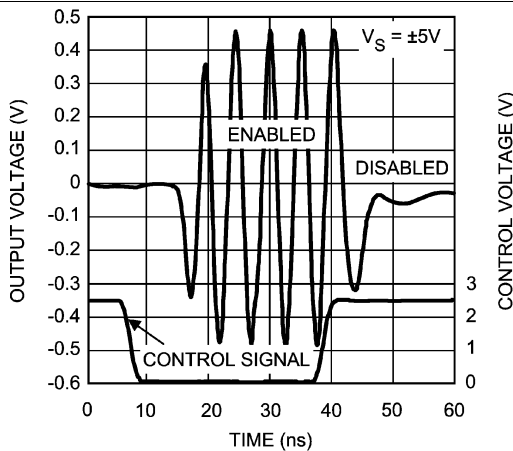


Figure 11. Disable Time

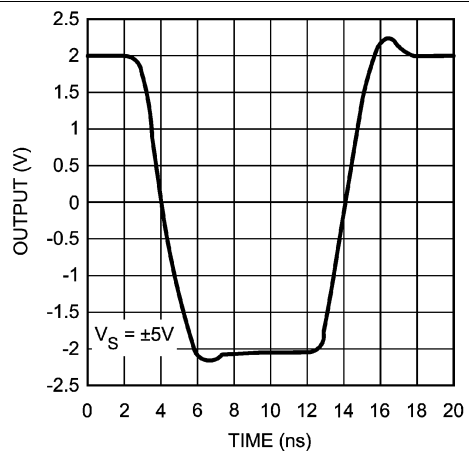


Figure 12. Pulse Response

Typical Characteristics (continued)

$V_S = \pm 5\text{ V}$ and $R_L = 100\ \Omega$ (unless otherwise noted)

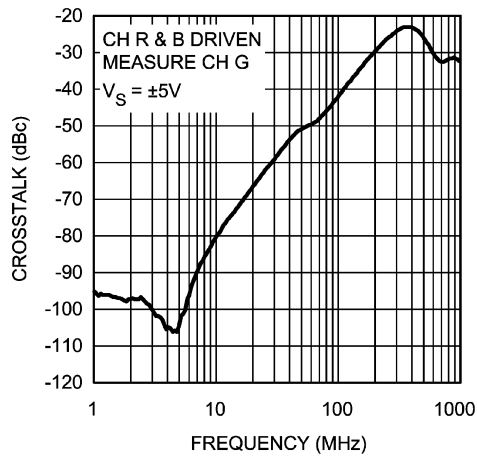


Figure 13. Crosstalk

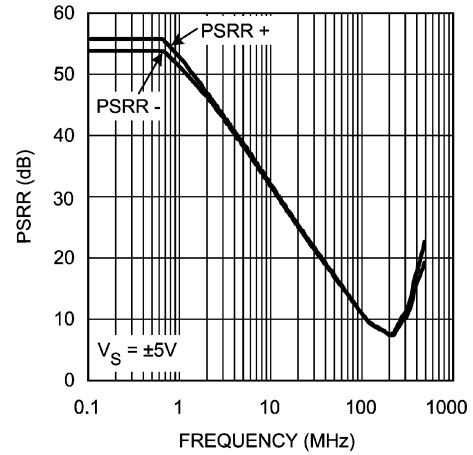


Figure 14. PSRR

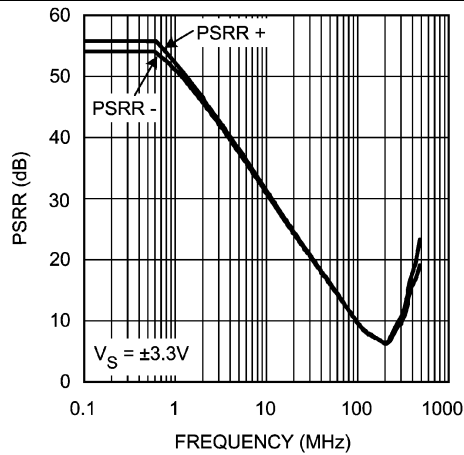


Figure 15. PSRR

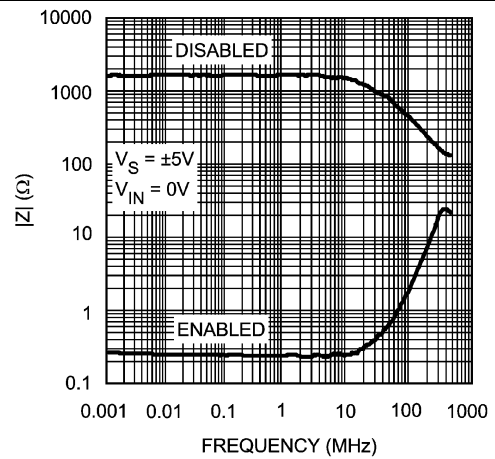


Figure 16. Closed-Loop Output Impedance

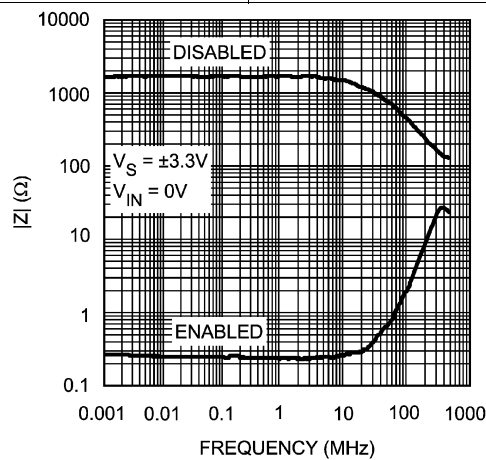


Figure 17. Closed-Loop Output Impedance

7 Detailed Description

7.1 Overview

The LMH6572 is a high-speed triple 2:1 analog multiplexer, optimized for very high speed and low distortion. With a fixed gain of 2 and excellent AC performance, the LMH6572 is ideally suited for switching high resolution, presentation grade video signals. The LMH6572 has no internal ground reference. Single or split supply configurations are both possible. The LMH6572 features very high speed channel switching and disable times. When disabled the LMH6572 output is high impedance, making multiplexer expansion possible by combining multiple devices.

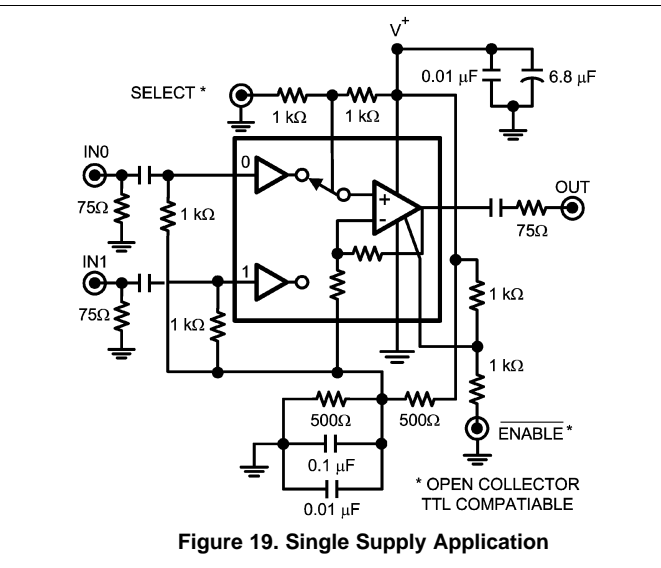
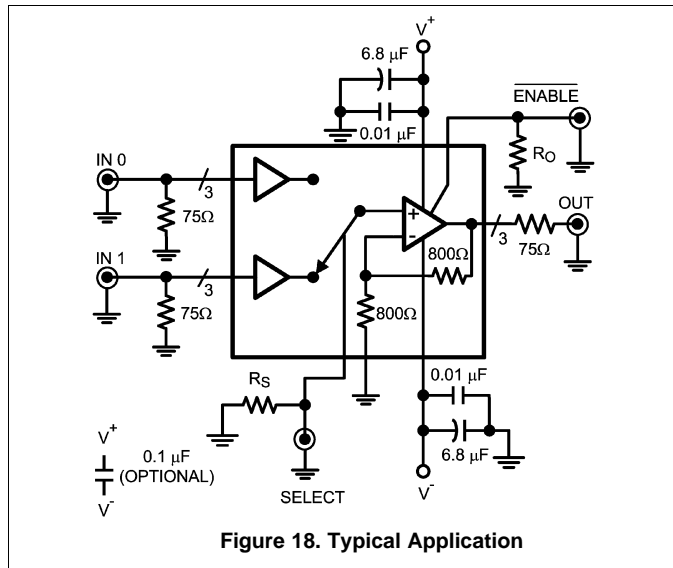
7.2 Feature Description

7.2.1 Single Supply Operation

The LMH6572 uses mid-supply referenced circuits for the select and disable pins. In order to use the LMH6572 in single supply configuration, it is necessary to use a circuit similar to [Figure 19](#). In this configuration the logical inputs are compatible with high breakdown open collector TTL, or open drain CMOS logic. In addition, the default logic state is reversed since there is a pull-up resistor on those pins. Single supply operation also requires the input to be biased to within the common mode input range of roughly $\pm 2V$ from the mid-supply point.

7.2.2 Video Performance

The LMH6572 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. [Figure 18](#) shows a typical configuration for driving a 75- Ω cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.



7.2.3 Gain Accuracy

The gain accuracy of the LMH6572 is accurate to $\pm 0.5\%$ (0.3% typical) and stable over temperature. The internal gain setting resistors, RF and RG, match very well; however, over process and temperature their absolute value will change.

Feature Description (continued)

7.2.4 Expanding the Multiplexer

It is possible to build higher density multiplexers by paralleling several LMH6572s. Figure 20 shows a 4:1 RGB MUX using two LMH6572s:

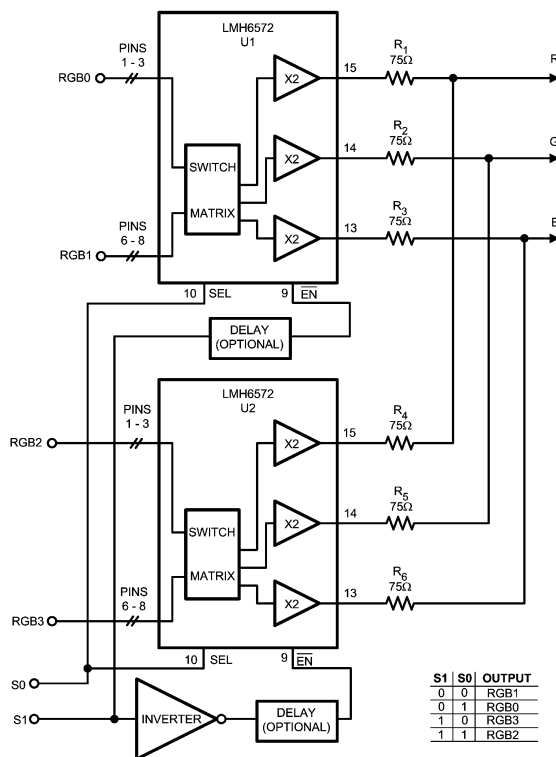


Figure 20. RGB MUX Using Two LMH6572's

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added prior to the $\overline{\text{ENABLE}}(\text{EN})$ pin of each device, as shown. Figure 21 shows one possible approach to this delay circuit. The delay circuit shown will delay $\overline{\text{ENABLE}}$'s H to L transitions (R_1 and C_1 decay) but will not delay its L to H transition.

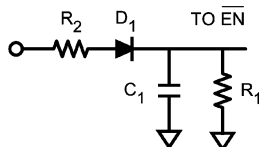


Figure 21. Delay Circuit Implementation

R_2 should be kept small compared to R_1 in order to not reduce the $\overline{\text{ENABLE}}$ voltage and to produce little or no delay to the $\overline{\text{ENABLE}}$ L to H transition.

With the $\overline{\text{ENABLE}}$ pin putting the output stage into a high impedance state, several LMH6572's can be tied together to form a larger input MUX. However, there is a slight loading effect on the active output caused by the off-channel feedback and gain set resistors, as shown in Figure 21. Figure 22 is assuming there are four LMH6572 devices tied together to form a triple 8:1 MUX. With the internal resistors valued at approximately 800 Ω , the gain error is about -0.57 dB, or about -6%.

Feature Description (continued)

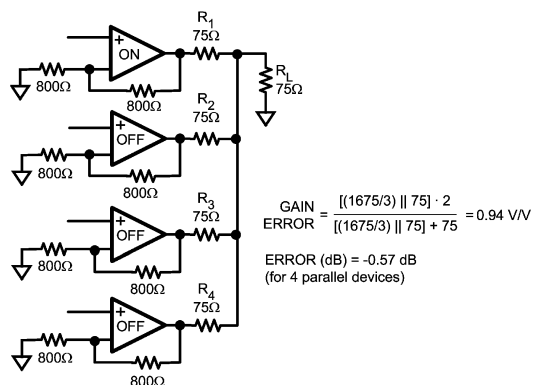


Figure 22. Multiplexer Input Expansion by Combining Outputs

An alternate approach would be to tie the outputs directly together and let all devices share a common back termination resistor in order to alleviate the gain error issue above.

The drawback in this case is the increased capacitive load presented to the output of each LMH6572 due to the offstate capacitance of the LMH6572.

Feature Description (continued)

7.2.5 Other Applications

The LMH6572 may be utilized in systems that involve a single RGB channel as well whenever there is a need to switch between different “flavors” of a single RGB input.

Here are some examples:

1. RGB positive polarity, negative polarity switch
2. RGB full resolution, high-pass filter switch

In each of these applications, the same RGB input occupies one set of inputs to the LMH6572 and the other “flavor” would be tied to the other input set.

7.2.5.1 Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor. Figure 23 shows the use of a series output resistor, R_{OUT} , to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 24 gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

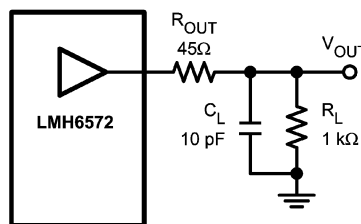
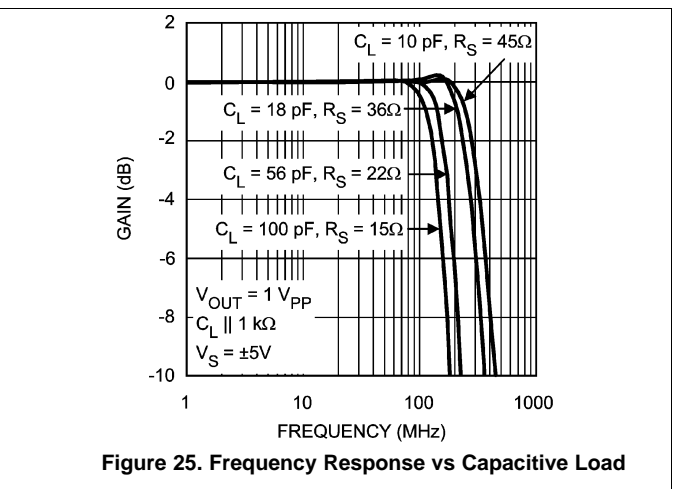
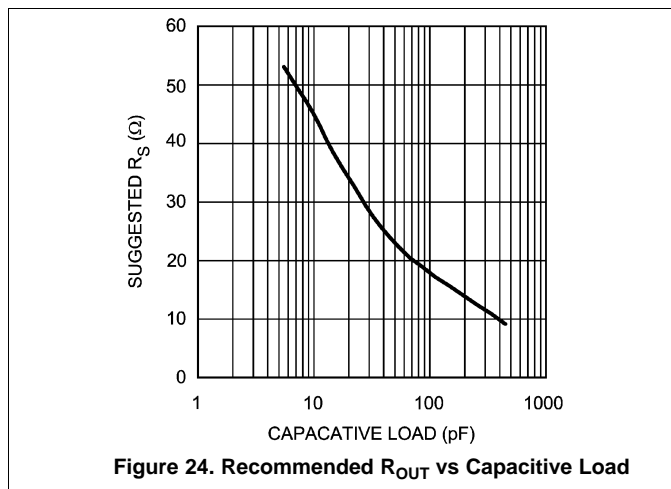


Figure 23. Decoupling Capacitive Loads



8 Power Supply Recommendations

8.1 Power Dissipation

The LMH6572 is optimized for maximum speed and performance in the small form factor of the standard SSOP package. To achieve its high level of performance, the LMH6572 consumes 23 mA of quiescent current, which cannot be neglected when considering the total package power dissipation limit. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6572:

1. Calculate the quiescent (no-load) power:

$$P_{AMP} = I_{CC} \cdot (V_S)$$

where

- $V_S = V^+ - V^-$ (1)

2. Calculate the RMS power dissipated in the output stage:

$$P_D (\text{rms}) = \text{rms} [(V_S - V_{OUT}) \cdot I_{OUT}]$$

where

- V_{OUT} and I_{OUT} are the voltage across and the current through the external load
- V_S is the total supply voltage (2)

3. Calculate the total RMS power:

$$P_T = P_{AMP} + P_D \quad (3)$$

The maximum power that the LMH6572 package can dissipate at a given temperature can be derived with the following equation:

$$P_{MAX} = (150^\circ\text{C} - T_{AMB}) / \theta_{JA}$$

where

- T_{AMB} = Ambient temperature ($^\circ\text{C}$)
- θ_{JA} = Thermal resistance, from junction to ambient, for a given package ($^\circ\text{C}/\text{W}$)
- For the SSOP package θ_{JA} is 125 $^\circ\text{C}/\text{W}$ (4)

8.2 ESD Protection

The LMH6572 is protected against electrostatic discharge (ESD) on all pins. The LMH6572 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6572 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

9 Layout

9.1 Layout Guidelines

Whenever questions about layout arise, use the LMH730151 evaluation board as a guide. To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device; however, the smaller ceramic capacitors should be placed as close to the device as possible. In [Figure 18](#) and [Figure 19](#), the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01 μF and 0.1 μF ceramic capacitors for each supply bypass.

9.1.1 Evaluation Boards

Texas Instruments provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with these boards.

DEVICE	PACKAGE	EVALUATION BOARD PART NUMBER
LMH6572	SSOP	LMH730151

An evaluation board can be shipped when a device sample request is placed with Texas Instruments.

10 デバイスおよびドキュメントのサポート

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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10.5 Glossary



SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6572MQ/NOPB	ACTIVE	SSOP	DBQ	16	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LH65 72MQ	
LMH6572MQX/NOPB	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LH65 72MQ	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6572MQX/NOPB	SSOP	DBQ	16	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

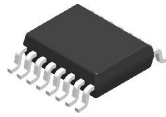

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6572MQX/NOPB	SSOP	DBQ	16	2500	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMH6572MQ/NOPB	DBQ	SSOP	16	95	495	8	4064	3.05

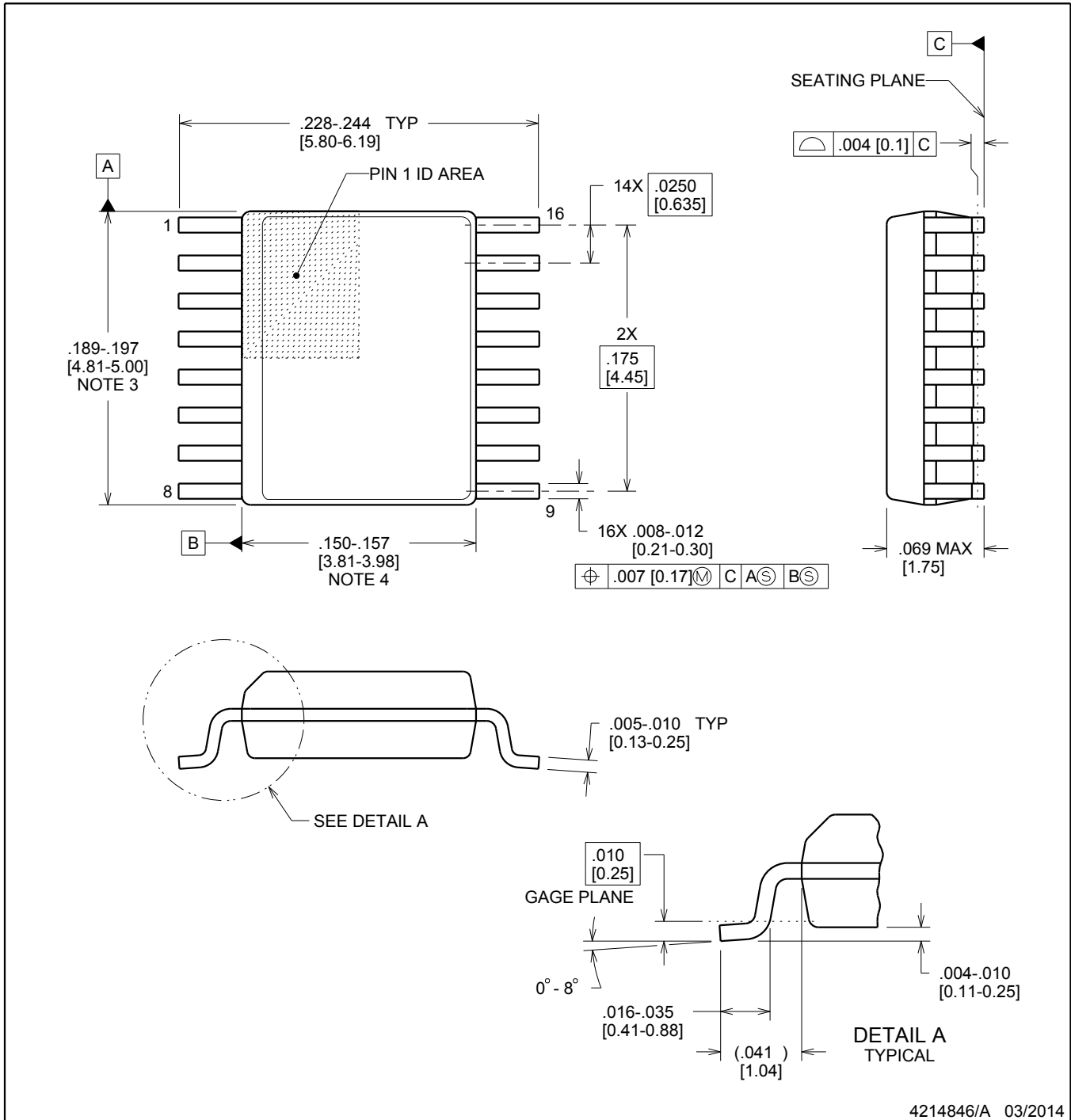


DBQ0016A

PACKAGE OUTLINE

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

NOTES:

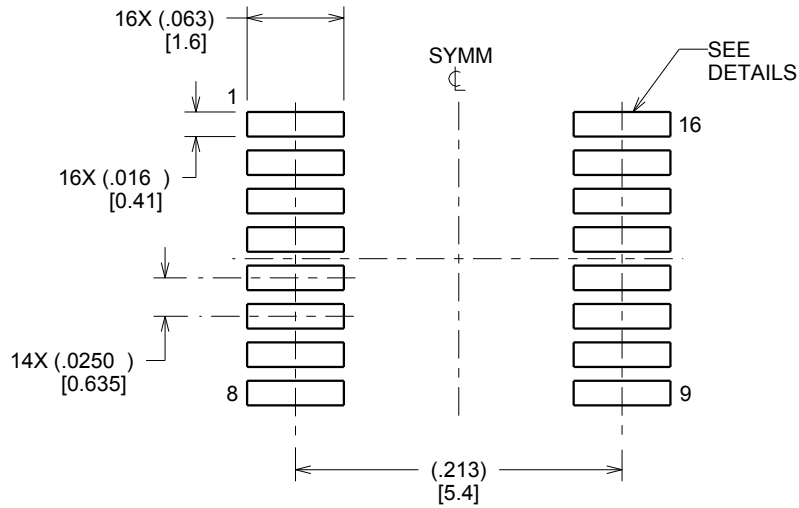
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

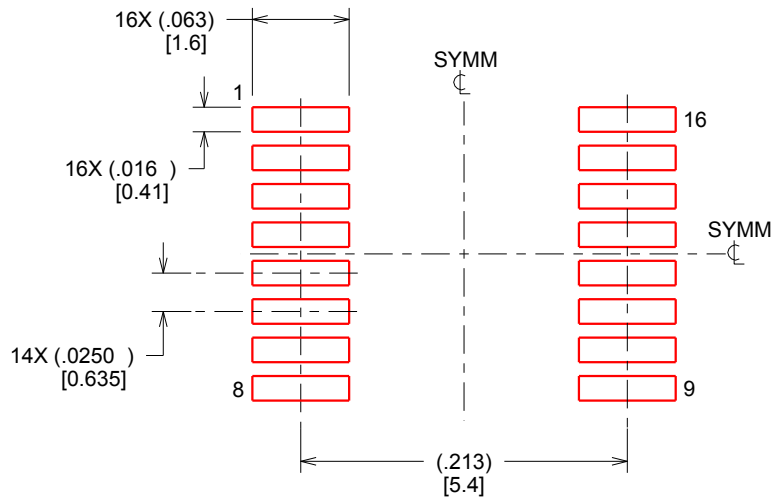
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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