TEXAS INSTRUMENTS
LMR36500
JAJSME4 – NOVEMBER 2023

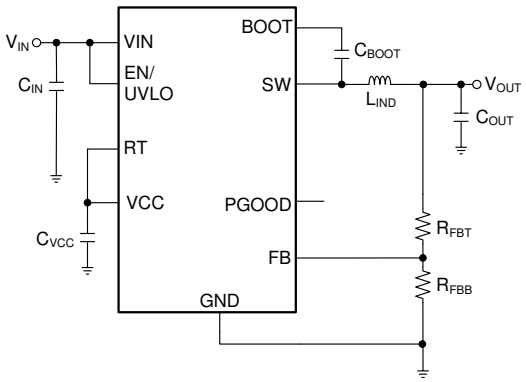
LMR36500 3V～65V、50-mA ワイド V_{IN} 同期整流降圧コンバータ

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 堅牢な産業用途向けの設計
  - 接合部温度範囲：-40℃～+150℃
  - 最大 70V の過渡入力に対応
  - 広い入力電圧範囲：3.0V (立ち下がりスレッショルド)～65V
  - スイッチ・ノードのリンギングを最小化し、EMI を低減
  - 可変および固定出力の 3.3V および 5V 電圧オプションが利用可能
- スケーラブルな産業用電源に対応した設計：
  - LMR36503 (65V、300mA) および LMR36506 (65V、600mA) とピン互換
  - 可変スイッチング周波数：200kHz～2.2MHz (RT ピン・バリアントの場合)
- 設計のサイズとコストを最小化：
  - 超小型、2mm × 2mm HotRod™ パッケージ
- 負荷範囲全体にわたって高効率かつ低消費電力：
  - 1MHz で 80% を上回るピーク効率 (3.3V V_{OUT})

2 アプリケーション

- ファクトリ・オートメーション：フィールド・トランスミッタとプロセス・センサ
- ビル・オートメーション：HVAC と防火に関する通知と検出器
- 家電製品：ガーデニング・ツールと電動工具
- ポータブル・エレクトロニクス：ヘッドホンとイヤホン



概略回路図

3 概要

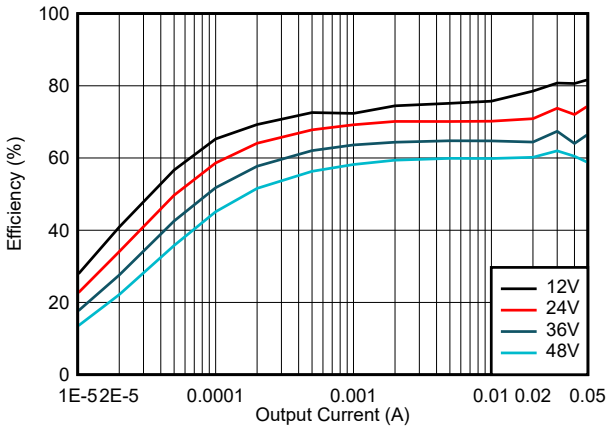
LMR36500 は、業界最小の 65V、50mA 同期整流降圧 DC/DC コンバータで、4mm² HotRod パッケージで供給されます。この使いやすいコンバータは、最大 70V の入力過渡電圧に対応でき、非常に優れた EMI 性能を実現するとともに、固定 3.3V、5V の他に可変出力電圧にも対応しています。

LMR36500 は、ピーク電流モード制御アーキテクチャと内部補償により、最小の出力容量で安定した動作を維持します。LMR36500 は、RT ピンからグランドへの抵抗を適切に選択することで、200kHz～2.2MHz の広い範囲の中から、目的の任意のスイッチング周波数で動作するよう外部からプログラムできます。高精度の EN/UVLO 機能により、スタートアップおよびシャットダウン中もデバイスを精密に制御できます。PGOOD フラグは、内蔵グリッチ・フィルタと遅延付き解除によってシステムの実際の状態を示すため、外部電圧のスーパーバイザは不要です。LMR36500 は設計サイズが小さく、豊富な機能セットがあるため、広範な産業用アプリケーションを簡単に実装できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
LMR36500	RPE (VQFN-HR、9)	2.00mm × 2.00mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



効率と出力電流の関係
V_{OUT} = 3.3V (固定)、1MHz、自動

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4 Device Comparison Table

ORDERABLE PART NUMBER (1)	RATED CURRENT	OUTPUT VOLTAGE	EXTERNAL SYNC	F_{SW}	SPREAD SPECTRUM
LMR36500P3RPE	50 mA	Fixed 3.3-V / Adjustable	No (Default PFM at light load)	Adjustable with RT resistor	No
LMR36500P5RPE(2)	50 mA	Fixed 5-V / Adjustable	No (Default PFM at light load)	Adjustable with RT resistor	No
LMR36500F3RPE	50 mA	Fixed 3.3-V / Adjustable	No (Default FPWM at light load)	Adjustable with RT resistor	No
LMR36500F5RPE(2)	50 mA	Fixed 5-V / Adjustable	No (Default FPWM at light load)	Adjustable with RT resistor	No

(1) For more information on device orderable part numbers, see セクション 9.1.1. Contact TI for details and availability of other device options.
(2) Preview information (not Production Data).

5 Pin Configuration and Functions

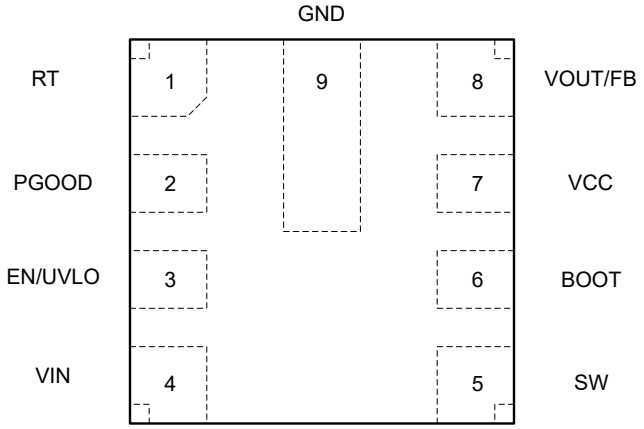


図 5-1. 9-Pin (2 mm × 2 mm) VQFN-HR RPE Package (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	RT	A	The switching frequency can be adjusted from 200 kHz to 2.2 MHz by selecting the appropriate valued resistor from this pin to GND. See セクション 7.3.2 for more details. *Do not float this pin.*
2	PGOOD	A	Open-drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. This pin goes low when EN = low. This pin can be open or grounded when not used.
3	EN/UVLO	A	Enable input to regulator. High = ON, Low = OFF. Can be connected directly to VIN. *Do not float this pin.*
4	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and GND.
5	SW	P	Regulator switch node. Connect to power inductor.
6	BOOT	P	Bootstrap supply voltage for internal high-side driver. Connect a high-quality 0.1-µF capacitor from this pin to the SW pin.
7	VCC	P	Internal LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
8	VOUT/FB	A	Fixed output options and adjustable output options are available with the VOUT/FB pin variant. Connect to the output voltage node for fixed V_{OUT}. Connect to tap point of feedback voltage divider for adjustable VOUT. See *Output Voltage Selection* for how to select feedback resistor divider values. Check *Device Comparison Table* for more details. *Do not float this pin.*
9	GND	G	Power ground terminal. Connect to system ground. Connect to C_{IN} with short, wide traces.
A = Analog, P = Power, G = Ground			

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (1)

PARAMETER		MIN	MAX	UNIT
Voltage	VIN to GND	–0.3	70	V
	EN to GND	–0.3	70	V
	SW to GND	–0.3	70.3	V
	PGOOD to GND	0	20	V
	VOUT/FB to GND	–0.3	16	V
	BOOT to SW	–0.3	5.5	V
	VCC to GND	–0.3	5.5	V
	RT to GND (RT variant)	–0.3	5.5	V
	MODE/SYNC to GND (MODE/SYNC variant)	–0.3	5.5	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD (Commercial) Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted) (1) (2)

		MIN	TYP	MAX	UNIT
Input voltage	Input voltage range after start-up	3.6		65	V
Output voltage	Output voltage range for adjustable output variants	1		16	V
Output current	LMR36500 load current range (3)	0		50	mA
Frequency setting	Selectable frequency range with RT (RT variant only)	0.2		2.2	MHz
Temperature	T_J juction temperature	–40		150	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics table.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
(3) Maximum continuous DC current can be derated when operating with high switching frequency or high ambient temperature. See Application section for details.

6.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application.

THERMAL METRIC (1)		LMR36500 VQFN (RPE) 9 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	85.7	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (LMR36500EVM)	60	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	27.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. This value was calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. It does not represent the performance obtained in an actual application. For design information see the Maximum Ambient Temperature section.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN_R}	Minimum operating input voltage (rising)	Rising threshold		3.4	3.55	V
V_{IN_F}	Minimum operating input voltage (falling)	Once operating; Falling threshold	2.45	2.7		V
I_{SD_13p5}	Shutdown quiescent current; measured at VIN pin (2)	V_{EN} = 0 V; V_{IN} = 13.5 V		0.5	1.1	µA
I_{SD_24p0}	Shutdown quiescent current; measured at VIN pin (2)	V_{EN} = 0 V; V_{IN} = 24 V		1	1.6	µA
$I_{Q\_13p5\_Fixed}$	Non-switching input current; measured at VIN pin (2) (4)	V_{IN} = V_{EN} = 13.5 V; $V_{OUT/FB}$ = 5.25 V, V_{RT} = 0 V; Fixed output	0.25	0.672	1.05	µA
$I_{Q\_13p5\_Adj}$	Non-switching input current; measured at VIN pin (2) (4)	V_{IN} = V_{EN} = 13.5 V; V_{FB} = 1.05 V, V_{RT} = 0 V; Adjustable output	14	17	23.1	µA
$I_{Q\_24p0\_Fixed}$	Non-switching input current; measured at VIN pin (2) (4)	V_{IN} = V_{EN} = 24 V; $V_{OUT/FB}$ = 5.25 V, V_{RT} = 0 V; Fixed output	0.8	1.2	1.7	µA
$I_{Q\_24p0\_Adj}$	Non-switching input current; measured at VIN pin (2) (4)	V_{IN} = V_{EN} = 24 V; V_{FB} = 1.05 V, V_{RT} = 0 V; Adjustable output	14	18	22	µA
I_{B_13p5}	Current into VOUT/FB pin (not switching) (2) (4)	V_{IN} = 13.5 V, $V_{OUT/FB}$ = 5.25 V, V_{RT} = 0 V; Fixed output	14	17	22	µA
I_{B_24p0}	Current into VOUT/FB pin (not switching) (2) (4)	V_{IN} = 24 V, $V_{OUT/FB}$ = 5.25 V, V_{RT} = 0 V; Fixed output	14	18	22	µA
ENABLE (EN PIN)						
$V_{EN\text{-}WAKE}$	Enable wake-up threshold		0.4			V
$V_{EN\text{-}VOUT}$	Precision enable high level		1.16	1.263	1.36	V
$V_{EN\text{-}HYST}$	Enable threshold hysteresis		0.285	0.35	0.425	V
$I_{LKG\text{-}EN}$	Enable input leakage current	V_{EN} = 3.3 V		0.2	8	nA

6.5 Electrical Characteristics (続き)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL LDO						
V_{CC}	Internal VCC voltage	3.6 V ≤ V_{IN} ≤ 65 V; Adjustable output option	3.2	3.3	3.4	V
I_{CC}	Bias regulator current limit			50	120	mA
$V_{CC-UVLO}$	Internal VCC undervoltage lockout	VCC rising undervoltage threshold	3	3.3	3.65	V
$V_{CC-UVLO-HYST}$	Internal VCC undervoltage lockout hysteresis	Hysteresis below $V_{CC-UVLO}$	0.4	0.8	1.2	V
CURRENT LIMITS						
$I_{SC-50mA}$	Short circuit high side current limit (3)	50 mA version	65	85	105	mA
$I_{LS-LIMIT-50mA}$	Low side current limit (3)	50 mA version	45	60	70	mA
$I_{PEAK-MIN-50mA}$	Minimum peak inductor current limit (3)	PFM Operation, 50 mA version; Duty Cycle = 0%	30	40	50	mA
I_{ZC}	Zero cross current (3)	Auto mode	0	2.5	5	mA
$I_{L-NEG-50mA}$	Sink current limit (negative) (3)	FPWM mode	-73	-60	-47	mA
POWER GOOD						
PG-OV	PGOOD upper threshold - rising	% of FB (Adjustable output) or % of VOUT/FB (Fixed output)	106	107	110	%
PG-UV	PGOOD lower threshold - falling	% of FB (Adjustable output) or % of VOUT/FB (Fixed output)	93	94	96.5	%
PG-HYS	PGOOD hysteresis - rising/falling	% of FB (Adjustable output) or % of VOUT/FB (Fixed output)	0.8	1.2	1.8	%
$V_{PG-VALID}$	Minimum input voltage for proper PG function		0.7	0.9	2	V
$R_{PG-EN5p0}$	PGOOD pulldown resistance	V_{EN} = 5.0 V, 1 mA pullup current	20	40	70	Ω
R_{PG-EN0}	PGOOD pulldown resistance	V_{EN} = 0 V, 1 mA pullup current	15	24	46	Ω
MOSFETS						
$R_{DSON-HS}$	High-side MOSFET on-resistance	Load = 50 mA (LMR36500 variant)		5		Ω
$R_{DSON-LS}$	Low-side MOSFET on-resistance	Load = 50 mA (LMR36500 variant)		3.5		Ω
$V_{BOOT-UVLO}$	BOOT - SW UVLO threshold		2.14	2.3	2.42	V
VOLTAGE FEEDBACK (VOUT/FB PIN)						
V_{OUT}	Output Voltage Accuracy for fixed V_{OUT}	V_{OUT} = 3.3-V, V_{IN} = 3.6 V to 65 V, FPWM	3.24	3.3	3.34	V
V_{OUT}	Output Voltage Accuracy for fixed V_{OUT} (4)	V_{OUT} = 5-V, V_{IN} = 5.5 V to 65 V, FPWM	4.93	5	5.08	V
V_{REF}	Internal reference voltage	V_{IN} = 3.6 V to 65 V, FPWM mode	0.985	1	1.01	V
I_{FB}	FB input current	Adjustable output, FB = 1 V		1	30	nA
SOFT START						
t_{SS}	Time from first SW pulse to V_{FB} at 90% of V_{REF}	V_{IN} ≥ 3.6 V	1.95	2.58	3.2	ms
POWER GOOD						
t_{RESET_FILTER}	Glitch filter time constant for PG function		15	25	40	µs
t_{PGOOD_ACT}	Delay time to PG high signal		1.7	1.956	2.16	ms
PWM LIMITS (SW)						
t_{ON-MIN}	Minimum switch on-time	V_{IN} = 24 V, I_{OUT} = 50 mA	35	60	85	ns
OSCILLATOR (RT)						

6.5 Electrical Characteristics (続き)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC_2p2MHz}	Internal oscillator frequency	RT = GND	2.1	2.2	2.3	MHz
f_{OSC_1p0MHz}	Internal oscillator frequency	RT = VCC	0.93	1	1.05	MHz
f_{ADJ_400kHz}	Accuracy of external frequency, 400 kHz	RT = 39.2 kΩ	0.34	0.4	0.46	MHz

(1) MIN and MAX limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) The current limit values in this table are tested, open loop, in production.
(4) Preview.

6.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 150°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STANDBY CURRENT						
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 13.5 V, $V_{OUT/FB}$ = 3.3 V, I_{OUT} = 0 A, PFM mode		6.5		µA
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 24 V, $V_{OUT/FB}$ = 3.3 V, I_{OUT} = 0 A, PFM mode		4		µA
OUTPUT VOLTAGE ACCURACY (VOUT/FB)						
$V_{OUT\_3p3V\_ACC}$	V_{OUT} = 3.3-V, V_{IN} = 3.6 V to 65 V, I_{OUT} = 0 A to full load (2)	FPWM mode	–1.5		1.5	%
$V_{OUT\_3p3V\_ACC}$	V_{OUT} = 3.3-V, V_{IN} = 3.6 V to 65 V, I_{OUT} = 0 A to full load (2)	AUTO mode	–1.5		2.5	%
$V_{OUT\_5p0V\_ACC}$	V_{OUT} = 5-V, V_{IN} = 5.5 V to 65 V, I_{OUT} = 0 A to full load (2) (3)	FPWM mode	–1.5		1.5	%
$V_{OUT\_5p0V\_ACC}$	V_{OUT} = 5-V, V_{IN} = 5.5 V to 65 V, I_{OUT} = 0 A to full load (2) (3)	AUTO mode	–1.5		2.5	%
PWM LIMITS (SW)						
$t_{OFF-MIN}$	Minimum switch off-time	I_{OUT} = 50 mA		70		ns
t_{ON-MAX}	Maximum switch on-time	I_{OUT} = 50 mA		4.4		µs
F_{MIN}	Minimum switching frequency	Drop-out		223		kHz
D_{MAX}	Maximum switch duty cycle (1)	Drop-out		98%		
THERMAL SHUTDOWN						
T_{SD-R}	Thermal shutdown rising	Shutdown threshold	158	168	180	°C
T_{SD-HYS}	Thermal shutdown hysteresis		8	10	15	°C

(1) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: f_{MIN} = 1 / (t_{ON-MAX} + $T_{OFF-MIN}$). D_{MAX} = (t_{ON-MAX}) / (t_{ON-MAX} + $t_{OFF-MIN}$).
(2) Deviation is with respect to V_{IN} = 13.5 V.
(3) Preview.

6.7 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_A = 25°C, V_{IN} = 13.5 V.

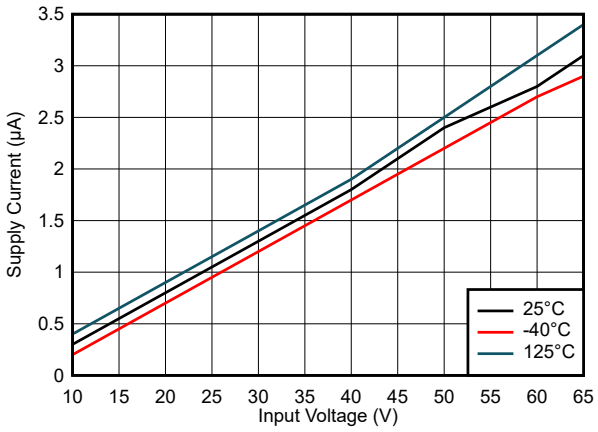
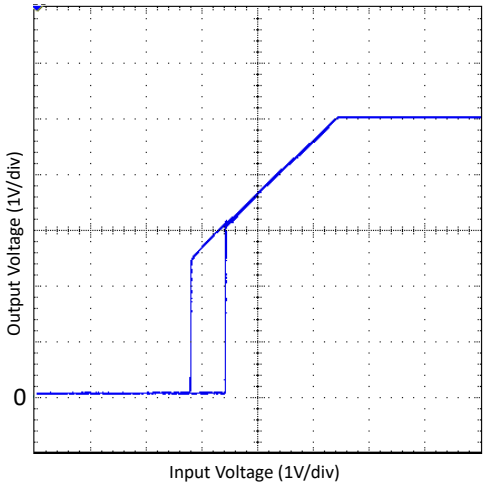
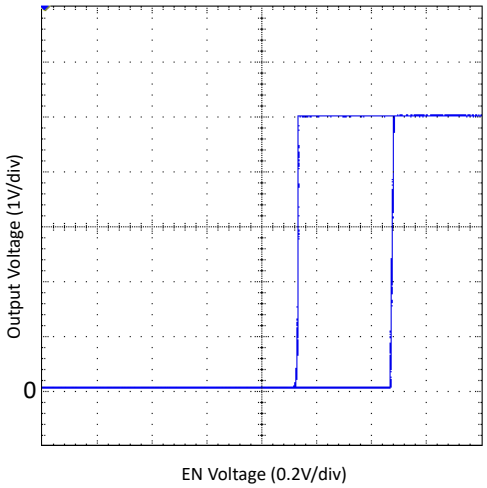


図 6-1. Shutdown Supply Current: EN = 0 V



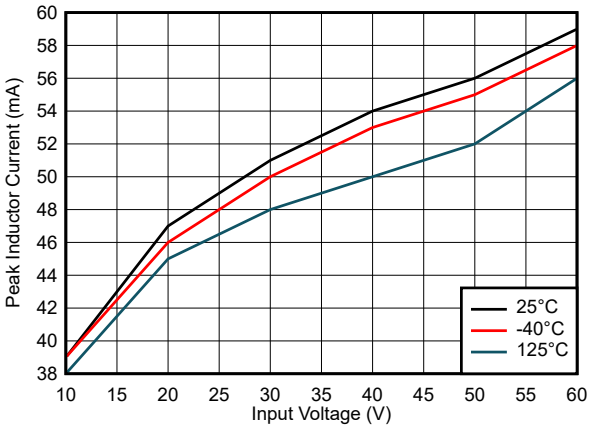
LMR36500F5 V_{IN} = 12 V Fixed I_{OUT} = 50 mA

図 6-2. Input Voltage UVLO Thresholds



LMR36500F5 V_{IN} = 12 V Fixed I_{OUT} = 50 mA

図 6-3. Precision Enable Thresholds



LMR36500P3 V_{OUT} = 3.3 V Fixed I_{OUT} = 0 mA
L = 220 µH

図 6-4. IPEAK-MIN

7 Detailed Description

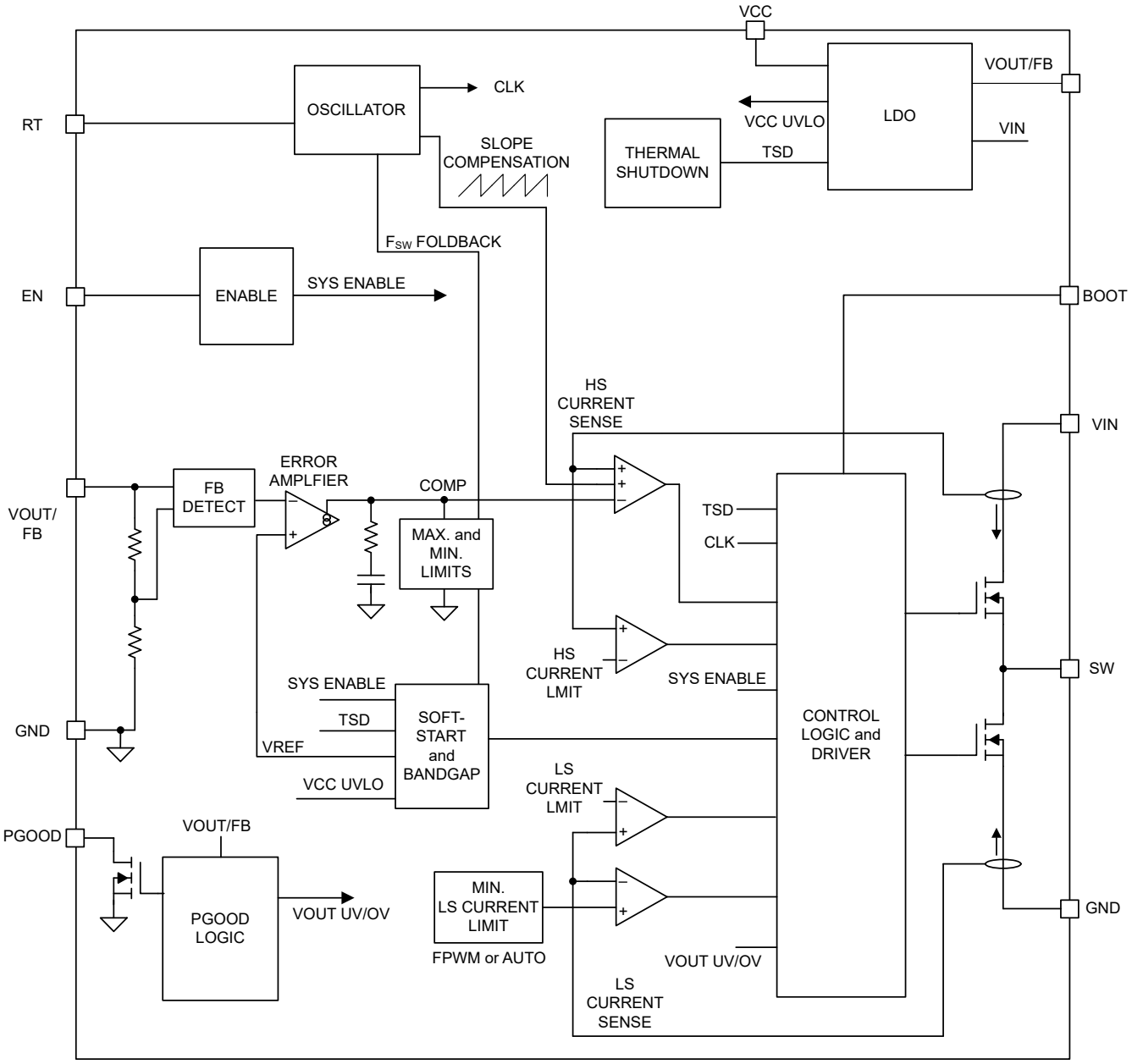
7.1 Overview

The LMR36500 is a wide input, low-quiescent current, synchronous buck converter that operates over a wide range of duty ratio and switching frequencies, from 200 kHz to 2.2 MHz. During wide input transients, if the minimum on time or the minimum off time cannot support the desired duty ratio at the higher switching frequency settings, the switching frequency is reduced automatically, allowing the LMR36500 to maintain the output voltage regulation. With an internally compensated design optimized for minimal output capacitors, the system design process with the LMR36500 is simplified significantly compared to other buck regulators available in the market.

The device is designed to minimize external component cost and design size while operating in all demanding industrial environments. An internally compensated control loop simplifies the design procedure, and is designed to reduce the required output capacitance, reducing design size and cost. The LMR36500 includes variants that can be set up to operate over a wide switching frequency range, from 200 kHz to 2.2 MHz, with the correct resistor selection from the RT pin to ground. To further reduce system cost, the PGOOD output feature with built-in delayed release allows the elimination of the reset supervisor in many applications.

The LMR36500 comes in an ultra-small 2-mm × 2-mm (HotRod) QFN package along with specially designed corner anchor pins for reliable board level solder connections. Given that the package size is very small and the increase reliability of solder connectivity due to corner anchor pins, the LMR36500 offers a reduced design size and high reliability for space constrained industrial applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable, Shutdown, and Start-up

The voltage at the EN/UVLO pin controls the start-up voltage and shutdown voltage of the LMR36500. There are three distinct modes set by the EN/UVLO pin; shut-down, standby and active. As long as the EN/UVLO pin voltage is less than $V_{EN-WAKE}$ the device is in shutdown mode. During shutdown mode, the input current drawn by the device typically is 0.5 µA (V_{IN} = 13.5 V). The internal LDO regulator is not operational. When the voltage at the EN/UVLO pin is greater than $V_{EN-WAKE}$ but less than $V_{EN-VOUT}$ the device enters the standby mode. In standby mode, the internal LDO is enabled. As the EN/UVLO pin voltage increases above $V_{EN-VOUT}$, the device enters active mode starting the feedback resistor detection. After feedback detect is completed, soft-start functionality is released to slowly increases the output voltage and switching starts. To stop switching and enter standby mode the EN/UVLO pin must fall below ($V_{EN-VOUT}$ – $V_{EN-HYST}$). Any further decrease in the EN/UVLO pin voltage below $V_{EN-WAKE}$ puts the device in shutdown. The various EN/UVLO threshold parameters and their values are listed in *セクション 6.5*. See セクション 7.3.6 for information about feedback resistor selection. 図 7-1 shows the precision enable behavior.

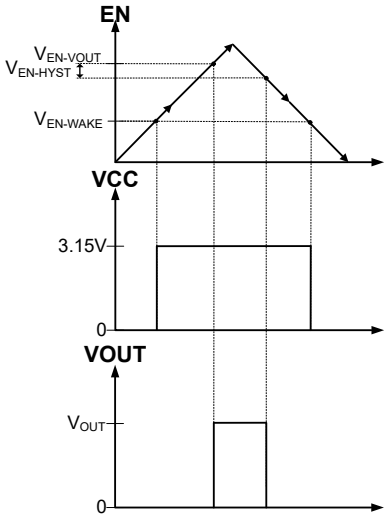


図 7-1. Precision Enable Behavior

External precision undervoltage lockout can be implemented with this functionality as shown in 図 7-2. See *セクション 8.2.2.9* for component selection.

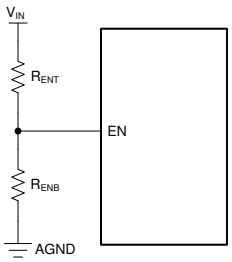


図 7-2. V_{IN} Undervoltage Lockout Using the EN/UVLO Pin

The high-voltage compliant EN/UVLO pin can be connected directly to the VIN input pin if external precision control is not needed. The EN/UVLO pin must not be allowed to float. The various EN threshold parameters are listed in the *セクション 6.5*. 図 7-1 shows the precision enable behavior. After EN/UVLO goes above $V_{EN-VOUT}$ with a delay of about 1 ms, the output voltage begins to rise with a soft-start and reaches close to the final value in about 2.58 ms (t_{ss}). After a delay of about 2 ms (t_{PGOOD_ACT}), the PGOOD flag goes high. During startup, the

device is not allowed to enter FPWM mode until the soft-start time has elapsed. Check セクション 8.2.2.9 for component selection. Refer to 図 7-3 for a typical start-up waveform.

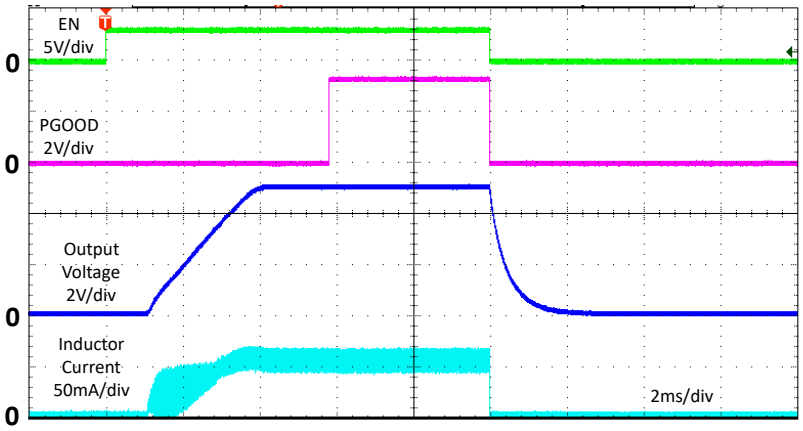


図 7-3. Enable Start-up V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 50 mA

7.3.2 Adjustable Switching Frequency (with RT)

The RT pin allows power designers to set the operating frequency between 200-kHz and 2.2-MHz depending on the needs of their application. See 図 7-4 to determine the resistor value needed for the desired switching frequency. See 表 7-1 for selection on programming the RT pin.

表 7-1. RT Pin Setting

RT INPUT	SWITCHING FREQUENCY
VCC	1 MHz
GND	2.2 MHz
RT to GND	Adjustable according to 図 7-4
Float (Not Recommended)	No Switching

式 1 can be used to calculate the value of RT for a desired frequency.

$$RT = \frac{18286}{Fsw^{1.021}} \quad (1)$$

where

- RT is the frequency setting resistor value (kΩ).
- F_{SW} is the switching frequency (kHz).

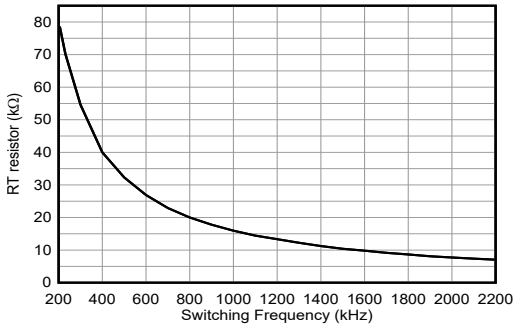


図 7-4. RT Values vs Frequency

7.3.3 Power-Good Output Operation

The power-good feature using the PGOOD pin of the LMR36500 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output remains low under device fault conditions, such as current limit and thermal shutdown, as well as during normal startup. A glitch filter prevents false flag operation for any short duration excursions in the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{RESET_FILTER} do not trip the power-good flag. Power-good operation can best be understood in reference to 図 7-5. 表 7-2 gives a more detailed breakdown the PGOOD operation. Here, V_{PG-UV} is defined as the PG-UV scaled version of the $V_{OUT-Reg}$ (target regulated output voltage) and V_{PG-HYS} as the PG-HYS scaled version of the $V_{OUT-Reg}$, where both PG-UV and PG-HYS are listed in *セクション 6.5*. During the initial power up, a total delay of 5 ms (typical) is encountered from the time the $V_{EN-VOUT}$ is triggered to the time that the power-good is flagged high. This delay only occurs during the device startup and is not encountered during any other normal operation of the power-good function. When EN/UVLO is pulled low, the power-good flag output is also forced low. With EN/UVLO low, power-good remains valid as long as the input voltage ($V_{PG-VALID}$ is ≥ 1 V (typical)).

The power-good output scheme consists of an open-drain n-channel MOSFET, which requires an external pullup resistor connected to a suitable logic supply. The power-good output scheme can also be pulled up to either V_{CC} or V_{OUT} through an appropriate resistor, as desired. If this function is not needed, the PGOOD pin can be open or grounded. Limit the current into this pin to ≤ 4 mA.

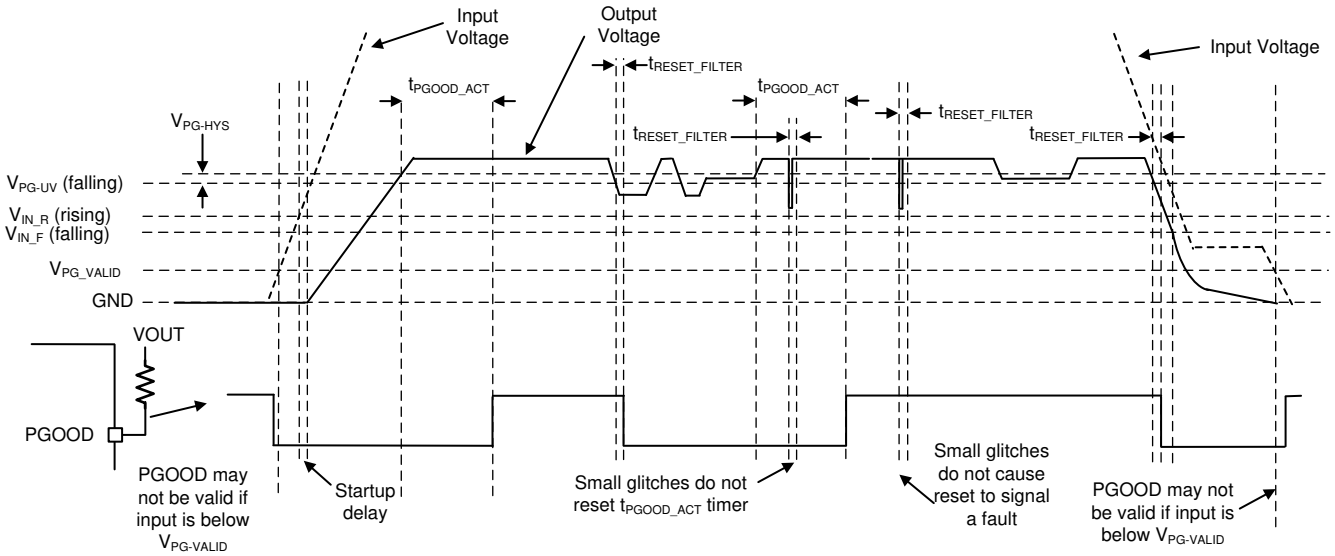


図 7-5. Power-Good Operation (OV Events Not Included)

表 7-2. Fault Conditions for PGOOD (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH t_{PGOOD_ACT} MUST PASS BEFORE PGOOD OUTPUT IS RELEASED)
$V_{OUT} < V_{PG-UV}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation: $V_{PG-UV} + V_{PG-HYS} < V_{OUT} < V_{PG-OV} - V_{PG-HYS}$
$V_{OUT} > V_{PG-OV}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation
$T_J > T_{SD-R}$	$T_J < T_{SD-F}$ AND output voltage in regulation
$EN < V_{EN-VOUT} - V_{EN-HYST}$	$EN > V_{EN-VOUT}$ AND output voltage in regulation
$V_{CC} < V_{CC-UVLO} - V_{CC-UVLO-HYST}$	$V_{CC} > V_{CC-UVLO}$ AND output voltage in regulation

7.3.4 Internal LDO, VCC UVLO, and VOUT/FB Input

The LMR36500 uses the internal LDO output and the VCC pin for the internal power supply. The VCC pin draws power either from the VIN (in adjustable output variants) or the VOUT/FB depending on how the output voltage

is configured. In the fixed output configuration, after the LMR36500 is active but has yet to regulate, the VCC rail continues to draw power from the VIN pin, until the VOUT/FB voltage reaches greater than 3.15 V (or when the device has reached steady-state regulation post the soft start). The VCC rail typically measures 3.15 V in both adjustable and fixed output variants. To prevent unsafe operation, VCC has an undervoltage lockout, which prevents switching if the internal voltage is too low. See $V_{VCC-UVLO}$ and $V_{VCC-UVLO-HYST}$ in *セクション 6.5*. During startup, VCC momentarily exceeds the normal operating voltage until $V_{VCC-UVLO}$ is exceeded, then drops to the normal operating voltage. Note that these undervoltage lockout values, when combined with the LDO dropout, drives the minimum input voltage rising and falling thresholds.

7.3.5 Bootstrap Voltage and $V_{BOOT-UVLO}$ (BOOT Terminal)

The high-side switch driver circuit requires a bias voltage higher than VIN to make sure the HS switch is turned on. The capacitor connected between BOOT and SW works as a charge pump to boost voltage on the BOOT terminal to (SW + VCC). The boot diode is integrated on the LMR36500 die to minimize physical design size. TI recommends a 100-nF capacitor rated for 10 V or higher for C_{BOOT}. The BOOT rail has an UVLO setting. This UVLO has a threshold of $V_{BOOT-UVLO}$ and is typically set at 2.3 V. If the C_{BOOT} capacitor is not charged above this voltage with respect to the SW pin, then the part initiates a charging sequence, turning on the low-side switch before attempting to turn on the high-side device.

7.3.6 Output Voltage Selection

In the LMR36500, each variant can be configured as a fixed output voltage or an adjustable output voltage. During device initialization the device configures the target output voltage to an internally selected value or an adjustable version by detecting if feedback resistors are present. When configuring the output voltage to be fixed value, simply connect the VOUT/FB pin to the system output voltage node. See *セクション 4* for the fixed output voltage setting of each variant.

To configure an adjustable output voltage, external feedback resistors are required as shown in 図 7-6. By connecting external feedback resistors with a parallel resistance greater than 5 kΩ but less than or equal to 10 kΩ (see *式 2*) the output voltage is set according as needed. The internal voltage reference is 1 V. Refer to セクション 8.2.2.2.1 for more details on how to adjust the output voltage.

When using the fixed-output configuration from the device family, simply connect the FB pin (identified as VOUT/FB pin for fixed-output variants in the rest of the datasheet) to the system output voltage node. See *セクション 4* for more details.

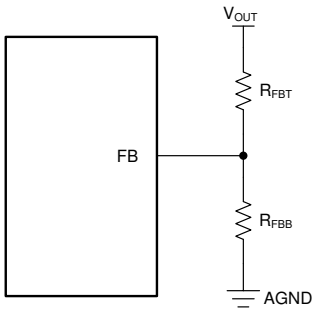


図 7-6. Setting Output Voltage for Adjustable Output Variant

$$5\ k\Omega\ <\ R_{FBT}\,||\,R_{FBB}\ \leq 10\ k\Omega \tag{2}$$

- R_{FBT} is the top resistor of the feedback divider
- R_{FBB} is the bottom resistor of the feedback divider

When configured in adjustable output voltage mode, an addition feed-forward capacitor, C_{FF}, in parallel with the R_{FBT}, can be used to optimize the phase margin and transient response. See *セクション 8.2.2.8* for more details. No additional resistor divider or feed-forward capacitor, C_{FF}, is needed in fixed-output variants.

7.3.7 Soft Start and Recovery from Dropout

When designing with the LMR36500, both soft start and recovery from dropout can cause slow rise in output voltage and must be considered as a two separate operating conditions, as shown in 図 7-7. These features ramp the output voltage at a controlled rate, keeping the output voltage from overshooting. See セクション 7.3.7.1 and セクション 7.3.7.2 for more details.

7.3.7.1 Soft Start

The soft-start feature allows the LMR3650x family of devices to gradually reach the steady state output voltage, reducing the startup stress in the system. Soft start is triggered by any of the following conditions:

- Voltage is applied to the VIN pin of the device, releasing undervoltage lockout.
- EN/UVLO voltage is sufficient to enter active mode.
- Recovery from shutdown due to over temperature protection.

After soft start is triggered, the internal reference is slowly ramped up. Assuming the output voltage is initially 0 V, the reference is ramped to 90% of the target output voltage in t_{SS}. During the soft-start time the switching mode is set to AUTO mode. AUTO mode activates diode emulation for the low-side MOSFET, not allowing negative inductor current. This allows the output voltage to be pre-biased, voltage already present on the output, during startup without discharging the output capacitor. 図 7-7 shows the difference between a non biased soft start and a pre-biased soft start.

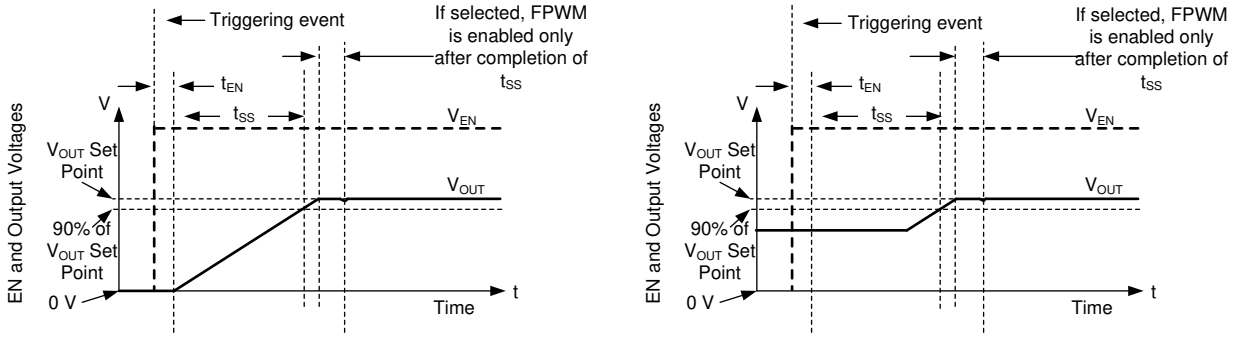


図 7-7. Soft Start with and Without Pre-biased Voltage

7.3.7.2 Recovery from Dropout

Any time the output voltage falls more than a few percent, output voltage ramps up slowly. This condition, called graceful recovery, differs from soft start in two important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.
- If the device mode is set to FPWM, the device mode continues to operate in that mode during the recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the LMR36500 can pull down on the output. Note that all protections that are present during normal operation are in place, preventing any catastrophic failure if output is shorted to a high voltage or ground.

Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below its set point is removed, the output climbs at the same speed as during start-up. For typical recovery from drop-out behavior, see 図 7-8 and 図 7-9

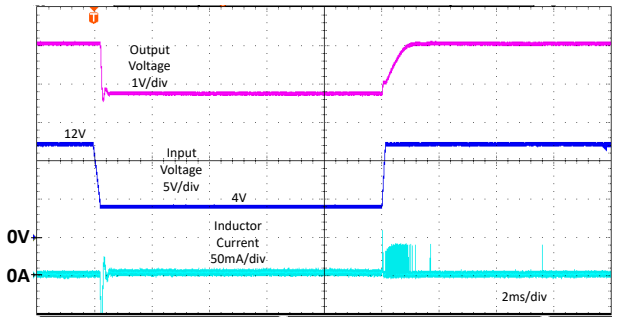


図 7-8. Dropout Performance: I_{OUT} = 0 A

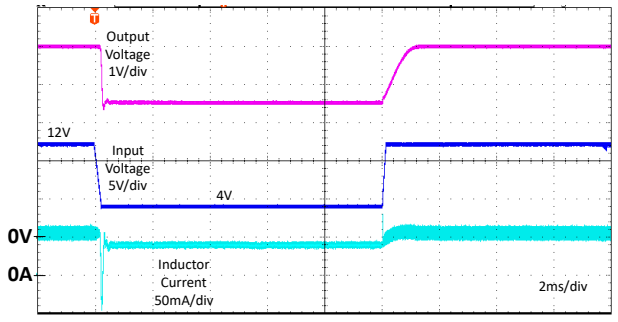


図 7-9. Dropout Performance: I_{OUT} = 50 mA

7.3.8 Current Limit and Short Circuit

The LMR36500 is protected from overcurrent conditions by cycle-by-cycle current limiting on both high-side and low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the typical peak-current mode control scheme. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to either the minimum of a fixed current set point or the output of the internal error amplifier loop minus the slope compensation every switching cycle. Because the output of the internal error amplifier loop has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty factor if duty factor is typically above 35%.

When the LS switch is turned on, the current going through the switch is also sensed and monitored. Like the high-side device, the low-side device has a turn-off commanded by the internal error amplifier loop. In the case of the low-side device, turn-off is prevented if the current exceeds this value, even if the oscillator normally starts a new switching cycle. Also like the high-side device, there is a limit on how high the turn-off current is allowed to be. This limit is called the low-side current limit, I_{VALMAX} in 図 7-10. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not to be turned on. The LS switch is turned off after the LS current falls below this limit and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

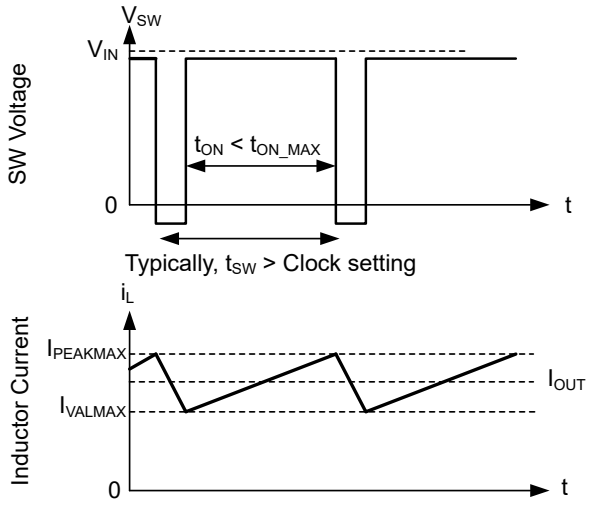


図 7-10. Current Limit Waveforms

Because the current waveform assumes values between $I_{PEAKMAX}$ and I_{VALMAX}, the maximum output current is very close to the average of these two values unless duty factor is very high. After operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

If the duty factor is very high, current ripple must be very low to prevent instability. Because current ripple is low, the part is able to deliver full current. The current delivered is very close to I_{VALMAX}.

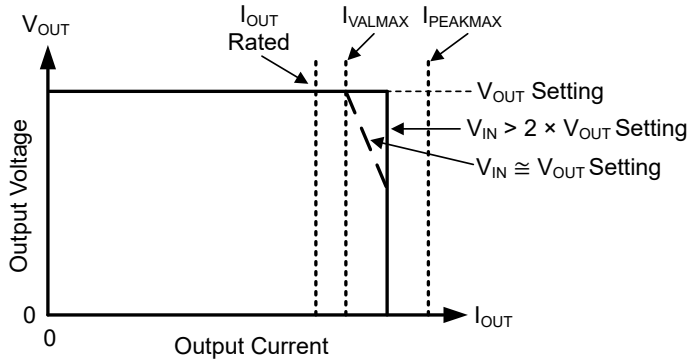


図 7-11. Output Voltage versus Output Current

Under most conditions, current is limited to the average of $I_{PEAKMAX}$ and I_{VALMAX}, which is approximately 1.3 times the maximum rated current. If input voltage is low, current can be limited to approximately I_{VALMAX}. Also note that the maximum output current does not exceed the average of $I_{PEAKMAX}$ and I_{VALMAX}. After the overload is removed, the part recovers as though in soft start.

Typical behavior when a short circuit is applied to the output can be seen in 図 7-12

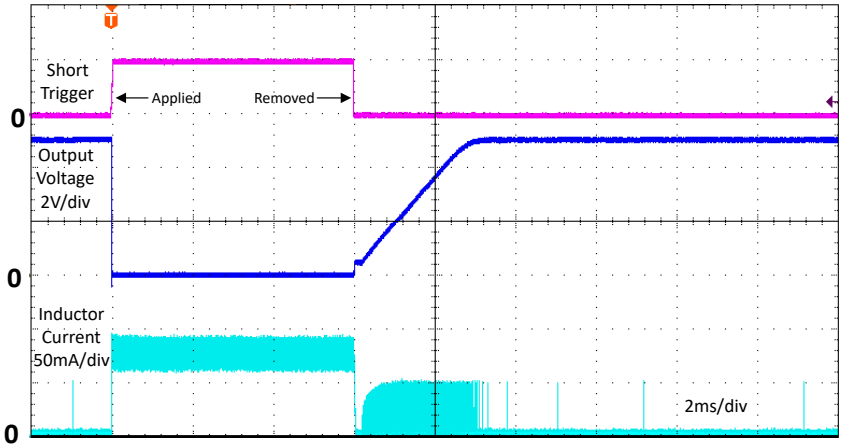


図 7-12. Typical Short-Circuit Behavior: V_{IN} = 24 V

7.3.9 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the device junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C (minimum). After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to approximately 158°C (typical). When the junction temperature falls below 158°C (typical), the LMR36500 attempts another soft start.

While the LMR36500 is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN/UVLO pin provides electrical on and off control of the device. When the EN/UVLO pin voltage is below 0.4 V, the internal LDO is disabled and there is no switching of the internal Power MOSFETs. In shutdown mode, the quiescent current drops to 0.5 µA, typically.

7.4.2 Standby Mode

When the EN/UVLO pin voltage is greater than the $V_{EN-WAKE}$ but less than $V_{EN-VOUT}$, the internal LDO is enabled. The precision enable circuitry, is enabled after VCC is above its undervoltage threshold ($V_{CC-UVLO}$). The internal power MOSFETs remain off unless the voltage on EN/UVLO pin voltage goes above its precision enable threshold ($V_{EN-VOUT}$).

7.4.3 Active Mode

The LMR36500 is in active mode whenever the EN/UVLO pin is above $V_{EN-VOUT}$, V_{IN} is high enough to satisfy V_{IN_R}, and no other fault conditions are present. The simplest way to enable the operation is to connect the EN/UVLO pin to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum V_{IN_R}.

In active mode, depending on the load current, input voltage, and output voltage, the LMR36500 is in one of five modes:

- ***Continuous Conduction Mode*** (CCM) with fixed switching frequency when load current is above half of the inductor current ripple
- ***AUTO Mode*** - Light Load Operation: PFM when switching frequency is decreased at very light load
- ***FPWM Mode*** - Light Load Operation: Continuous Conduction Mode (CCM) when the load current is lower than half of the inductor current ripple
- ***Minimum on-time***: At high input voltage and low output voltages, the switching frequency is reduced to maintain regulation.
- ***Dropout mode***: When switching frequency is reduced to minimize voltage dropout.

7.4.3.1 CCM Mode

The following operating description of the LMR36500 refers to the *Functional Block Diagram* and to the waveforms in 図 7-13. The LMR36500 has two behaviors while lightly loaded, AUTO mode and FPWM mode. Regardless of the light load operation configuration, the converter operates in CCM when the load current is greater than half the inductor ripple current.

In CCM, the LMR36500 supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) switches with varying duty cycle (D). During the HS switch on-time, the SW pin voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. The converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period:

$$D = T_{ON} / T_{SW} \quad (3)$$

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \quad (4)$$

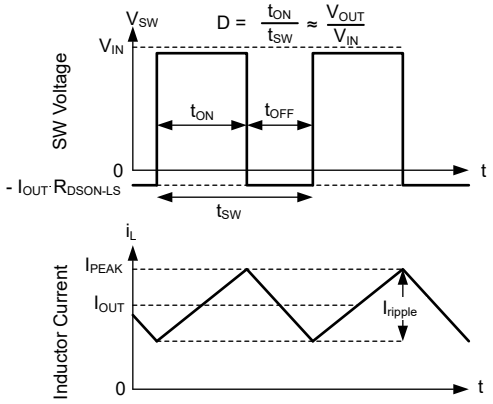


図 7-13. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

7.4.3.2 AUTO Mode - Light Load Operation

AUTO mode operation allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the LMR36500 operates in depends on which variant from this family is selected. Note that all parts operate in FPWM mode when synchronizing frequency to an external signal.

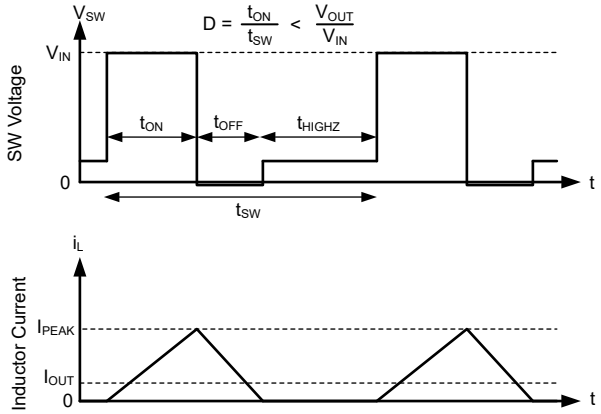
The light load operation is employed in the LMR36500 only in the auto mode. The light load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation. See 図 7-14.
- Frequency reduction. See 図 7-15.

Note that while these two features operate together to improve light load efficiency, they operate independent of each other.

7.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



In auto mode, the low-side device is turned off after SW node current is near zero. As a result, after output current is less than half of what inductor ripple is in CCM, the part operates in DCM which is equivalent to the statement that diode emulation is active.

図 7-14. PFM Operation

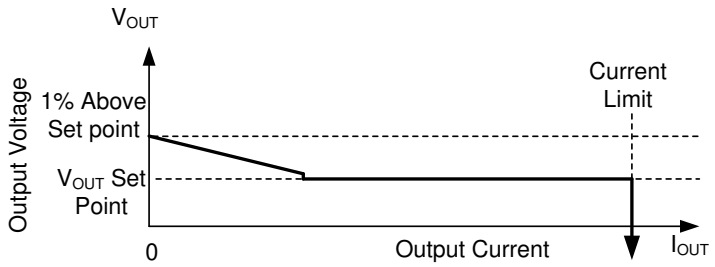
The LMR36500 has a minimum peak inductor current setting (see $I_{PEAK-MIN}$ in *セクション 6.5*) while in auto mode. After current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

7.4.3.2.2 Frequency Reduction

The LMR36500 implements frequency reduction for several reasons:

1. Light load operation
2. Minimum on-time operation, see セクション 7.4.3.4
3. Dropout operation, see セクション 7.4.3.5

At light load, the switchinig frequency of the LMR36500 decreases and the output voltage increase sdue to increased output voltage impedance. This function is enabled whenever the internal error amplifier compensation output, COMP, an internal signal, is low and there is an offset between the regulation set point of FB and the voltage applied to FB. The net effect is that there is larger output impedance while lightly loaded in auto mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.



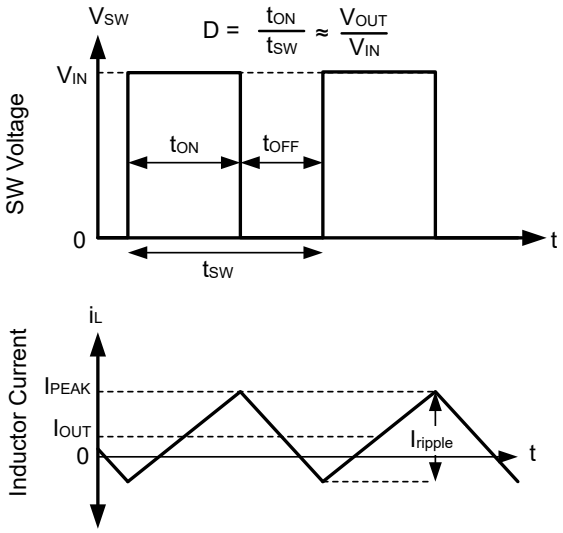
In auto mode, after output current drops below approximately 1/10th the rated current of the part, output resistance increases so that output voltage is 1% high while the buck is completely unloaded.

図 7-15. Steady State Output Voltage versus Output Current in Auto Mode

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on V_{OUT}. If the DC offset on V_{OUT} is not acceptable, a dummy load at V_{OUT} or FPWM Mode can be used to reduce or eliminate this offset.

7.4.3.3 FPWM Mode - Light Load Operation

In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry, see *Electrical Characteristics* for reverse current limit values.



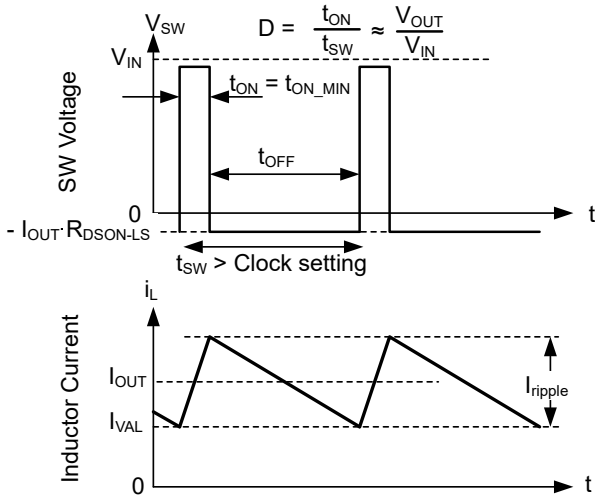
In FPWM mode, Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple}.

図 7-16. FPWM Mode Operation

For all devices, in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time even while lightly loaded, allowing good behavior during faults which involve output being pulled up.

7.4.3.4 Minimum On-time Operation

The LMR36500 continues to regulate output voltage even if the input-to-output voltage ratio requires an on-time less than the minimum. This action is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the converter is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input-to-output voltage ratio is too high, such that the inductor current peak value exceeds the peak command dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Because on-time is fixed at its minimum value, this type of operation resembles that of a device using a Constant On-Time (COT) control scheme; see 図 7-17.



In valley control mode, minimum inductor current is regulated, not peak inductor current.

図 7-17. Valley Current Mode Operation

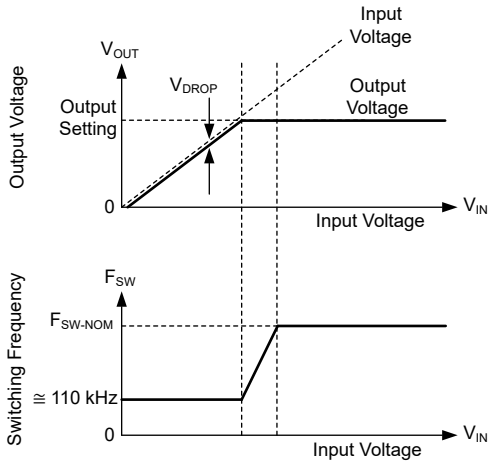
7.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency, duty cycle is limited by minimum off-time. After this limit is reached as shown in 図 7-19 if clock frequency is maintained, the output voltage falls. Instead of allowing the output voltage to drop, the LMR36500 extends the high side switch on-time past the end of the clock cycle until the needed peak inductor current is achieved. The clock is allowed to start a new cycle after peak inductor current is achieved or after a pre-determined maximum on-time, t_{ON-MAX}. As a result, after the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off-time, $t_{OFF-MIN}$, frequency drops to maintain regulation. As shown in 図 7-18 if input voltage is low enough so that output voltage cannot be regulated even with an on-time of t_{ON-MAX}, output voltage drops to slightly below the input voltage by V_{DROP}. For additional information on recovery from dropout, refer back to セクション 7.3.7.2.

The dropout performance of any buck regulator is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As mentioned, this device automatically reduces the switching frequency to maximize the effective duty-cycle in drop-out mode. There are two definitions of *dropout* voltage used in this data sheet. For both definitions, the dropout voltage is the difference between the input and output voltage under a specific condition. For the first definition, the difference is taken when the switching frequency just begins to drops. For this condition, the output voltage is within regulation. For the second definition, the difference is taken when the output voltage has fallen by 1% of the nominal regulation value. In this condition, the switching frequency has reached the lower limit. The lower frequency limit can be calculated using 式 5. While the maximum effective duty cycle is calculated using 式 6. For detailed drop-out calculations, contact your TI representative.

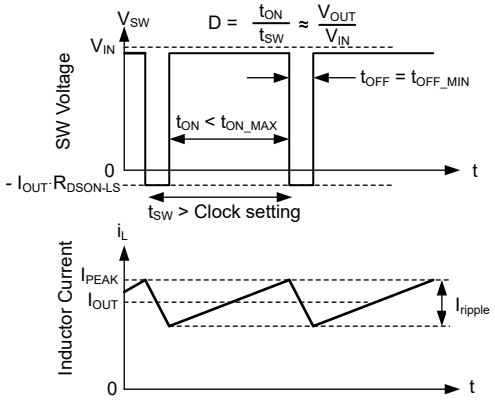
$$F_{MIN} = \frac{1}{T_{ON-MAX} + T_{OFF-MIN}} \tag{5}$$

$$D_{MAX} = \frac{T_{ON-MAX}}{T_{ON-MAX} + T_{OFF-MIN}} \tag{6}$$



Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110 kHz, input voltage tracks output voltage.

図 7-18. Frequency and Output Voltage in Dropout



Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON-MAX}.

図 7-19. Dropout Waveforms

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMR36500 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 50 mA. The following design procedure can be used to select components for the LMR36500.

注

All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This usage can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

8.2 Typical Application

図 8-1 and 図 8-2 show typical application circuits for the LMR36500. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is designed for a certain range of external inductance and output capacitance. As a quick-start guide, 表 8-1 provides typical component values for a range of the most common output voltages.

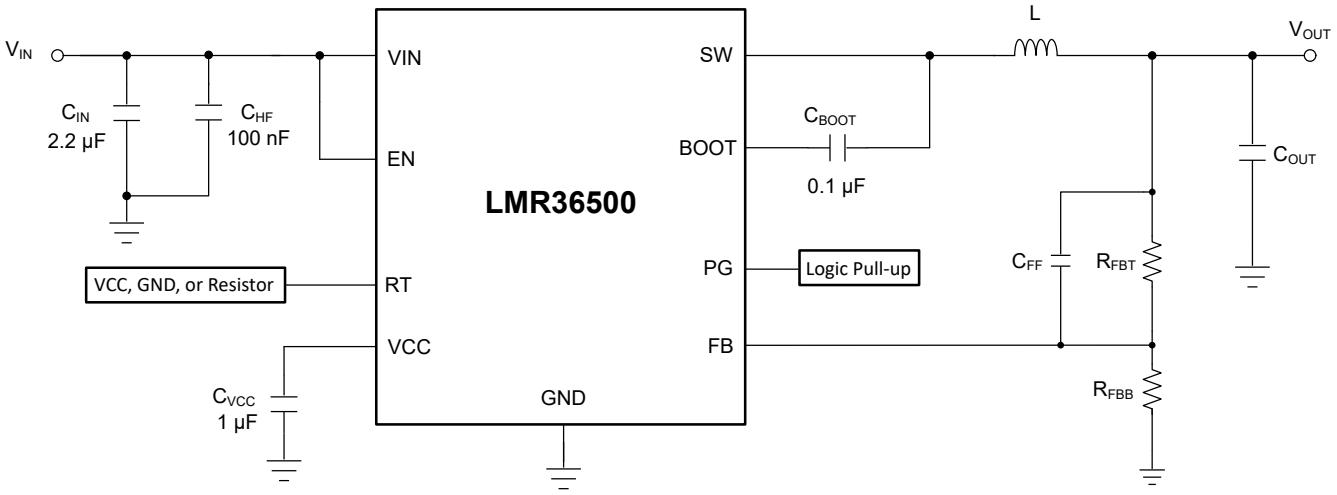


図 8-1. Example Application Circuit: ADJ Output Voltage Mode

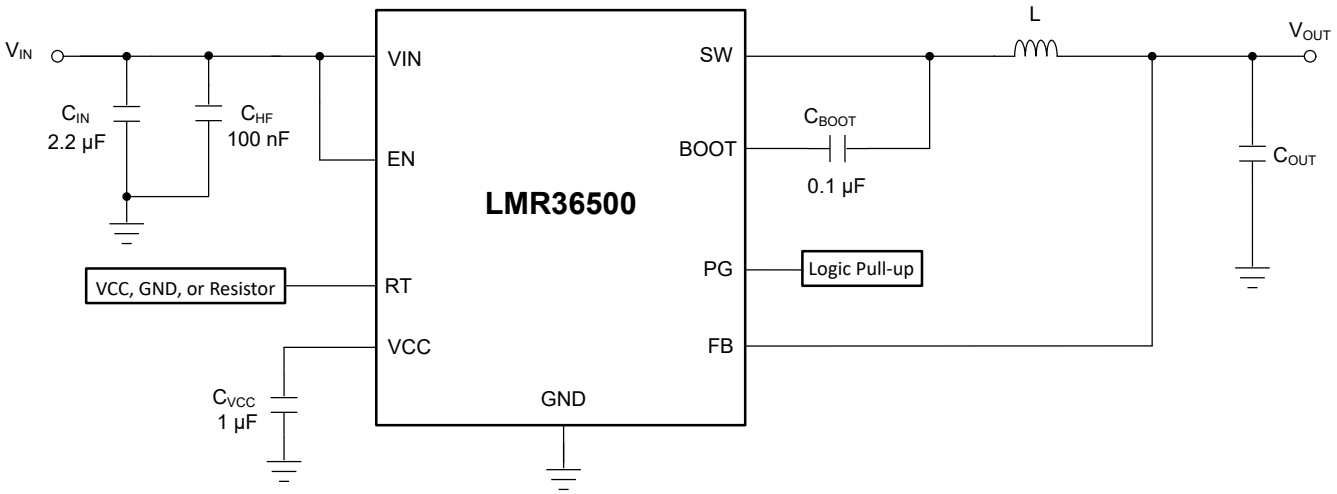


図 8-2. Example Application Circuit: Fixed Output Voltage Mode

表 8-1. Typical External Component Values(1)

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	NOMINAL C_{OUT} Under D.C. Bias	R_{FBT} (Ω)	R_{FBB} (Ω)	C_{FF} (pF)	C_{IN}	C_{BOOT}	C_{VCC}
500	5	330	4 µF	Fixed	Fixed	N/A	2.2 µF + 100 nF	100 nF	1 µF
1000	5	220	3 µF	Fixed	Fixed	N/A	2.2 µF + 100 nF	100 nF	1 µF
2200	5	100	2 µF	Fixed	Fixed	N/A	2.2 µF + 100 nF	100 nF	1 µF
500	3.3	330	4 µF	Fixed	Fixed	N/A	2.2 µF + 100 nF	100 nF	1 µF
1000	3.3	150	4 µF	Fixed	Fixed	N/A	2.2 µF + 100 nF	100 nF	1 µF
2200	3.3	68	3 µF	Fixed	Fixed	N/A	2.2 µF + 100 nF	100 nF	1 µF
500	1.8	220	4 µF	10 kΩ	12.4 kΩ	0	2.2 µF + 100 nF	100 nF	1 µF

表 8-1. Typical External Component Values(1) (続き)

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	NOMINAL C_{OUT} Under D.C. Bias	R_{FBT} (Ω)	R_{FBB} (Ω)	C_{FF} (pF)	C_{IN}	C_{BOOT}	C_{VCC}
1000	1.8	100	4 µF	10 kΩ	12.4 kΩ	0	2.2 µF + 100 nF	100 nF	1 µF
2200	1.8	33	4 µF	10 kΩ	12.4 kΩ	0	2.2 µF + 100 nF	100 nF	1 µF
500	12	680	4 µF	100 kΩ	9.09 kΩ	120	2.2 µF + 100 nF	100 nF	1 µF
1000	12	330	4 µF	100 kΩ	9.09 kΩ	120	2.2 µF + 100 nF	100 nF	1 µF
2200	12	150	4 µF	100 kΩ	9.09 kΩ	120	2.2 µF + 100 nF	100 nF	1 µF

(1) These designs are based on an input voltage range of 12 V to 48 V and a maximum load current of 50 mA.

8.2.1 Design Requirements

セクション 8.2.2 provides a detailed design procedure based on 表 8-2.

表 8-2. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	24 V (6 V to 65 V)
Output voltage	5 V
Maximum output current	0 A to 50 mA
Switching frequency	1000 kHz

8.2.2 Detailed Design Procedure

The following design procedure applies to 表 8-2 and 図 8-2 .

8.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this example, 1000 kHz is used, by connecting the RT pin to VCC.

8.2.2.2 Setting the Output Voltage

VOUT / FB of the device can be either connected directly to the output capacitor or a midpoint of a feedback resistor divider. When connected directly to the output capacitor, the device assumes that a fixed output voltage of either 3.3 V or 5 V is desired. The 3.3-V or 5-V fixed output options are factory trimmed and it is unique to a specific device. See セクション 4 for the selection of fixed output voltage versions.

For this design example we need an output voltage of 5-V, so we select the LMR36500P5 device.

8.2.2.2.1 V_{OUT} / FB for Adjustable Output

If other voltages are desired, V_{OUT} / FB can be connected to a feedback resistor divider network to set the output voltage. The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the V_{OUT} / FB pin equal to the internal reference voltage, V_{REF}. The converter determines whether fixed output voltage or adjustable output voltage is required by sensing the resistance of the feedback path during start-up. To make sure that the converter regulates to the desired output voltage, the typical minimum value for the parallel combination of R_{FBT} and R_{FBB} is 5 kΩ while the typical maximum value is 10 kΩ as shown in 式 7. 式 8 can be used as a starting point to determine the value of R_{FBT}. Reference 表 8-3 for a list of acceptable resistor values for various output voltages.

The resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended maximum value for R_{FBT} is 200 kΩ.

$$5\ k\Omega\ <\ R_{FBT}\left|\right|R_{FBB}\ \leq 10\ k\Omega \tag{7}$$

$$R_{FBT} \leq 10\ k\Omega \times \frac{V_{OUT}}{1\ V} \tag{8}$$

表 8-3. Recommended Feedback Resistor Values for Various Output Voltages

V_{OUT} (V)	R_{FBT} (1) (kΩ)	R_{FBB} (1) (kΩ)
1.2	10.2	51.1
2.5	24.9	16.5
3.3	33.2	14.3
5	49.9	12.4
12	110	10

(1) R_{FBT} and R_{FBB} are based on 1% standard resistor values.

8.2.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, use the maximum device current. 式 9 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, choose K = 0.4 and find an inductance of L = 200 µH. Select the next standard value of L = 220 µH.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUT\ max}} \times \frac{V_{OUT}}{V_{IN}} \tag{9}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, $I_{PEAKMAX}$ (see *Electrical Characteristics*). The saturation current rating of the inductor being as large as the high-side switch current limit ensures that the inductor does not saturate, even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{VALMAX}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This fast rise can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies above about 1 MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

To avoid subharmonic oscillation, when operating at duty cycles of 50% and greater, the inductance value must not be less than that given in 式 10:

$$L\ \geq 15.6 \times \frac{V_{OUT}}{F_{SW}} \tag{10}$$

The maximum inductance is limited by the minimum current ripple for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

8.2.2.4 Output Capacitor Selection

The current mode control scheme of this device allows operation over a wide range of output capacitance. The output capacitor bank is usually limited by the load transient requirements and stability rather than the output voltage ripple. Please refer to 表 8-1 for typical output capacitor value(s) for 3.3-V and 5-V output voltages. Based on 表 8-1, for a 5-V output design, you can choose the recommended 3-µF (typically 2x 2.2-µF) ceramic

output capacitor for this example. For other designs with other output voltages, WEBENCH can be used as a starting point for selecting the value of output capacitor.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

8.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. The typical value for this capacitor is 2.2-µF. This capacitance must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example a 2.2-µF, 100-V, X7R (or better) ceramic capacitor is chosen. The 100 nF must also be rated at 100 V with an X7R dielectric.

Using an electrolytic capacitor on the input in parallel with the ceramics is desirable. This statement is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from 式 11 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{11}$$

8.2.2.6 C_{BOOT}

The requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 16 V is required.

8.2.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see *セクション 7.3.3*). A value in the range of 10 kΩ to 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 3.15 V; see *Electrical Characteristics* for limits.

8.2.2.8 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feed forward Capacitor application report* is helpful when experimenting with a feedforward capacitor.

Due to the nature of the feedback detect circuitry, the value of C_{FF} must be limited to make sure that the desired output voltage is established when configuring for adjustable output voltages. Follow 式 12 to make sure C_{FF} remains below the maximum value.

$$C_{FF} < C_{OUT} \times \frac{\sqrt{V_{OUT}}}{1.2M\Omega} \quad (12)$$

8.2.2.9 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. An input UVLO level different than that provided internal to the device is can be accomplished by using the circuit shown in 図 8-3. The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then 式 13and 式 14 are used to calculate R_{ENT} and V_{OFF}, respectively.

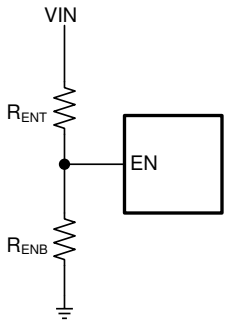


図 8-3. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-VOUT}} - 1\right) \times R_{ENB} \quad (13)$$

$$V_{OFF} = V_{ON} \times \left(1 - \frac{V_{EN-HYS}}{V_{ENVOUT}}\right) \quad (14)$$

where

- V_{ON} is the V_{IN} turn-on voltage.
- V_{OFF} is the V_{IN} turn-off voltage.

8.2.2.10 Maximum Ambient Temperature

As with any power conversion device, the LMR36500 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device and PCB combination. The maximum junction temperature for the LMR36500 must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. 式 15 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in *Semiconductor and IC Package Thermal Metrics application report*, the value of $R_{\Theta JA}$ given in the *Thermal Information Table*, is not valid for design purposes and must not be used for estimating the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application. For more information, refer to the *Semiconductor and IC Package Thermal Metrics application report*.

$$I_{OUT|MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \times \frac{\eta}{1-\eta} \times \frac{1}{V_{OUT}} \quad (15)$$

where

- η is the efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature and flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

A typical example of $R_{\theta JA}$ versus copper board area can be found in 図 8-4 . The copper area given in the graph is for each layer. For a 4-layer PCB design, the top and bottom layers are 2-oz. copper each, while the inner layers are 1 oz. For a 2-layer PCB design, the top and bottom layers are 2-oz. copper each. Note that the data given in these graphs are for illustration purposes only, and the actual performance in any given application depends on all of the factors mentioned above.

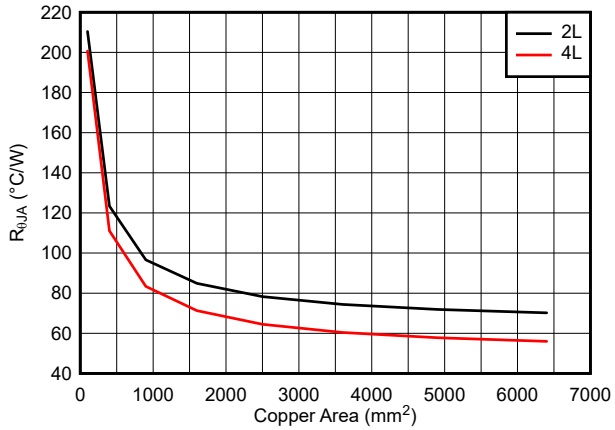


図 8-4. Typical $R_{\theta JA}$ vs Copper Area

The IC junction temperature can be estimated for a given operating condition using 式 16.

$$T_J \approx T_A + R_{\theta JA} \times \text{IC Power Loss} \quad (16)$$

where

- T_J is the IC junction temperature (°C).
- T_A is the ambient temperature (°C).
- $R_{\theta JA}$ is the thermal resistance (°C/W)
- IC Power Loss is the power loss for the IC (W).

The IC Power loss mentioned above is the overall power loss minus the loss that comes from the inductor DC Resistance. The overall power loss can be approximated by using WEBENCH for a specific operating condition and temperature.

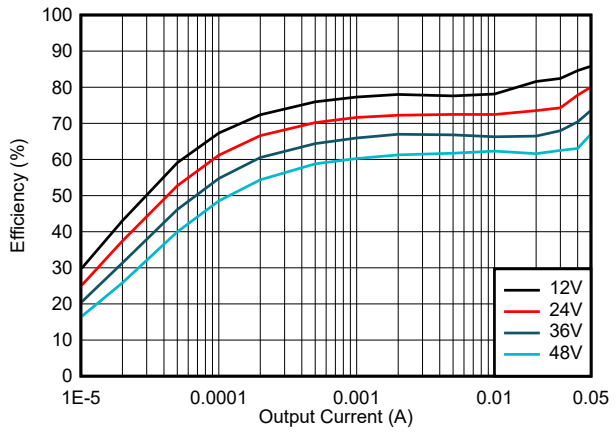
Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight application report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages application report*
- *Semiconductor and IC Package Thermal Metrics application report*
- *Thermal Design Made Simple with LM43603 and LM43602 application report*

- *PowerPAD™ Thermally Enhanced Package application report*
- *PowerPAD™ Made Easy application report*
- *Using New Thermal Metrics application report*
- *PCB Thermal Calculator*

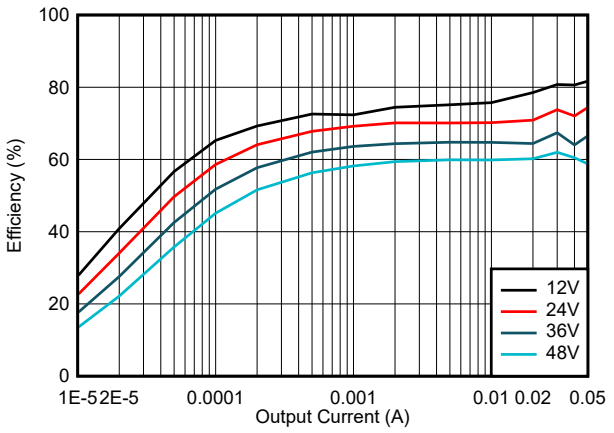
8.2.3 Application Curves

The data in this section was taken with the LMR36500EVM. All curves are typical at T_A = 25ºC. See 表 8-4 for details.



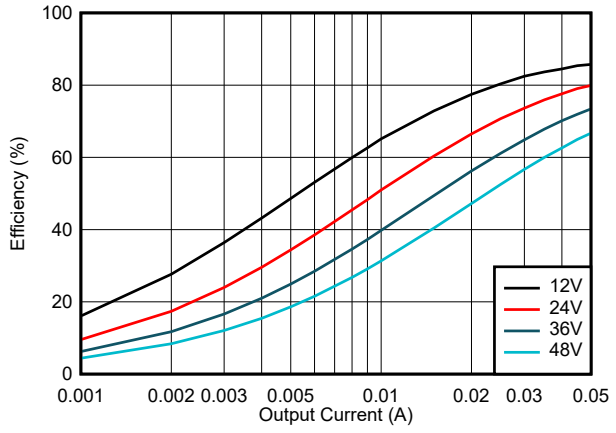
LMR36500P5 V_{OUT} = 5 V Fixed 1 MHz (AUTO)

図 8-5. Efficiency



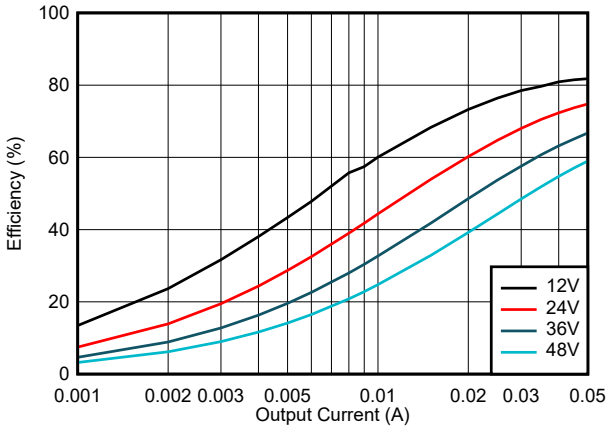
LMR36500P3 V_{OUT} = 3.3 V Fixed 1 MHz (AUTO)

図 8-6. Efficiency



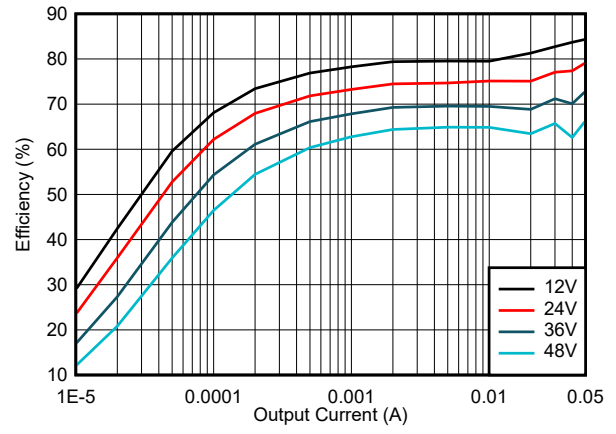
LMR36500F5 V_{OUT} = 5 V Fixed 1 MHz (FPWM)

図 8-7. Efficiency



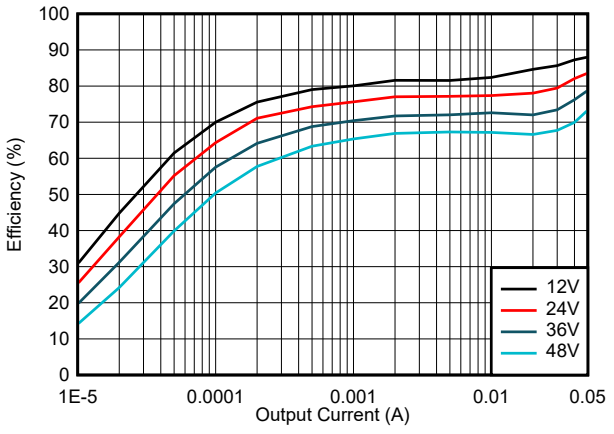
LMR36500F3 V_{OUT} = 3.3 V Fixed 1 MHz (FPWM)

図 8-8. Efficiency



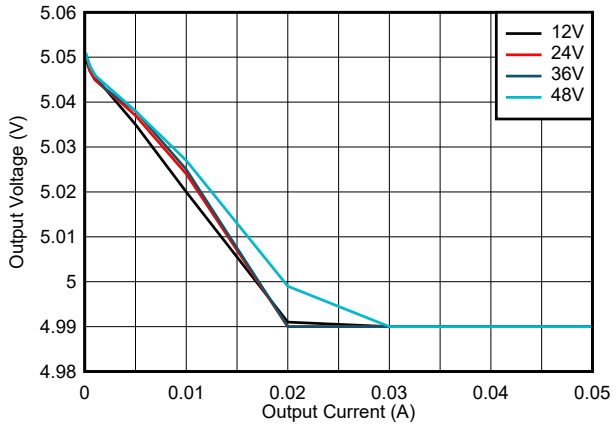
LMR36500P3 V_{OUT} = 3.3 V Fixed 600 kHz (AUTO)

図 8-9. Efficiency



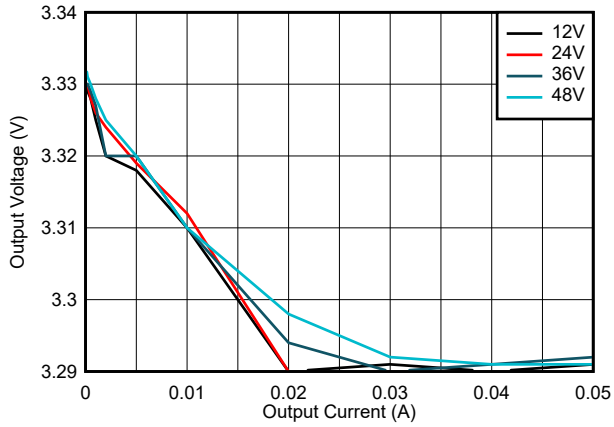
LMR36500P5 V_{OUT} = 5 V Fixed 600 kHz (AUTO)

図 8-10. Efficiency



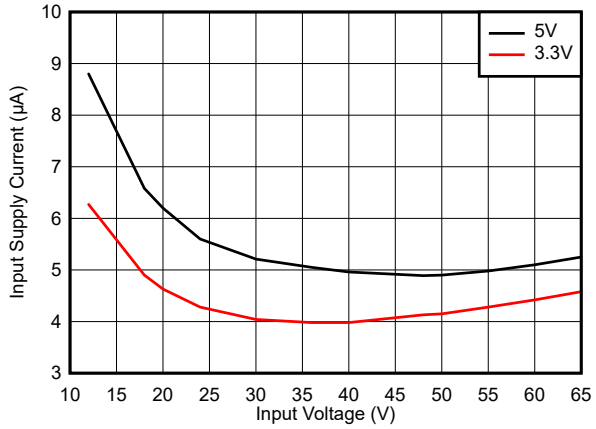
LMR36500P5 V_{OUT} = 5 V Fixed 1 MHz (AUTO)

図 8-11. Line and Load Regulation



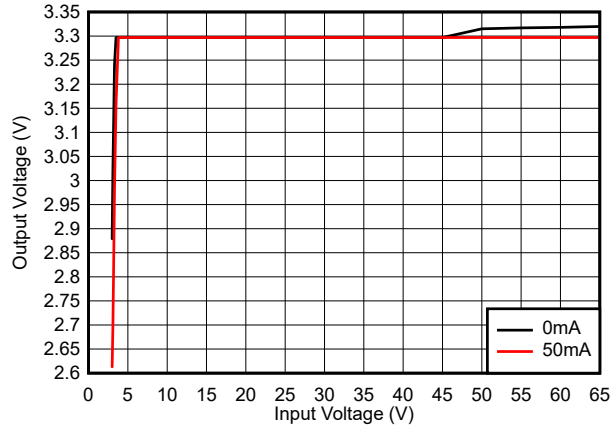
LMR36500P3 V_{OUT} = 3.3 V Fixed 1 MHz (AUTO)

図 8-12. Line and Load Regulation



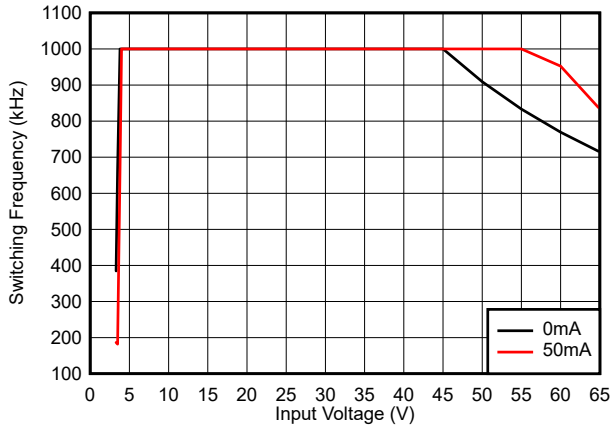
LMR36500P (fixed) I_{OUT} = 0 mA 1 MHz (AUTO)

図 8-13. No Load Input Current



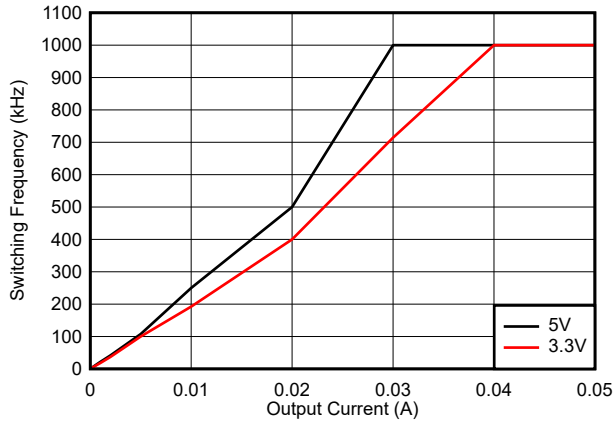
LMR36500P3 V_{OUT} = 3.3 V Fixed 1 MHz (FPWM)

図 8-14. Output Voltage vs Input Voltage



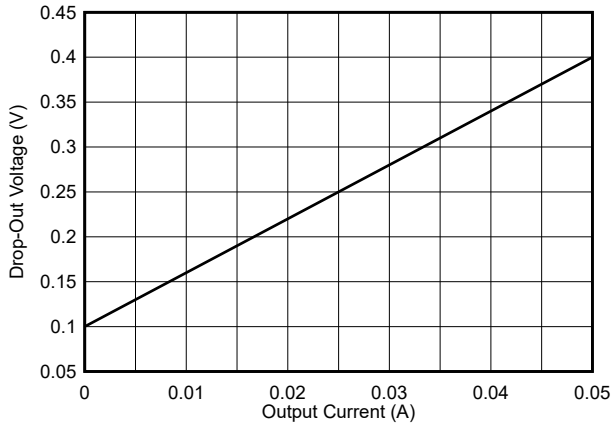
LMR36500P3 V_{OUT} = 3.3 V Fixed 1 MHz (AUTO)

図 8-15. Switching Frequency vs Input Voltage



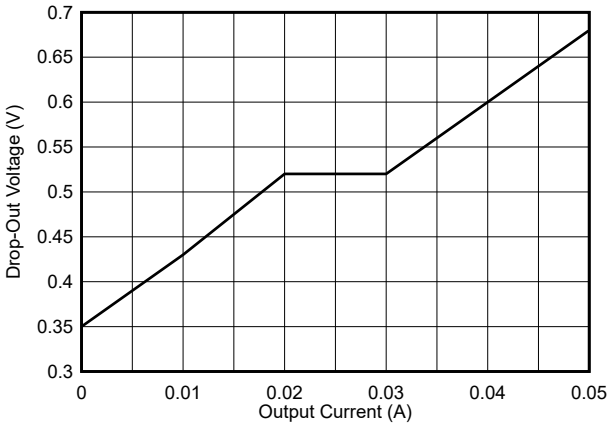
LMR36500P3 V_{IN} = 12 V Fixed 1 MHz (AUTO)

図 8-16. Switching Frequency vs Output Current



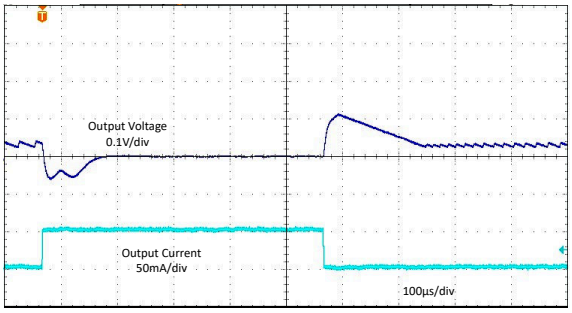
LMR36500P5 V_{OUT} = 5 V Fixed 1 MHz (AUTO)

図 8-17. Drop-Out Voltage to –1% V_{OUT}



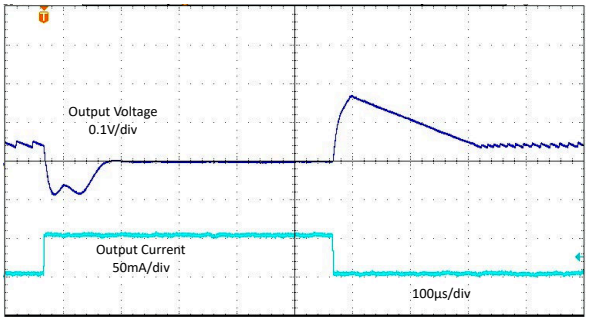
LMR36500P5 V_{OUT} = 5 V Fixed 1 MHz (AUTO)

図 8-18. Drop-Out Voltage to Frequency Fold-back



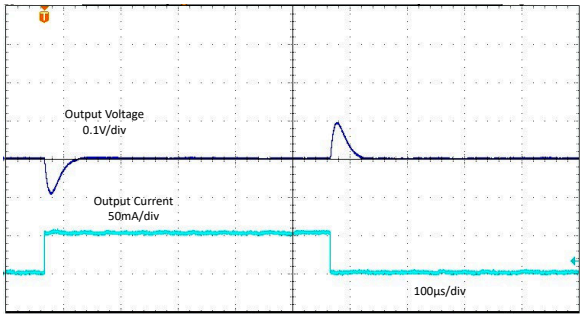
LMR36500P3 V_{OUT} = 3.3 V Fixed 1 MHz (AUTO)
V_{IN} = 12 V Iout = 5 mA to 50 mA

図 8-19. Load Transient



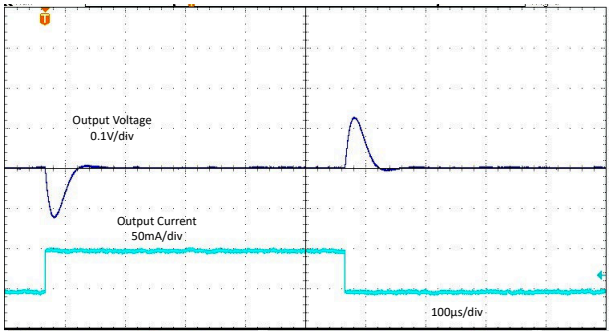
LMR36500P5 V_{OUT} = 5 V Fixed 1 MHz (AUTO)
V_{IN} = 12 V Iout = 5 mA to 50 mA

図 8-20. Load Transient



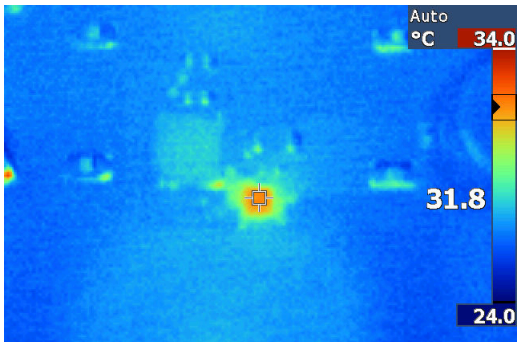
LMR36500F3 V_{OUT} = 3.3 V Fixed 1 MHz (FPWM)
V_{IN} = 12 V Iout = 0 mA to 50 mA

図 8-21. Load Transient



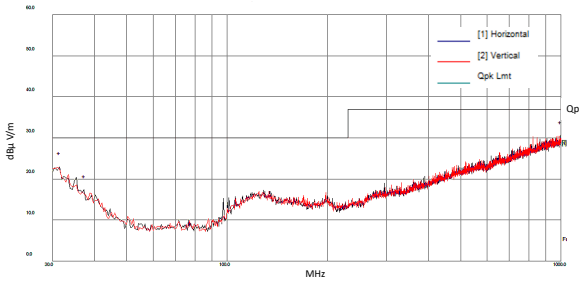
LMR36500F5 V_{OUT} = 5 V Fixed 1 MHz (FPWM)
V_{IN} = 12 V Iout = 0 mA to 50 mA

図 8-22. Load Transient



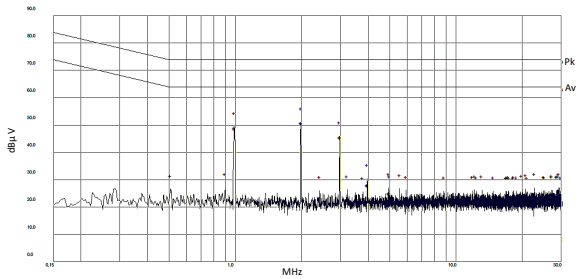
V_{OUT} = 5 V　I_{OUT} = 50 mA　1 MHz (AUTO)
V_{IN} = 65 V

図 8-23. Thermal Image (LMR36500EVM)



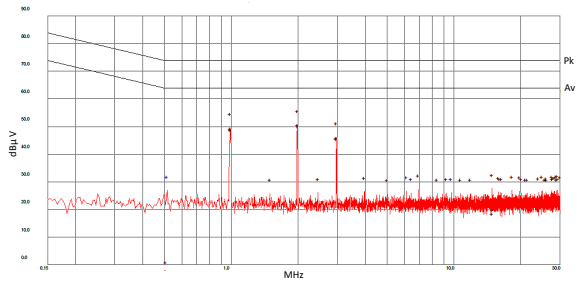
LMR36500P5　V_{OUT} = 5 V Fixed　1 MHz (FPWM)
V_{IN} = 24 V　No EMI Filter　C_{IN} = 3x 2.2µF

図 8-24. Radiated Emissions



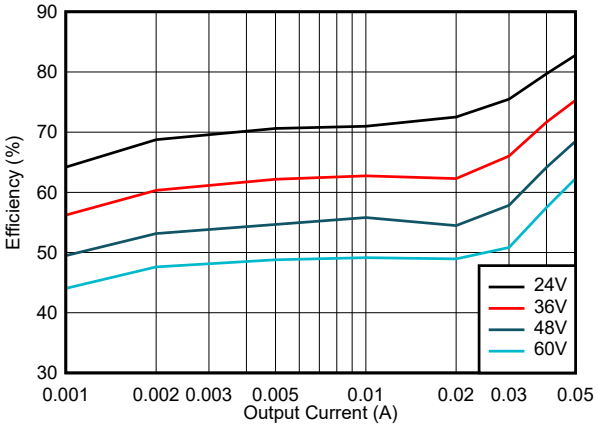
LMR36500P5　V_{OUT} = 5 V Fixed　1 MHz (FPWM)
V_{IN} = 24 V　No EMI Filter　C_{IN} = 3x 2.2µF

図 8-25. Conducted Emissions (positive)



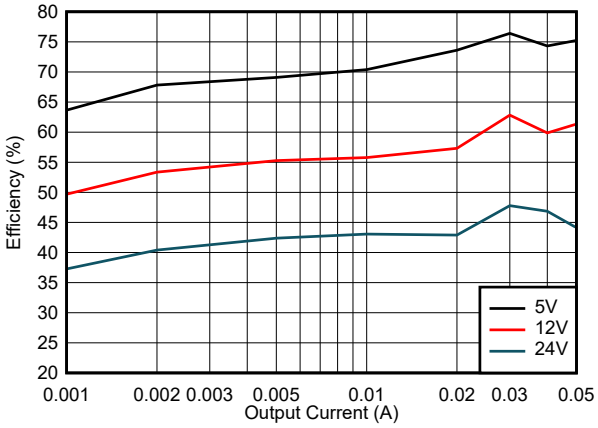
LMR36500P5　V_{OUT} = 5 V Fixed　1 MHz (FPWM)
V_{IN} = 24 V　No EMI Filter　C_{IN} = 3x 2.2µF

図 8-26. Conducted Emissions (Negative)



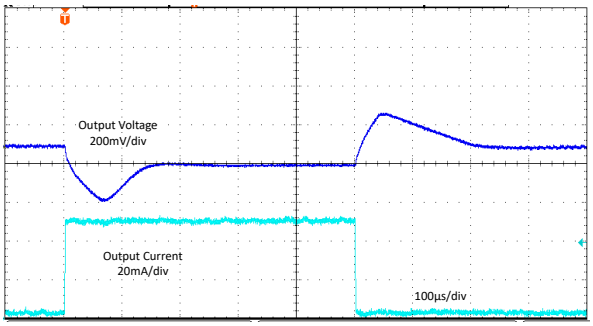
LMR36500P　V_{OUT} = 12 V (ADJ)　1 MHz (AUTO)

図 8-27. Efficiency



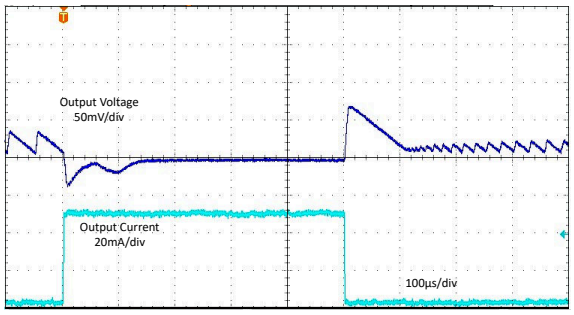
LMR36500P　V_{OUT} = 1.8 V (ADJ)　1 MHz (AUTO)

図 8-28. Efficiency



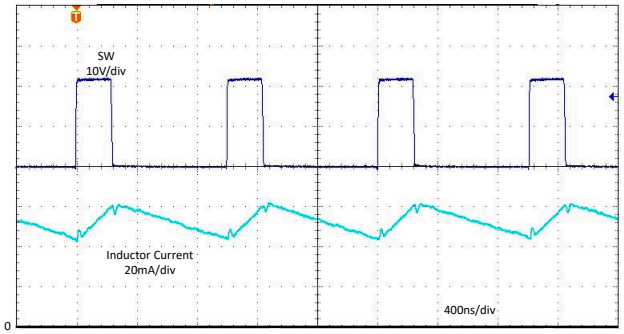
LMR36500P V_{OUT} = 12 V (ADJ) 1 MHz (AUTO)
V_{IN} = 24 V Iout = 5 mA to 50 mA

図 8-29. Load Transient



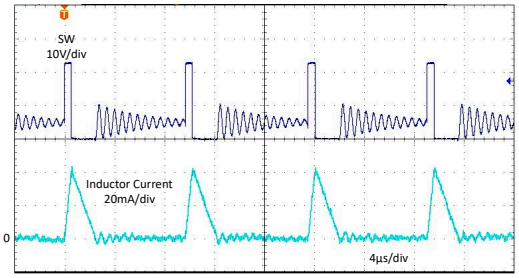
LMR36500P V_{OUT} = 1.8 V (ADJ) 1 MHz (AUTO)
V_{IN} = 12 V Iout = 5 mA to 50 mA

図 8-30. Load Transient



LMR36500P5 V_{OUT} = 5 V 1 MHz (AUTO)
V_{IN} = 24 V Iout = 50 mA

図 8-31. Typical Switching Waveforms



LMR36500P5 V_{OUT} = 5 V 1 MHz (AUTO)
V_{IN} = 24 V Iout = 5 mA

図 8-32. Typical Switching Waveforms

表 8-4. BOM for Typical Application Curves

Output Voltage	Frequency	R_{FBB}	R_{FBT}	C_{OUT}	L	C_{FF}
5 V (fixed)	1 MHz	OPEN	0 Ω	2 × 2.2 µF	220 µH, 1.1 Ω, MSS5131-224MLC	N/A
3.3 V (fixed)	1 MHz	OPEN	0 Ω	2 × 2.2 µF	220 µH, 1.1 Ω, MSS5131-224MLC	N/A
1.8 V	1 MHz	12.1 kΩ	10 kΩ	2 × 2.2 µF	220 µH, 1.1 Ω, MSS5131-224MLC	0 pF
12 V	1 MHz	9.09 kΩ	100 kΩ	2 × 2.2 µF	330 µH, 1.6Ω, MSS5131-334MLB	150 pF
5 V (fixed)	600 kHz	OPEN	0 Ω	2 × 2.2 µF	330 µH, 0.81 Ω, 744775233	N/A
3.3 V (fixed)	600 kHz	OPEN	0 Ω	2 × 2.2 µF	330 µH, 0.81 Ω, 744775233	N/A

8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the ESD specifications found in *ESD (Commercial) Ratings*.
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique a design and PCB layout to help make the project a success.

8.4 Power Supply Recommendations

The characteristics of the input supply must be compatible with *セクション 6* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 式 17.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{17}$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kind of issues is to limit the distance from the input supply to the regulator or plan to use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help dampen the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This usage can lead to instability, as well as some of the effects mentioned above, unless designed carefully. The *AN-2162 Simple Success With Conducted EMI From DC/DC Converters User's Guide* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

8.5 Layout

8.5.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in 図 8-33. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the

converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. 図 8-34 shows a recommended layout for the critical components of the .

1. *Place the input capacitors as close as possible to the VIN and GND terminals.*
2. *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins. Route the SW pin to the N/C pin and used to connect the BOOT capacitor to SW.
4. *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.
6. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. *Provide enough PCB area for proper heat-sinking.* As stated in *セクション 8.2.2.10*, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
8. *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies application report*
- *Simple Switcher PCB Layout Guidelines application report*
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x application report*

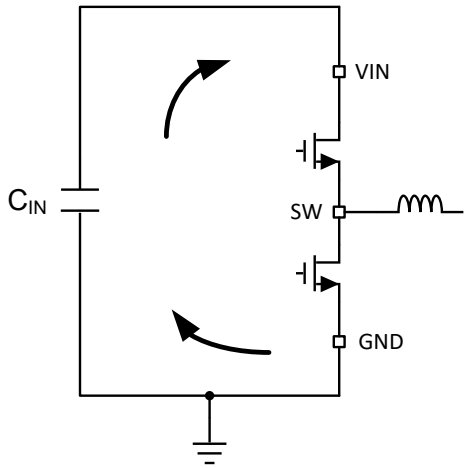


図 8-33. Current Loops with Fast Edges

8.5.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the GND pin to the ground planes using vias next to the bypass capacitors. The GND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.

TI recommends providing adequate device heat-sinking by having enough copper near the GND pin. See 図 8-34 for example layout. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

8.5.2 Layout Example

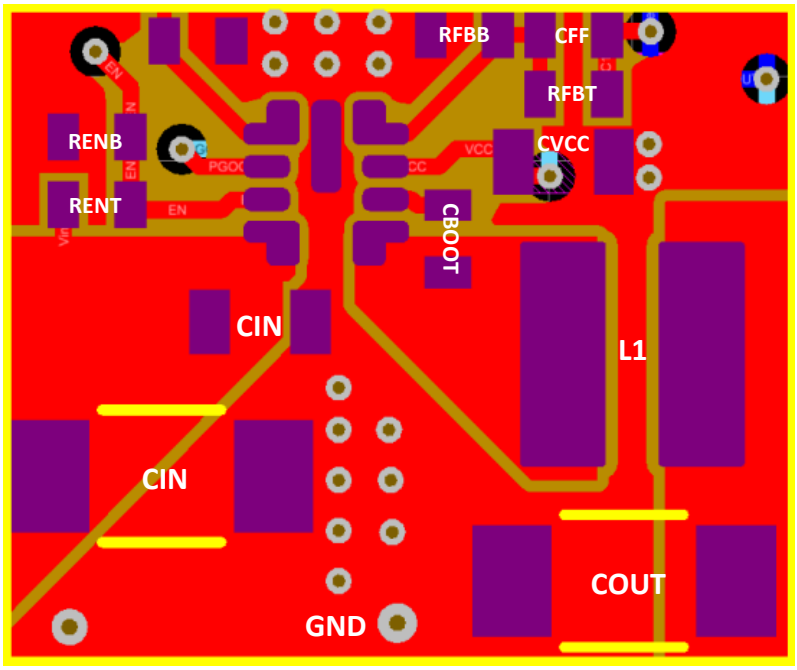


図 8-34. Example Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

図 9-1 shows the device naming nomenclature of the LMR36500. See セクション 4 for the availability of each variant. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options; minimum order quantities apply.

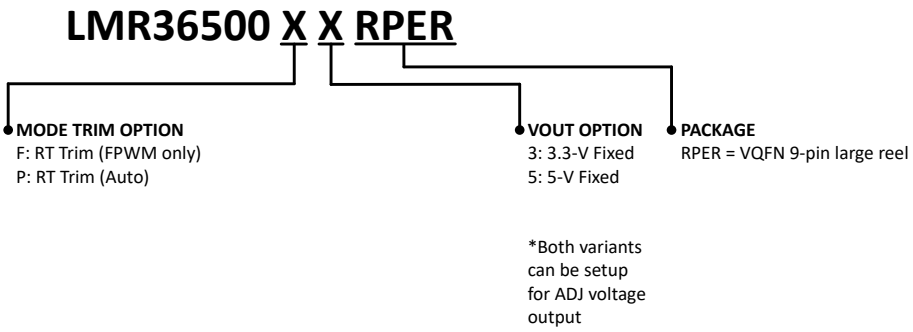


図 9-1. Device Naming Nomenclature

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Thermal Design by Insight not Hindsight application report*
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages application report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics application report*
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602 application report*
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package application report*
- Texas Instruments, *PowerPAD™ Made Easy application report*
- Texas Instruments, *Using New Thermal Metrics application report*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies application report*
- Texas Instruments, *Simple Switcher PCB Layout Guidelines application report*
- Texas Instruments, *Construction Your Power Supply- Layout Considerations Seminar*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x application report*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントを工キスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.5 Trademarks

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9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2023	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR36500F3RPER	ACTIVE	VQFN-HR	RPE	9	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	FL01	Samples
LMR36500F5RPER	ACTIVE	VQFN-HR	RPE	9	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	FL02	Samples
LMR36500P3RPER	ACTIVE	VQFN-HR	RPE	9	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	FL03	Samples
LMR36500P5RPER	ACTIVE	VQFN-HR	RPE	9	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	FL04	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

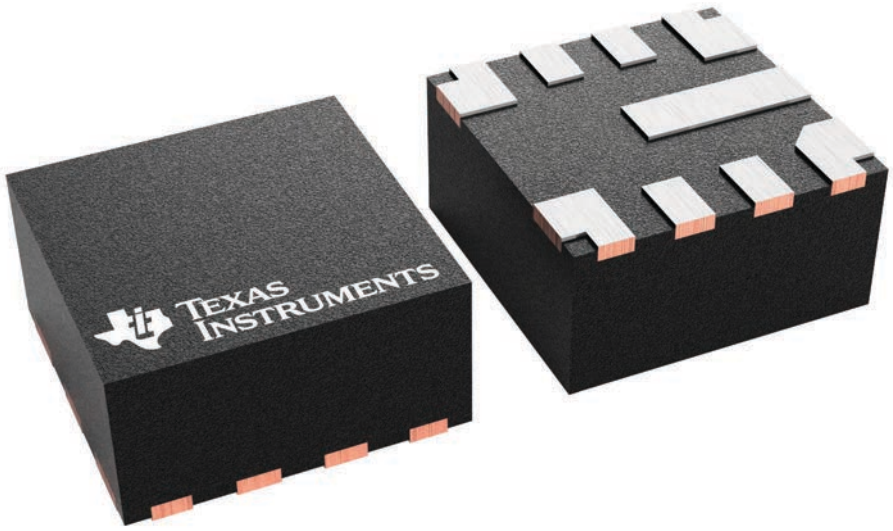
RPE 9

VQFN-HR - 1.0 mm max height

2 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



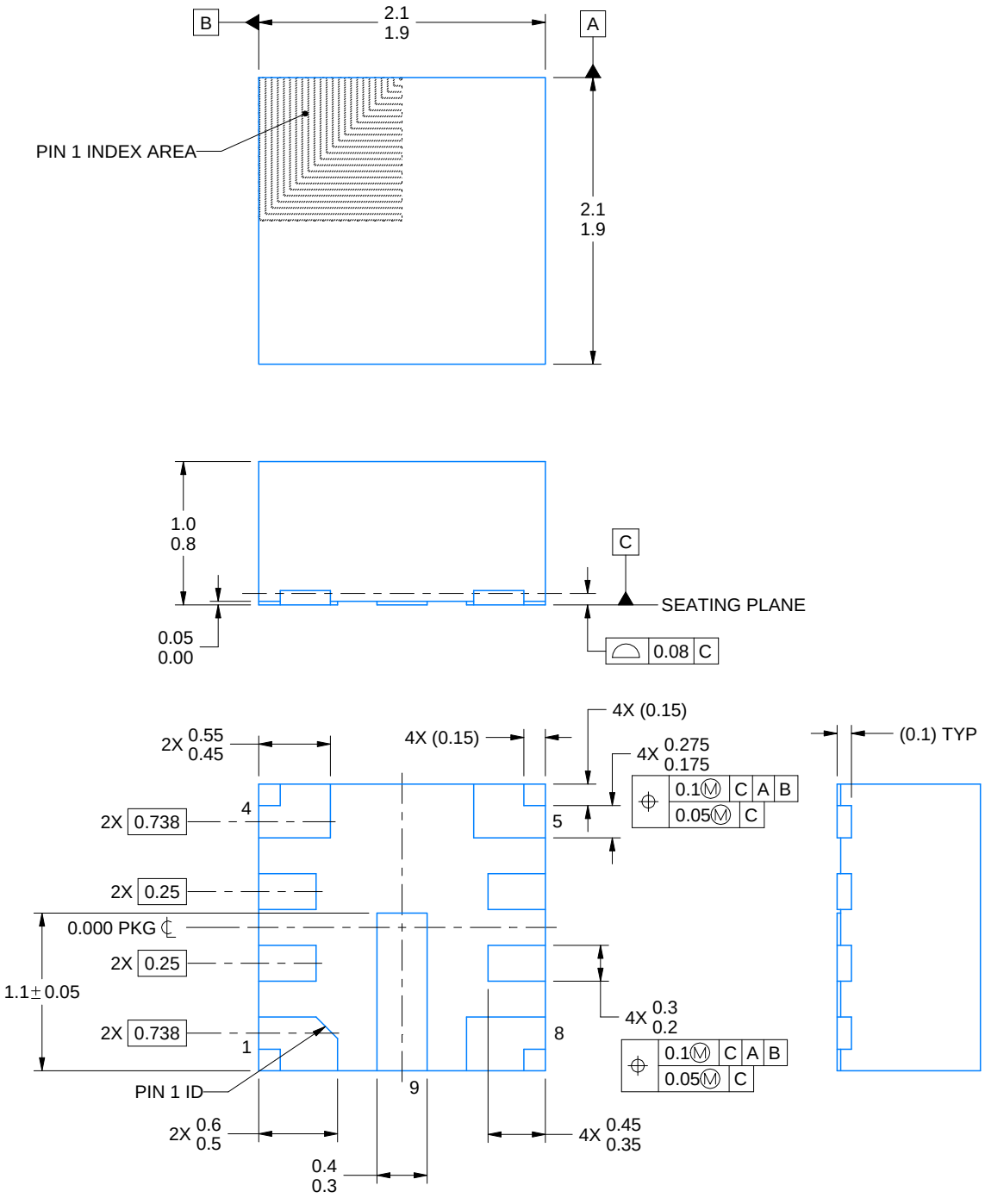
4227057/A

PACKAGE OUTLINE

RPE0009B

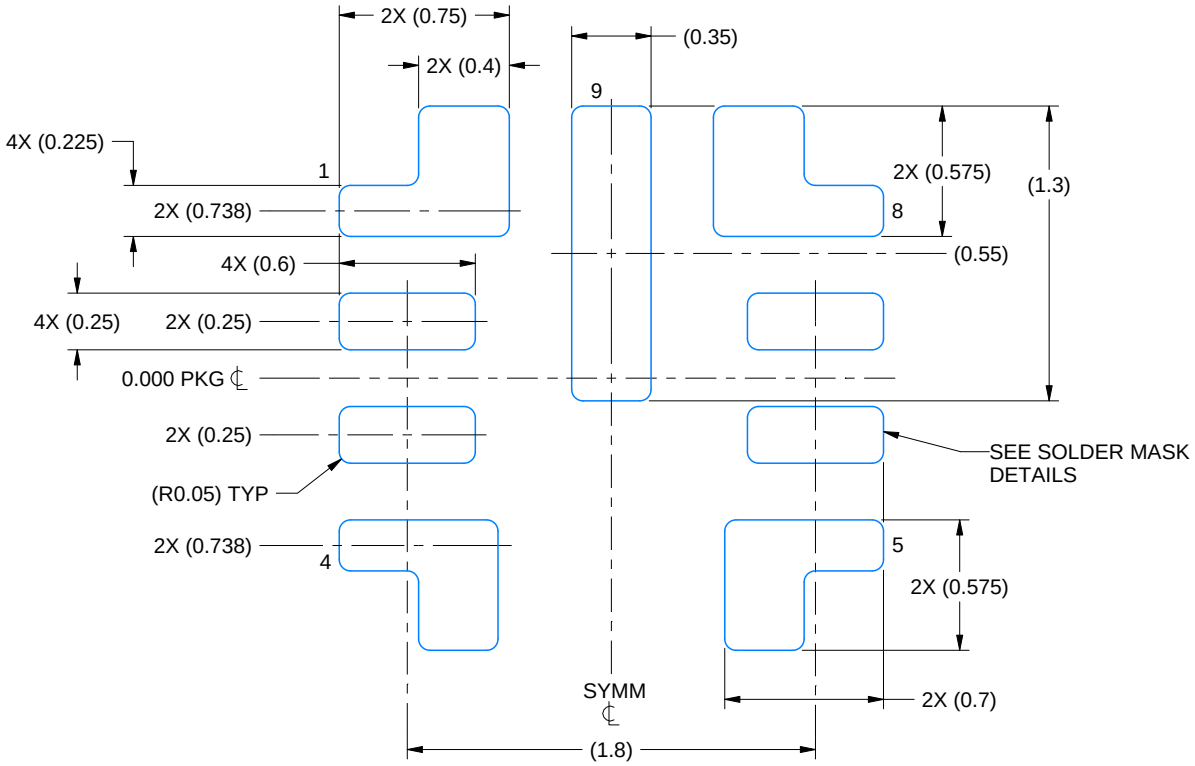
VQFN-HR - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

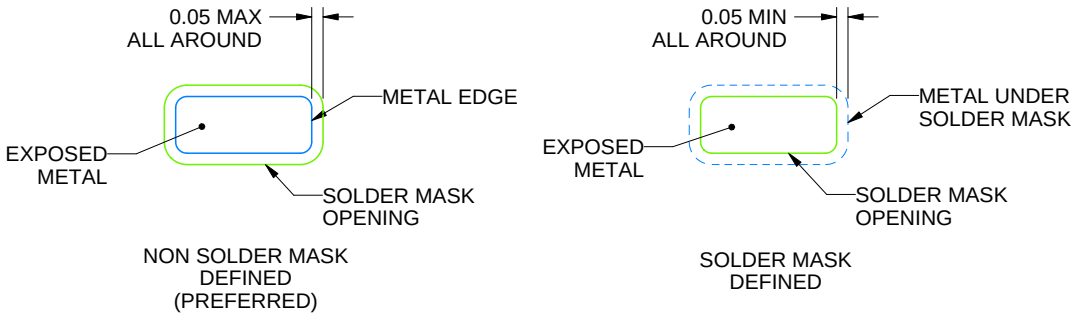


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

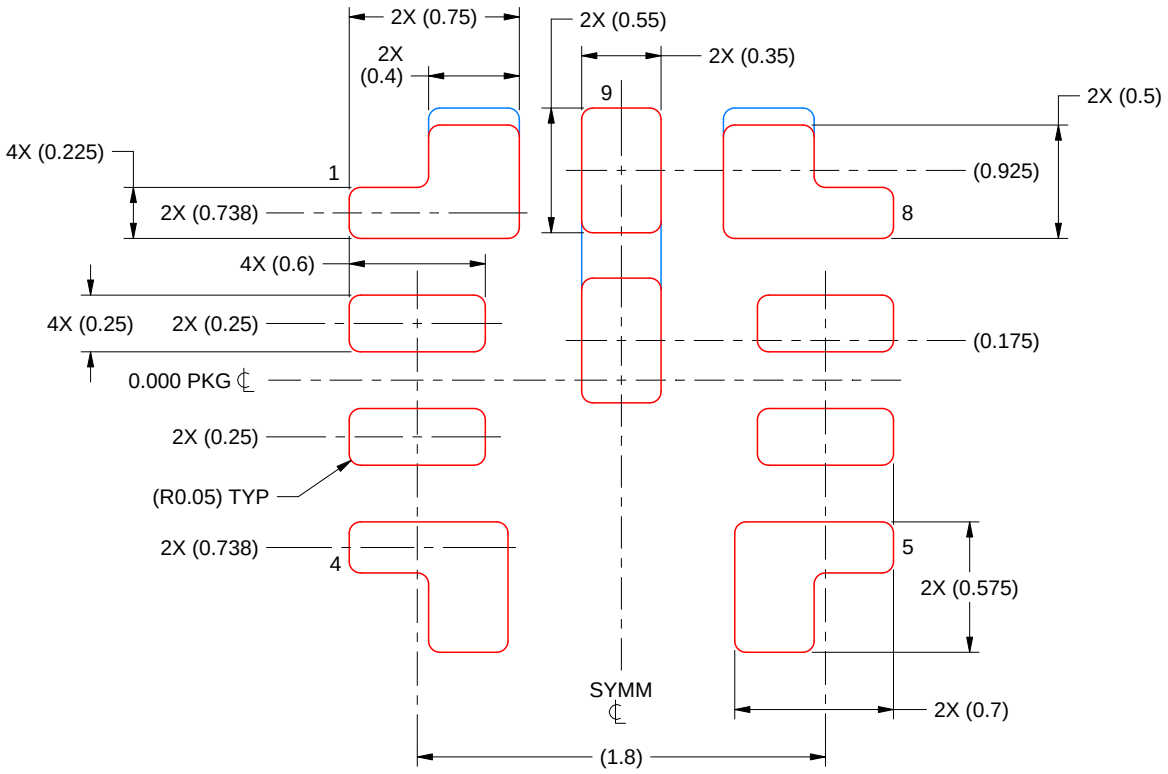


SOLDER MASK DETAILS

4227033/B 09/2023

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

PADS 1 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 9:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

DWG_NO:5/REV:5 MM_YYYY:5

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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