# LMR516x5 4.3V ～ 60V、2.5A/3.5A、同期整流降圧コンバータ、低 I$_Q$

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 堅牢な産業用アプリケーション向けの構成：
  - 入力電圧範囲：4.3V～60V
  - 連続出力電流：2.5A または 3.5A
  - 低い動作時静止電流：29µA
  - 最小スイッチング オン時間：70ns
  - スイッチング周波数：400kHz および 1.1MHz
  - 周波数スペクトラム拡散 (PFM バリエーション)
  - 接合部温度範囲：-40℃～150℃
  - 最大デューティ サイクル：96%
  - プリバイアスされた出力への単調スタートアップ
  - ヒカップ モードによる短絡保護
  - 高精度のイネーブル
  - 基準電圧の許容誤差：±1%
- 小型の設計サイズと使いやすさ：
  - 同期整流器内蔵
  - 使いやすさを実現した内部補償
  - SOT-23 パッケージ
- ピン互換パッケージの各種オプション
  - PFM および強制 PWM (FPWM) オプション
- WEBENCH® Power Designer により、LMR516x5 を使用するカスタム設計を作成

2 アプリケーション

- 主な家電製品
- PLC、DCS、PAC
- スマート メーター
- V$_{IN}$ が広い汎用電源
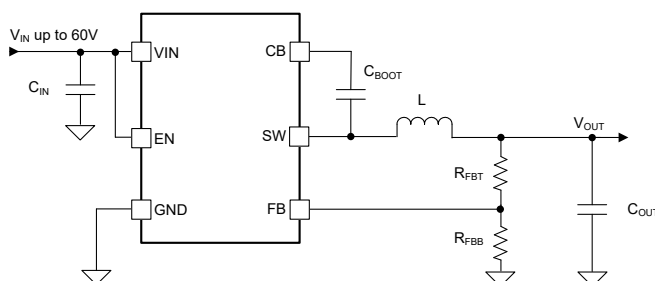
3 概要

LMR516x5 は、最大 2.5A または 3.5A の負荷電流を駆動でき、V$_{IN}$ が広く使いやすい同期整流降圧コンバータです。このデバイスは、4.3V～60V の広い入力電圧範囲で動作し、レギュレートされていない電源からの電源調整を行うさまざまな産業用アプリケーションに適しています。
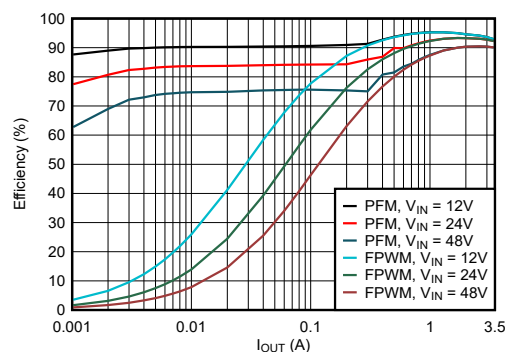
LMR516x5 は、400kHz または 1.1MHz のスイッチング周波数で動作し、比較的小型のインダクタを使用でき、設計サイズの最適化が可能です。このデバイスは、軽負荷時に高効率を実現するパルス周波数変調 (PFM バージョン)と、一定の周波数を維持しながら負荷範囲全体にわたって出力電圧リップルを小さくできる強制パルス幅変調 (PFM バージョン)を備えており、ソフト・スタートと補償回路が内部に実装されており、最小限の外付け部品で使用できます。

このデバイスには、サイクル単位の電流制限、ヒカップ モード短絡保護、過剰な電力消費時のサーマル シャットダウンなどの保護機能が組み込まれています。

製品情報

部品番号 [3]	パッケージ[1]	パッケージ サイズ[2]
LMR51625	DDC (SOT-23-THN、6)	2.9mm × 2.8mm
LMR51635		

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。
(3) デバイス比較表を参照してください。

概略回路図

効率と出力電流との関係、
V$_{OUT}$ = 5V、400kHz

Table of Contents

Product Folder Links: *LMR51625 LMR51635*

English Data Sheet: SLUSF64

4 Device Comparison Table

ORDERABLE PART NUMBER	OUTPUT CURRENT	FREQUENCY	PFM OR FPWM	SPREAD SPECTRUM	OUTPUT
LMR51625XDDCR	2.5A	400kHz	PFM	Yes	Adjustable
LMR51625XFDDCR	2.5A	400kHz	FPWM	No	Adjustable
LMR51625YDDCR	2.5A	1100kHz	PFM	Yes	Adjustable
LMR51625YFDDCR	2.5A	1100kHz	FPWM	No	Adjustable
LMR51635XDDCR	3.5A	400kHz	PFM	Yes	Adjustable
LMR51635XFDDCR	3.5A	400kHz	FPWM	No	Adjustable
LMR51635YDDCR	3.5A	1100kHz	PFM	Yes	Adjustable
LMR51635YFDDCR	3.5A	1100kHz	FPWM	No	Adjustable

5 Pin Configuration and Functions
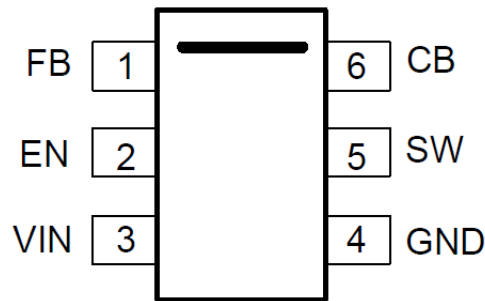
図 5-1. 6-Pin SOT-23-THN, DDC Package (Top View)

表 5-1. Pin Functions

PIN NAME	NO	TYPE[1]	DESCRIPTION
FB	1	A	Feedback input to the converter. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
EN	2	A	Precision enable input to the converter. Do not float. High = On, low = Off. Can be tied to VIN. Precision enable input allows an adjustable UVLO by an external resistor divider.
VIN	3	P	Supply input pin to the internal bias LDO and high-side FET. Connect to the input supply and input bypass capacitors C_{IN}. Input bypass capacitors must be directly connected to this pin and GND.
GND	4	G	Power ground pins. Connected to the source of low-side FET internally. Connect to system ground, ground side of C_{IN} and C_{OUT}. The path to C_{IN} must be as short as possible.
SW	5	P	Switching output of the converter. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to the power inductor.
CB	6	P	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.

(1) A = Analog, P = Power, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

Over junction temperature range of –40°C to 150°C (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	VIN to GND	–0.3	63	V
Input voltage	EN to GND	–0.3	V_{IN} + 0.3	V
Input voltage	FB to GND	–0.3	5.5	V
Output voltage	SW to GND	–0.3	63	V
Output voltage	SW to GND less than 10ns transients	–3.5	65	V
Output voltage	CB to SW	–0.3	5.5	V
Junction temperature T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)[1]

		MIN	NOM	MAX	UNIT
Input voltage	VIN to GND	4.3		60	V
Input voltage	EN	0		V_{IN}	V
Input voltage	FB	0		4.5	V
Output voltage	V_{OUT} [2]	0.8		30	V
Output current	I_{OUT} (LM51625)[3]		2.5		A
Output current	I_{OUT} (LM51635) [3]		3.5		A
T_J	Operating junction temperature[4]	–40		+150	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not specify specific performance limits. For compliant specifications, see Electrical Characteristics table.
(2) Under no conditions can the output voltage be allowed to fall below zero volts.
(3) Maximum continuous DC current can be derated when operating with high switching frequency or high ambient temperature. See Application section for details.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 150℃.

6.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. These values do not represent the performance obtained in an actual application. For example, with a 4-layer PCB, a $R_{\theta JA}$ = 48.5°C/W can be achieved.

THERMAL METRIC[1]		LMR516x5	UNIT
		DDC(SOT-23-THN)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.2	°C/W
$R_{\theta JA(effective)}$	Junction-to-ambient thermal resistance with TI EVM	48.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits[1] are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.3V to 60V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current (non-switching) [2]	V_{EN} = 3V, PFM variant only		26	46	µA
I_{SUPPLY}	Input supply current when in regulation[3]	V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0A, R_{FBT} = 1MΩ, PFM variant		29		µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0V		2.0		µA
UVLO						
$V_{IN\_UVLO(R)}$	V_{IN} UVLO rising threshold	V_{IN} rising		4.0	4.25	V
$V_{IN\_UVLO(F)}$	V_{IN} UVLO falling threshold	V_{IN} falling		3.8		V
$V_{IN\_UVLO(H)}$	V_{IN} UVLO hysteresis			0.2		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.103	1.226	1.349	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.887	0.985	1.084	V
$I_{EN(P2)}$	EN pin sourcing current post EN rising threshold	V_{EN} = 3V		10	50	nA
REFERENCE VOLTAGE						
V_{FB}	Reference voltage		0.792	0.8	0.808	V
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 0.8V		0.2		nA
SWITCHING FREQUENCY						
$f_{SW1(CCM)}$	Switching frequency, CCM operation	"Y" version, V_{IN} = 24V	0.99	1.1	1.21	MHz
$f_{SW1(CCM)}$	Switching frequency, CCM operation	"X" version, V_{IN} = 24V	360	400	440	kHz
F_{Dither}	Switching frequency dithering[3]	PFM option, requency dithering over center frequency		±8.5%		
START-UP						
t_{SS}	Internal fixed soft-start time	The time of internal reference to increase from 0.08V to 0.72V		4.0		ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	I_{SW} = –100mA		85		mΩ

資料に関するフィードバック(ご意見やお問い合わせ)を送信　　　5

6.5 Electrical Characteristics (続き)

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits[1] are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.3V to 60V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	I_{SW} = 100mA		45		mΩ
t_{ON-MIN}	Minimum ON pulse width	V_{IN} = 24V, I_{OUT} = 1A		70		ns
t_{ON-MAX}	Maximum ON pulse width	V_{IN} = 24V, I_{OUT} = 1A		5		µs
$t_{OFF-MIN}$	Minimum OFF pulse width	V_{IN} = 24V		200		ns
CURRENT LIMITS AND HICCUP						
$I_{HS\_PK(OC)}$	High-side peak current limit [4]	3.5A version	4.2	5.1	6.0	A
	High-side peak current limit [4]	2.5A version	2.9	3.7	4.5	A
$I_{LS\_V(OC)}$	Low-side valley current limit [4]	3.5A version	3.2	4.0	4.8	A
	Low-side valley current limit [4]	2.5A version	2.3	2.8	3.3	A
$I_{LS(NOC)}$	Low-side negative current limit[4]	FPWM option, 3.5A version		–3.0		A
	Low-side negative current limit[4]	FPWM option, 2.5A version		–2.0		A
I_{ZC}	Zero-cross detection current threshold			0		A
V_{HICCUP}	FB pin voltage required to trip short circuit hiccup mode [3]			0.32		V
t_{HICCUP}	Time between current-limit hiccup burst [3]			85		ms
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold [3]	Temperature rising		165		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis [3]			20		°C

(1)   MIN and MAX limits are 100% production tested at 25℃. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2)   This is the current used by the device open loop. The value does not represent the total input current of the system when in regulation.
(3)   Not production tested. Specified by correlation by design.
(4)   The current limit values in this table are tested, open loop, in production. These values can differ from those found in a closed loop application.

6.6 Typical Characteristics

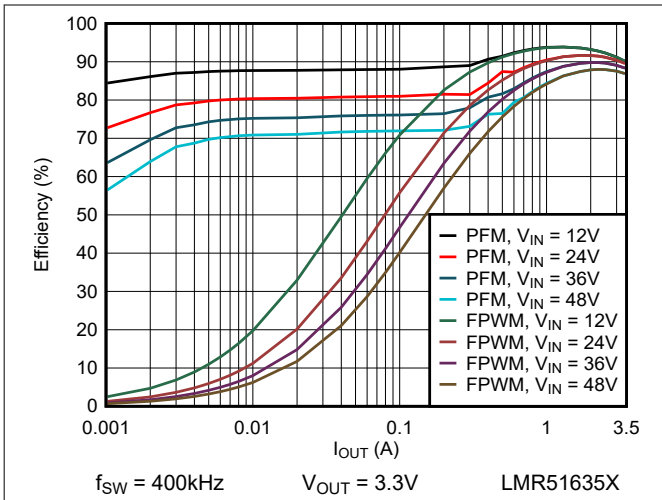V_{IN} = 24V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise specified.

f_{SW} = 400kHz V_{OUT} = 3.3V   LMR51635X

図 6-1. 3.3V Efficiency Versus Load Current

f_{SW} = 400kHz V_{OUT} = 5V   LMR51635X

図 6-2. 5V Efficiency Versus Load Current

f_{SW} = 1100kHz V_{OUT} = 3.3V   LMR51635Y

図 6-3. 3.3V Efficiency Versus Load Current

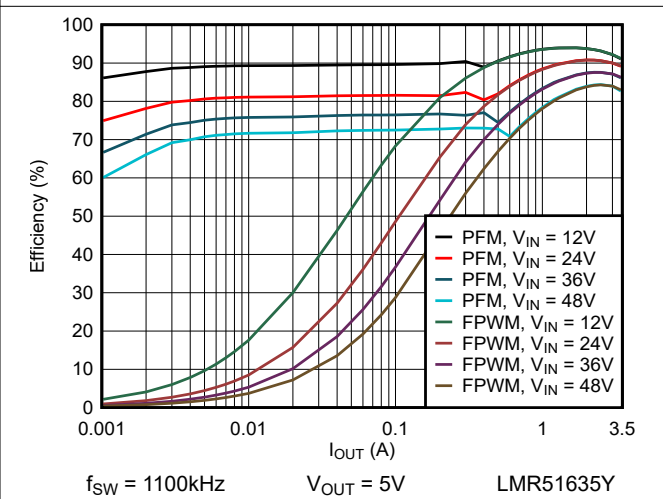
f_{SW} = 1100kHz V_{OUT} = 5V   LMR51635Y
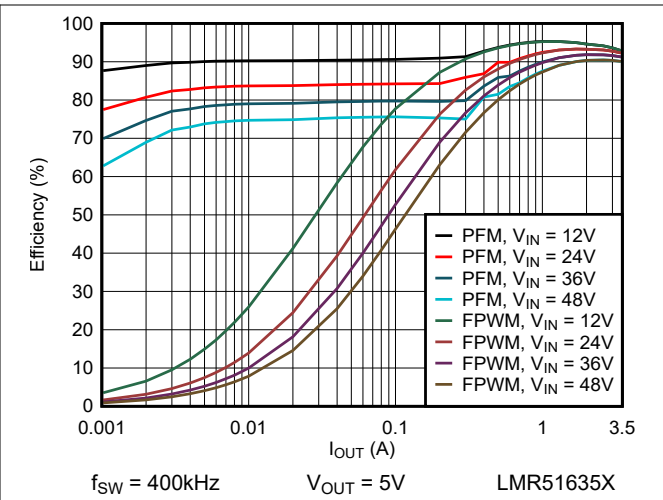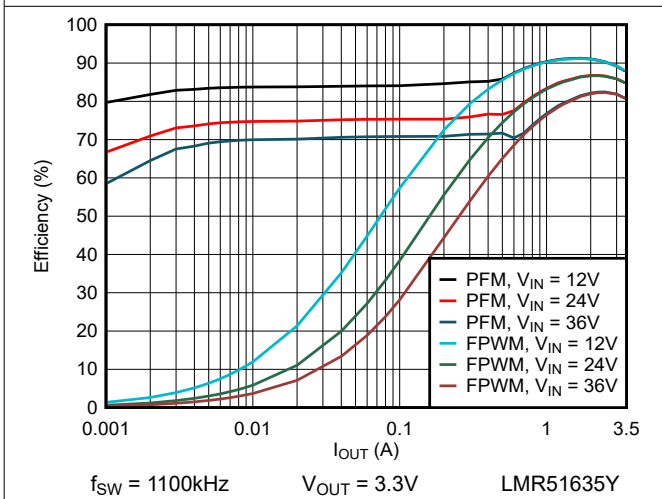
図 6-4. 5V Efficiency Versus Load Current

6.6 Typical Characteristics (continued)

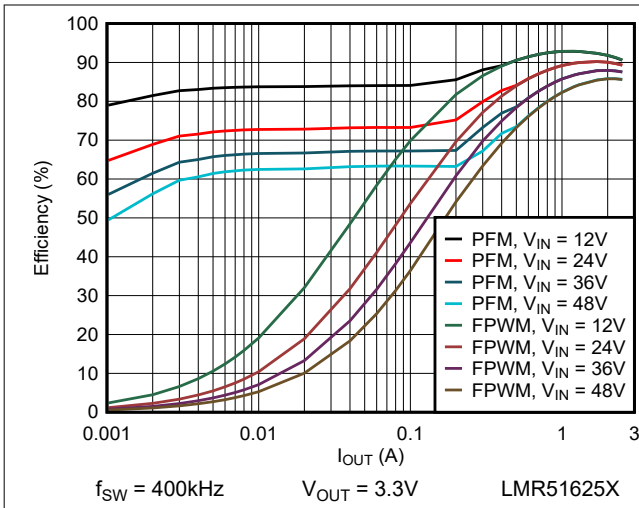V_{IN} = 24V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise specified.

f_{SW} = 400kHz V_{OUT} = 3.3V   LMR51625X

図 6-5. 3.3V Efficiency Versus Load Current

f_{SW} = 400kHz V_{OUT} = 5V   LMR51625X

図 6-6. 5V Efficiency Versus Load Current

f_{SW} = 1100kHz V_{OUT} = 3.3V   LMR51625Y

図 6-7. 3.3V Efficiency Versus Load Current

f_{SW} = 1100kHz V_{OUT} = 5V   LMR51625Y

図 6-8. 5V Efficiency Versus Load Current

f_{SW} = 400kHz V_{OUT} = 5V   LMR51635X
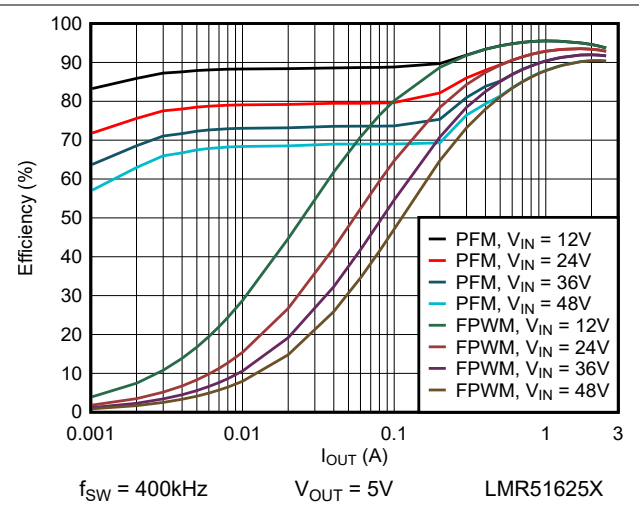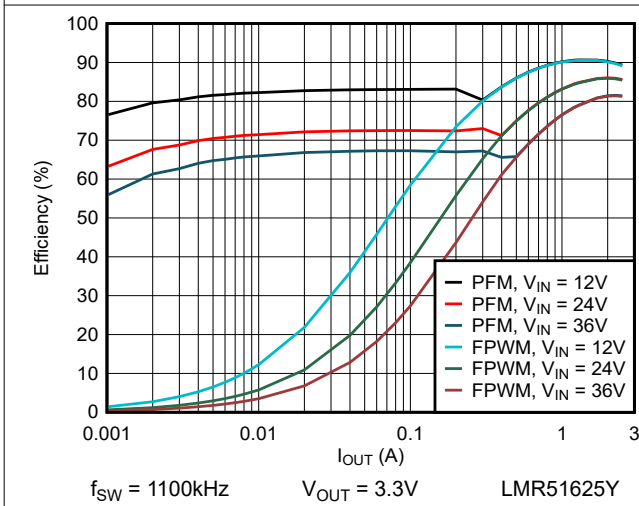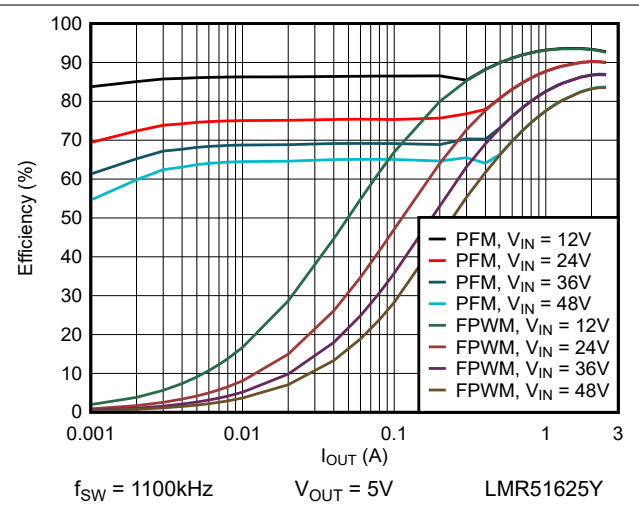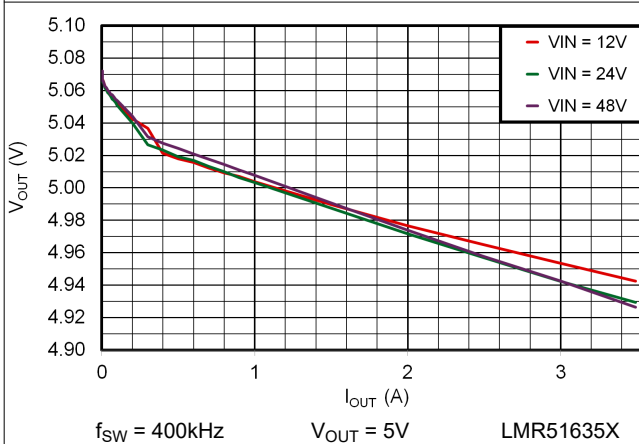
図 6-9. Line and Load Regulation

f_{SW} = 400kHz V_{OUT} = 5V   LMR51635X

図 6-10. 5V Dropout

Product Folder Links: *LMR51625 LMR51635*

English Data Sheet: SLUSF64
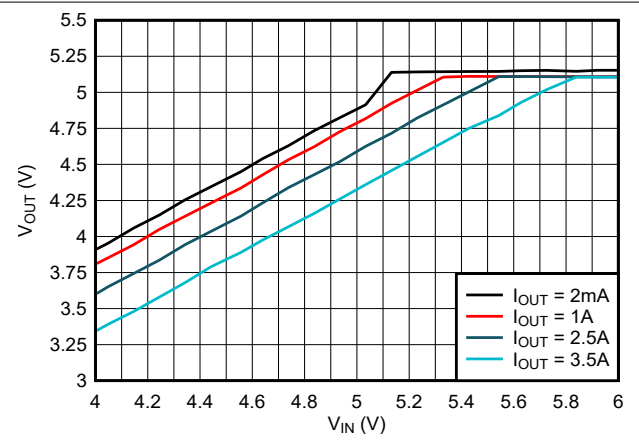
6.6 Typical Characteristics (continued)

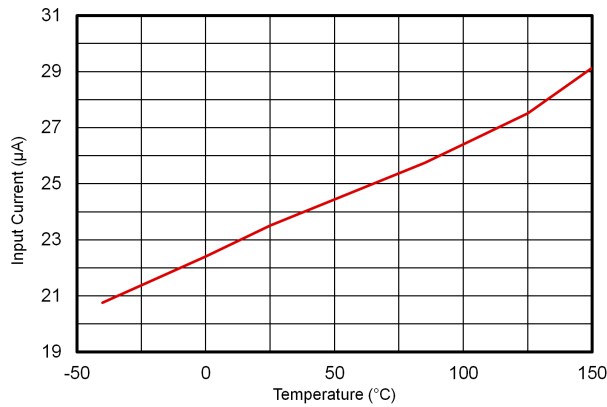V_{IN} = 24V, f_{SW} = 400kHz, T_A = 25°C, unless otherwise specified.
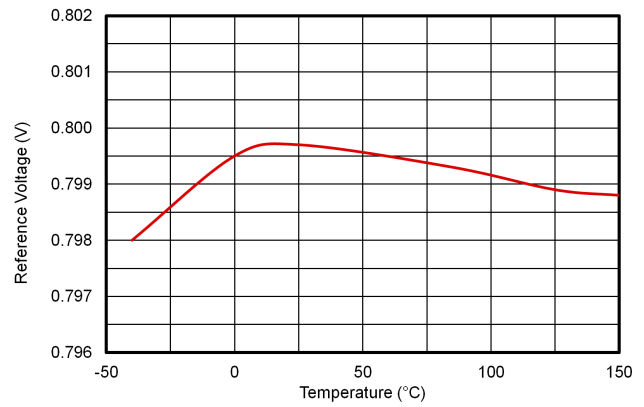
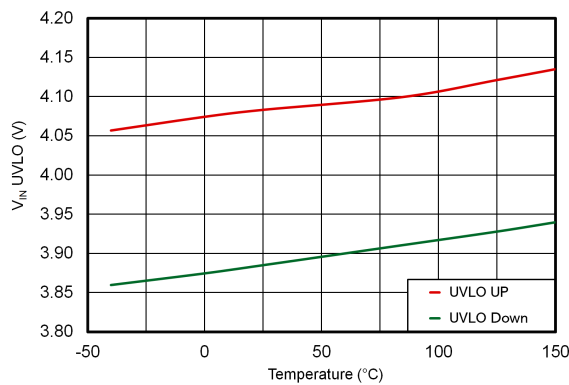図 6-11. I_Q vs Temperature

図 6-12. Reference Voltage vs Temperature

図 6-13. V_{IN} UVLO vs Temperature
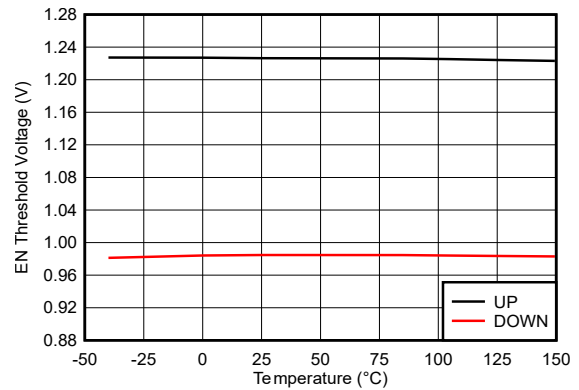
図 6-14. Precision Enable Thresholds
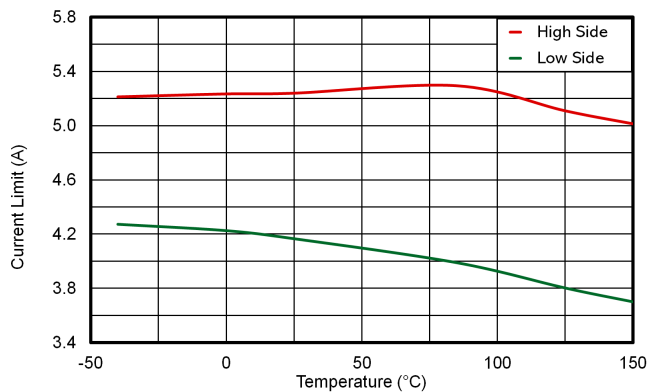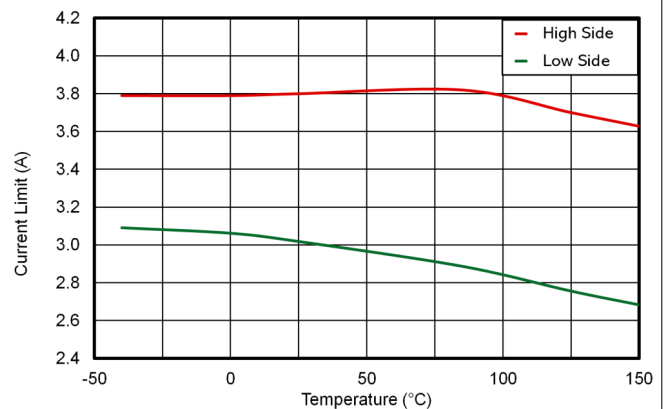
図 6-15. LMR51635 HS and LS Current Limit vs Temperature

図 6-16. LMR51625 HS and LS Current Limit vs Temperature

資料に関するフィードバック(ご意見やお問い合わせ)を送信

Product Folder Links: *LMR51625 LMR51635*

English Data Sheet: SLUSF64

7 Detailed Description

7.1 Overview

The LMR516x5 converter is an easy-to-use, synchronous, step-down, DC/DC converter operating from a 4.3V to 60V supply voltage. The LMR51635 is capable of delivering up to 3.5A DC load current in a very small design size, while the LMR51625 is capable of delivering up to 2.5A load current. The family has multiple versions applicable to various applications. See セクション 4 for detailed information.

The LMR516x5 employs fixed-frequency peak-current mode control. The PFM version enters PFM mode at light load to achieve high efficiency. The FPWM version achieves low output voltage ripple, tight output voltage regulation, and constant switching frequency at light load. The device is internally compensated, which reduces design time and requires few external components.

Additional features, such as precision enable and internal soft start, provide a flexible and easy-to-use design for a wide range of applications. Protection features include the following:

- Thermal shutdown
- V_{IN} undervoltage lockout
- Cycle-by-cycle current limit
- Hiccup mode short-circuit protection

This family of devices requires very few external components and has a pinout designed for simple, optimal PCB layout.

7.2 Functional Block Diagram

Product Folder Links: *LMR51625 LMR51635*

English Data Sheet: *SLUSF64*
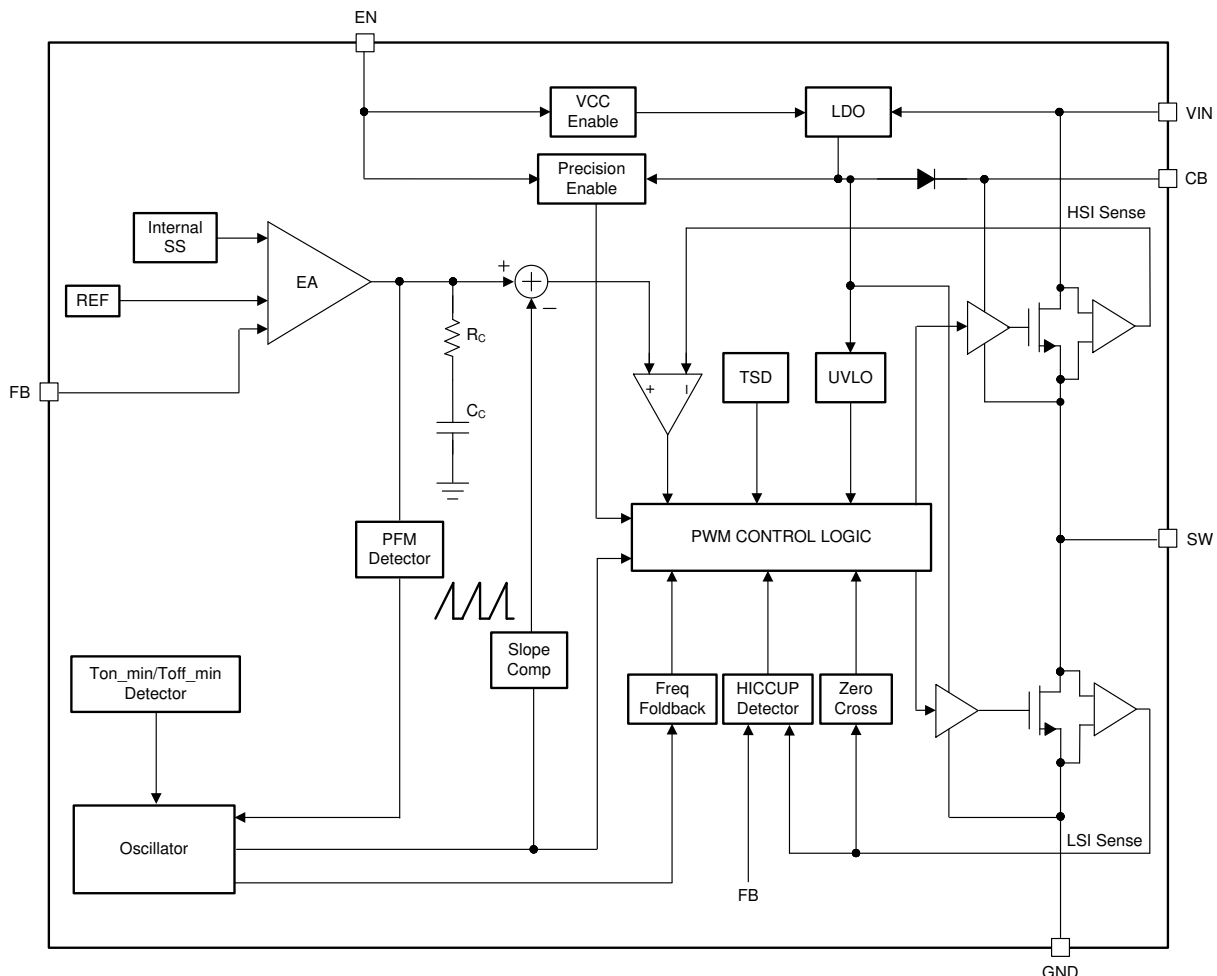
7.3 Feature Description

7.3.1 Fixed Frequency Peak Current Mode Control

The following operating description of the LMR516x5 refers to セクション 7.2 and to the waveforms in 図 7-1. The LMR516x5 is a step-down, synchronous, buck converter with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LMR516x5 supplies a regulated output voltage by turning on the high-side and low-side NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope of $(V_{IN} - V_{OUT}) / L$. When the high-side switch is turned off by the control logic, the low-side switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the low-side switch with a slope of $-V_{OUT} / L$. The control parameter of a buck converter is defined as Duty Cycle $D = t_{ON} / T_{SW}$, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.
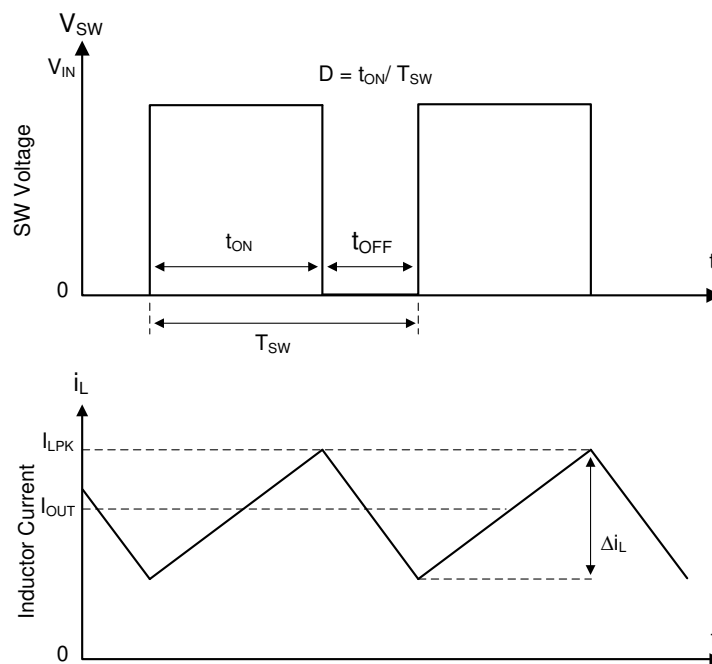

図 7-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LMR516x5 employs fixed-frequency peak-current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak-current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, making designing easy and providing stable operation when using a variety of output capacitors. The converter operates with fixed switching frequency at normal load conditions. During light-load condition, the LMR51635 operates in PFM mode to maintain high efficiency (PFM version) or in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency (FPWM version).

7.3.2 Adjustable Output Voltage

A precision 0.8V reference voltage (V_{REF}) is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from V_{OUT} to the FB pin. TI recommends to use 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor, R_{FBB}, for the desired divider current and use 式 1 to calculate the top-side resistor, R_{FBT}. The recommended range for R_{FBT} is 10kΩ to 100kΩ. A lower R_{FBT} value can be used if pre-loading is desired to reduce the V_{OUT} offset in PFM operation. Lower R_{FBT} values reduce efficiency at very light load. Less static

current goes through a larger R_{FBT} value and can be more desirable when light-load efficiency is critical. However, TI does not recommend R_{FBT} values larger than 1MΩ because R_{FBT} values larger than 1MΩ make the feedback path more susceptible to noise. Larger R_{FBT} values require a more carefully designed feedback path trace from the feedback resistors to the feedback pin of the device. The tolerance and temperature variation of the resistor divider network affect the output voltage regulation.
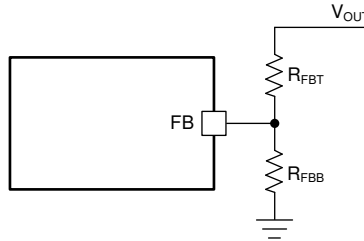

図 7-2. Output Voltage Setting

$$R_{FBT} = \frac{(V_{OUT} - V_{REF})}{V_{REF}} \times R_{FBB} \tag{1}$$

7.3.3 Enable

The voltage on the EN pin controls the ON, OFF operation of the LMR516x5. A voltage of less than 0.88V shuts down the device, while a voltage of greater than 1.35V is required to start the converter. The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the LMR516x5 is to connect EN to VIN. This connection allows self-start-up of the LMR516x5 when V_{IN} is within the operating range.

Many applications benefit from the employment of an enable divider, R_{ENT} and R_{ENB} (図 7-3) to establish a precision system UVLO level for the converter. A system UVLO can be used for supplies operating from utility power as well as battery power. A system UVLO can be used for sequencing, making sure of reliable operation, or supplying protection, such as a battery discharge level. An external logic signal can also be used to drive the EN input for system sequencing and protection.

注

The EN pin voltage must not to be greater than V_{IN} + 0.3V. TI does not recommend to apply EN voltage when V_{IN} is 0V.
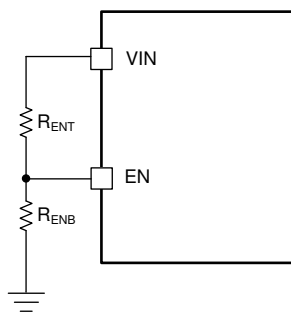
図 7-3. System UVLO by Enable Divider

7.3.4 Minimum ON Time, Minimum OFF Time, and Frequency Foldback

The minimum ON time (t_{ON-MIN}) is the shortest duration of time that the high-side switch can be turned on. t_{ON-MIN} is typically 70ns for the LMR516x5. The minimum OFF time ($t_{OFF-MIN}$) is the shortest duration of time that the high-side switch can be off. $t_{OFF-MIN}$ is typically 200ns. In CCM operation, t_{ON-MIN} and $t_{OFF-MIN}$ limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

Product Folder Links: *LMR51625 LMR51635*

English Data Sheet: SLUSF64

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \tag{2}$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW} \tag{3}$$

Given a required output voltage, the maximum V_{IN} without frequency foldback can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}} \tag{4}$$

The minimum V_{IN} without frequency foldback can be calculated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\_MIN}} \tag{5}$$

In the LMR516x5, a frequency foldback scheme is employed once the t_{ON-MIN} or $t_{OFF-MIN}$ is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle.

The on time decreases while V_{IN} voltage increases. Once the on time decreases to t_{ON-MIN}, the switching frequency starts to decrease while V_{IN} continues to go up, which lowers the duty cycle further to keep V_{OUT} in regulation according to 式 2.

The frequency foldback scheme also works after larger duty cycle is needed under a low V_{IN} condition. The frequency decreases after the device hits the $t_{OFF-MIN}$, which extends the maximum duty cycle according to 式 3. In such condition, the frequency can be as low as approximately 190kHz. A wide range of frequency foldback allows for the LMR516x5 output voltage to stay in regulation with a much lower supply voltage V_{IN}, which leads to a lower effective dropout.

With frequency foldback while maintaining a regulated output voltage, V_{IN_MAX} is raised and V_{IN_MIN} is lowered by decreased f_{SW}.

7.3.5 Bootstrap Voltage

The LMR516x5 provides an integrated bootstrap voltage converter. A small capacitor between the CB and SW pins provides the gate drive voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch is on. The recommended value of the bootstrap capacitor is 0.1µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16V for stable performance over temperature and voltage.

7.3.6 Overcurrent and Short-Circuit Protection

The LMR516x5 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The high-side switch current is sensed when the high-side is turned on after a set blanking time. The high-side switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. See セクション 7.2 for more details. The peak current of high-side switch is limited by a clamped maximum peak current threshold I_{sc} which is constant.

The current going through the low-side MOSFET is also sensed and monitored. When the low-side switch turns on, the inductor current begins to ramp down. The low-side switch is not turned OFF at the end of a switching cycle if the current is above the low-side current limit, I_{LS_LIMIT}. The low-side switch is kept ON so that inductor current keeps ramping down until the inductor current ramps below I_{LS_LIMIT}. Then, the low-side switch is turned

OFF and the high-side switch is turned on after a dead time. After I_{LS_LIMIT} is achieved, peak and valley current limit controls the maximum current delivered and can be calculated using 式 6.

$$I_{OUT\_MAX} = \frac{I_{LS\_LIMIT} + I_{SC}}{2} \qquad (6)$$

If the feedback voltage is lower than 40% of the V_{REF}, the current of the low-side switch triggers I_{LS_LIMIT} for 64 consecutive cycles and hiccup current protection mode is activated. In hiccup mode, the converter shuts down and keeps off for a period of hiccup, T_{HICCUP}, (85ms typical) before the LMR516x5 tries to start again. If overcurrent or a short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, preventing overheating and potential damage to the device.

For the FPWM version, the inductor current is allowed to go negative. When this current exceeds the low-side negative current limit, I_{LS_NEG}, the low-side switch is turned off and high-side switch is turned on immediately. This is used to protect the low-side switch from excessive negative current.

7.3.7 Soft Start

The integrated soft-start circuit prevents input inrush current impacting the LMR516x5 and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. The typical soft-start time is 4ms.

The LMR516x5 also employs overcurrent protection blanking time, T_{OCP_BLK} (8ms typical), at the beginning of power up. Without this feature, in applications with a large amount of output capacitors and high V_{OUT}, the inrush current is large enough to trigger the current-limit protection, which can cause a false start as the device enters into hiccup mode. This action results in a continuous recycling of soft start without raising up to the programmed output voltage. The LMR516x5 is able to charge the output capacitor to the programmed V_{OUT} by controlling the average inductor current during the start-up sequence in the blanking time, T_{OCP_BLK}.

7.3.8 Thermal Shutdown

The LMR516x5 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 165°C. Both high-side and low-side FETs stop switching in thermal shutdown. After the die temperature falls below 145°C, the device reinitiates the power-up sequence controlled by the internal soft-start circuitry.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical ON, OFF control for the LMR516x5. When V_{EN} is below 0.88V, the device is in shutdown mode. The LMR516x5 also employs V_{IN} undervoltage lockout protection (UVLO). If V_{IN} voltage is below the UVLO threshold of 3.8V(typical), the converter is turned off.

7.4.2 Active Mode

The LMR516x5 is in active mode when both V_{EN} and V_{IN} are above the respective operating threshold. The simplest way to enable the LMR516x5 is to connect the EN pin to VIN pin. This connection allows self-start-up when the input voltage is in the operating range of 4.3V to 60V. See セクション 7.3.3 for details on setting these operating levels.

In active mode, depending on the load current, the LMR516x5 is in one of four modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is greater than half of the peak-to-peak inductor current ripple (for both PFM and FPWM versions)
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is less than half of the peak-to-peak inductor current ripple(only for PFM version)
3. Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load (only for PFM version)
4. Forced pulse width modulation mode (FPWM) with fixed switching frequency even at light load (only for FPWM version)

7.4.3 CCM Mode

Continuous conduction mode (CCM) operation is employed in the LMR516x5 when the load current is greater than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode and the maximum output current of 2.5A or 3.5A can be supplied by the LMR51625 or LMR51635 respectively.

7.4.4 Light Load Operation (PFM Version)

For the PFM version, when the load current is lower than half of the peak-to-peak inductor current in CCM, the LMR516x5 operates in discontinuous conduction mode (DCM), also known as diode emulation mode (DEM). In DCM operation, the low-side switch is turned off when the inductor current drops to I_{LS_ZC} (0mA typical) to improve efficiency. Both switching losses and conduction losses are reduced in DCM, compared to forced PWM operation at light load.

During light load operation, pulse frequency modulation (PFM) mode is activated to maintain high efficiency operation. When either the minimum high-side switch ON time t_{ON-MIN} or the minimum peak inductor current I_{PEAK_MIN} (typically 600mA for LMR51625 or 800mA for LMR51635) is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to a significant drop in effective switching frequency.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMR516x5 is a step-down DC-to-DC converter to convert a higher input voltage to a lower output DC voltage with a maximum output current of 2.5A for LMR51625 or 3.5A for LMR51635. The following design procedure can be used to select components for the LMR51635. Alternately, the WEBENCH software can be used to generate complete designs. When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. Go to ti.com for more details.

8.2 Typical Application

The LMR51635 only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. 図 8-1 shows a basic schematic.
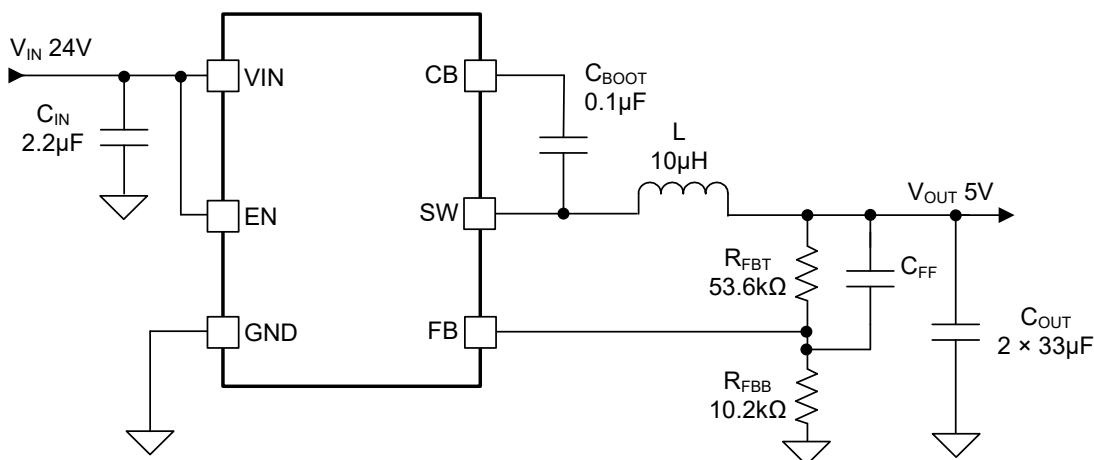

図 8-1. Application Circuit

The external components must fulfill the needs of the application and the stability criteria of the control loop of the device. 表 8-1 and 表 8-2 can be used to simplify the output filter component selection.

表 8-1. Typical External Component Values for LMR51625, 2.5A Output Current

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} [1]	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{FF}
400	3.3	10	2 × 33uF / 10V	31.6	10.2	Open
	5	15	2 × 22uF / 16V	53.6	10.2	Open
	12	22	22uF / 35V	143	10.2	Open
1100	3.3	3.3	33uF / 10V	31.6	10.2	Open
	5	4.7	22uF / 16V	53.6	10.2	Open

(1) Ceramic capacitor is used in this table. All the C_{OUT} values are after derating.

Product Folder Links: *LMR51625 LMR51635*

English Data Sheet: SLUSF64

表 8-2. Typical External Component Values for LMR51635, 3.5A Output Current

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} [1]	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{FF}
400	3.3	5.6	2 × 47uF / 10V	31.6	10.2	Open
	5	10	2 × 33uF / 16V	53.6	10.2	Open
	12	15	10uF + 22uF / 35V	143	10.2	Open
1100	3.3	2.2	2 × 22uF / 10V	31.6	10.2	Open
	5	3.3	33uF / 16V	53.6	10.2	Open

(1)   Ceramic capacitor is used in this table. All the C_{OUT} values are after derating.

8.2.1 Design Requirements

The detailed design procedure is described based on a design example. For this design example, use the parameters listed in 表 8-3 as the input parameters.

表 8-3. Design Example Parameters

PARAMETER	VALUE
Input voltage, V_{IN}	24V typical, range from 6V to 60V
Output voltage, V_{OUT}	5V ±3%
Maximum output current, I_{OUT_MAX}	3.5A
Output overshoot, undershoot (0.87A to 2.63A)	5%
Output voltage ripple	0.5%
Operating frequency	400kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR516x5 device with the WEBENCH® Power Designer.

1.   Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2.   Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3.   Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

• Run electrical simulations to see important waveforms and circuit performance
• Run thermal simulations to understand board thermal performance
• Export customized schematic and layout into popular CAD formats
• Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Set-Point

The output voltage of the LMR51635 device is externally adjustable using a resistor divider network. The divider network is comprised of a top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. 式 7 is used to determine the output voltage of the converter:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \tag{7}$$

Choose the value of R_{FBB} to be 10.2kΩ. With the desired output voltage set to 5V and the V_{REF} = 0.8V, the R_{FBT} value can then be calculated using 式 7. The formula yields to a value 53.55kΩ, a standard value of 53.6kΩ is selected.

8.2.2.3 Switching Frequency

The higher switching frequency allows for lower value inductors and smaller output capacitors, which results in smaller design size and lower component cost. However, higher switching frequency brings more switching loss, making the design less efficient and produce more heat. The switching frequency is also limited by the minimum on time of the integrated power switch, the input voltage, the output voltage, and the frequency shift limitation as mentioned in セクション 7.3.4.

For this example, the default switching frequency of 400kHz is selected.

8.2.2.4 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use 式 9 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} must be 20% to 60% of maximum I_{OUT} supported by converter. During an instantaneous overcurrent operation event, the RMS and peak inductor current can be high. The inductor saturation current must be higher than peak current limit level.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \tag{8}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{9}$$

In general, choosing lower inductance in switching power supplies is preferable because this choice usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. Too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered. Too low of an inductance also generates more inductor core loss because the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, TI recommends to have adequate amount of inductor ripple current. A larger inductor ripple current improves the comparator signal-to-noise ratio.

For this design example, choose K_{IND} = 0.35. The minimum inductor value is calculated to be 9.35µH. Choose the nearest standard 10µH power inductor with a capability of 4.2A RMS current and 6A saturation current.

8.2.2.5 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. Minimizing the output capacitance to keep cost and size down is generally desirable. The output capacitor or capacitors, C_{OUT}, must be chosen with care because the choice directly affects the steady state output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient. The output voltage ripple is essentially composed of two parts. One part is caused by the inductor ripple current flowing through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \tag{10}$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{11}$$

The two components of the voltage ripple are not in-phase, therefore, the actual peak-to-peak ripple is less than the sum of the two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rates. When a large load step occurs, output

capacitors provide the required charge before the inductor current can slew to an appropriate level. The control loop of the converter usually requires eight or more clock cycles to regulate the inductor current equal to the new load level during this time. The output capacitance must be large enough to supply the current difference for eight clock cycles to maintain the output voltage within the specified range. 式 12 shows the minimum output capacitance needed for a specified V_{OUT} overshoot and undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times (I_{OH} - I_{OL})}{f_{SW} \times \Delta V_{OUT\_SHOOT}}$$

(12)

where

- K_{IND} = Ripple ratio of the inductor current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{OUT_SHOOT} = Target output voltage overshoot or undershoot

For this design example, the target output ripple is 25mV. Assuming $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 25mV, choose K_{IND} = 0.35. 式 10 yields ESR no larger than 20mΩ and 式 11 yields C_{OUT} no smaller than 15.2µF. For the target overshoot and undershoot limitation of this design, ΔV_{OUT_SHOOT} is 250mV. The C_{OUT} can be calculated to be no less than 70µF by 式 12. Two 33µF, 16V ceramic capacitors are used.

8.2.2.6 Input Capacitor Selection

The LMR51635 requires a high frequency input decoupling capacitor and a bulk capacitor is needed depending on the application. The typical recommended value for the high frequency decoupling capacitor is 2.2µF or higher. TI recommends a high-quality ceramic type X5R or X7R with sufficiency voltage rating. The voltage rating must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, normally a voltage rating of twice the maximum input voltage is recommended. For this design, two 2.2µF, X7R dielectric capacitor rated for 100V is used for the input decoupling capacitor. The equivalent series resistance (ESR) is approximately 10mΩ, and the current rating is 1A. Include a capacitor with a value of 0.1µF for high-frequency filtering and place as close as possible to the device pins.

8.2.2.7 Bootstrap Capacitor

Every LMR516x5 design requires a bootstrap capacitor, C_{BOOT}. The recommended bootstrap capacitor is 0.1µF and rated at 16V or higher. The bootstrap capacitor is located between the SW pin and the CB pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

8.2.2.8 Undervoltage Lockout Set-Point

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. Use the following equation to determine the V_{IN} UVLO level.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{EBT} + R_{ENB}}{R_{ENB}}$$

(13)

The EN rising threshold (V_{ENH}) for LMR516x5 is set to be 1.226V (typical). Choose a value of 100kΩ for R_{ENB} to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6.0V, then the value of R_{ENT} can be calculated using :

$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{EN(R)}} - 1\right) \times R_{ENB}$$

(14)

The above equation yields a value of 389.4kΩ. A standard value of 390kΩ is selected. The resulting falling UVLO threshold, equal to 4.83V, can be calculated by 式 15 where EN hysteresis voltage, V_{EN_HYS}, is 0.241V (typical).

$$V_{IN\_FALLING} = V_{EN(F)} \times \frac{R_{EBT} + R_{ENB}}{R_{ENB}}$$

(15)

Product Folder Links: *LMR51625 LMR51635*

English Data Sheet: SLUSF64

8.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 400kHz, L = 10µH, C_{OUT} = 2 × 33µF, T_A = 25°C.
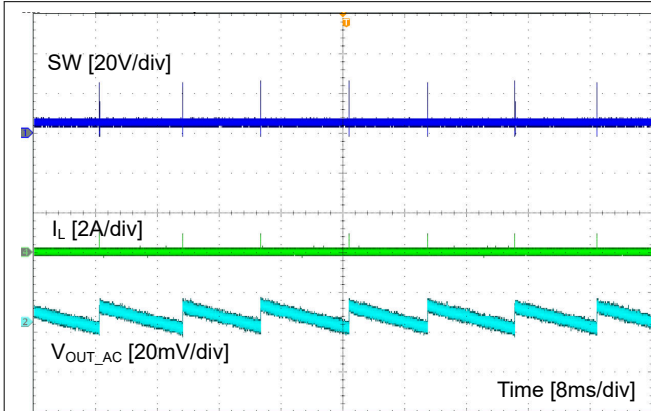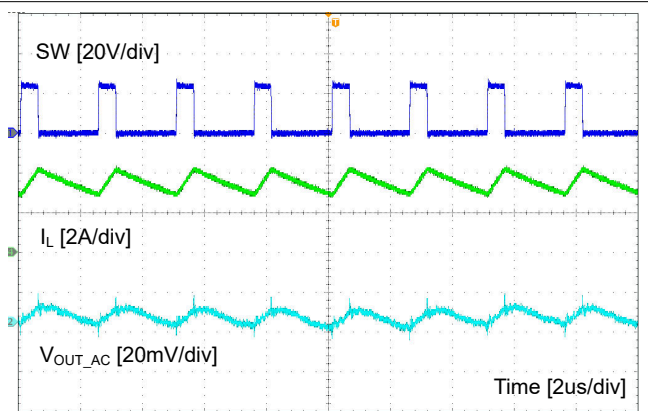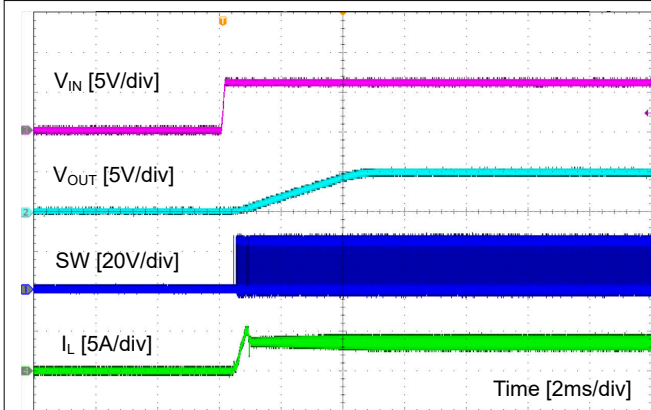

図 8-2. Ripple at No Load

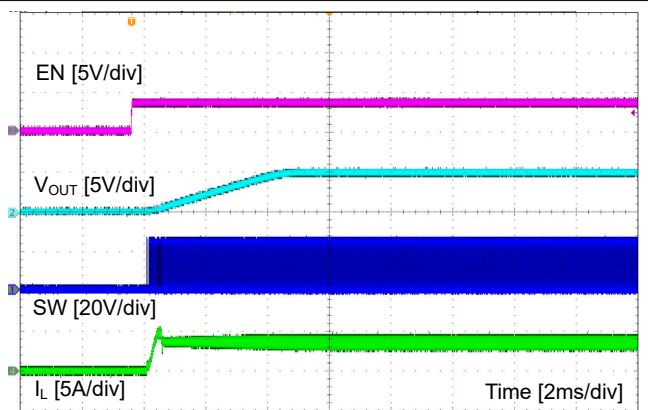図 8-3. Ripple at Full Load

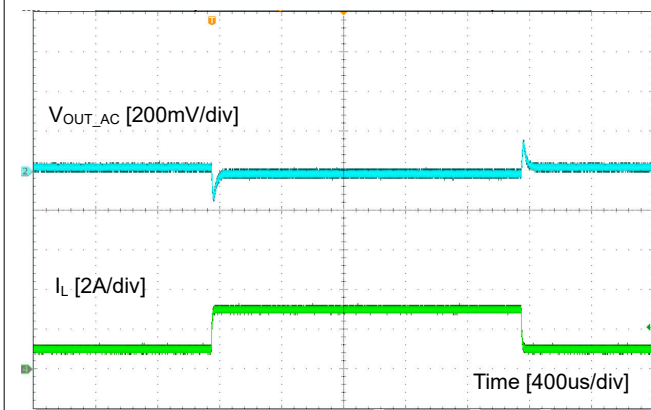図 8-4. Start-Up by V_{IN}
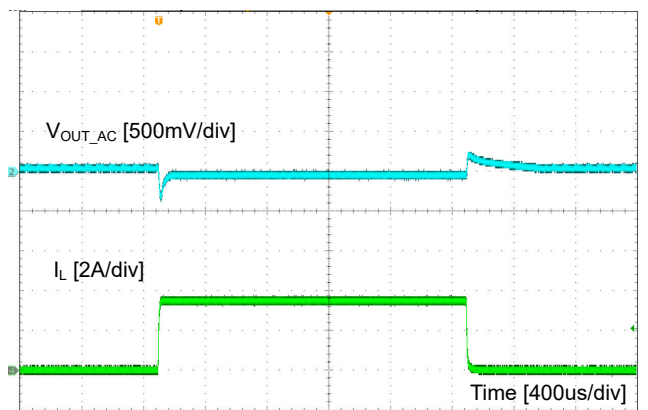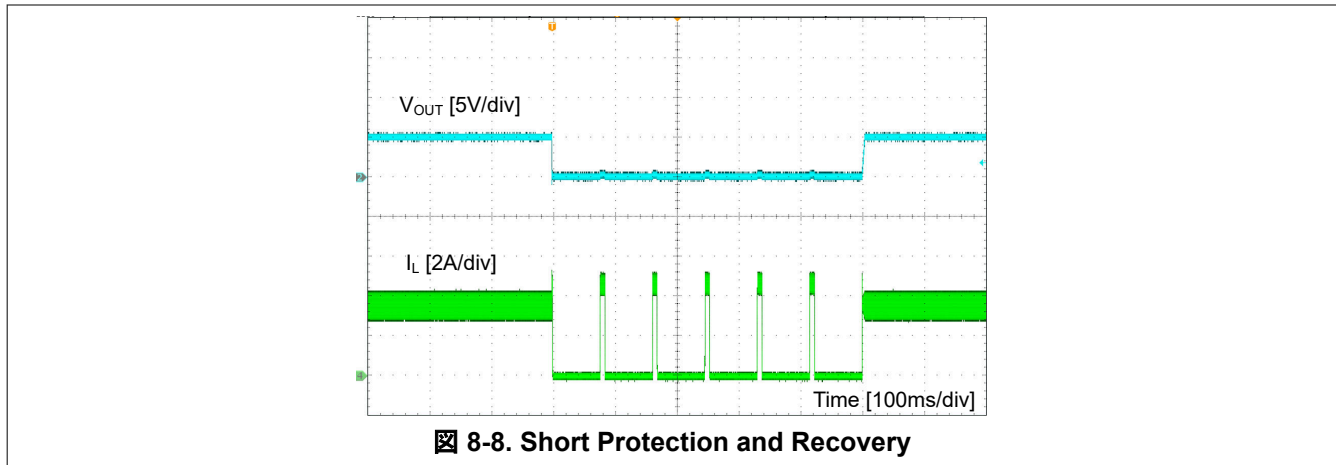

図 8-5. Start-Up by EN

図 8-6. Load Transient

図 8-7. Load Transient

図 8-8. Short Protection and Recovery

8.3 Power Supply Recommendations

The LMR516x5 is designed to operate from an input voltage supply range between 4.3V and 60V. This input supply must be well-regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR516x5 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR516x5 additional bulk capacitance can be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 10µF or 22µF electrolytic capacitor is a typical choice.

8.4 Layout

8.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

- Place the input bypass capacitor C_{IN} as close as possible to the VIN and GND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the GND pin.
- Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB}, must be located close to the FB pin. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
- Use ground plane in one of the middle layers as noise shielding and heat dissipation path if possible.
- Make V_{IN}, V_{OUT}, and ground bus connections as wide as possible. This action reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- Provide enough PCB area for proper heat sinkin. *Note that the package of this device dissipates heat through all pins*. Wide traces must be used for all pins except where noise considerations dictate minimization of area. Use an array of heat-sinking vias to connect the top side ground plane to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Make sure enough copper area is used for heat-sinking to keep the junction temperature below 150°C.

8.4.1.1 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more EMI is generated. High frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing a ceramic bypass capacitor or capacitors as close as possible to the VIN and GND pins is the key to EMI reduction.

The SW pin connecting to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for high current

Product Folder Links: *LMR51625 LMR51635*

English Data Sheet: *SLUSF64*

conduction path to minimize parasitic resistance. The output capacitors must be placed close to the V_{OUT} end of the inductor and closely grounded to GND pin.

8.4.1.2 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, place the resistor divider close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so the pin is a high impedance node and very sensitive to noise. Placing the resistor divider closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so corrects for voltage drops along the traces and provides the best output accuracy. The voltage sense trace from the load to the feedback resistor divider must be routed away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This action is most important when high value resistors are used to set the output voltage. TI recommends to route the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path, such that there is a ground plane in between the feedback trace and inductor/SW node polygon. This action provides further shielding for the voltage feedback path from EMI noises.
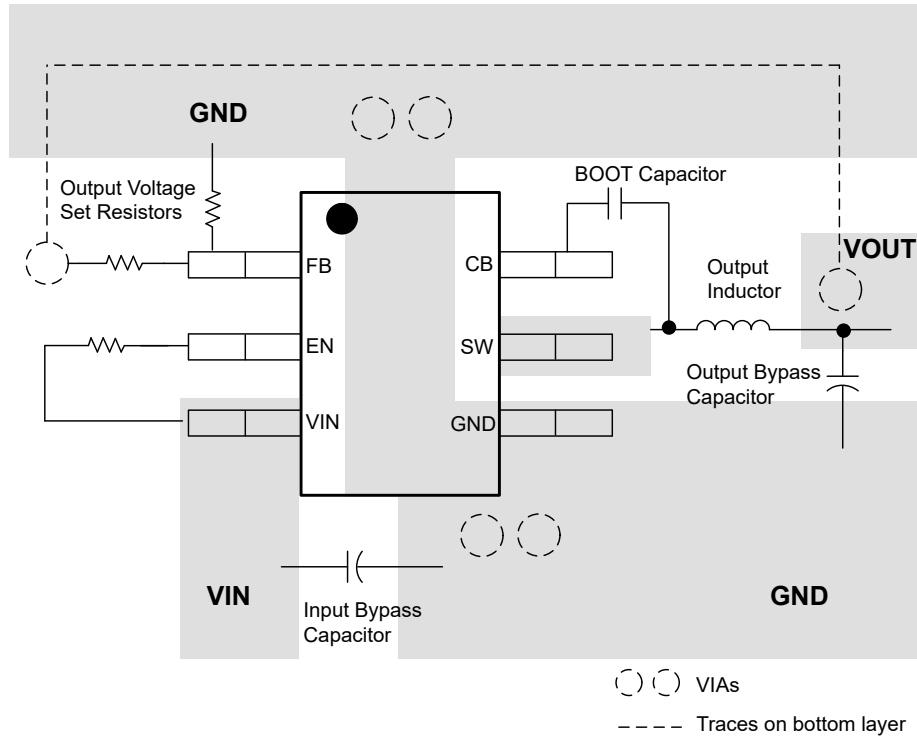
8.4.2 Layout Example

図 8-9. Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR516x5 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application report

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2024) to Revision B (January 2025) **Page**

• データシート全体に LMR51625 とサポート情報を追加..1
• データシート全体に LMR51635XF と LMR51635Y とサポート情報を追加..1

Changes from Revision * (August 2024) to Revision A (November 2024) **Page**

• ドキュメントのステータスを「事前情報」から「量産データ」に変更...1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

資料に関するフィードバック(ご意見やお問い合わせ) を送信

Product Folder Links: *LMR51625 LMR51635*

English Data Sheet: SLUSF64

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR51625XDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	625X	Samples
LMR51625XFDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	25XF	Samples
LMR51625YDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	625Y	Samples
LMR51625YFDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	25YF	Samples
LMR51635XDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	635X	Samples
LMR51635XFDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	35XF	Samples
LMR51635YDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	635Y	Samples
LMR51635YFDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	35YF	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR51625XDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51625XFDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51625YDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51625YFDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51635XDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51635XFDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51635YDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR51635YFDDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR51625XDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR51625XFDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR51625YDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR51625YFDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR51635XDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR51635XFDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR51635YDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMR51635YFDDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0

3.05
2.55

1.75
1.45

B

A

PIN 1
INDEX AREA

1

6

4X 0.95

1.9

3.05
2.75

3

4

6X 0.5
0.3

⊕ 0.2 Ⓜ C A B

1.1
0.7

⌒ 0.1 C

4X 0° -15°

0.1
0.0 TYP

4X 4° -15°

0° -8° TYP

C

0.20
0.12 TYP

SEATING PLANE

0.25

GAGE PLANE

0.6
0.3 TYP

4214841/E   08/2024
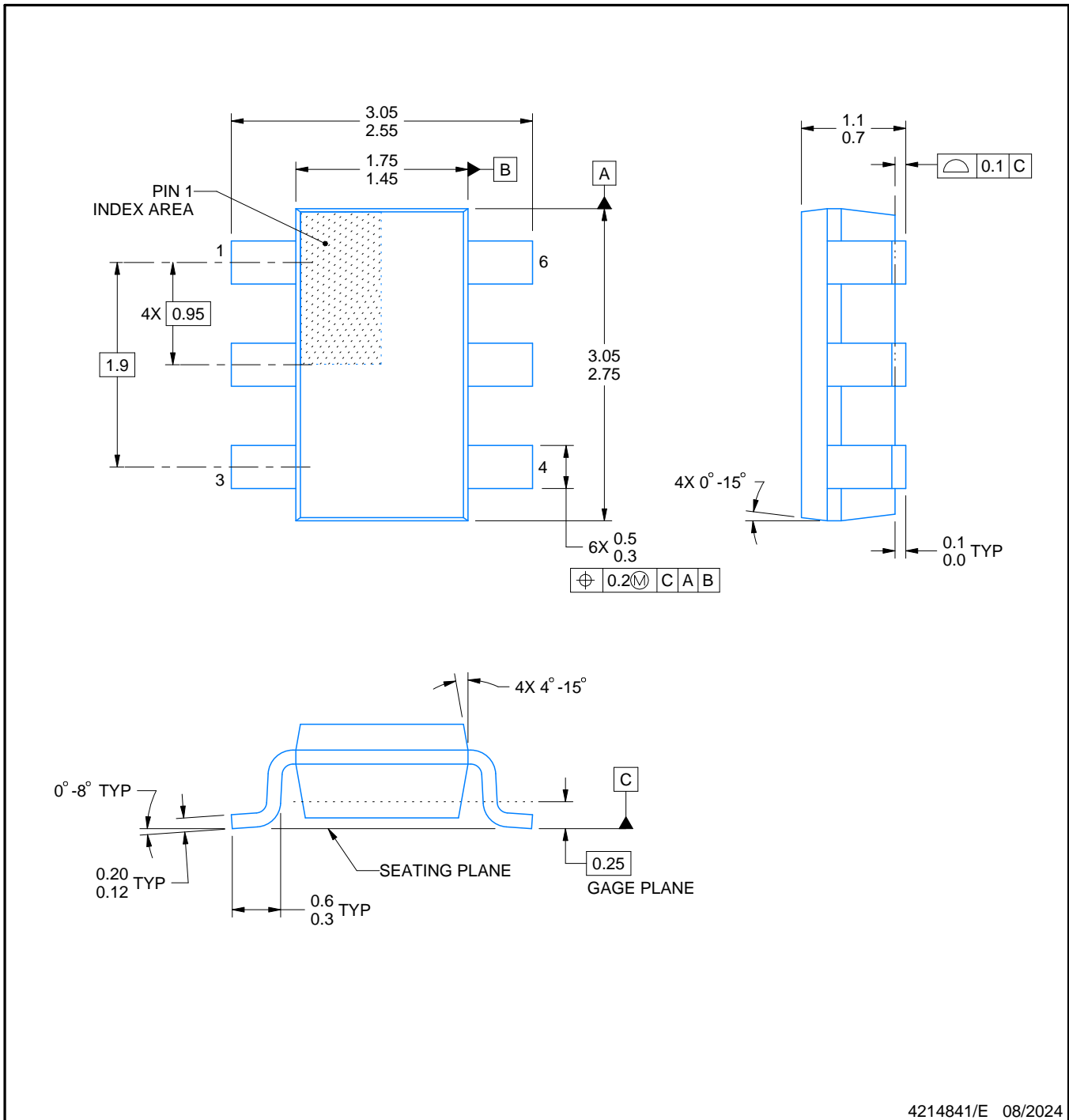
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

SYMM

6X (1.1)

1

6X (0.6)

6

SYMM

4X (0.95)

3

4

(R0.05) TYP

(2.7)
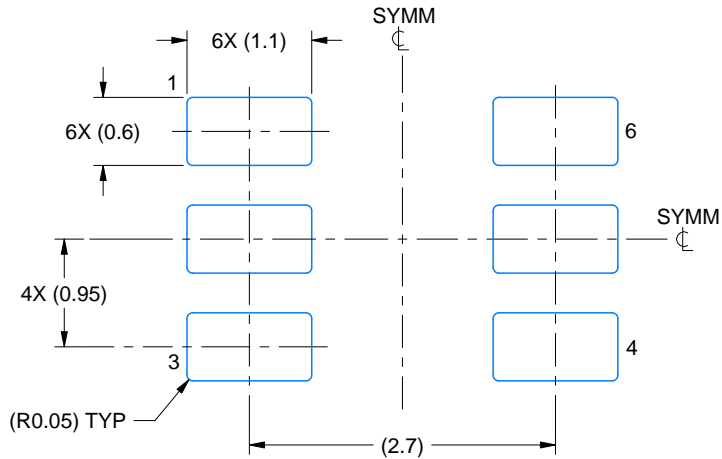
LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.07 MAX
ARROUND

0.07 MIN
ARROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
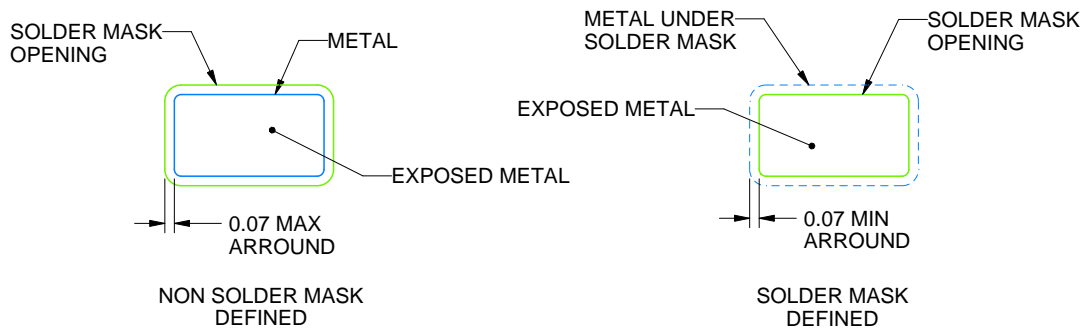
SOLDERMASK DETAILS

4214841/E   08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SYMM

6X (1.1)

1

6X (0.6)

SYMM

4X(0.95)

3

4

6

(R0.05) TYP

(2.7)
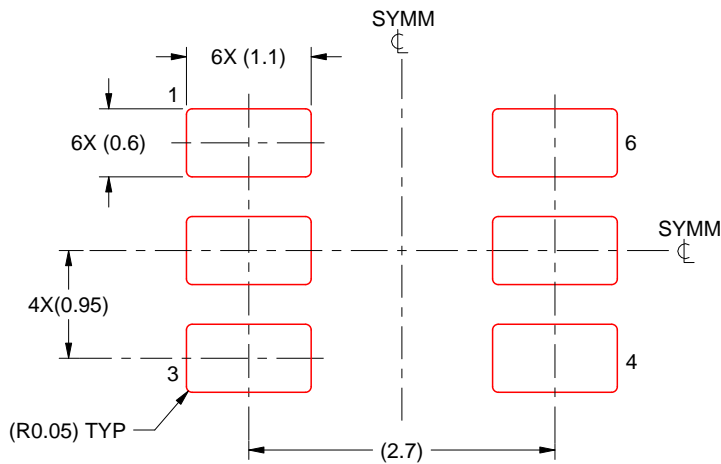
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E   08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.