TEXAS INSTRUMENTS
LMV551, LMV552, LMV554
JAJSAE5H – FEBRUARY 2007 – REVISED AUGUST 2016

LMV55x 3MHz、Micropower RROアンプ

1 特長

- 3Vおよび5Vでの性能を規定
- 高いユニティ・ゲイン帯域幅: 3MHz
- 消費電流(アンプごと): 37µA
- CMRR: 93dB
- PSRR: 90dB
- スルーレート: 1V/µs
- 100kΩ負荷における出力スイング: レールから70mV
- 全高調波歪み: 1kHz、2kΩにおいて0.003%
- 温度範囲: -40℃～125℃

2 アプリケーション

- アクティブ・フィルタ
- 携帯機器
- 車載用機器
- バッテリ電源システム
- センサおよび計測機器

3 概要

LMV55xは高性能、低消費電力のオペアンプで、TIの先進のVIP50プロセスにより実装されています。3MHzの帯域幅を持ちながら、アンプごとに37µAの電流しか消費せず、このクラスのオペアンプとしては極めて優れた帯域幅/電力比を実現しています。これらの超低消費電力アンプはユニティ・ゲイン安定で、広い帯域幅を必要とする超低消費電力アプリケーション向けの非常に優れたソリューションです。

LMV55xにはレール・ツー・レール出力段があり、同相入力範囲がグランドより低い電圧まで拡張されています。

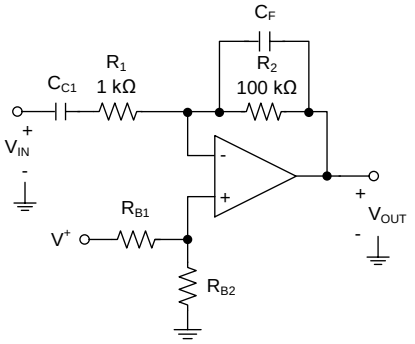
LMV55xは、2.7V～5.5Vの範囲の電源電圧で動作します。これらのアンプは広い温度範囲(-40℃～125℃)で動作するため、車載用アプリケーション、センサ・アプリケーションに加えて、携帯用計測機器アプリケーションにも最適です。LMV551は超小型の5ピンのSC70および5ピンのSOT-23パッケージで供給されます。LMV552は8ピンのVSSOPパッケージで供給されます。LMV554は14ピンのTSSOPで供給されます。

製品情報(1)

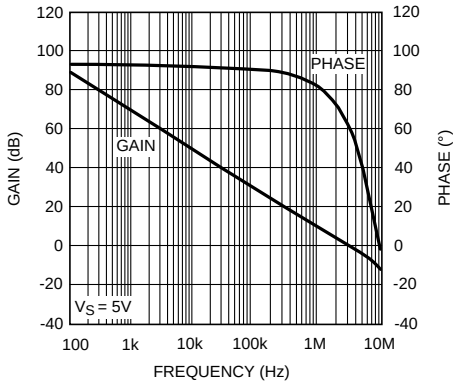
型番	パッケージ	本体サイズ(公称)
LM551	SOT-23 (5)	2.90mm×1.60mm
	SC70 (5)	2.00mm×1.25mm
LMV552	VSSOP (8)	3.00mm×3.00mm
LMV554	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



オープン・ループ・ゲインおよび位相と周波数との関係



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision G (February 2013) から **Revision H** に変更 **Page**

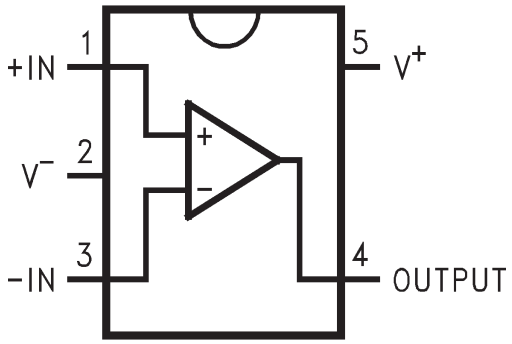
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- Changed values in the *Thermal Information* table to align with JEDEC standards. ... 5

Revision F (February 2013) から **Revision G** に変更 **Page**

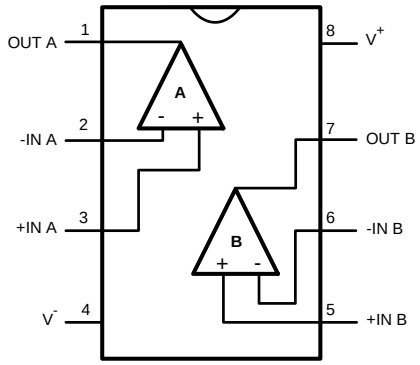
- Changed layout of National Semiconductor Data Sheet to TI format. ... 18

5 Pin Configuration and Functions

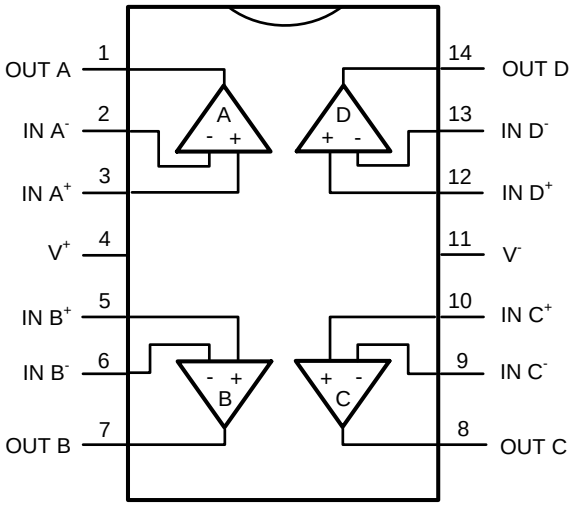
DBV and DCK Packages
5-Pin SOT-23 and SC70
Top View



DGK Package
8-Pin VSSOP
Top View



PW Package
14-Pin TSSOP
Top View



Pin Functions: LMV551

PIN		TYPE(1)	DESCRIPTION
NAME	LMV551 SOT-23, SC70		
+IN	1	I	Noninverting Input
-IN	3	I	Inverting Input
OUT	4	O	Output
V-	2	P	Negative Supply
V+	5	P	Positive Supply

(1) I = Input; O = Output; P = Power

Pin Functions: LMV552 and LMV554

PIN			TYPE(1)	DESCRIPTION
NAME	LMV552 SOIC, VSSOP	LMV554 SOIC, TSSOP		
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input, channel C
–IN D	—	13	I	Inverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V+	8	4	P	Positive (highest) power supply
V–	4	11	P	Negative (lowest) power supply

(1) I = Input; O = Output; P = Power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{IN} Differential (at V^+ = 5 V)		±2.5	V
Supply voltage ($V^+ – V^–$)		6	V
Voltage at input/output pins	$V^–$ –0.3	V^+ +0.3	V
Junction temperature, T_J (3)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)		±2000	V
		Machine model (MM)(2)	LMV551	±100	
			LMV552 / LMV554	±250	

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7.
(2) Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Temperature (1)	–40		125	°C
Supply voltage ($V^+ – V^–$)	2.7		5.5	V

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

6.4 Thermal Information

THERMAL METRIC(1)		LMV551		LMV552	LMV554	UNIT
		DBV (SOT-23)	DCK (SC70)	DGK (VSSOP)	PW (TSSOP)	
		5 PINS	5 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	213.6	303.5	200.3	134.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	174.8	135.5	89.1	60.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.6	81.1	120.9	77.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	56.6	8.4	21.7	11.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	72.2	80.4	119.4	76.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: 3 V

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 3 V, V^- = 0 V, V_{CM} = $V^+/2$ = V_O. (1)

PARAMETER		TEST CONDITIONS			MIN (2)	TYP (2)	MAX (2)	UNIT
V_{OS}	Input offset voltage	T_A = 25°C				1	3	mV
		T_A = –40°C to 125°C					4.5	
TC V_{OS}	Input offset average drift	T_A = –40°C to 125°C				3.3		µV/°C
I_B	Input bias current (3)	T_A = 25°C				20	38	nA
I_{OS}	Input offset current	T_A = 25°C				1	20	nA
CMRR	Common mode rejection ratio	0 V ≤ V_{CM} 2 V	T_A = 25°C		74	92		dB
			T_A = –40°C to +125°C		72			
PSRR	Power supply rejection ratio	3 ≤ V^+ ≤ 5 V, V_{CM} = 0.5 V	LMV551 and LMV552	T_A = 25°C	80	92		dB
				T_A = –40°C to +125°C	78			
			LMV554	T_A = 25°C	78	92		
				T_A = –40°C to +125°C	76			
		2.7 ≤ V^+ ≤ 5.5 V, V_{CM} = 0.5 V	LMV551 and LMV552	T_A = 25°C	80	92		
				T_A = –40°C to +125°C	78			
			LMV554	T_A = 25°C	78	92		
				T_A = -40°C to +125°C	76			
CMVR	Input common-mode voltage	CMRR ≥ 68 dB	T_A = 25°C		0		2.1	V
		CMRR ≥ 60 dB	T_A = -40°C to +125°C		0		2.1	
A_{VOL}	Large signal voltage gain	0.4 ≤ V_O ≤ 2.6, R_L = 100 kΩ to $V^+/2$	LMV551 and LMV552	T_A = 25°C	81	90		dB
				T_A = –40°C to +125°C	78			
			LMV554	T_A = 25°C	79	90		
				T_A = –40°C to +125°Ce	77			
		0.4 ≤ V_O ≤ 2.6, R_L = 10 kΩ to $V^+/2$	T_A = 25°C		71	80		
			T_A = -40°C to +125°C		68			
V_O	Output swing high	R_L = 100 kΩ to $V^+/2$		T_A = 25°C		40	48	mV from rail
				T_A = –40°C to +125°C			58	
		R_L = 10 kΩ to $V^+/2$		T_A = 25°C		85	100	
				T_A = –40°C to +125°C			120	
	Output swing low	R_L = 100 kΩ to $V^+/2$		T_A = 25°C		50	65	
				T_A = –40°C to +125°C			77	
		R_L = 10 kΩ to $V^+/2$		T_A = 25°C		95	110	
				T_A = –40°C to +125°C			130	
I_{SC}	Output short circuit current	Sourcing (4)				10		mA
		Sinking (4)				25		
I_S	Supply current per amplifier	T_A = 25°C				34	42	µA
		T_A = –40°C to +125°C					52	
SR	Slew rate	A_V = +1, 10% to 90% (5)				1		V/µs

(1) Electrical Table values apply only for factor testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J = T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Positive current corresponds to current flowing into the device.
(4) The part is not short-circuit protected and is not recommended for operation with heavy resistive loads.
(5) Slew rate is the average of the rising and falling slew rates.

Electrical Characteristics: 3 V (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 3 V, V^- = 0 V, $V_{CM} = V^+/2 = V_O$. (1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (2)	MAX (2)	UNIT
Φm	Phase margin	R_L = 10 kΩ, C_L = 20 pF		75		°
GBW	Gain bandwidth product			3		MHz
e_n	Input-referred voltage noise	f = 100 kHz		70		nV/√Hz
		f = 1 kHz		70		
I_n	Input-referred current noise	f = 100 kHz		0.1		pA/√Hz
		f = 1 kHz		0.15		
THD	Total harmonic distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ		0.003%		

6.6 Electrical Characteristics: 5 V

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = 0 V, $V_{CM} = V^+/2 = V_O$. (1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input offset voltage	T_A = 25°C			1	3	mV
		T_A = –40°C to +125°C				4.5	
TC V_{OS}	Input offset average drift	T_A = 25°C			3.3		µV/°C
I_B	Input bias current (4)	T_A = 25°C			20	38	nA
I_{OS}	Input offset current				1	20	nA
CMRR	Common mode rejection ratio	T_A = 25°C		76	93		nA
		T_A = –40°C to +125°C		74			
PSRR	Power supply rejection ratio	3 V ≤ V^+ ≤ 5 V to V_{CM} = 0.5 V	T_A = 25°C	78	90		dB
			T_A = –40°C to +125°C	75			
		2.7 V ≤ V^+ ≤ 5.5 V to V_{CM} = 0.5 V	T_A = 25°C	78	90		
			T_A = –40°C to +125°C	75			
CMVR	Input common-mode voltage	CMRR ≥ 68 dB CMRR ≥ 60 dB	T_A = 25°C	0		4.1	V
			T_A = –40°C to +125°C	0		4.1	
A_{VOL}	Large signal voltage gain	0.4 ≤ V_O ≤ 4.6, R_L = 100 kΩ to $V^+/2$		78	90		dB
				75			
		0.4 ≤ V_O ≤ 4.6, R_L = 10 kΩ to $V^+/2$		75	80		
				72			
V_O	Output swing high	R_L = 100 kΩ to $V^+/2$	T_A = 25°C		70	92	mV from rail
			T_A = –40°C to +125°C			122	
		R_L = 10 kΩ to $V^+/2$	T_A = 25°C		125	155	
			T_A = –40°C to +125°C			210	
	Output swing low	R_L = 100 kΩ to $V^+/2$	T_A = 25°C		60	70	
			T_A = –40°C to +125°C			82	
		R_L = 10 kΩ to $V^+/2$	T_A = 25°C		110	130	
			T_A = –40°C to +125°C			155	
I_{SC}	Output short-circuit current	Sourcing (5)			10		mA
		Sinking (5)			25		
I_S	Supply current per amplifier	T_A = 25°C			37	46	µA
		T_A = –40°C to +125°C				54	

(1) Electrical Table values apply only for factor testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J = T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Positive current corresponds to current flowing into the device.
(5) The part is not short-circuit protected and is not recommended for operation with heavy resistive loads.

Electrical Characteristics: 5 V (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = 0 V, $V_{CM} = V^+/2 = V_O$. (1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
SR	Slew rate	A_V = +1, V_O = 1 V_{PP} 10% to 90% (6)		1		V/µs
Φm	Phase margin	R_L = 10 kΩ, C_L = 20 pF		75		°
GBW	Gain bandwidth product			3		MHz
e_n	Input-referred voltage noise	f = 100 kHz		70		nV/√Hz
		f = 1 kHz		70		
I_n	Input-referred current noise	f = 100 kHz		0.1		pA/√Hz
		f = 1 kHz		0.15		
THD	Total harmonic distortion	f = 1 kHz, A_V = 2, R_L = 2 kΩ		0.003%		

(6) Slew rate is the average of the rising and falling slew rates.

6.7 Typical Characteristics

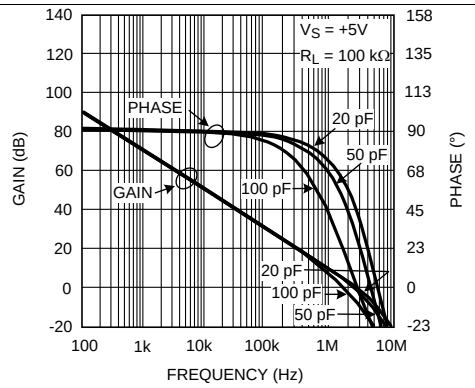


Figure 1. Open-Loop Gain and Phase With Capacitive Load

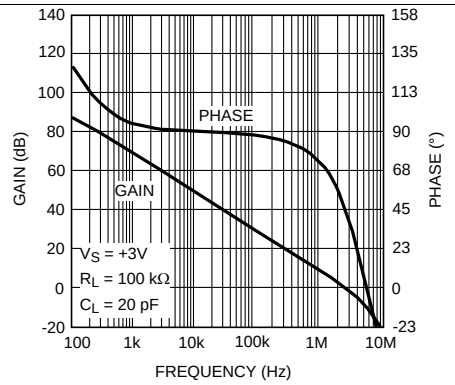


Figure 2. Open-Loop Gain and Phase With Resistive Load

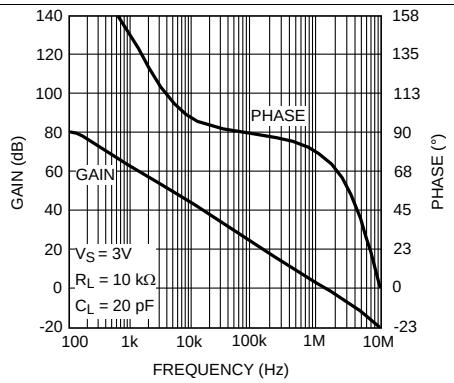


Figure 3. Open-Loop Gain and Phase With Resistive Load

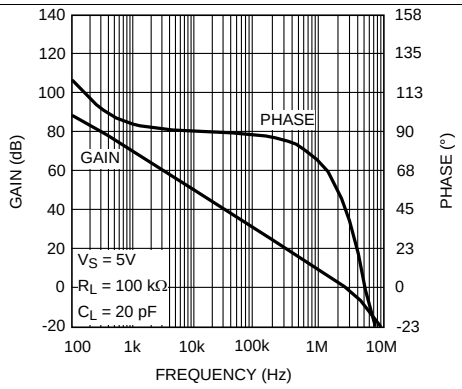


Figure 4. Open-Loop Gain and Phase With Resistive Load

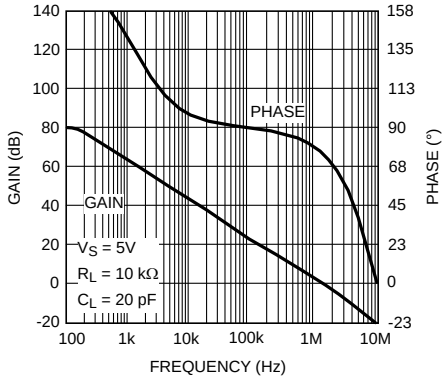


Figure 5. Open-Loop Gain and Phase With Resistive Load

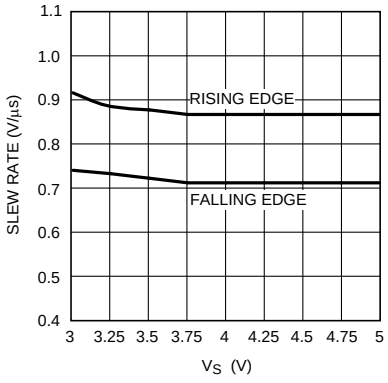


Figure 6. Slew Rate vs Supply voltage

Typical Characteristics (continued)

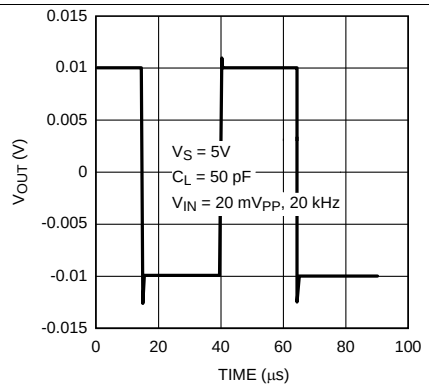


Figure 7. Small-Signal Transient Response

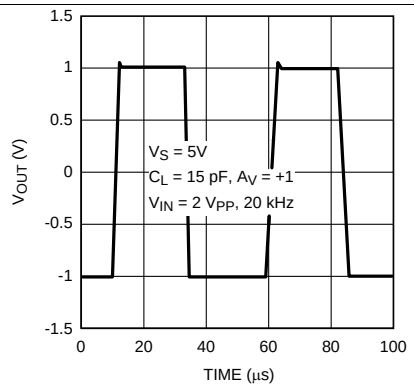


Figure 8. Large-Signal Transient Response

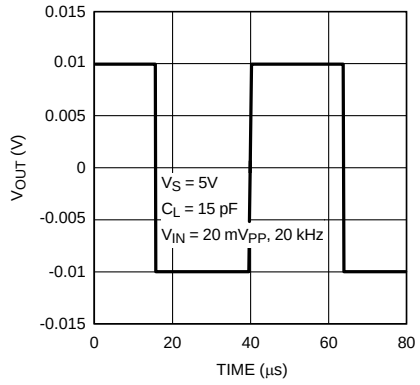


Figure 9. Small-Signal Transient Response

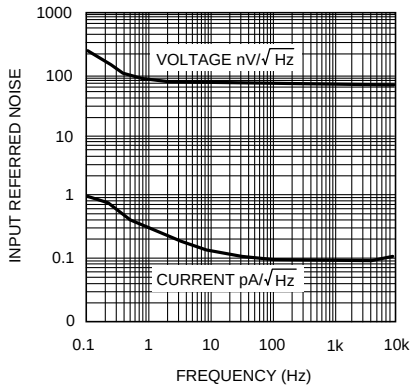


Figure 10. Input Referred Noise vs Frequency

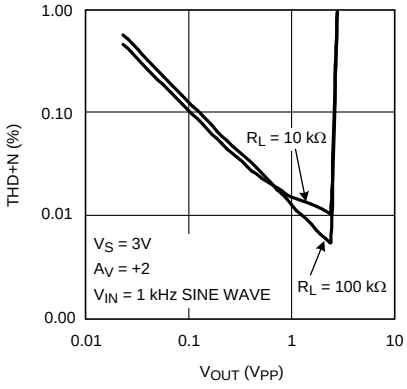


Figure 11. THD+N vs Amplitude at 3 V

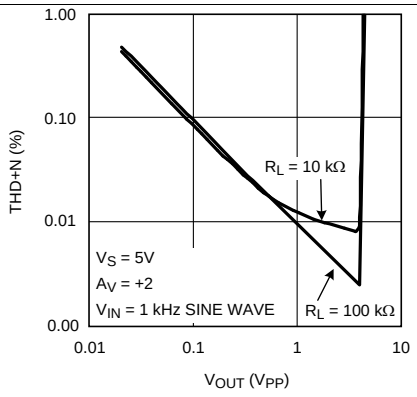


Figure 12. THD+N vs Amplitude at 5 V

Typical Characteristics (continued)

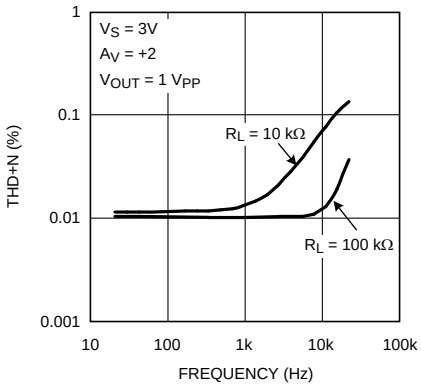


Figure 13. THD+N vs Amplitude

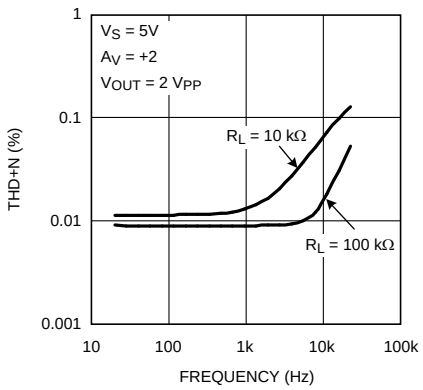


Figure 14. THD+N vs Amplitude

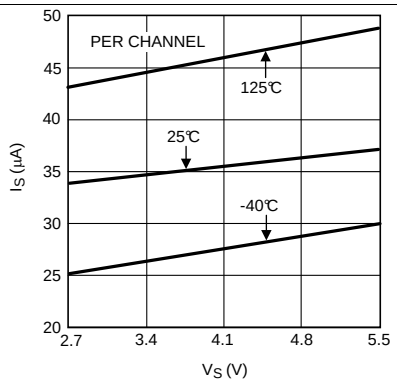


Figure 15. Supply Current vs Supply Voltage

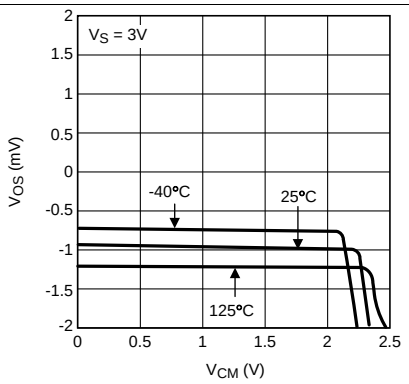


Figure 16. V_{OS} vs V_{CM}

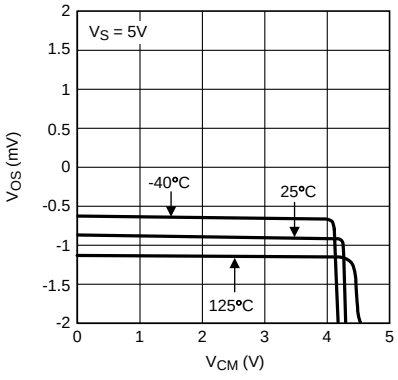


Figure 17. V_{OS} vs V_{CM}

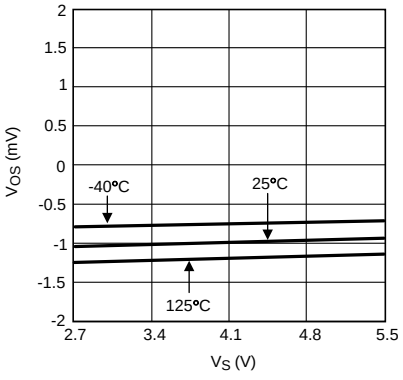


Figure 18. V_{OS} vs Supply Voltage

Typical Characteristics (continued)

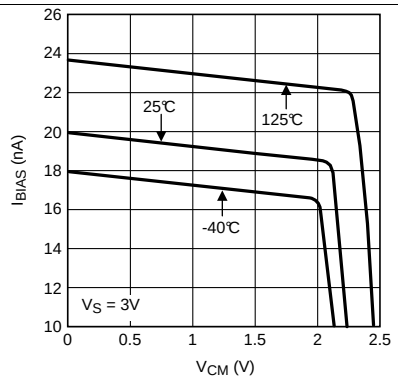


Figure 19. I_{BIAS} vs V_{CM}

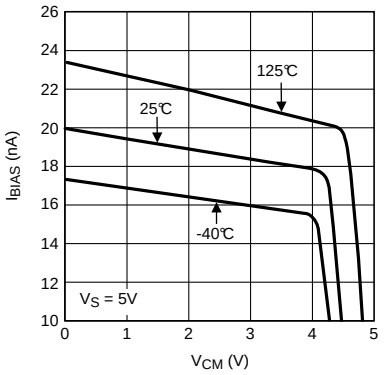


Figure 20. I_{BIAS} vs V_{CM}

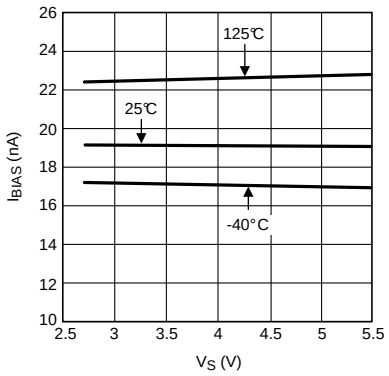


Figure 21. I_{BIAS} vs Supply Voltage

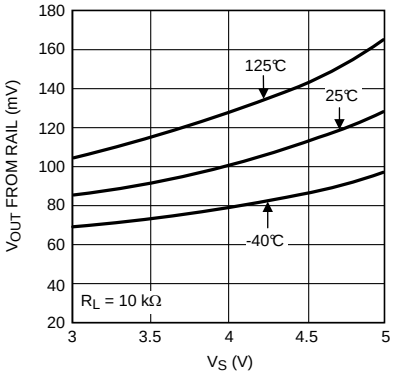


Figure 22. Positive Output Swing vs Supply Voltage

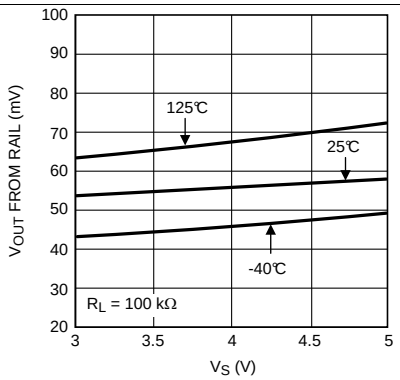


Figure 23. Negative Output Swing vs Supply Voltage

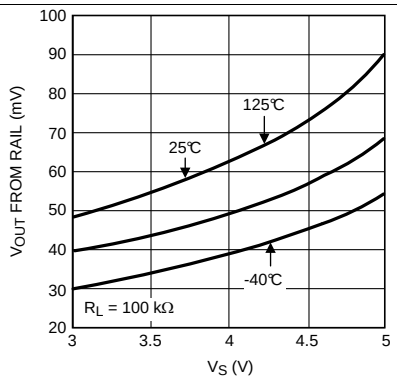


Figure 24. Positive Output Swing vs Supply Voltage

Typical Characteristics (continued)

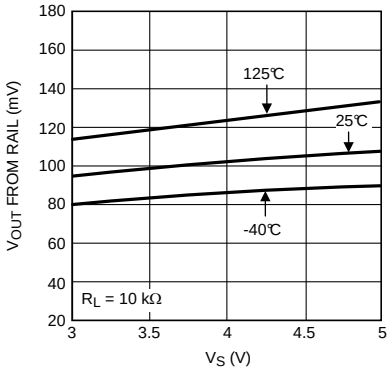


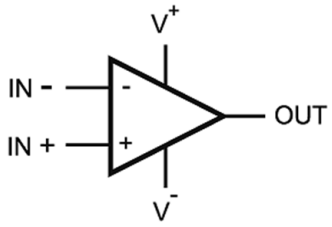
Figure 25. Negative Output Swing vs Supply Voltage

7 Detailed Description

7.1 Overview

The LMV55x are high performance, low power operational amplifiers implemented with TI's advanced VIP50 process. They feature 3 MHz of bandwidth while consuming only 37 µA of current per amplifier, which is an exceptional bandwidth to power ratio in this op amp class. These amplifiers are unity gain stable and provide an excellent solution for low power applications requiring a wide bandwidth.

7.2 Functional Block Diagram



(Each Amplifier)

7.3 Feature Description

The differential inputs of the amplifier consist of a noninverting input (+IN) and an inverting input (–IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ - IN^-) \quad (1)$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 100 dB (100,000x, or 10 uV per volt).

7.3.1 Low Voltage and Low Power Operation

The LMV55x have performance ensured at supply voltages of 3 V and 5 V and are ensured to be operational at all supply voltages from 2.7 V to 5.5 V. For this supply voltage range, the LMV55x draw the extremely low supply current of less than 37 µA per amp.

7.3.2 Wide Bandwidth

The bandwidth to power ratio of 3 MHz to 37 µA per amplifier is one of the best bandwidth to power ratios ever achieved. This makes these devices ideal for low power signal processing applications such as portable media players and instrumentation.

7.3.3 Low Input Referred Noise

The LMV55x provide a flatband input referred voltage noise density of 70 nV/$\sqrt{Hz}$, which is significantly better than the noise performance expected from an ultra low power op amp. They also feature the exceptionally low 1/f noise corner frequency of 4 Hz. This noise specification makes the LMV55x ideal for low power applications such as PDAs and portable sensors.

7.3.4 Ground Sensing and Rail-to-Rail Output

The LMV55x each have a rail-to-rail output stage, which provides the maximum possible output dynamic range. This is especially important for applications requiring a large output swing. The input common mode range includes the negative supply rail which allows direct sensing at ground in a single supply operation.

Feature Description (continued)

7.3.5 Small Size

The small footprints of the LMV55x packages save space on printed circuit boards, and enable the design of smaller and more compact electronic products. Long traces between the signal source and the op amp make the signal path susceptible to noise. By using a physically smaller package, the amplifiers can be placed closer to the signal source, reducing noise pickup and enhancing signal integrity.

7.4 Device Functional Modes

7.4.1 Stability Of Op Amp Circuits

7.4.1.1 Stability and Capacitive Loading

As seen in the Phase Margin vs Capacitive Load graph, the phase margin reduces significantly for C_L greater than 100 pF. This is because the op amp is designed to provide the maximum bandwidth possible for a low supply current. Stabilizing them for higher capacitive loads would have required either a drastic increase in supply current, or a large internal compensation capacitance, which would have reduced the bandwidth of the op amp. Hence, if the LMV55x are to be used for driving higher capacitive loads, they must be externally compensated.

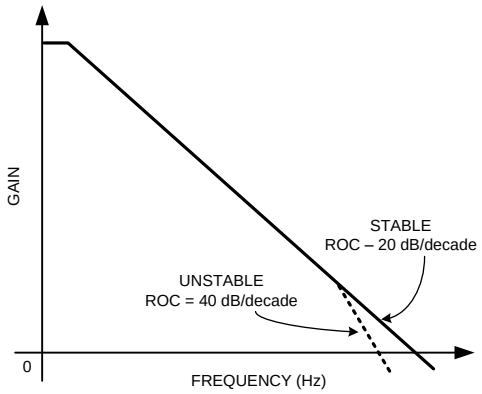


Figure 26. Gain vs Frequency for an Op Amp

An op amp, ideally, has a dominant pole close to DC, which causes its gain to decay at the rate of 20 dB/decade with respect to frequency. If this rate of decay, also known as the rate of closure (ROC), remains the same until the op amp's unity gain bandwidth, the op amp is stable. If, however, a large capacitance is added to the output of the op amp, it combines with the output impedance of the op amp to create another pole in its frequency response before its unity gain frequency (Figure 26). This increases the ROC to 40 dB/ decade and causes instability.

In such a case a number of techniques can be used to restore stability to the circuit. The idea behind all these schemes is to modify the frequency response such that it can be restored to an ROC of 20 dB/decade, which ensures stability.

7.4.1.1.1 In the Loop Compensation

Figure 27 illustrates a compensation technique, known as 'in the loop' compensation, that employs an RC feedback circuit within the feedback loop to stabilize a non-inverting amplifier configuration. A small series resistance, R_S, is used to isolate the amplifier output from the load capacitance, C_L, and a small capacitance, C_F, is inserted across the feedback resistor to bypass C_L at higher frequencies.

Device Functional Modes (continued)

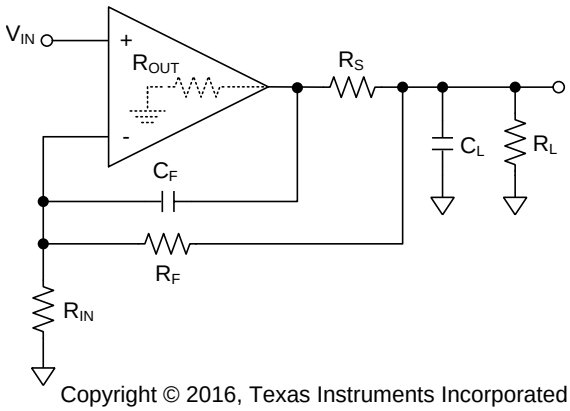


Figure 27. In the Loop Compensation

The values for R_S and C_F are decided by ensuring that the zero attributed to C_F lies at the same frequency as the pole attributed to C_L. This ensures that the effect of the second pole on the transfer function is compensated for by the presence of the zero, and that the ROC is maintained at 20 dB/decade. For the circuit shown in Figure 27 the values of R_S and C_F are given by Equation 2. Values of R_S and C_F required for maintaining stability for different values of C_L, as well as the phase margins obtained, are shown in Table 1. R_F, R_{IN}, and R_L are to be 10 kΩ, while R_{OUT} is 340Ω.

$$R_S = \frac{R_{OUT} R_{IN}}{R_F}$$

$$C_F = \left(1 + \frac{1}{A_{CL}}\right)\left(\frac{R_F + 2R_{IN}}{R_F^2}\right) C_L R_{OUT} \quad (2)$$

Table 1. Phase Margins

C_L (pF)	R_S (Ω)	C_F (pF)	PHASE MARGIN (°)
50	340	8	47
100	340	15	42
150	340	22	40

Although this methodology provides circuit stability for any load capacitance, it does so at the price of bandwidth. The closed loop bandwidth of the circuit is now limited by R_F and C_F.

7.4.1.1.2 Compensation by External Resistor

In some applications it is essential to drive a capacitive load without sacrificing bandwidth. In such a case, in the loop compensation is not viable. A simpler scheme for compensation is shown in Figure 28. A resistor, R_{ISO}, is placed in series between the load capacitance and the output. This introduces a zero in the circuit transfer function, which counteracts the effect of the pole formed by the load capacitance and ensures stability. The value of R_{ISO} to be used should be decided depending on the size of C_L and the level of performance desired. Values ranging from 5 Ω to 50 Ω are usually sufficient to ensure stability. A larger value of R_{ISO} results in a system with less ringing and overshoot, but also limits the output swing and the short-circuit current of the circuit.

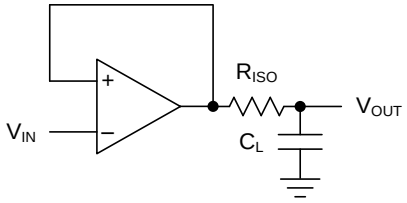


Figure 28. Compensation by Isolation Resistor

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV55x have an operating supply voltage range from 2.7 V to 5.5 V. These amplifiers can operate over a wide temperature range (−40°C to 125°C), making them a great choice for automotive applications, sensor applications as well as portable instrumentation applications.

With a wide unity gain bandwidth of 3 MHz, low input referred noise density and an excellent BW to supply current ratio, the LMV55x are well suited for low-power filtering applications. Active filter topologies, such as the Sallen-Key low pass filter shown in Figure 29, are very versatile, and can be used to design a wide variety of filters (Chebyshev, Butterworth or Bessel). For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier and premature roll-off. The Sallen-Key topology, in particular, can be used to attain a wide range of Q, by using positive feedback to reject the undesired frequency range.

8.2 Typical Application

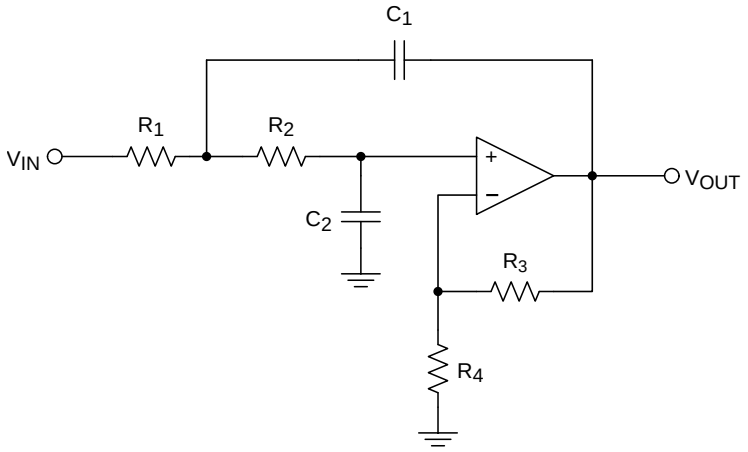


Figure 29. Two Pole Sallen-Key Low Pass Filter

8.2.1 Design Requirements

As a design example:

Require: A_{LP} = 10, less than 1dB passband ripple, and a cutoff frequency of 1kHz.

8.2.2 Detailed Design Procedure

There are many resources discussing the Sallen-Key lowpass filter topology.

Texas Instruments has made filter design easy by creating on-line and stand alone design tools, such as Webench Filter Designer and Filter Pro Desktop.

For this design, the stand-alone Filter Pro Desktop is used.

For the design, the following parameters are entered into the Filterpro software:

1. Filter Type = Lowpass
2. Gain = 10 V/V (20dB)
3. Passband Frequency = 1 kHz

Typical Application (continued)

4. Allowable Ripple = 1 dB
5. Filter Order = Checked and set to 2
6. Response Type = Butterworth
7. Filter Topology = Sallen-Key
8. Component Tolerance - Resistor = E96 1%
9. Component Tolerance - Capacitor = E6 20%

After entering these values, FilterPro returns the following recommended values:

1. R1 = 44.2 kΩ
2. R2 = 38.3 kΩ
3. R3 = 2.49 kΩ
4. R4 = 22.6 kΩ
5. C1 = 10 nF
6. C2 = 1.5 nF

The LMV55x is targeted for low power operation. The above resistor values are assumed for a *standard* power application. To save power, both quiescent and dynamic, the values of the resistors can be increased.

The largest consumer of power is the gain setting feedback resistors R3 and R4, as these are DC coupled and represent a constant DC load to the amplifier. If the output is biased at 2.5 V, then 2.5 V / (22.6 k + 2.49 k) = 99.6 µA is flowing through the feedback network. This is significantly more than the 37uA quiescent current of the amplifier alone! Increasing the size of the feedback resistors by a decade from 22.6k to 226k, the current in the feedback network can be reduced down to 9.9uA.

Increasing the resistor values requires a proportional decrease in the values of the capacitors. If a resistor value is increased 10×, then the corresponding capacitor value must be decreased 10×. However, note that increasing the resistor values increases the contributed noise, and decreasing the capacitors to small values increases the sensitivity to stray capacitance.

There is a decision to be made about also scaling the filter components (R1, R2, C1 & C2). R1 and R2 are AC coupled to the output, so the only DC current flowing through these resistors is the input bias current of the LMV55x (typically 20 nA). However, large AC currents can flow through C2 and C1 during large signal swings. Scaling the filter components also reduces the peak AC signal currents. If the AC signals are expected to large (several Vpp) and frequent, then scaling the filter values may be beneficial to overall power consumption. If the expected AC signals are small, it may not be worth the noise tradeoff to scale these values.

Because the LMV55x has a bipolar input, to maintain DC accuracy, the equivalent resistance seen by each amplifier input should be equal to cancel the bias current effects.

To maintain DC accuracy through bias current cancelling, the following relationship should be maintained:

$$(R1 + R2) = (R3 // R4) \quad (3)$$

Fortunately, the filter Pro software makes changing and recalculating the values easy. By changing the value of any of the filter components (R1, R2, C1 & C2) in the schematic tab, the program automatically recalculates and scale these components. Conversely, changing the gain feedback components (R3 or R4) also causes the other feedback resistor to scale. However, Filter Pro does NOT maintain the relationship between the feedback and filter elements as described in Equation 3 above. The feedback resistor values can be 'seeded' and scaled appropriately, as long as the original feedback resistor ratio is maintained.

Typical Application (continued)

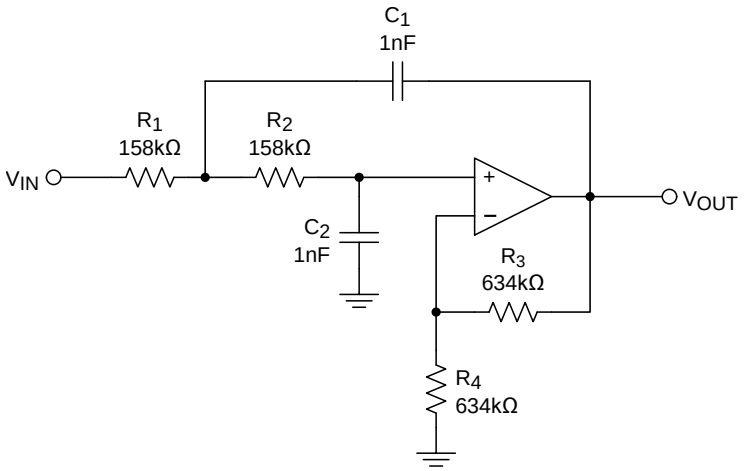


Figure 30. 1kHz Sallen-Key Low Pass Filter with Values

8.2.3 Application Curve

Figure 31 shows the simulated results of the example 1-KHz Sallen-Key Low Pass Filter.

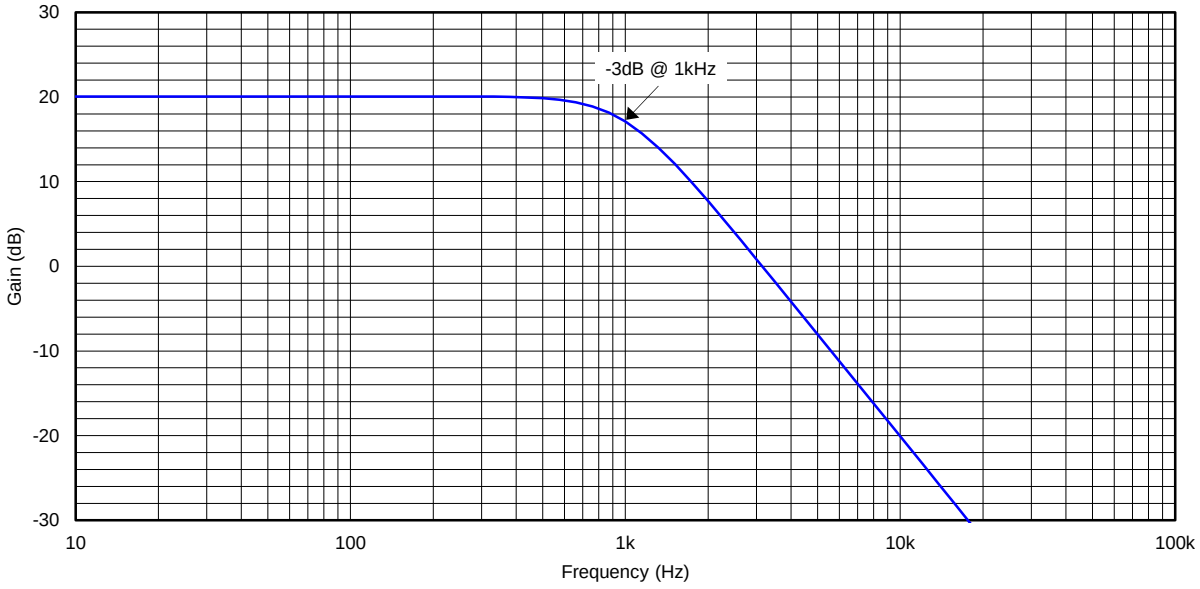


Figure 31. 1KHz, 2-Pole Sallen-Key Low Pass Filter Results

8.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistence to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external Schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 kΩ per volt).

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the op amp power supply pins. For single-supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

10 Layout

10.1 Layout Guidelines

The V^+ pin should be bypassed to ground with a low-ESR capacitor.

The optimum placement is closest to the V^+ and ground pins.

Take care to minimize the loop area formed by the bypass capacitor connection between V^+ and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

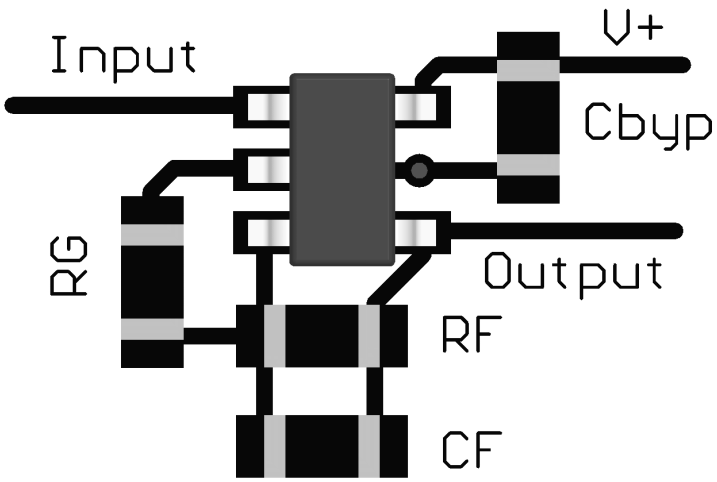


Figure 32. SOT-23 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

LMV551 PSPICEモデル(SNOM060)

LMV552 PSPICEモデル(SNOM061)

LMV554 PSPICEモデル(SNOM062)

TINA-TI SPICEベースのアナログ・シミュレーション・プログラム

DIP アダプタ評価モジュール

TIユニバーサル・オペアンプ評価モジュール

TI Filterproソフトウェア

11.2 ドキュメントのサポート

11.2.1 関連資料

追加アプリケーションについては、*『AN-31 オペアンプ回路コレクション』*(SNLA140)を参照してください。

11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LMV551	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LMV552	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LMV554	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 商標

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11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV551MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AF3A	Samples
LMV551MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AF3A	Samples
LMV551MG/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A94	Samples
LMV551MGX/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A94	Samples
LMV552MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AH3A	Samples
LMV552MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AH3A	Samples
LMV554MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV55 4MT	Samples
LMV554MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV55 4MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

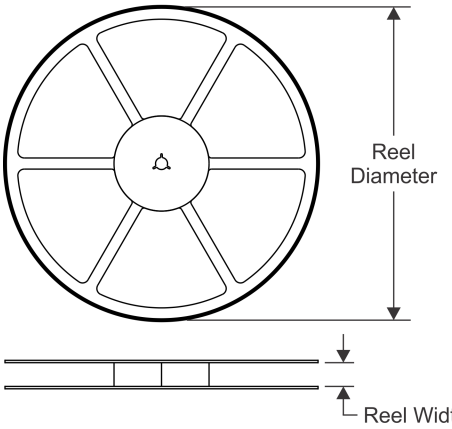
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

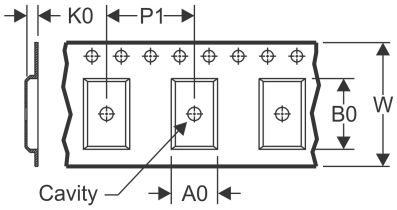
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

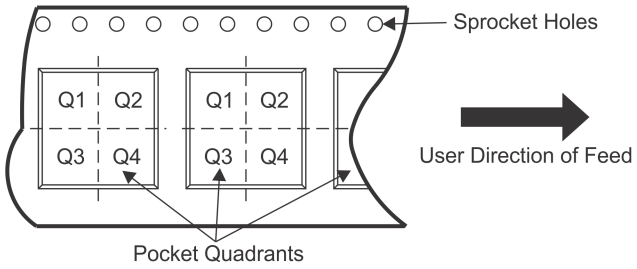


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

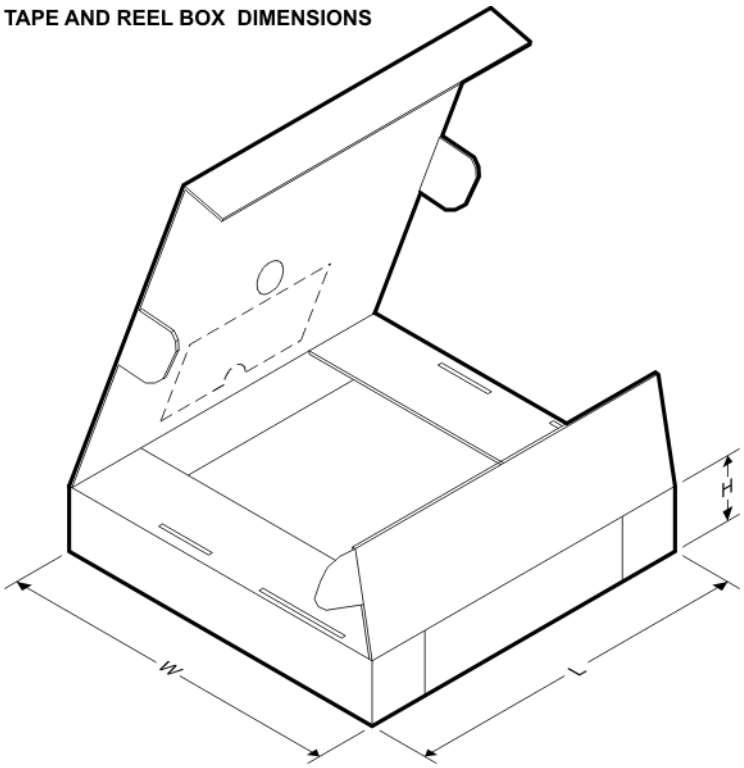
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV551MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV551MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV551MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV551MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV552MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV552MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV554MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

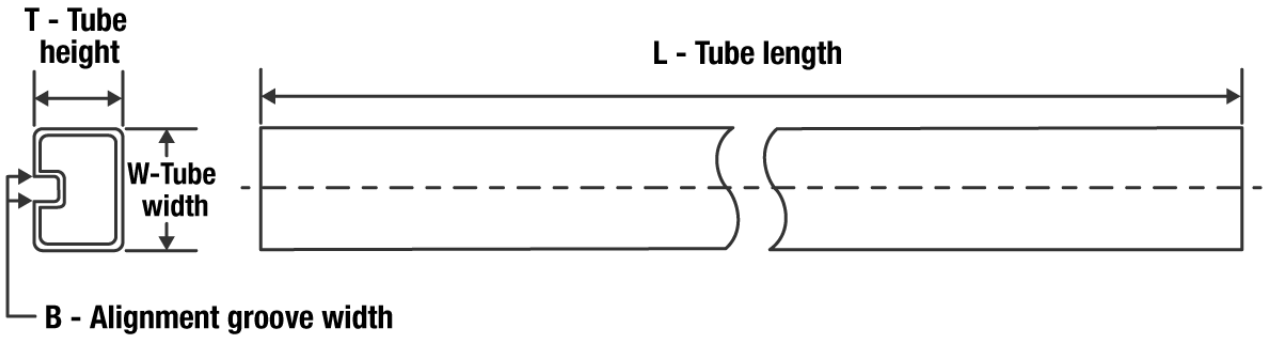
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV551MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV551MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV551MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV551MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LMV552MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV552MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV554MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

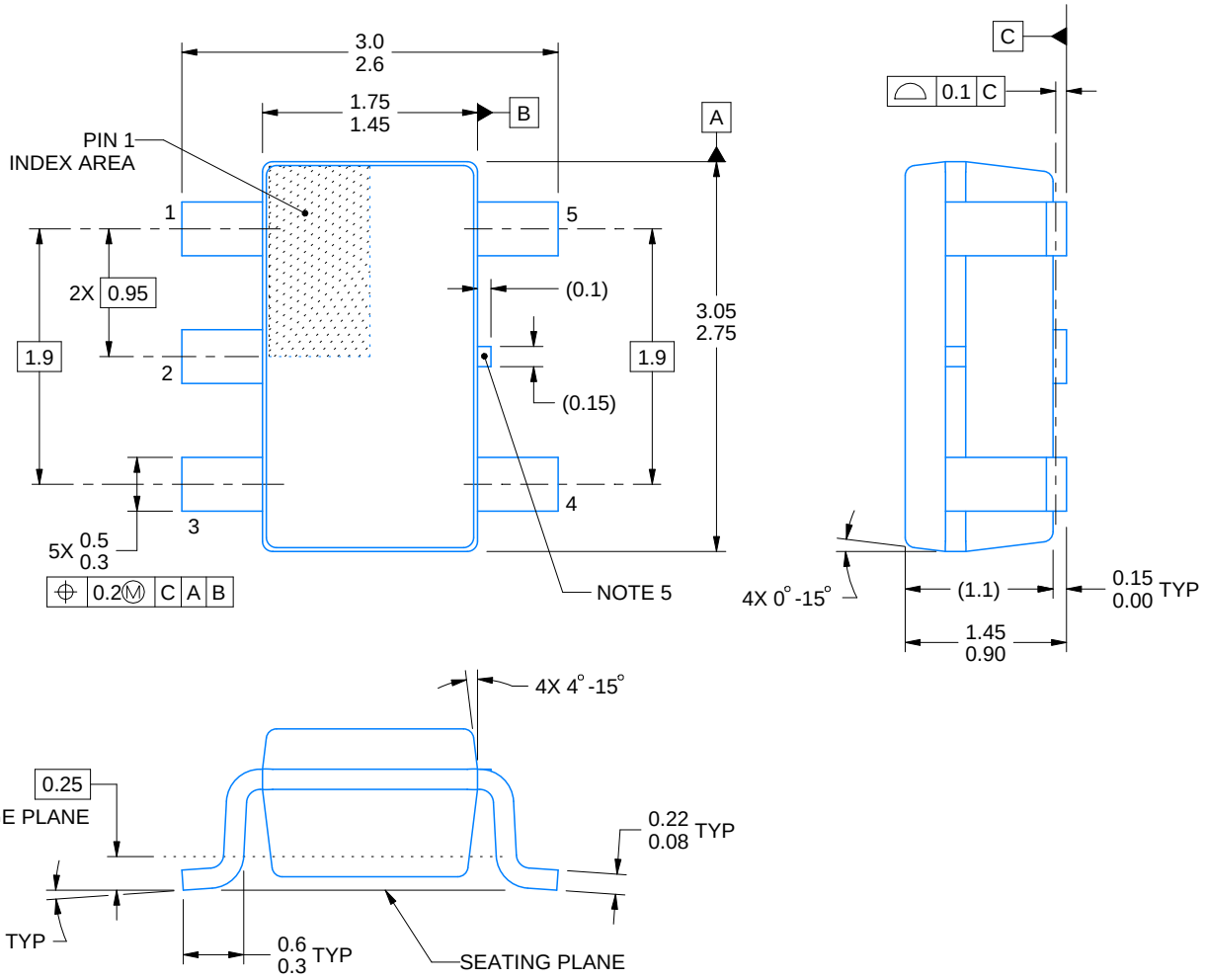
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV554MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

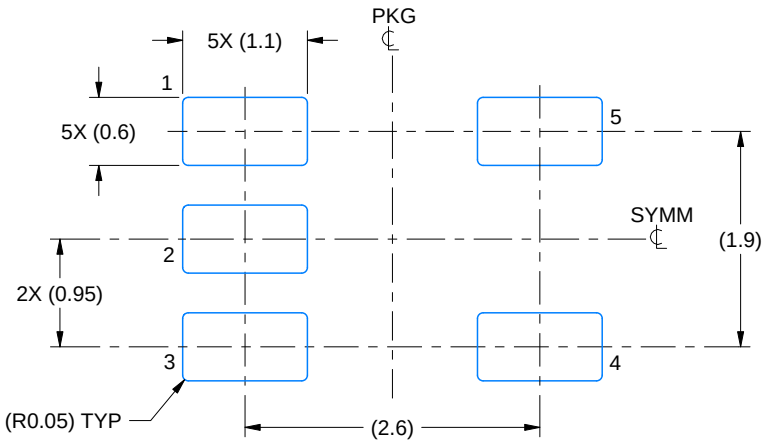
SMALL OUTLINE TRANSISTOR



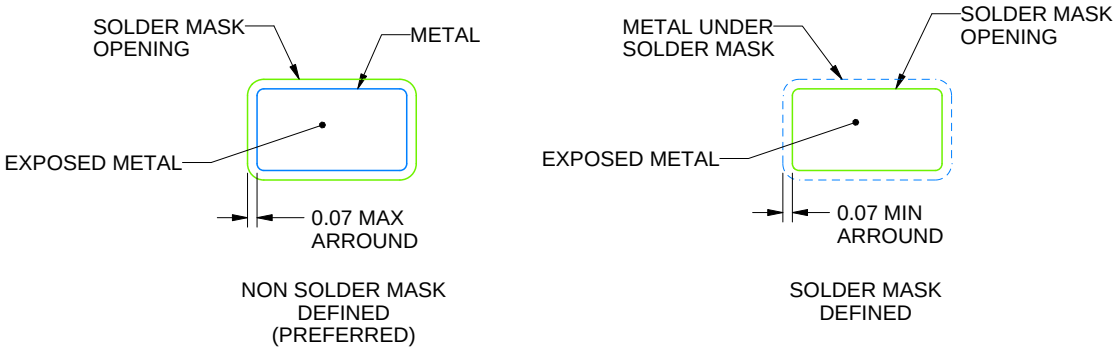
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

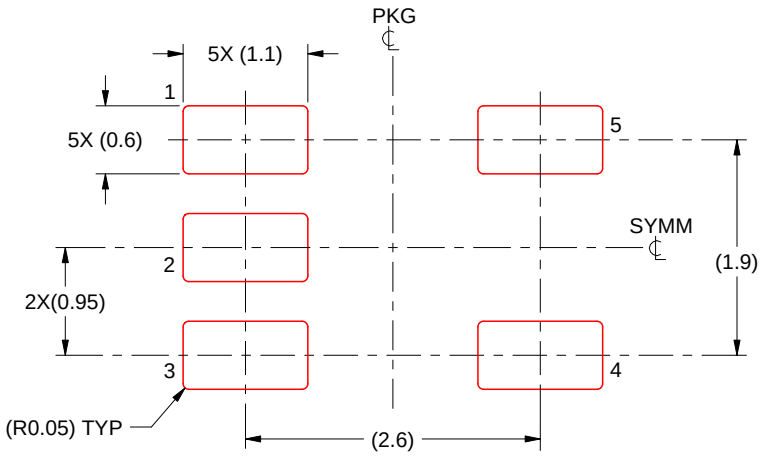


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

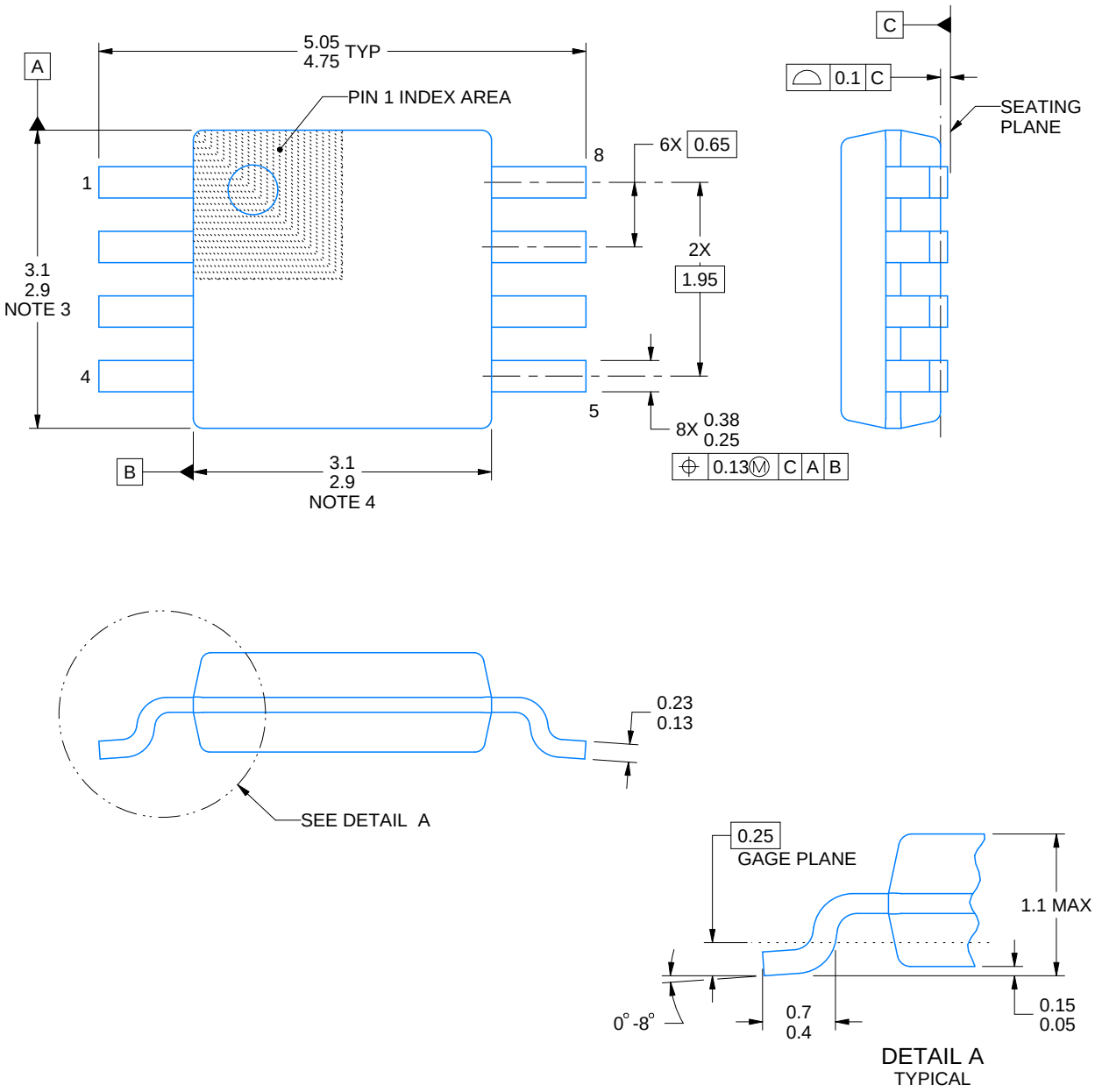
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

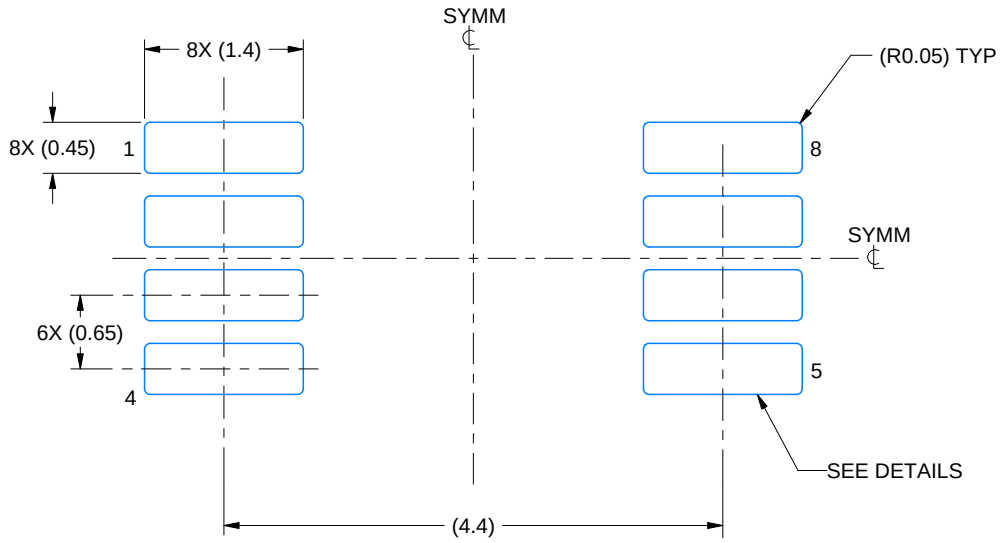
SMALL OUTLINE PACKAGE



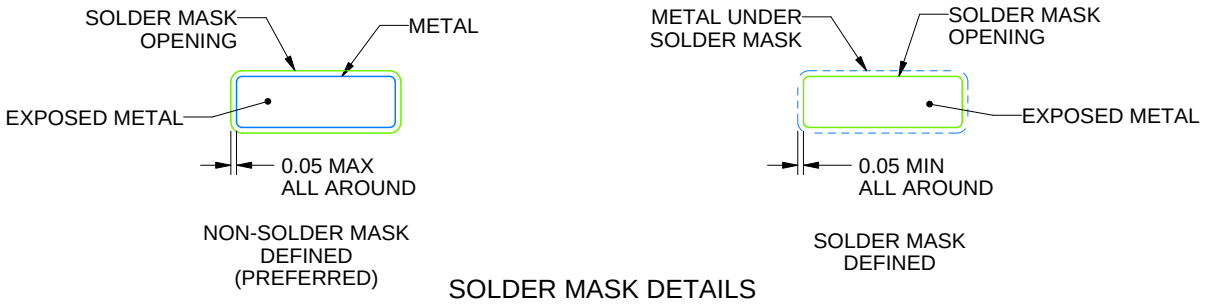
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

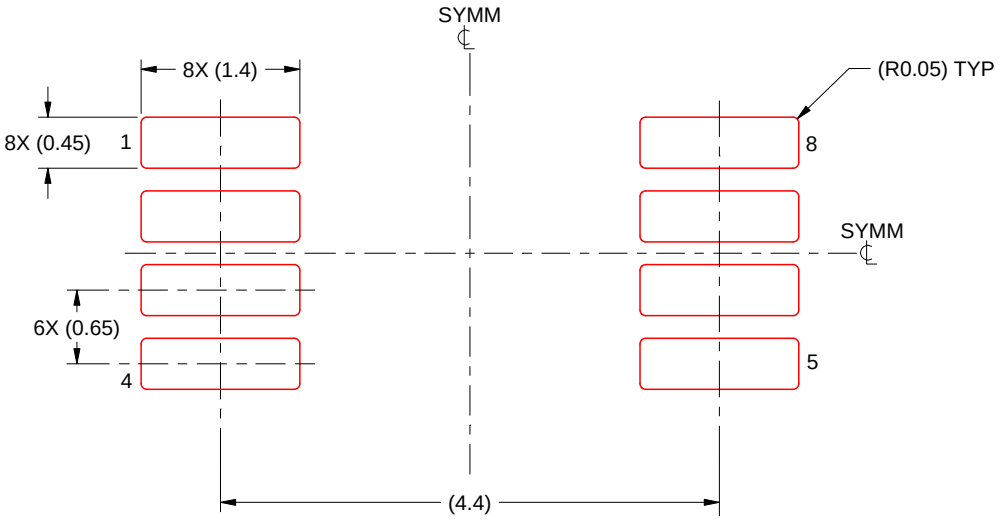


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

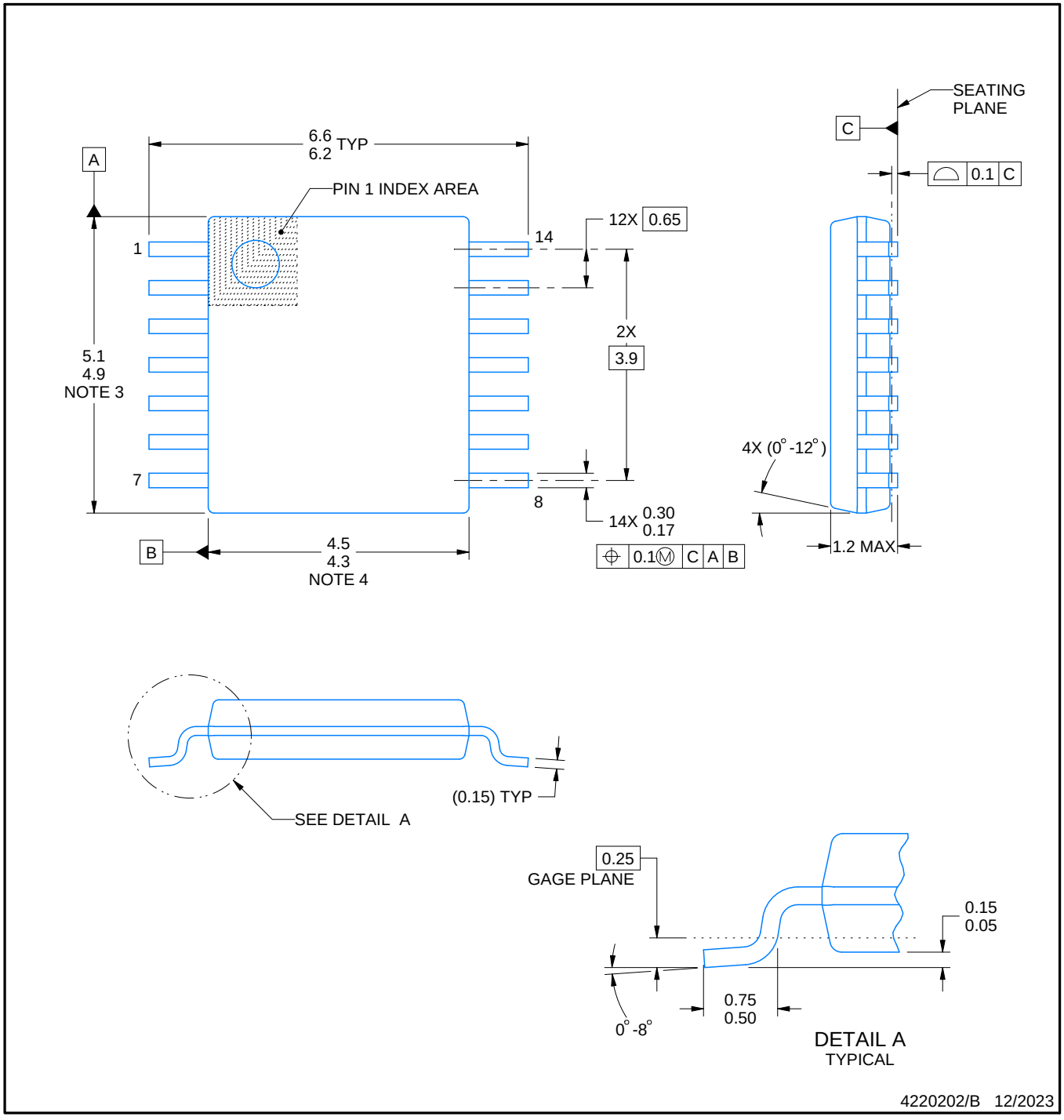
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

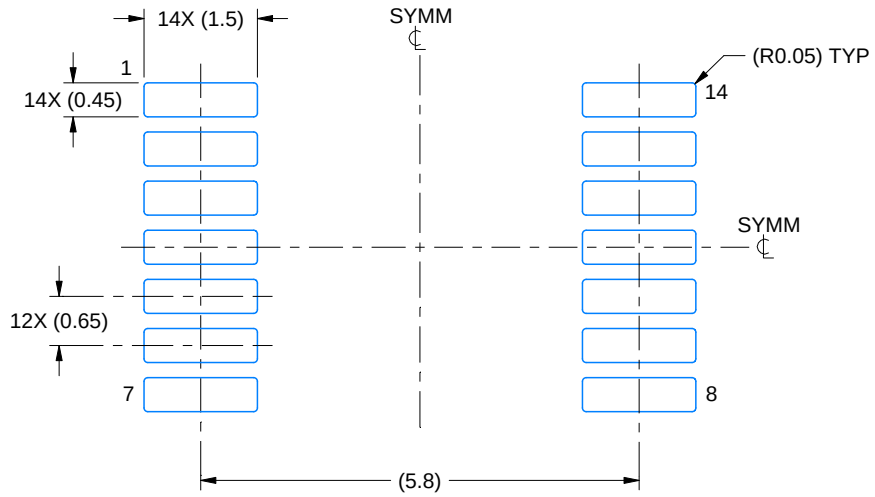
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

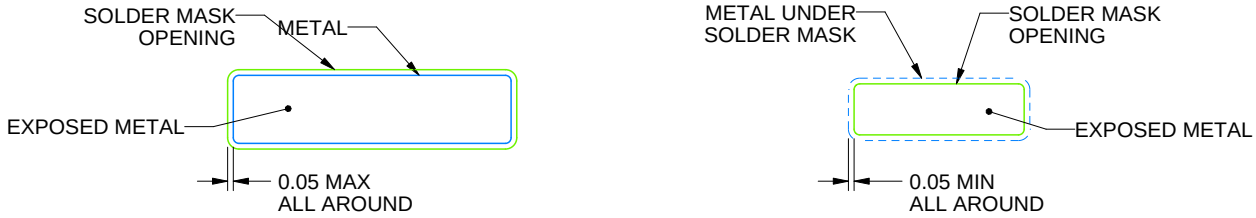


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

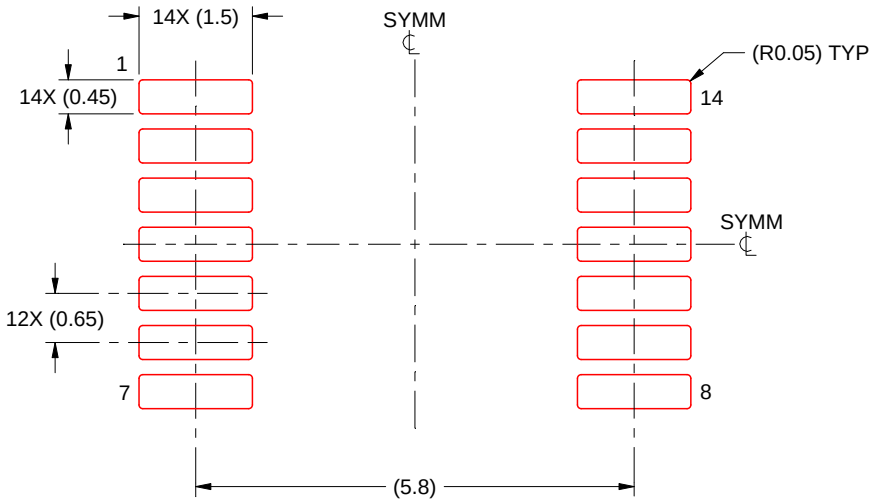


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

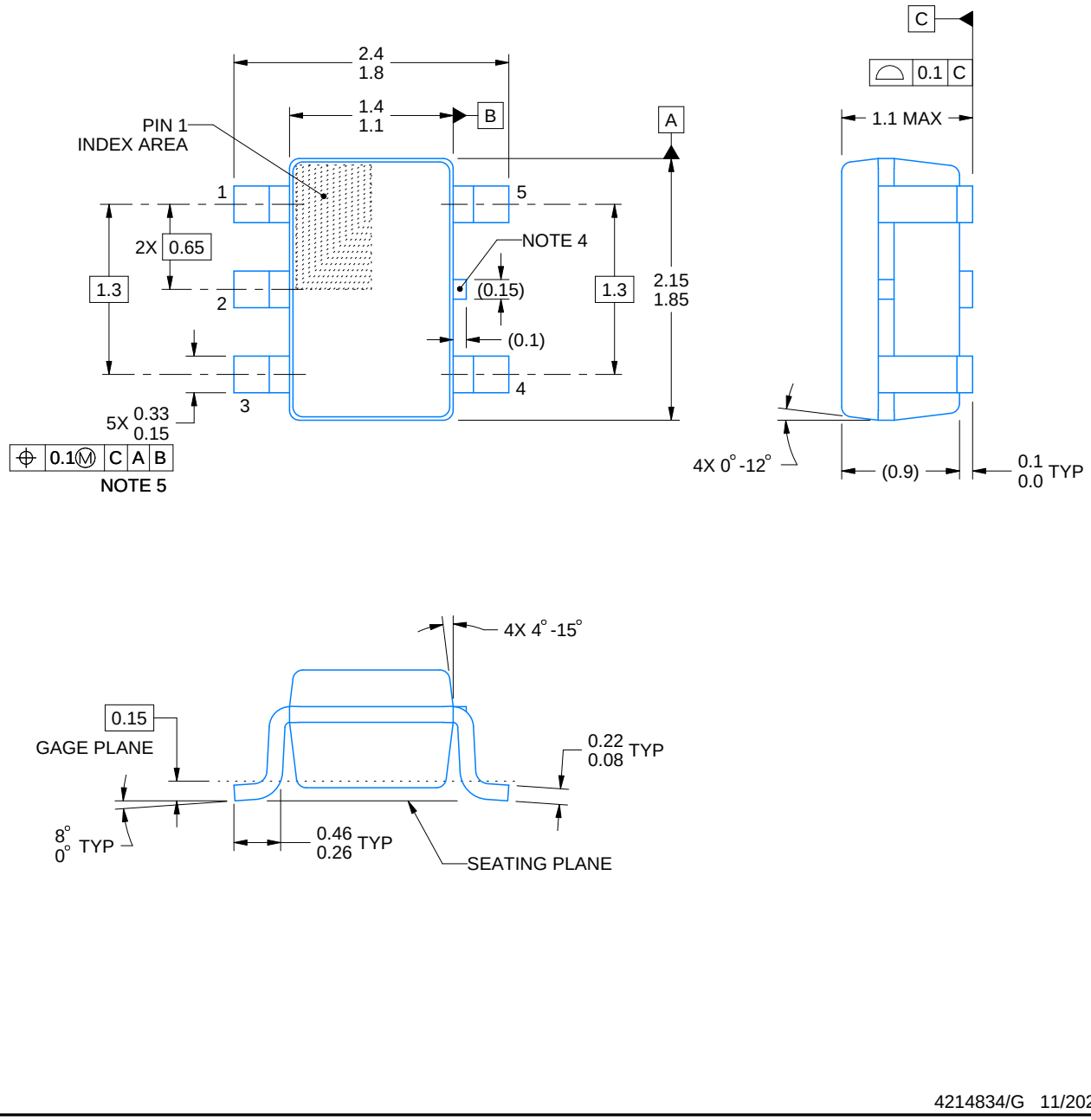
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

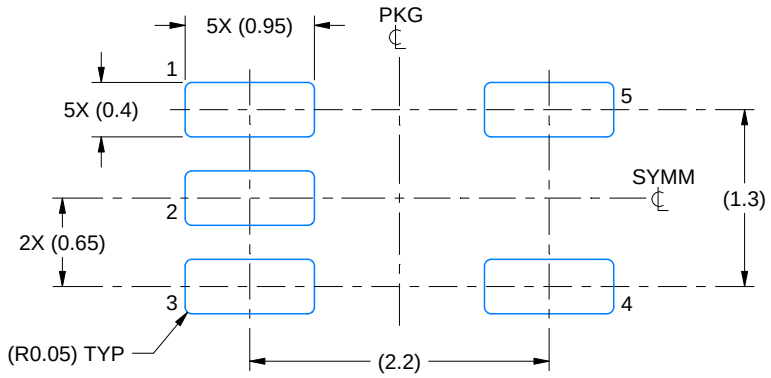
SMALL OUTLINE TRANSISTOR



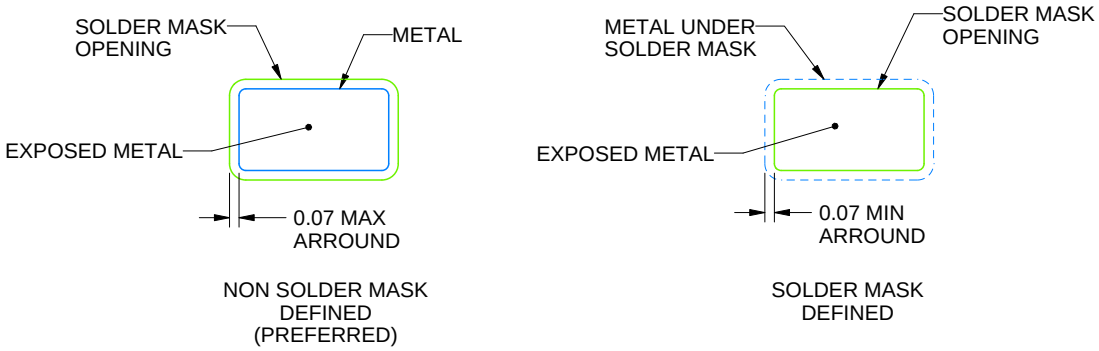
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

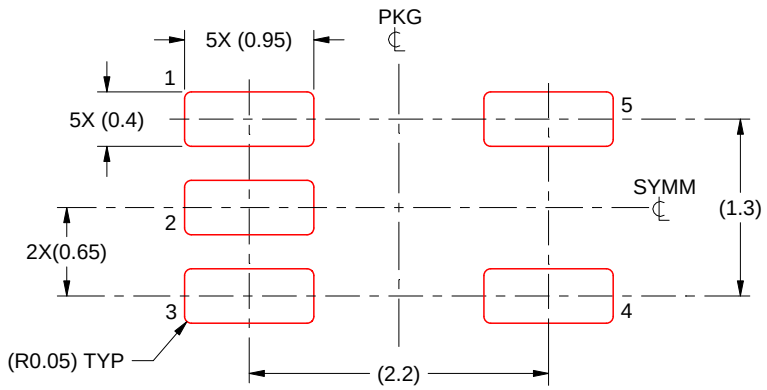


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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