LMV71x-N 低消費電力、RRIOオペアンプ、大出力電流駆動およびシャットダウン・オプション付き

1 特長

- 低いオフセット電圧: 3mV (最大値)
- ゲイン帯域幅積: 5MHz (標準値)
- スルーレート: 5v/µs (標準値)
- 容積を削減できるパッケージ: 5ピンおよび6ピンのSOT-23
- シャットダウンからのターンオン時間: 10µs未満
- 工業用温度範囲: -40℃～85℃
- シャットダウン・モードでの消費電流: 0.2µA (標準値)
- 2.7Vと5Vにおけるパフォーマンスの保証
- ユニティ・ゲインで安定
- レール・ツー・レール入出力
- 600Ωの負荷を駆動可能

2 アプリケーション

- ワイヤレス電話
- GSM、TDMA、CDMAのパワー・アンプ制御
- AGCおよびRFパワー検出器
- 温度補償
- ワイヤレスLAN
- Bluetooth
- HomeRF

3 概要

LMV710-N、LMV711-N、LMV715-Nは、CMOS入力段を持つBiCMOSオペアンプです。これらのデバイスは、RRを超える入力コモンモード電圧範囲、レール・ツー・レール出力、高い出力電流駆動能力を備えています。これらのデバイスは、5MHzの帯域幅と5V/µsのスルー・レートを実現します。

LMV711およびLMV715では、独立したシャットダウン・ピンを使用してデバイスをディセーブルでき、消費電流が0.2µA (標準値)まで低下します。また、ターンオン時間が10µs未満であることも特長です。これらのデバイスは、携帯電話、ポケベル、パームトップ・コンピュータなど電力の制限が厳しい用途に理想的なソリューションです。さらに、LMV715がシャットダウン状態になると、出力はトライステートになります。

LMV710は容積を節約できる5ピンのSOT-23パッケージで提供されます。LMV711およびLMV715は、容積を節約できる6ピンのSOT-23パッケージで提供されます。

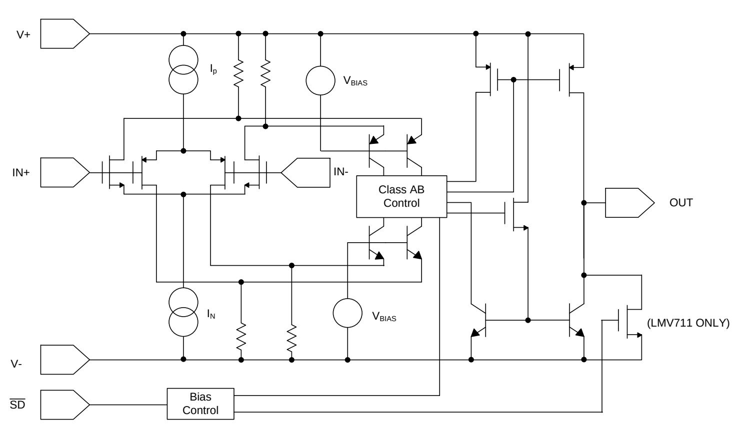
LMV71x-Nデバイスは、携帯電話などバッテリ駆動の携帯電子機器における低消費電力、低コスト、小型化への要求を満たすよう設計されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMV710-N	SOT-23 (5)	2.92mm×1.50mm
LMV711-N LMV715-N	SOT-23 (6)	2.92mm×1.50mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図 – LMV711



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4 改訂履歴

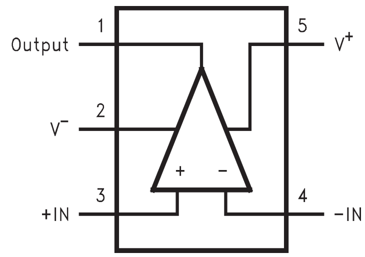
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision J (March 2013) から **Revision K** に変更 **Page**

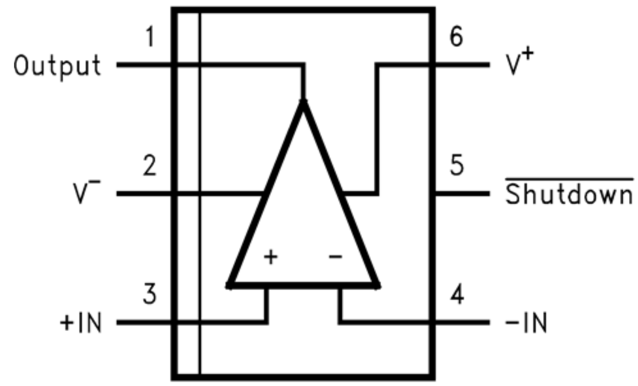
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

5 Pin Configuration and Functions

LMV710 DBV Package
5-Pin SOT-23
Top View



LMV711, LMV715 DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	DBV (5)	DBV (6)		
+IN	3	3	I	Noninverting input
–IN	4	4	I	Inverting input
Output	1	1	O	Output
$\overline{\text{Shutdown}}$	—	5	I	Active low enable input
V^+	5	6	P	Positive supply input
V^-	2	2	P	Supply negative input

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Differential input voltage	±Supply voltage		
Voltage at input or output pin	$(V^-) - 0.4$	$(V^+) + 0.4$	V
Supply voltage ($V^+ - V^-$)		5.5	V
Output short circuit to V^+	See(3)		
Output short circuit to V^-	See(4)		
Current at input pin		±10	mA
Mounting temperature, infrared or convection (20 sec)		235	°C
Junction temperature, $T_{J(MAX)}$(5)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Shorting circuit output to V^+ will adversely affect reliability.
(4) Shorting circuit output to V^- will adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)(2)	±2000	V
		Machine model (MM)(3)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human-body model, 1.5 kΩ in series with 100 pF.
(3) Machine model, 0 Ω in series with 100 pF.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage	2.7	5	V
Temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMV710-N	LMV711-N	LMV715-N	UNIT
		DBV (SOT-23)	DBV (SOT-23)	DBV (SOT-23)	
		5 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	265	265	265	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	131.6	139	156.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.1	38.5	32.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.2	28.6	34	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.5	37.9	32.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics – 2.7 V

T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.35 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OS}	Input offset voltage	V_{CM} = 0.85 V and V_{CM} = 1.85 V	T_J = 25°C		0.4	3	mV
			T_J = –40°C to 85°C			3.2	
I_B	Input bias current				4		pA
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 2.7 V	T_J = 25°C	50	75		dB
			T_J = –40°C to 85°C	45			
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 5 V, V_{CM} = 0.85 V	T_J = 25°C	70	110		dB
			T_J = –40°C to 85°C	68			
		2.7 V ≤ V^+ ≤ 5 V, V_{CM} = 1.85 V	T_J = 25°C	70	95		
			T_J = –40°C to 85°C	68			
V_{CM}	Input common-mode voltage range	For CMRR ≥ 50 dB	V–	–0.2	–0.3		V
			V+		3	2.9	
I_{SC}	Output short-circuit current	Sourcing, V_O = 0 V	T_J = 25°C	15	28		mA
			T_J = –40°C to 85°C	12			
		Sinking, V_O = 2.7 V	T_J = 25°C	25	40		
			T_J = –40°C to 85°C	22			
V_O	Output swing	R_L = 10 kΩ to 1.35 V VID = 100 mV	T_J = 25°C	2.62	2.68		V
			T_J = –40°C to 85°C	2.6			
		R_L = 10 kΩ to 1.35 V VID = –100 mV	T_J = 25°C		0.01	0.12	
			T_J = –40°C to 85°C			0.15	
		R_L = 600 Ω to 1.35 V VID = 100 mV	T_J = 25°C	2.52	2.55		
			T_J = –40°C to 85°C	2.5			
		R_L = 600 Ω to 1.35 V VID = –100 mV	T_J = 25°C		0.05	0.23	
			T_J = –40°C to 85°C			0.3	
V_O(SD)	Output voltage level in shutdown mode	LMV711 only			50	200	mV
I_O(SD)	Output leakage current in shutdown mode	LMV715 only			1		pA
C_O(SD)	Output capacitance in shutdown mode	LMV715 only			32		pF
I_S	Supply current	ON mode	T_J = 25°C		1.22	1.7	mA
			T_J = –40°C to 85°C			1.9	
		Shutdown mode, V_{SD} = 0 V			0.002	10	µA
A_V	Large signal voltage	Sourcing, R_L = 10 kΩ, V_O = 1.35 V to 2.3 V	T_J = 25°C	80	115		dB
			T_J = –40°C to 85°C	76			
		Sinking, R_L = 10 kΩ, V_O = 0.4 V to 1.35 V	T_J = 25°C	80	113		
			T_J = –40°C to 85°C	76			
		Sourcing, R_L = 600 Ω, V_O = 1.35 V to 2.2 V	T_J = 25°C	80	110		
			T_J = –40°C to 85°C	76			
		Sinking, R_L = 600 Ω, V_O = 0.5 V to 1.35 V	T_J = 25°C	80	100		
			T_J = –40°C to 85°C	76			
SR	Slew rate[3]				5		V/µs
GBWP	Gain-bandwidth product				5		MHz
φ_m	Phase margin				60		°
T_{ON}	Turnon time from shutdown				<10		µs

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Number specified is the slower of the positive and negative slew rates.

Electrical Characteristics – 2.7 V (continued)

T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.35 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{SD}	Shutdown pin voltage range	ON mode	2.4	1.5	2.7	V
		Shutdown mode	0	1	0.8	
e_n	Input-referred voltage noise	f = 1 kHz		20		nV/√Hz

6.6 Electrical Characteristics – 3.2 V

T_J = 25°C, V^+ = 3.2 V, V^- = 0 V, and V_{CM} = 1.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_O	Output Swing	I_O = 6.5 mA	T_J = 25°C	2.95	3		V
			T_J = –40°C to 85°C	2.92			
			T_J = 25°C		0.01	0.18	
			T_J = –40°C to 85°C			0.25	

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

6.7 Electrical Characteristics – 5 V

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2.5 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input offset voltage	V_{CM} = 0.85 V and V_{CM} = 1.85 V	T_J = 25°C		0.4	3	mV
			T_J = –40°C to 85°C			3.2	
I_B	Input bias current				4		pA
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 5 V	T_J = 25°C	50	70		dB
			T_J = –40°C to 85°C	48			
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 5 V, V_{CM} = 0.85 V	T_J = 25°C	70	110		dB
			T_J = –40°C to 85°C	68			
		2.7 V ≤ V^+ ≤ 5 V, V_{CM} = 1.85 V	T_J = 25°C	70	95		
			T_J = –40°C to 85°C	68			
V_{CM}	Input common-mode voltage range	For CMRR ≥ 50 dB	V–	–0.2	–0.3		V
			V+		5.3	5.2	
I_{SC}	Output short-circuit current	Sourcing, V_O = 0 V	T_J = 25°C	25	35		mA
			T_J = –40°C to 85°C	21			
		Sinking, V_O = 5 V	T_J = 25°C	25	40		
			T_J = –40°C to 85°C	21			
V_O	Output swing	R_L = 10 kΩ to 2.5 V VID = 100 mV	T_J = 25°C	4.92	4.98		V
			T_J = –40°C to 85°C	4.9			
		R_L = 10 kΩ to 2.5 V VID = –100 mV	T_J = 25°C		0.01	0.12	
			T_J = –40°C to 85°C			0.15	
		R_L = 600 Ω to 2.5 V VID = 100 mV	T_J = 25°C	4.82	4.85		
			T_J = –40°C to 85°C	4.8			
		R_L = 600 Ω to 2.5 V VID = –100 mV	T_J = 25°C		0.05	0.23	
			T_J = –40°C to 85°C			0.3	
V_O(SD)	Output voltage level in shutdown mode	LMV711 only			50	200	mV
I_O(SD)	Output leakage current in shutdown mode	LMV715 only			1		pA

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

Electrical Characteristics – 5 V (continued)

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2.5 V, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
C_O(SD)	Output capacitance in shutdown mode	LMV715 only			32		pF
I_S	Supply current	ON mode	T_J = 25°C		1.17	1.7	mA
			T_J = –40°C to 85°C			1.9	
		Shutdown mode			0.2	10	µA
A_V	Large signal voltage gain	Sourcing, R_L = 10 kΩ, V_O = 2.5 V to 4.6 V	T_J = 25°C	80	123		dB
			T_J = –40°C to 85°C	76			
		Sinking, R_L = 10 kΩ, V_O = 0.4 V to 2.5 V	T_J = 25°C	80	120		
			T_J = –40°C to 85°C	76			
		Sourcing, R_L = 600 Ω, V_O = 2.5 V to 4.5 V	T_J = 25°C	80	110		
			T_J = –40°C to 85°C	76			
		Sinking, R_L = 600 Ω, V_O = 0.5 V to 2.5 V	T_J = 25°C	80	118		
			T_J = –40°C to 85°C	76			
SR	Slew rate(3)				5		V/µs
GBWP	Gain-bandwidth product				5		MHz
φ_m	Phase margin				60		°
T_{ON}	Turnon time from shutdown				<10		µs
V_{SD}	Shutdown pin voltage range	ON mode		2.4	2	5	V
		Shutdown mode		0	1.5	0.8	
e_n	Input-referred voltage noise	f = 1 kHz			20		nV/$\sqrt{\text{Hz}}$

(3) Number specified is the slower of the positive and negative slew rates.

6.8 Typical Characteristics

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

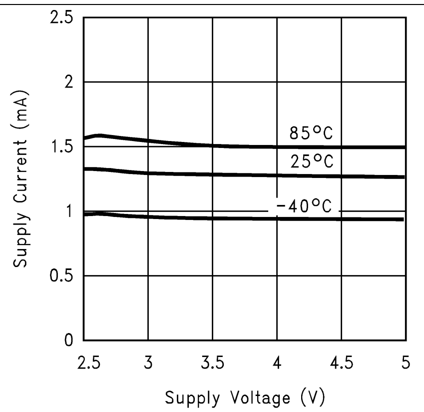


Figure 1. Supply Current vs Supply Voltage (ON Mode)

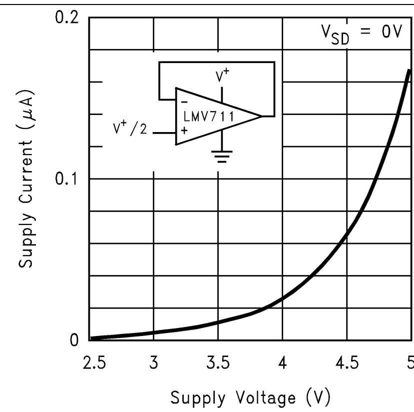


Figure 2. LMV711, LMV715 Supply Current vs Supply Voltage (Shutdown Mode)

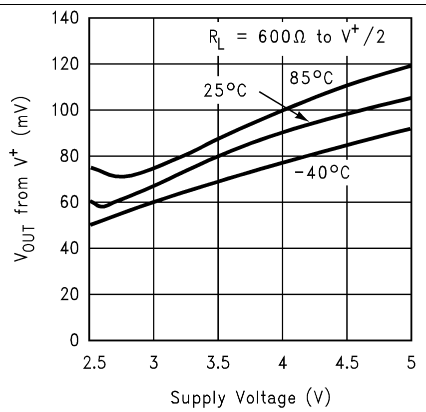


Figure 3. Output Positive Swing vs Supply Voltage

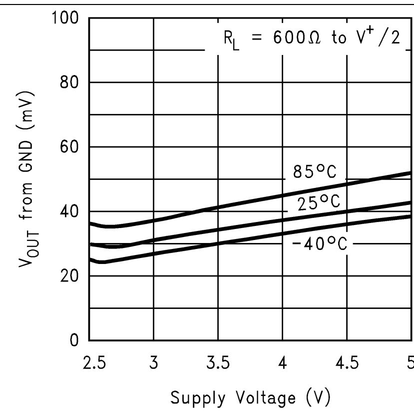


Figure 4. Output Negative Swing vs Supply Voltage

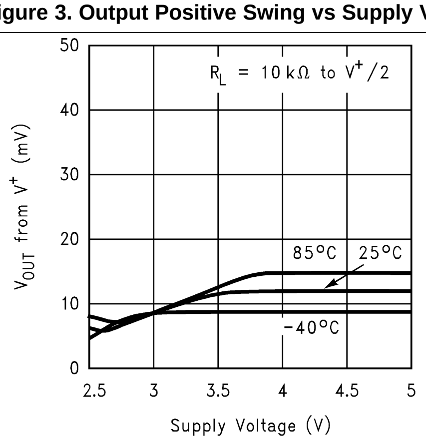


Figure 5. Output Positive Swing vs Supply Voltage

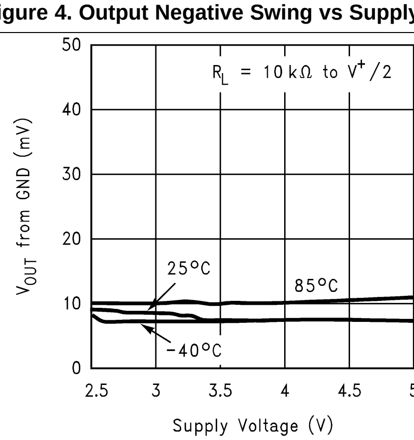


Figure 6. Output Negative Swing vs Supply Voltage

Typical Characteristics (continued)

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

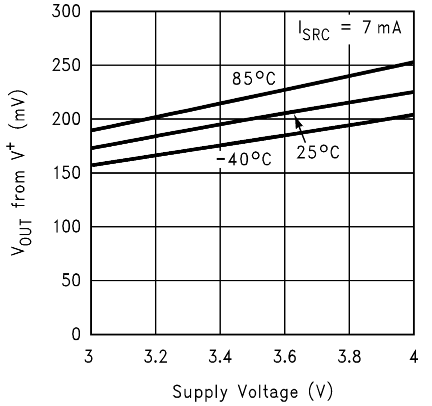


Figure 7. Output Positive Swing vs Supply Voltage

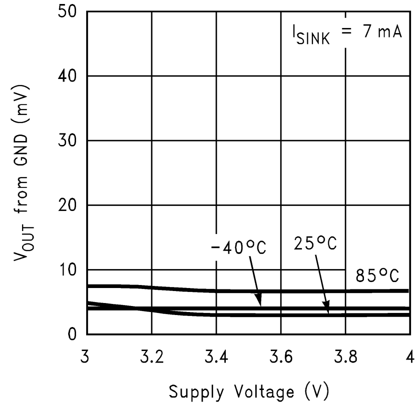


Figure 8. Output Negative Swing vs Supply Voltage

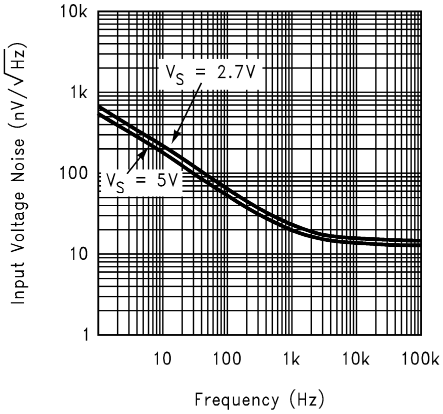


Figure 9. Input Voltage Noise vs Frequency

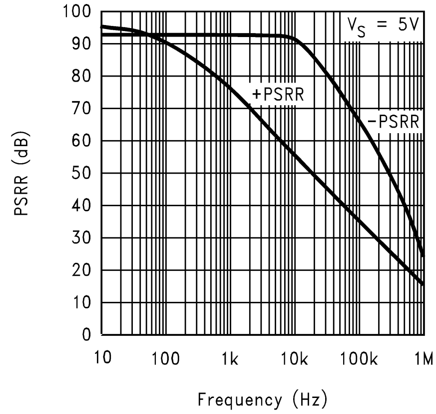


Figure 10. PSRR vs Frequency

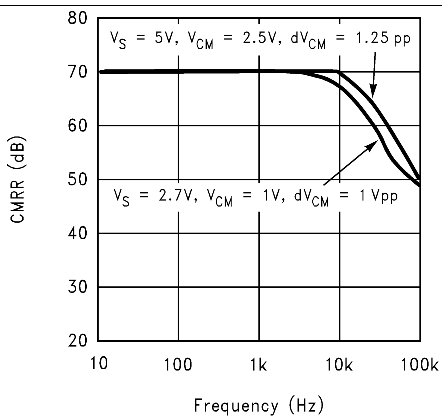


Figure 11. CMRR vs Frequency

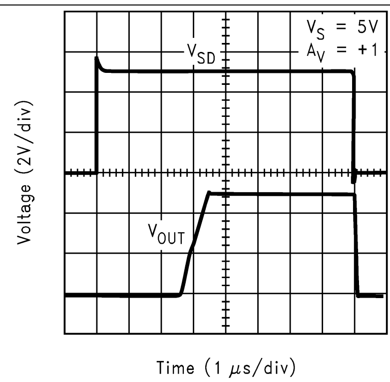


Figure 12. LMV711 and LMV715 Turnon Characteristics

Typical Characteristics (continued)

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

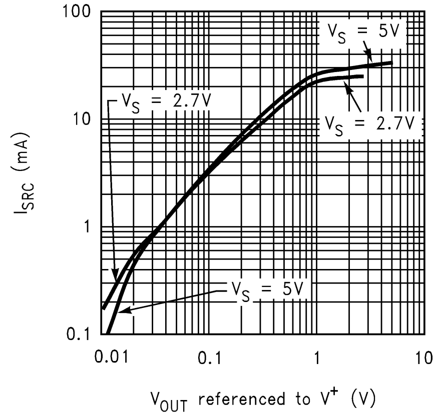


Figure 13. Sourcing Current vs Output Voltage

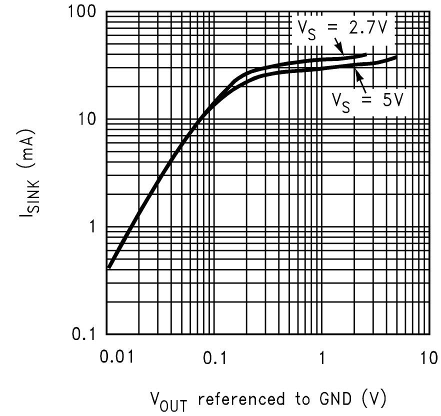


Figure 14. Sinking Current vs Output Voltage

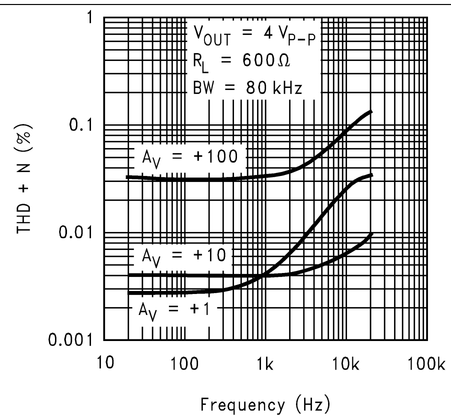


Figure 15. Thd+N vs Frequency (V_S = 5 V)

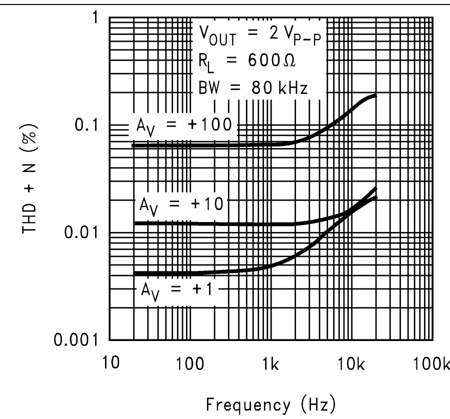


Figure 16. Thd+N vs Frequency (V_S = 2.7 V)

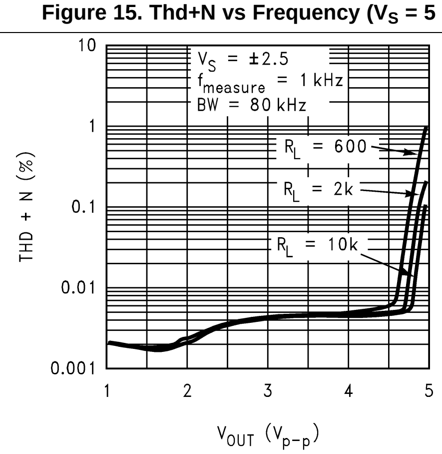


Figure 17. Thd+N vs V_{OUT}

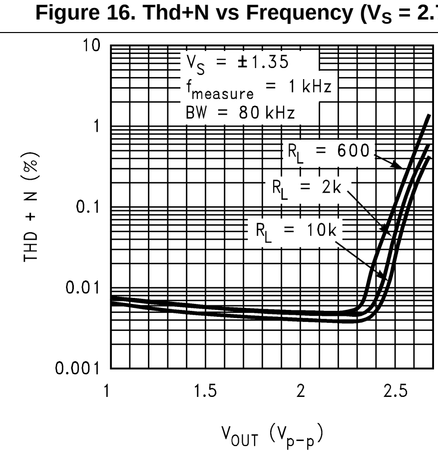


Figure 18. Thd+N vs V_{OUT}

Typical Characteristics (continued)

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

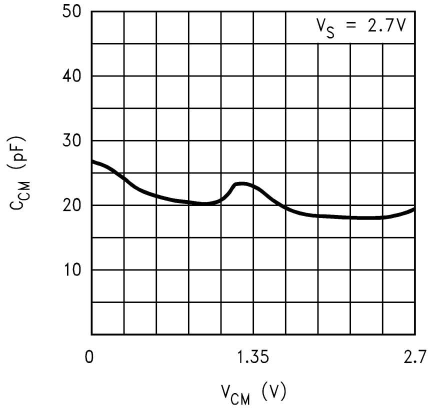


Figure 19. C_{CM} vs V_{CM}

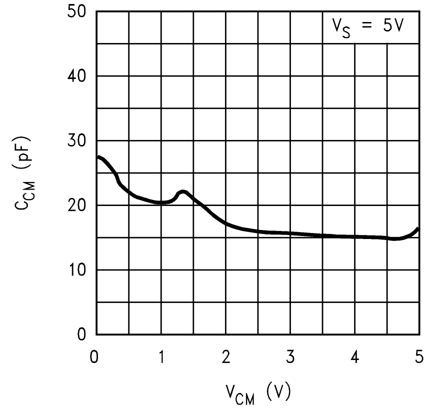


Figure 20. C_{CM} vs V_{CM}

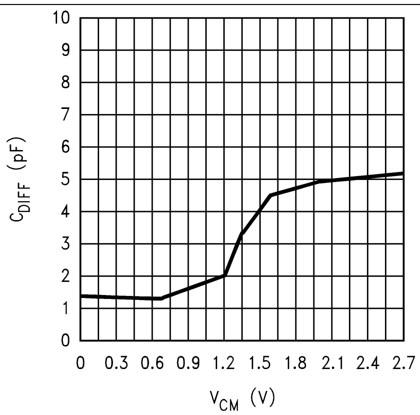


Figure 21. C_{DIFF} vs V_{CM} (V_S = 2.7 V)

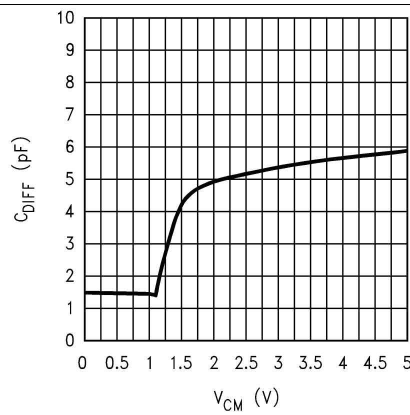


Figure 22. C_{DIFF} vs V_{CM} (V_S = 5 V)

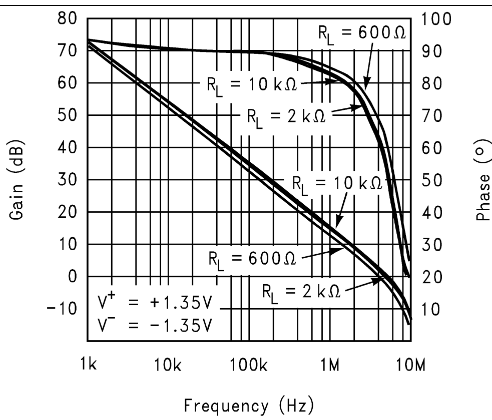


Figure 23. Open-Loop Frequency Response

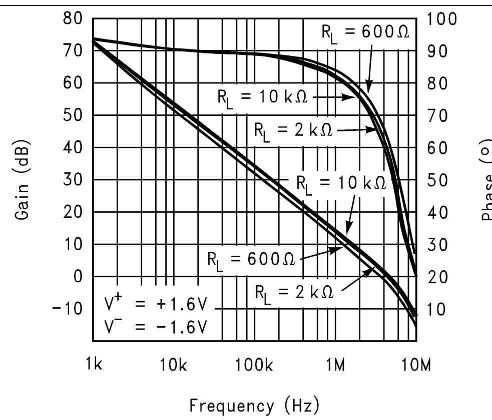


Figure 24. Open-Loop Frequency Response

Typical Characteristics (continued)

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

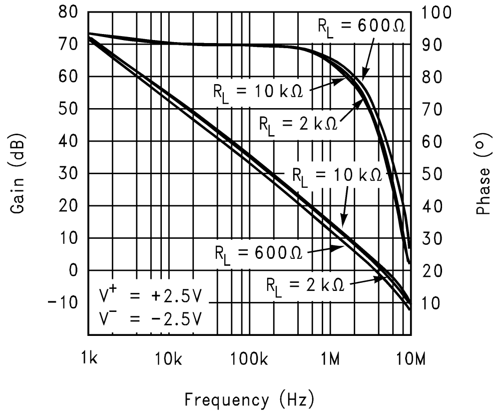


Figure 25. Open-Loop Frequency Response

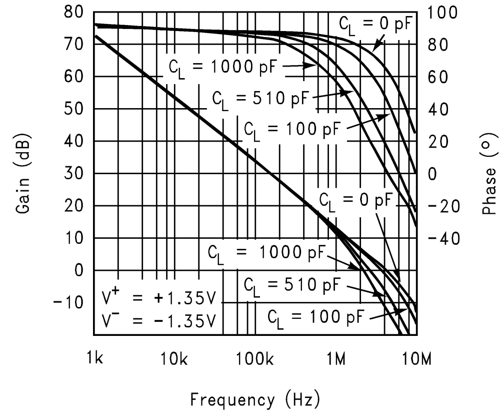


Figure 26. Open-Loop Frequency Response

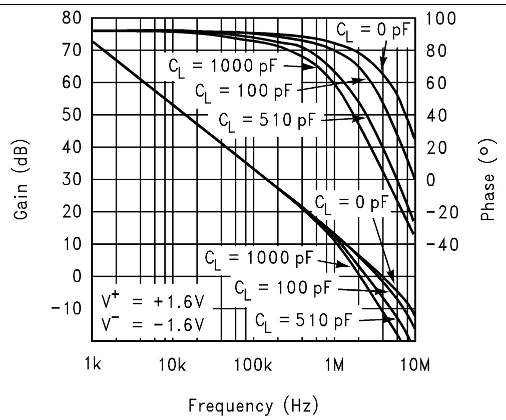


Figure 27. Open-Loop Frequency Response

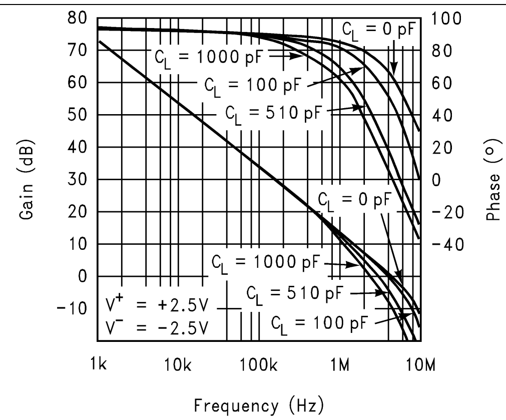


Figure 28. Open-Loop Frequency Response

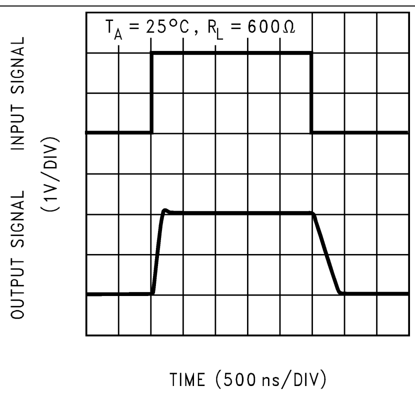


Figure 29. Noninverting Large Signal Pulse Response

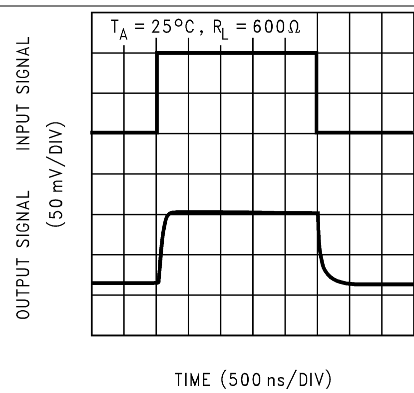


Figure 30. Noninverting Small Signal Pulse Response

Typical Characteristics (continued)

V_S = 5 V, single supply, T_A = 25°C (unless otherwise noted)

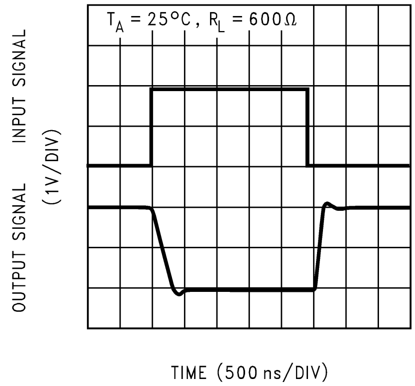


Figure 31. Inverting Large-Signal Pulse Response

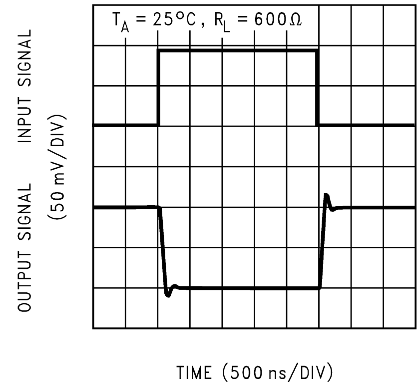


Figure 32. Inverting Small-Signal Pulse Response

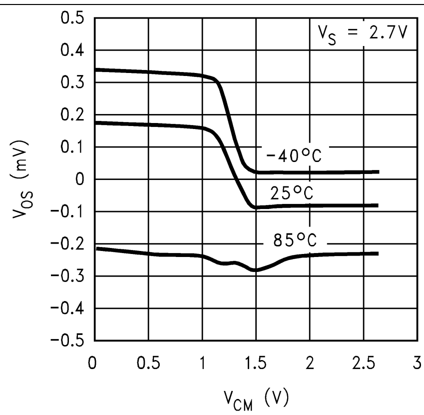


Figure 33. V_{OS} vs V_{CM}

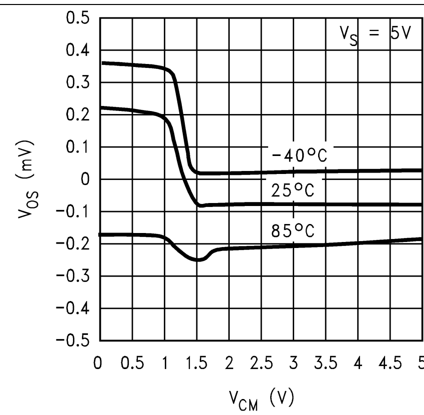


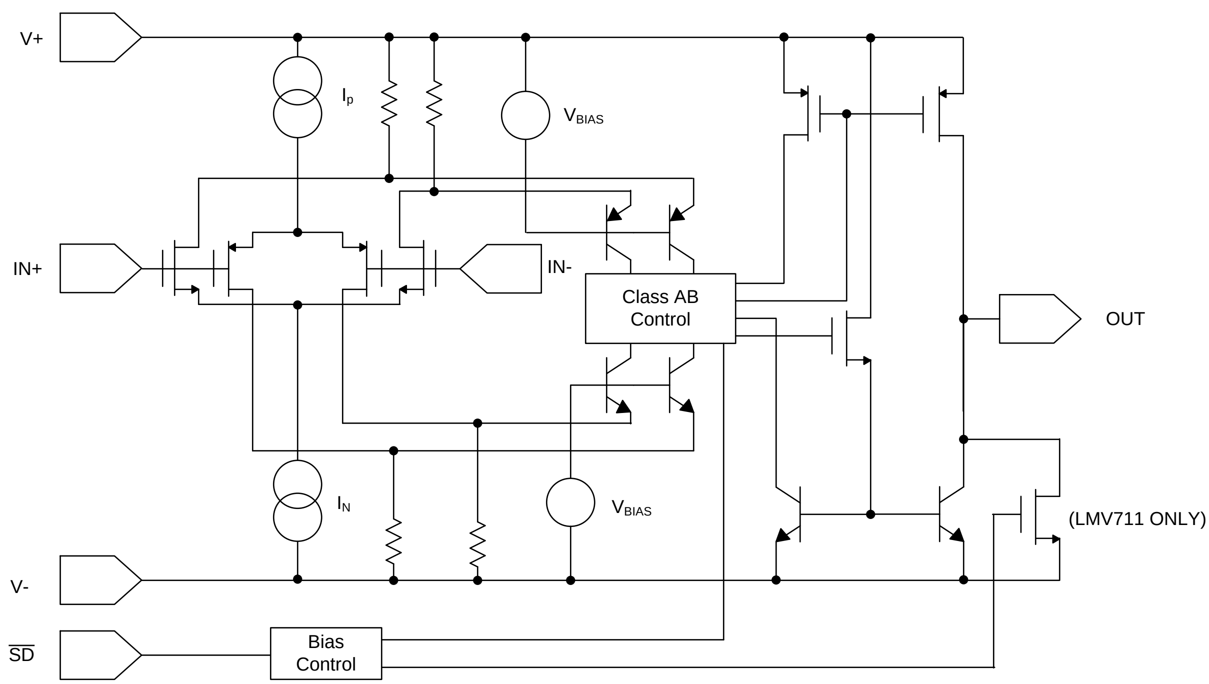
Figure 34. V_{OS} vs V_{CM}

7 Detailed Description

7.1 Overview

The LMV710-N, LMV711-N, and LMV715-N operational amplifiers provide a CMOS input stage, high current drive rail-to-rail output, and a greater than RR input common mode voltage range. They also provide a slew rate of 5 V/µs at a bandwidth of 5 MHz.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Supply Bypassing

The application circuits in this datasheet do not show the power supply connections and the associated bypass capacitors for simplification. When the circuits are built, it is always required to have bypass capacitors. Ceramic disc capacitors (0.1 µF) or solid tantalum (1 µF) with short leads, and located close to the IC are usually necessary to prevent interstage coupling through the power supply internal impedance. Inadequate bypassing will manifest itself by a low frequency oscillation or by high frequency instabilities. Sometimes, a 10-µF (or larger) capacitor is used to absorb low frequency variations and a smaller 0.1-µF disc is paralleled across it to prevent any high frequency feedback through the power supply lines.

7.3.2 Shutdown Mode

The LMV711 and LMV715 have a shutdown pin. To conserve battery life in portable applications, they can be disabled when the shutdown pin voltage is pulled low. For LMV711 during shutdown mode, the output stays at about 50 mV from the lower rail, and the current drawn from the power supply is 0.2 µA (typical). This makes the LMV711 an ideal solution for power sensitive applications. For the LMV715 during shutdown mode, the output is tri-stated.

The shutdown pin must never be left unconnected. In applications where shutdown operation is not required and the LMV711 or LMV715 is used, the shutdown pin must be connected to V^+. Leaving the shutdown pin floating results in an undefined operation mode and the device may oscillate between shutdown and active modes.

Feature Description (continued)

7.3.3 Rail-to-Rail Input

The rail-to-rail input is achieved by using paralleled PMOS and NMOS differential input stages (see *Functional Block Diagram*). When the common mode input voltage changes from ground to the positive rail, the input stage goes through three modes. First, the NMOS pair is cutoff and the PMOS pair is active. At around 1.4 V, both PMOS and NMOS pairs operate, and finally the PMOS pair is cutoff and NMOS pair is active. Because both input stages have their own offset voltage (V_{OS}), the offset of the amplifier becomes a function of the common-mode input voltage (see Figure 33 and Figure 34 in *Typical Characteristics*).

As shown in the curve, the V_{OS} has a crossover point at 1.4 V above V^-. Proper design must be done in both DC- and AC-coupled applications to avoid problems. For large input signals that include the V_{OS} crossover point in their dynamic range, it causes distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover point. For example, in a unity-gain buffer configuration and with V_S = 5 V, a 3-V peak-to-peak signal center at 2.5 V contains input-crossover distortion. To avoid this, the input signal must be centered at 3.5 V instead. Another way to avoid large signal distortion is to use a gain of −1 circuit which avoids any voltage excursions at the input terminals of the amplifier (see Figure 35). In this circuit, the common-mode DC voltage (V_{CM}) can be set at a level away from the V_{OS} crossover point.

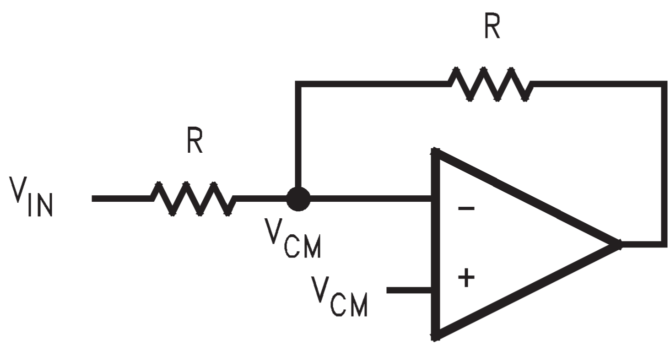


Figure 35. Inverting Configuration

When the input is a small signal and this small signal falls inside the V_{OS} transition range, the gain, CMRR and some other parameters is degraded. To resolve this problem, the small signal must be placed such that it avoids the V_{OS} crossover point.

To achieve maximum output swing, the output must be biased at mid-supply. This is normally done by biasing the input at mid-supply. But with supply voltage range from 2 V to 3.4 V, the input of the op amp must not be biased at mid-supply because of the transition of the V_{OS}. Figure 36 shows an example of how to get away from the V_{OS} crossover point and maintain a maximum swing with a 2.7-V supply. Figure 37 shows the waveforms of V_{IN} and V_{OUT}.

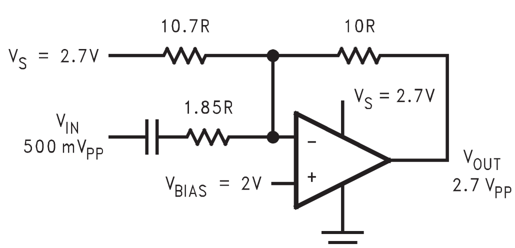


Figure 36. Vout biasing Example

Feature Description (continued)

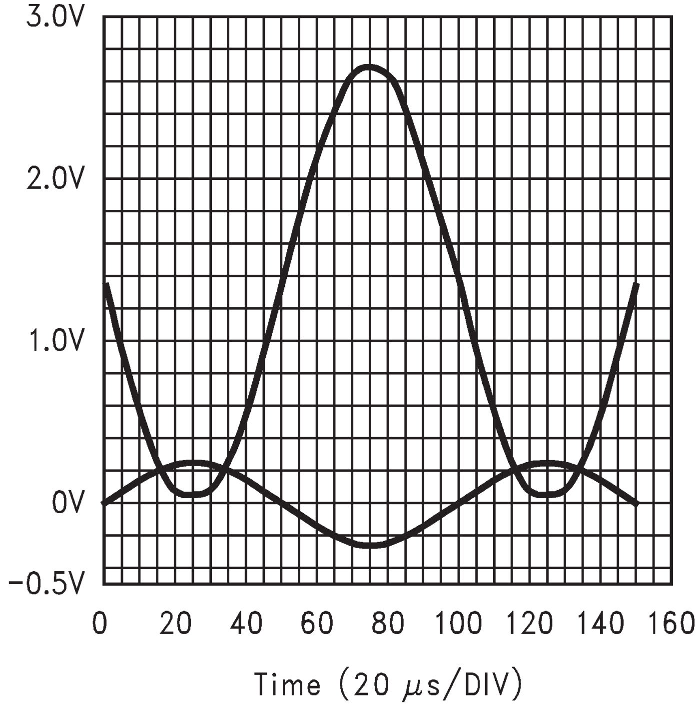


Figure 37. Vout biasing Output Results

The inputs can be driven 300 mV beyond the supply rails without causing phase reversal at the output. However, the inputs must not be allowed to exceed the maximum ratings.

7.4 Device Functional Modes

7.4.1 Compensation of Input Capacitance

In the application (Figure 38) where a large feedback resistor is used, the feedback resistor can react with the input capacitance of the op amp and introduce an additional pole to the close loop frequency response.

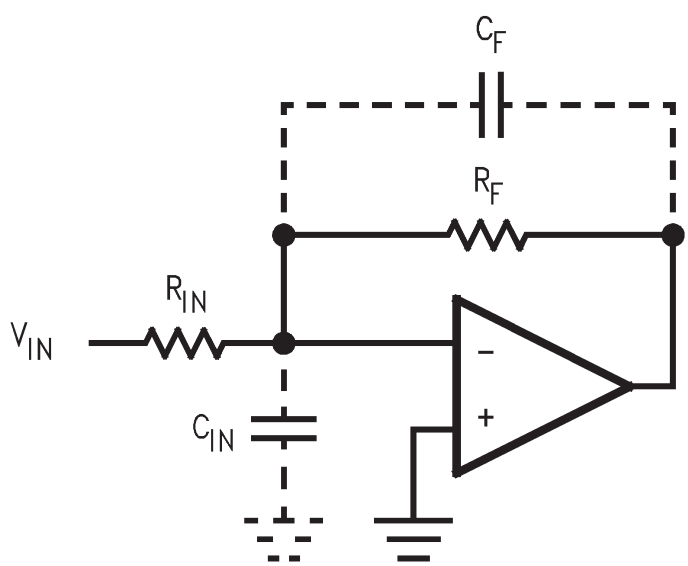


Figure 38. Cancelling the Effect of Input Capacitance

Device Functional Modes (continued)

This pole occurs at frequency f_p with Equation 1.

$$f_P = \frac{1}{2\pi(R_{IN} \parallel R_F)C_{IN}} \quad (1)$$

Any stray capacitance due to external circuit board layout, any source capacitance from transducer or photodiode connected to the summing node is added to the input capacitance. If f_p is less than or close to the unity-gain bandwidth (5 MHz) of the op amp, the phase margin of the loop is reduced and can cause the system to be unstable.

To avoid this problem, make sure that f_p occurs at least 2 octaves beyond the expected −3 dB frequency corner of the close loop frequency response. If not, a feedback capacitor C_F can be placed in parallel with R_F such that Equation 2.

$$\frac{1}{2\pi R_F C_F} = \frac{1}{2\pi(R_{IN} \parallel R_F)(C_F + C_{IN})} \quad (2)$$

The paralleled R_F and C_F introduce a zero, which cancels the effect from the pole.

7.4.2 Capacitive Load Tolerance

The LMV71x-N can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, circuit in Figure 39 can be used.

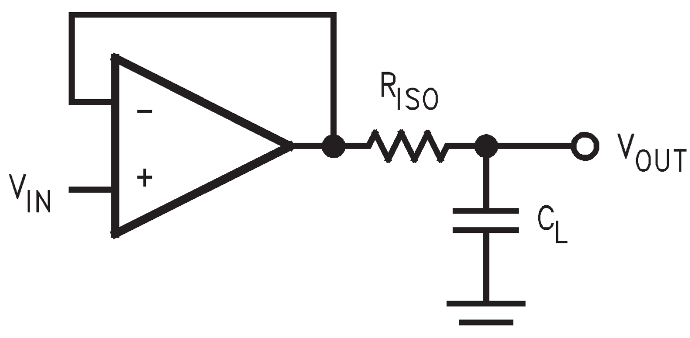


Figure 39. Indirectly Driving a Capacitive Load Using Resistive Isolation

In Figure 39, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} is. But the DC accuracy is not great when the R_{ISO} gets bigger. If there were a load resistor in Figure 39, the output would be voltage divided by R_{ISO} and the load resistor.

The circuit in Figure 40 is an improvement to the one in Figure 39 because it provides DC accuracy as well as AC stability. In this circuit, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high-frequency component of the output signal back to the inverting input of the amplifier, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F . This in turn slows down the pulse response.

Device Functional Modes (continued)

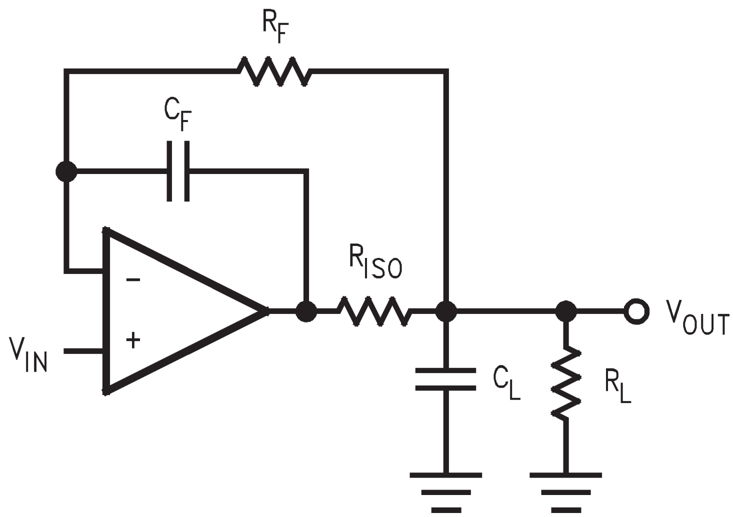


Figure 40. Indirectly Driving a Capacitive a Load With DC Accuracy

8 Application and Implementation

NOTE

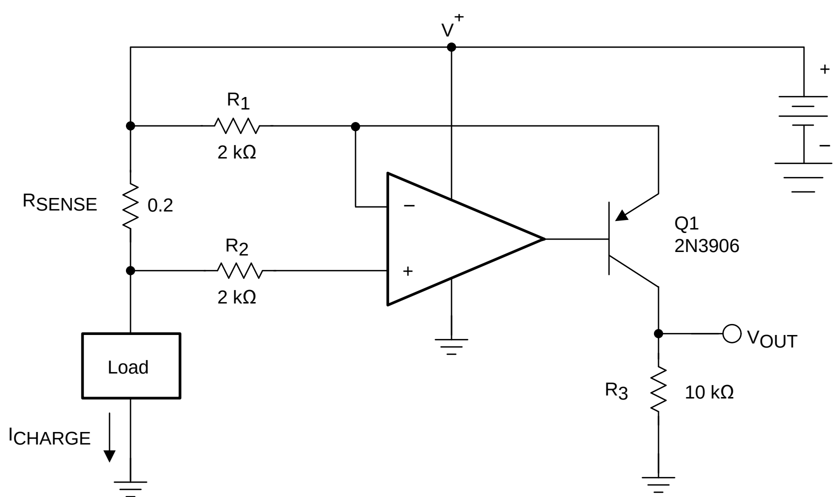
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV71x family of amplifiers features low voltage, low power, and rail-to-rail output operational amplifiers designed for low-voltage portable applications.

8.2 Typical Applications

8.2.1 High-Side Current-Sensing



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\,\Omega \bullet I_{Charge}$$

Figure 41. High-Side, Current-Sensing Schematic

8.2.1.1 Design Requirements

The high-side, current-sensing circuit (Figure 41) is commonly used in a battery charger to monitor charging current to prevent over charging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV71x are ideal for this application because its common-mode input range goes up to the rail.

8.2.1.2 Detailed Design Procedure

As seen in (Figure 41), the I_{CHARGE} current flowing through sense resistor R_{SENSE} develops a voltage drop equal to V_{SENSE}. The voltage at the negative sense point is now less than the positive sense point by an amount proportional to the V_{SENSE} voltage.

The low-bias currents of the LMV71x cause little voltage drop through R_2, so the negative input of the LMV71x amplifier is at essentially the same potential as the negative sense input.

The LMV71x detects this voltage error between its inputs and servo the transistor base to conduct more current through Q1, increasing the voltage drop across R_1 until the LMV71x inverting input matches the noninverting input. At this point, the voltage drop across R_1 now matches V_{SENSE}.

I_G, a current proportional to I_{CHARGE}, flows according to Equation 3.

Typical Applications (continued)

$$I_G = V_{RSENSE} / R_1 = (R_{SENSE} \times I_{CHARGE}) / R_1 \quad (3)$$

I_G also flows through the gain resistor R_3 developing a voltage drop equal to Equation 4.

$$V_3 = I_G \times R_3 = (V_{RSENSE} / R_1) \times R_3 = ((R_{SENSE} \times I_{CHARGE}) / R_2) \times R_3 \quad (4)$$

$$V_{OUT} = (R_{SENSE} \times I_{CHARGE}) \times G$$

where

- $G = R_3 / R_1$ (5)

The other channel of the LMV71x may be used to buffer the voltage across R3 to drive the following stages.

8.2.1.3 Application Curve

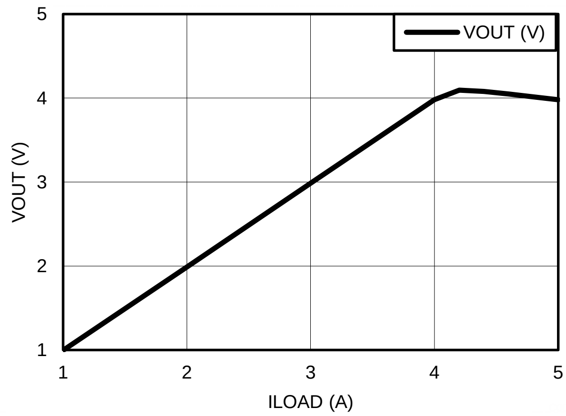


Figure 42. High-Side Current-Sensing Results

8.2.2 Peak Detector

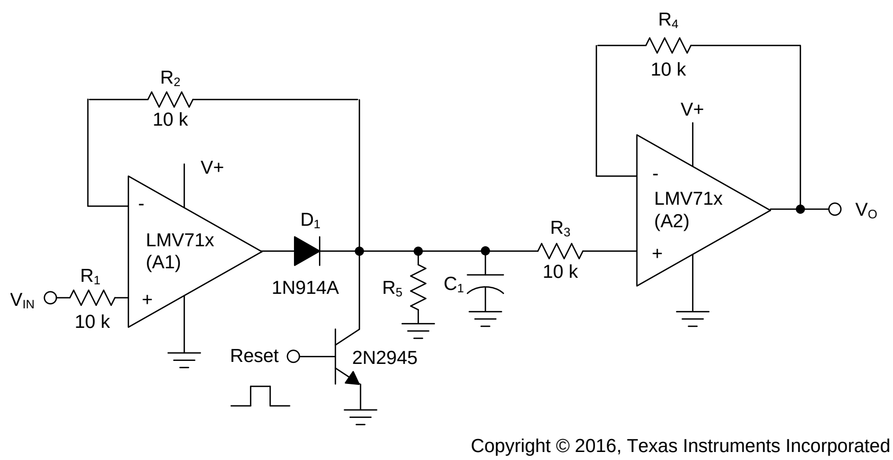


Figure 43. Peak Detector

8.2.2.1 Design Requirements

A peak detector outputs a DC voltage equal to the peak value of the applied AC signal. Peak detectors are used in many applications, such as test equipment, measurement instrumentation, ultrasonic alarm systems, and so forth. Figure 43 shows the schematic diagram of a peak detector using LMV71x-N. This peak detector basically consists of a clipper, a parallel RC network, and a voltage follower.

Typical Applications (continued)

8.2.2.2 Detailed Design Procedure

An AC voltage source applied to V_{IN} charges capacitor C1 to the peak of the input. Diode D1 conducts positive *half cycles*, charging C1 to the waveform peak. Including D1 inside the feedback loop of the amplifier removes the voltage drop of D1 and allows an accurate peak detection of V_{IN} on C1. When the input waveform falls below the DC *peak* stored on C1, D1 is reverse biased. The low input bias current of A1 and the reverse biasing of D1 limits current leakage from C1. As a result, C1 retains the peak value even as the waveform drops to zero. A2 further isolates the peak value on C1 while completing the peak detector circuit by operating as a voltage follower and reporting the peak voltage of C1 at its output.

R5 and C1 are properly selected so that the capacitor is charged rapidly to V_{IN}. During the holding period, the capacitor slowly discharge through C1, through leakage of the capacitor and the reverse-biased diode, or op amp bias currents. In any cases the discharging time constant is much larger than the charge time constant. And the capacitor can hold its voltage long enough to minimize the output ripple.

Resistors R2 and R3 limit the current into the inverting input of A1 and the noninverting input of A2 when power is disconnected from the circuit. The discharging current from C1 during power off may damage the input circuitry of the op amps.

The peak detector is reset by applying a positive pulse to the reset transistor. The charge on the capacitor is dumped into ground, and the detector is ready for another cycle.

The maximum input voltage to this detector must be less than ($V^+ - V_D$), where V_D is the forward voltage drop of the diode. Otherwise, the input voltage must be scaled down before applying to the circuit.

8.2.3 GSM Power Amplifier Control Loop

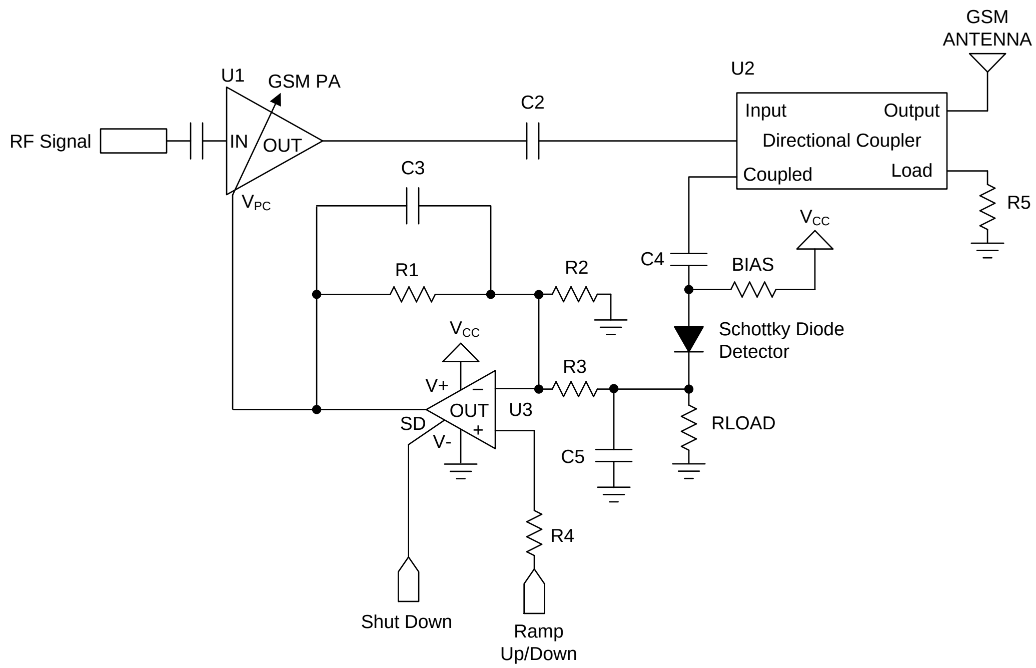


Figure 44. GSM P.A. Control Loop

8.2.3.1 Design Requirements

The control loop in Figure 44 controls the output power level of a GSM mobile phones. The control loop is used to avoid intermodulation of Base Station receivers, to prevent intermodulation with other mobile phones, and to minimize power consumption depending on the distance between mobile and base station

Typical Applications (continued)

8.2.3.2 Detailed Design Procedure

There are four critical sections in the GSM Power Amplifier Control Loop. The class-C R_F power amplifier provides amplification of the R_F signal. A directional coupler couples small amount of R_F energy from the output of the R_F P. A. to an envelope detector diode. The detector diode senses the signal level and rectifies it to a DC level to indicate the signal strength at the antenna. An op amp is used as an error amplifier to process the diode voltage and ramping voltage. This loop control the power amplifier gain through the op amp and forces the detector diode voltage and ramping voltage to be equal. Power control is accomplished by changing the ramping voltage.

The LMV71x-N are well suited as an error amplifier in this application. The LMV711 or LMV715 have an extra shutdown pin to switch the op amp to shutdown mode. In shutdown mode, the LMV711 or LMV715 consume very low current. The LMV711 provides a ground voltage to the power amplifier control pin V_{PC}. Therefore, the power amplifier can be turned off to save battery life. The LMV715 output is tri-stated when in shutdown.

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the power supply pins of the operational amplifier. For single supply, place a capacitor between V^+ and $V^–$ supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between $V^–$ and ground.

10 Layout

10.1 Layout Guidelines

To properly bypass the power supply, several locations on a printed-circuit board must be considered. A 6.8-µF or greater tantalum capacitor must be placed at the point where the power supply for the amplifier is introduced onto the board. Another 0.1-µF ceramic capacitor must be placed as close as possible to the power supply pin of the amplifier. If the amplifier is operated in a single power supply, only the V^+ pin requires a bypass with a 0.1-µF capacitor. If the amplifier is operated in a dual power supply, both V^+ and $V^–$ pins must be bypassed. It is good practice to use a ground plane on a printed-circuit board to provide all components with a low inductive ground connection.

10.2 Layout Example

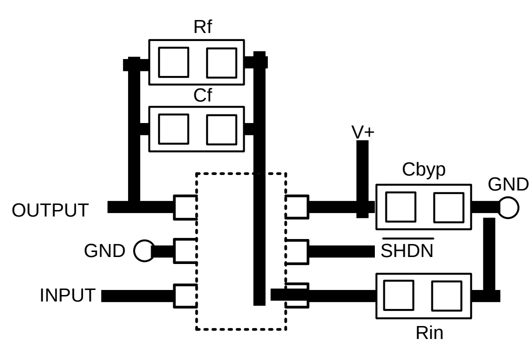


Figure 45. LMV711 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

開発サポートについては、以下を参照してください。

- LMV710 PSPICEモデル(LMV711およびLMV715に適応可能)
- SPICEベースのアナログ・シミュレーション・プログラム、TINA-TI
- DIPアダプタ評価モジュール、DIPアダプタEVM
- TIユニバーサル・オペアンプ評価モジュール、オペアンプEVM
- TIソフトウェア、FilterPro

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『ハンダ付けの絶対最大定格』*(SNOA549)
- *『AN-29 ICオペアンプのFETと比較した入力電流の優位性』*(SNOA624)
- *『AN-31オペアンプ回路コレクション』*(SNLA140)
- *『AN-71 LM4250プログラマブル・オペアンプを使用するMicropower回路』*(SNOA652)
- *『AN-127 LM143 モノリシック高電圧オペアンプのアプリケーション』*(SNVA516)

11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LMV710-N	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LMV711-N	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LMV715-N	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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11.5 コミュニティ・リソース

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.7 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.8 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV710M5/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A48A
LMV710M5/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A48A
LMV710M5X/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A48A
LMV710M5X/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	A48A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

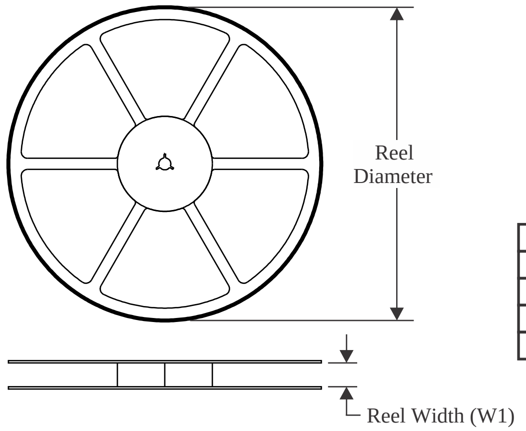
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

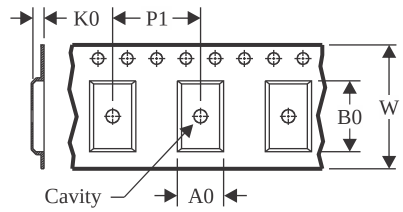
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

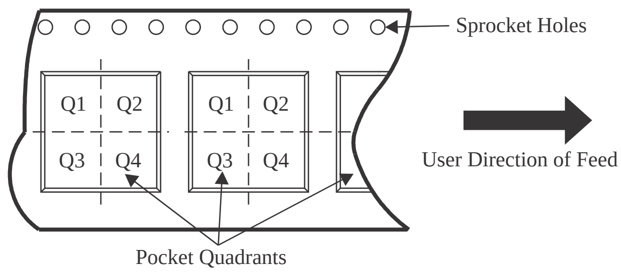


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

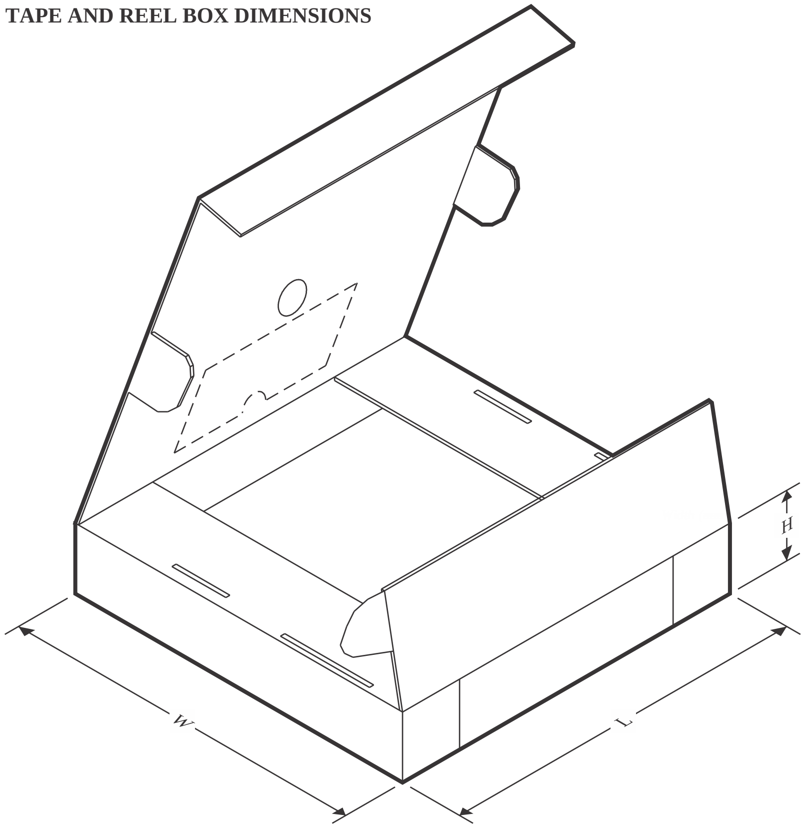
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

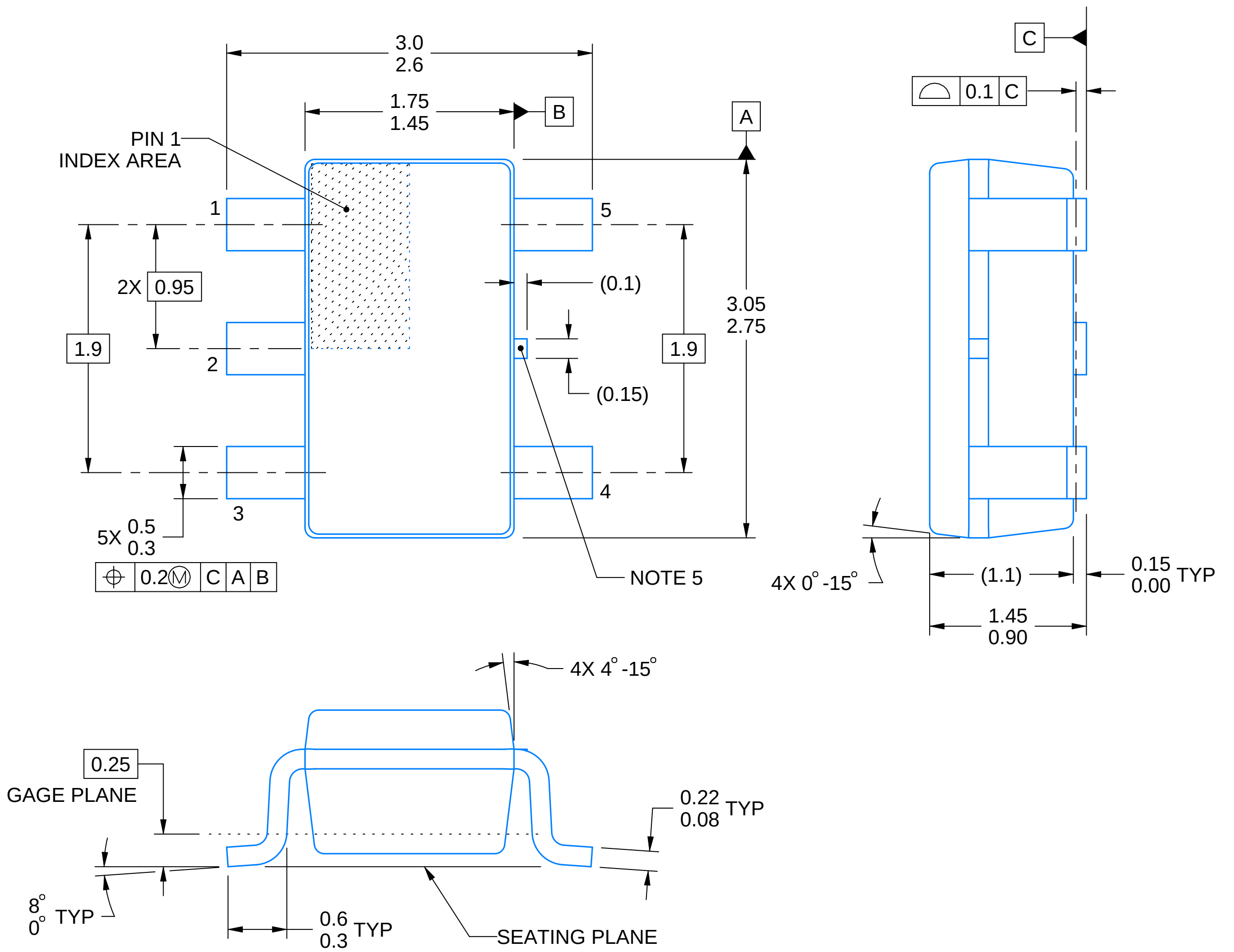
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV710M5/NOPB	SOT-23	DBV	5	1000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV710M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV710M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV710M5X/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV710M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV710M5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV710M5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV710M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0



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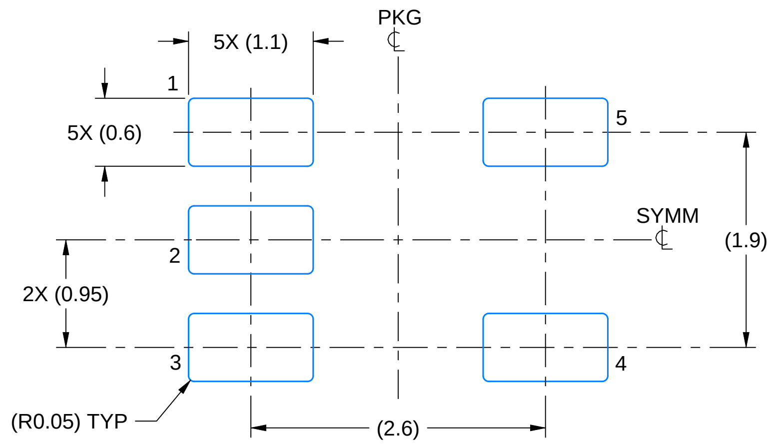
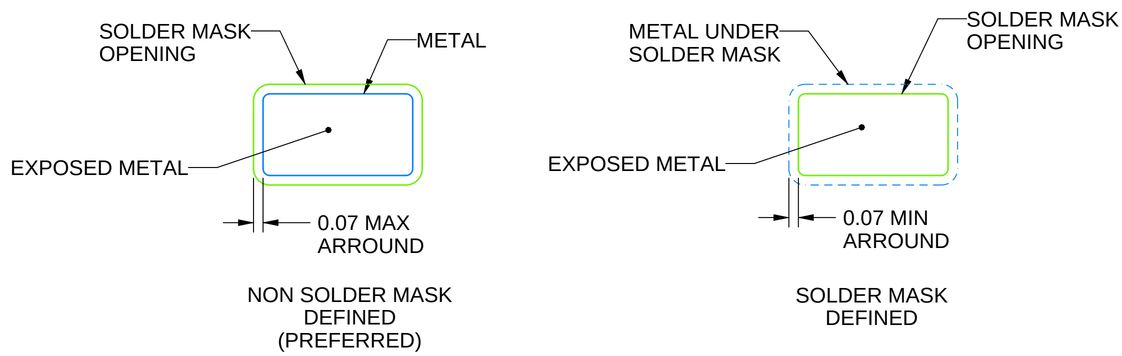
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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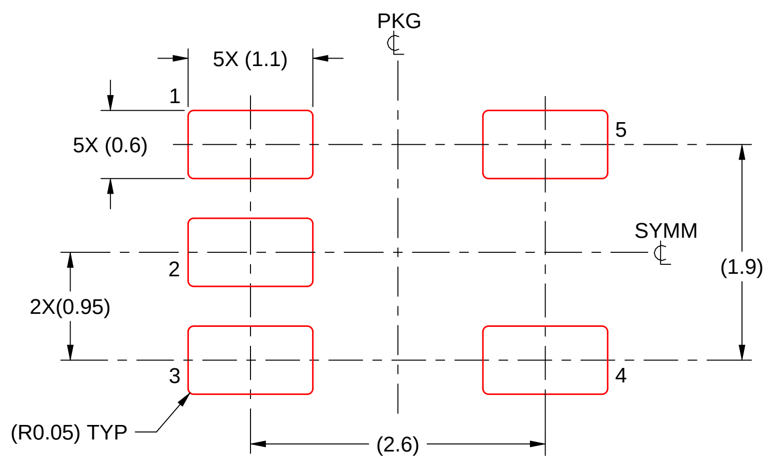
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項