参考資料

Texas Instruments
LP2992
JAJSS37K – NOVEMBER 2001 – REVISED DECEMBER 2023

LP2992 マイクロパワー、250mA、低ノイズ、超低ドロップアウト レギュレータ、SOT-23 および WSON パッケージ、超低 ESR の出力コンデンサで使用するように設計

1 特長

- V_{IN} 範囲 (新チップ)：2.5V～16V
- V_{OUT} 範囲 (新チップ)：
    - 1.2V～5.0V (固定、100mV ステップ)
- V_{OUT} 精度：
    - ±1% (A グレードの従来チップ)
    - ±1.5% (標準グレードの従来チップ)
    - ±0.5% (新チップのみ)
- 負荷および温度の全範囲にわたって ±1% の出力精度 (新チップの場合)
- 出力電流：最大 250 mA
- 低い I_Q (新チップ)：69μA (I_{LOAD} = 0 mA の場合)
- 低い I_Q (新チップ)：875μA (I_{LOAD} = 250 mA の場合)
- シャットダウン電流：
    - 0.01μA (標準値) (従来チップ)
    - 1.12μA (標準値) (新チップ)
- 低ノイズ：30μV_{RMS} (10nF のバイパス・コンデンサを使用した場合)
- 出力電流制限および過熱保護
- 2.2μF のセラミック・コンデンサで安定動作
- 高い PSRR：1kHz で 70dB、1MHz で 40dB
- 動作時接合部温度：-40℃～125℃
- パッケージ：5 ピン SOT-23 (DBV)

2 アプリケーション

- 洗濯機 / 乾燥機
- 陸上移動無線
- アクティブ・アンテナ・システムの mMIMO
- コードレス電動工具
- モータ・ドライブおよび制御基板

3 概要

LP2992 は、固定出力で入力範囲の広い、低ノイズ、低ドロップアウトの電圧レギュレータで、2.5V～16V の入力電圧範囲に対応し、最大 250mA の負荷電流を供給できます。LP2992 は、1.2V～5.0V の出力範囲をサポートしています (新チップの場合)。

さらに、LP2992 (新チップ) は、負荷および温度の全範囲にわたって 1% の出力精度を備えており、低電圧マイクロコントローラ (MCU) およびプロセッサのニーズを満たすことができます。

30μV_{RMS} (10nF のバイパス・コンデンサを使用) の低い出力ノイズと、1kHz で 70dB、1MHz で 40dB を上回る広い帯域幅の PSRR 性能により、上流側 DC/DC コンバータのスイッチング周波数を低くすることができ、さらに、レギュレータ後のフィルタ処理を最小限に抑えることができます。

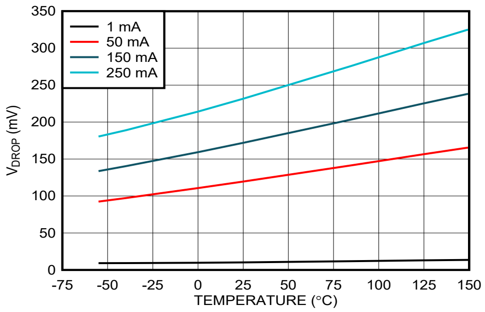
内部ソフトスタート時間および電流制限保護により、スタートアップ時の突入電流が減少し、入力静電容量を最小化しました。過電流および過熱保護などの一般的な保護機能を備えています。

LP2992 は、5 ピン、2.9mm × 2.8mm の SOT-23 (DBV) パッケージで供給されます。

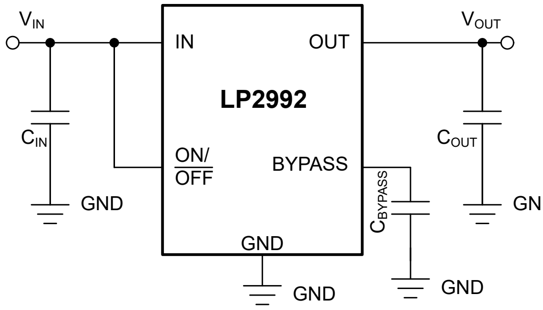
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ (2)
LP2992	DBV (SOT-23、5)	2.9mm × 2.8mm
	WSON (6)	3.29 mm×2.92 mm

(1) 詳細については、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



新チップのドロップアウト電圧と温度との関係



代表的なアプリケーション回路

English Data Sheet: SNVS171

Table of Contents

4 Pin Configuration and Functions

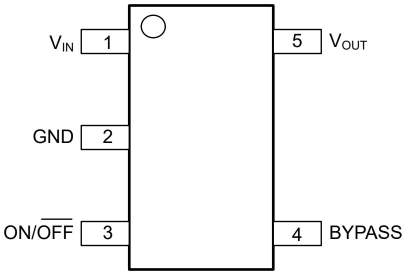


図 4-1. DBV Package, 5-Pin SOT-23 (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BYPASS	4	I/O	BYPASS pin to achieve low noise performance. Connecting an external capacitor between BYPASS pin and ground reduces reference voltage noise. See the セクション 5.3 section for more information.
GND	2	—	Ground
ON/$\overline{OFF}$	3	I	Enable pin for the LDO. Driving the ON/$\overline{OFF}$ pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the セクション 5.4 table. Tie this pin to V_{IN} if unused.
V_{IN}	1	I	Input supply pin. Use a capacitor with a value of 1 µF or larger from this pin to ground. See セクション 7.1.2 for more information.
V_{OUT}	5	O	Output of the regulator. Use a capacitor with a value of 2.2 µF or larger from this pin to ground(1). See the セクション 7.1.2 section for more information.

(1) The nominal output capacitance must be greater than 1 µF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 1 µF.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage range (for legacy chip)	–0.3	16	V
	Continuous input voltage range(for new chip)	–0.3	18	
V_{OUT}	Output voltage range (for legacy chip)	–0.3	9	
	Output voltage range(for new chip)	–0.3	V_{IN} + 0.3 or 9 (whichever is smaller)	
V_{BYPASS}	BYPASS pin voltage range (for new chip)	–0.3	3	
$V_{ON/\overline{OFF}}$	ON/$\overline{\text{OFF}}$ pin voltage range (for legacy chip)	–0.3	16	
	ON/$\overline{\text{OFF}}$ pin voltage range (for new chip)	–0.3	18	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–55	150	°C
		–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages with respect to GND.

5.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	±1000	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage (for legacy chip)	2.2		16	V
	Supply input voltage (for new chip)	2.5		16	
V_{OUT}	Output voltage (for legacy chip)	1.2		10.0	
	Output voltage (for new chip)	1.2		5.0	
V_{BYPASS}	Bypass voltage		1.2		
$V_{ON/\overline{OFF}}$	Enable voltage (for legacy chip)	0		V_{IN}	
	Enable voltage (for new chip)	0		16	
I_{OUT}	Output current	0		250	mA
C_{IN} (1)	Input capacitor		1		µF
C_{OUT}	Output capacitor (for legacy chip)	2.2	4.7		µF
	Output capacitance (for new chip) (1)	1	2.2	200	
T_J	Operating junction temperature	–40		125	°C

(1) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 1 µF minimum for stability.

5.4 Electrical Characteristics

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	I_L = 1 mA	Legacy chip (standard grade)	–1.5		1.5	%
			Legacy chip (A grade)	–1.0		1.0	
			New chip	–0.5		0.5	
		1 mA ≤ I_L ≤ 50 mA	Legacy chip (standard grade)	–2.5		2.5	
			Legacy chip (A grade)	–1.5		1.5	
			New chip	–0.5		0.5	
		1 mA ≤ I_L ≤ 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip (standard grade)	–3.5		3.5	
			Legacy chip (A grade)	–2.5		2.5	
			New chip	–1		1	
		1 mA ≤ I_L ≤ 250 mA	Legacy chip (standard grade)	–4		4	
			Legacy chip (A grade)	–3.5		3.5	
			New chip	–0.5		0.5	
		1 mA ≤ I_L ≤ 250 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip (standard grade)	–5		5	
			Legacy chip (A grade)	–4.5		4.5	
			New chip	–1		1	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V	Legacy chip		0.007	0.014	%/V
			New chip		0.002	0.014	
		$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip		0.007	0.032	
			New chip		0.002	0.032	
$V_{IN(MIN)}$	Minimum input voltage required to maintain output regulation		Legacy chip		2.05		V
			New chip		2.05		
	Minimum input voltage required to maintain output regulation	–40°C ≤ T_J ≤ 125°C	Legacy chip			2.2	
			New chip			2.35	

5.4 Electrical Characteristics (続き)

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 μF, and C_{OUT} = 2.2 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GND}	GND pin current	I_{OUT} = 0 mA	Legacy chip		65	95	μA
			New chip		69	95	
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			125	
			New chip			123	
		I_{OUT} = 1 mA	Legacy chip		75	110	
			New chip		78	110	
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			170	
			New chip			140	
		I_{OUT} = 50 mA	Legacy chip		350	600	
			New chip		380	440	
		I_{OUT} = 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			1000	
			New chip			650	
		I_{OUT} = 150 mA	Legacy chip		850	1500	
			New chip		765	890	
		I_{OUT} = 150 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			2500	
			New chip			1060	
		I_{OUT} = 250 mA	Legacy Chip		1500	2300	
			New Chip		875	1010	
		I_{OUT} = 250 mA, –40°C ≤ T_J ≤ 125°C	Legacy Chip			4000	
			New Chip			1200	
		$V_{ON/OFF}$ < 0.3 V, V_{IN} = 16 V	Legacy chip		0.01	0.8	
			New chip		1.25	1.75	
		$V_{ON/OFF}$ < 0.15 V, V_{IN} = 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip		0.05	2	
			New chip		1.12	2.75	

5.4 Electrical Characteristics (続き)

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage(1)	I_{OUT} = 0 mA	Legacy chip		0.5	2.5	mV
			New chip		1	2.75	
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			4	
			New chip			3	
		I_{OUT} = 1 mA	Legacy chip		5	9	
			New chip		11.5	14	
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			12	
			New chip			17	
		I_{OUT} = 50 mA	Legacy chip		100	125	
			New chip		120	145	
		I_{OUT} = 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			180	
			New chip			184	
		I_{OUT} = 150 mA	Legacy chip		260	325	
			New chip		180	198	
		I_{OUT} = 150 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			470	
			New chip			254	
		I_{OUT} = 250 mA	Legacy chip		450	575	
			New chip		225	260	
		I_{OUT} = 250 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			850	
			New chip			340	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage	Low = Output OFF	Legacy chip		0.55		V
			New chip		0.72		
		Low = Output OFF, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			0.15	
			New chip			0.15	
		High = Output ON	Legacy chip		1.4		
			New chip		0.85		
		High = Output ON, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip	1.6			
			New chip	1.6			
$I_{ON/\overline{OFF}}$	ON/OFF input current	$V_{ON/OFF}$ = 0 V, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			–2	µA
			New chip			–0.9	
$I_{ON/\overline{OFF}}$	ON/OFF input current	$V_{ON/OFF}$ = 0 V	Legacy chip		0.01		µA
			New chip		0.42		
IO(PK)	Peak output current	V_{OUT} ≥ $V_{O(NOM)}$ –5% (steady state)	Legacy chip	300	350		mA
			New chip	300	350		
$I_{O(SC)}$	Short output current	R_L = 0 Ω (steady state)	Legacy chip		400		
			New chip		375		
$\Delta V_O/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, C_{BYPASS} = 10 nF, C_{OUT} = 10 µF	Legacy chip		45		dB
			New chip		78		
V_n	Output noise voltage	Bandwidth = 300 Hz to 50 kHz, C_{BYPASS} = 10 nF, C_{OUT} = 2.2 µF, V_{OUT} = 3.3 V	Legacy chip		30		µVRMS
			New chip		30		

(1) Dropout voltage (V_{DO}) is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1 V differential. V_{DO} is measured with V_{IN} = $V_{OUT(nom)}$ – 100 mV for fixed output devices.

5.5 Thermal Information

THERMAL METRIC(1)		Legacy Chip (2)	New Chip (2)	UNIT
		DBV (SOT23-5)	DBV (SOT23-5)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.7	178.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122.6	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.9	47.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.7	15.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.4	46.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the *Impact of board layout on LDO thermal performance* application report.

5.6 Typical Characteristics

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{\text{OFF}}$ pin is tied to the IN pin (unless otherwise noted)

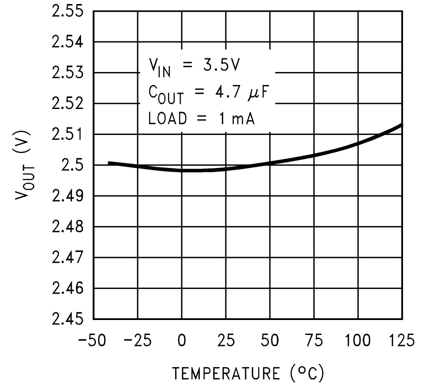
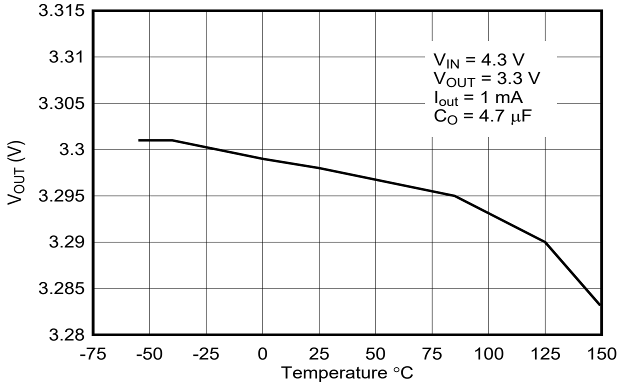


図 5-1. V_{OUT} vs Temperature for Legacy Chip



V_{IN} = 4.3 V, V_{OUT} = 3.3 V (for new chip)

図 5-2. V_{OUT} vs Temperature for New Chip

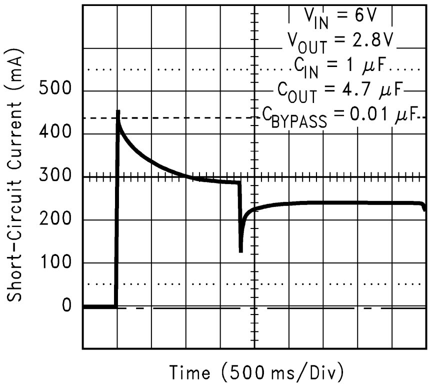
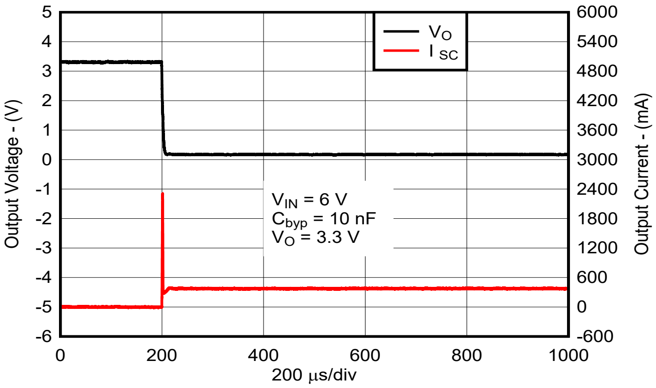


図 5-3. Short-Circuit Current for Legacy Chip



V_{IN} = 6 V

図 5-4. Short-Circuit Current vs Time for New Chip

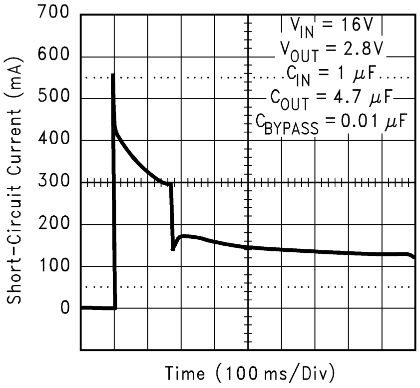
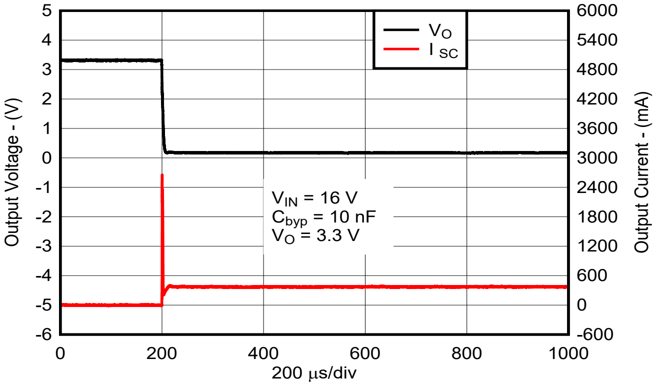


図 5-5. Short-Circuit Current for Legacy Chip



V_{IN} = 16 V

図 5-6. Short-Circuit Current vs Time for New Chip

5.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin (unless otherwise noted)

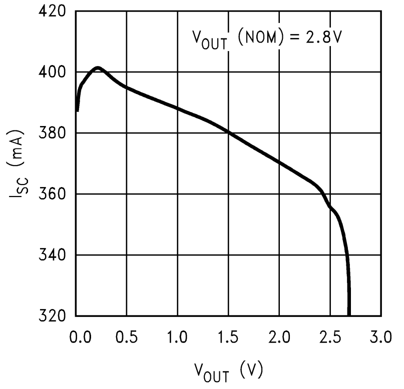
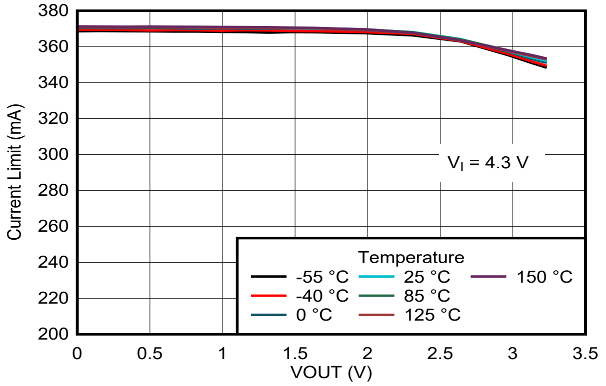


図 5-7. Short-Circuit Current vs Output Voltage for Legacy Chip



V_{OUT} = 3.3 (for new chip)

図 5-8. Short-Circuit Current vs Output Voltage for New Chip

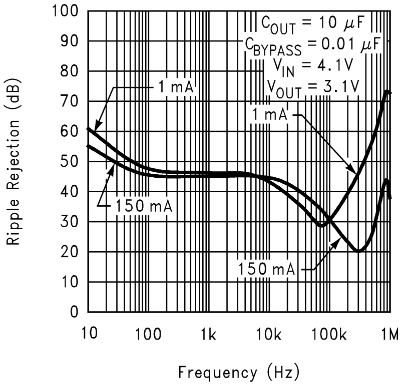


図 5-9. Ripple Rejection vs Frequency for Legacy Chip

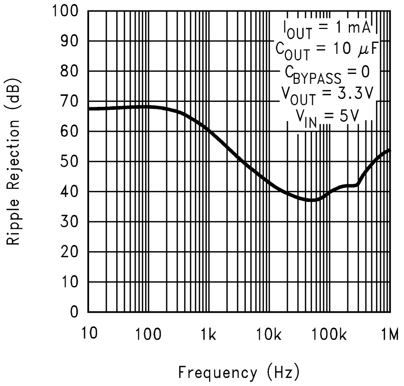


図 5-10. Ripple Rejection vs Frequency for Legacy Chip

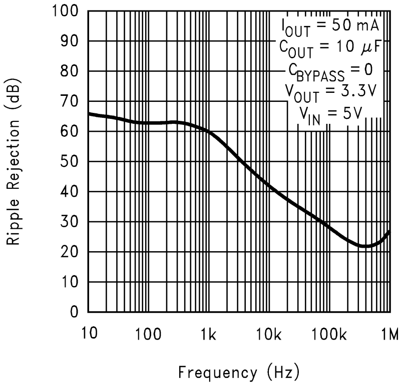


図 5-11. Ripple Rejection vs Frequency for Legacy Chip

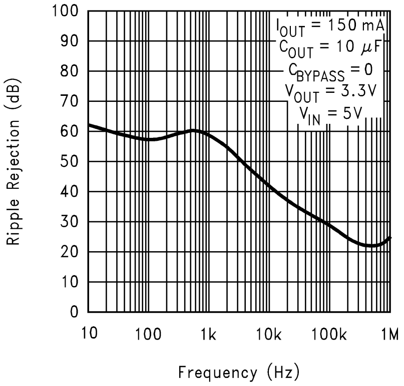
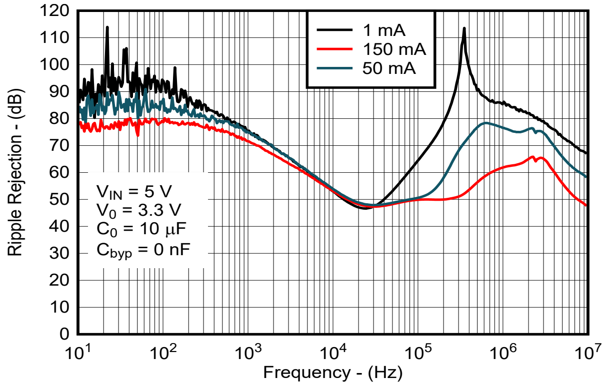


図 5-12. Ripple Rejection vs Frequency for Legacy Chip

5.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{\text{OFF}}$ pin is tied to the IN pin (unless otherwise noted)



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF, C_{BYP} = 0 nF

図 5-13. Ripple Rejection vs Frequency for New Chip

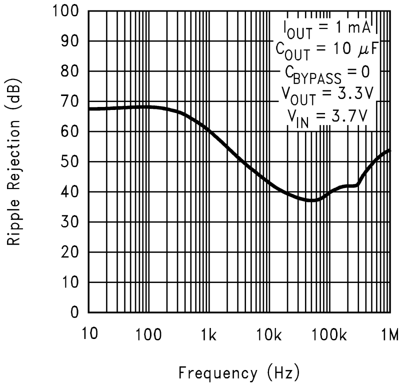


図 5-14. Ripple Rejection vs Frequency for Legacy Chip

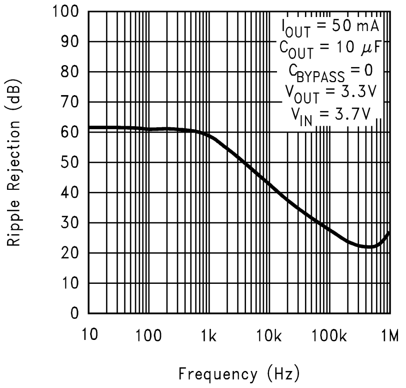


図 5-15. Ripple Rejection vs Frequency for Legacy Chip

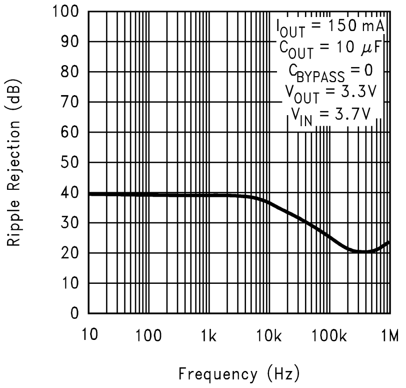
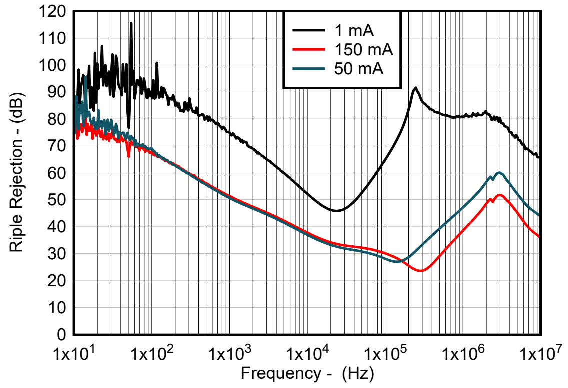


図 5-16. Ripple Rejection vs Frequency for Legacy Chip



V_{IN} = 3.7 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF, C_{BYP} = 0 nF

図 5-17. Ripple Rejection vs Frequency for New Chip

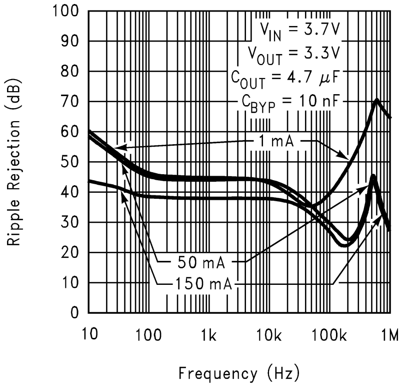


図 5-18. Ripple Rejection vs Frequency for Legacy Chip

5.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{\text{OFF}}$ pin is tied to the IN pin (unless otherwise noted)

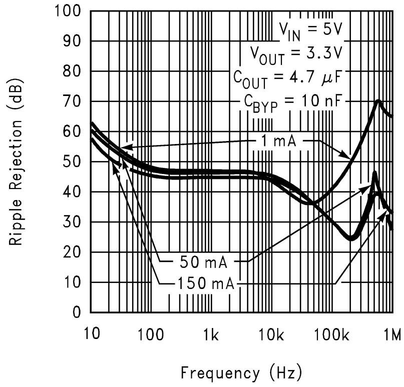
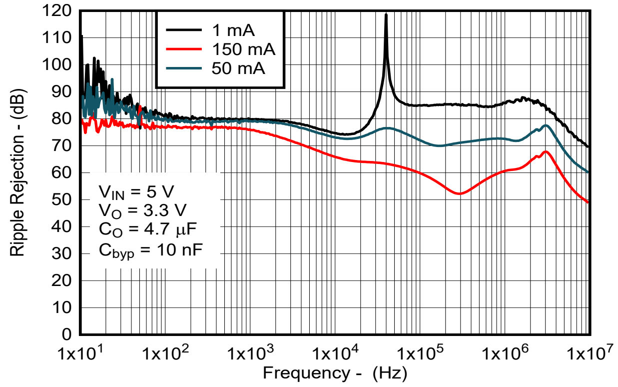


図 5-19. Ripple Rejection vs Frequency for Legacy Chip



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF, C_{BYP} = 10 nF

図 5-20. Ripple Rejection vs Frequency for New Chip

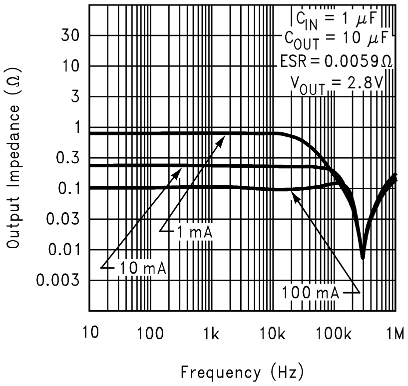


図 5-21. Output Impedance vs Frequency for Legacy Chip

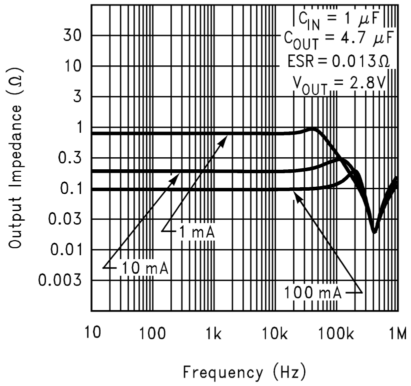


図 5-22. Output Impedance vs Frequency for Legacy Chip

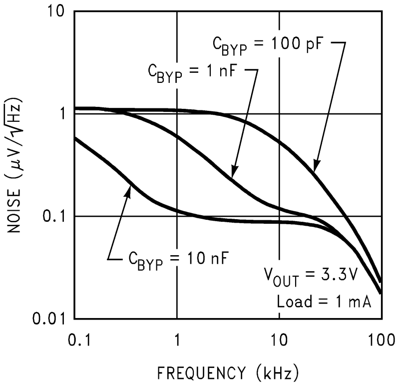


図 5-23. Output Noise Density for Legacy Chip

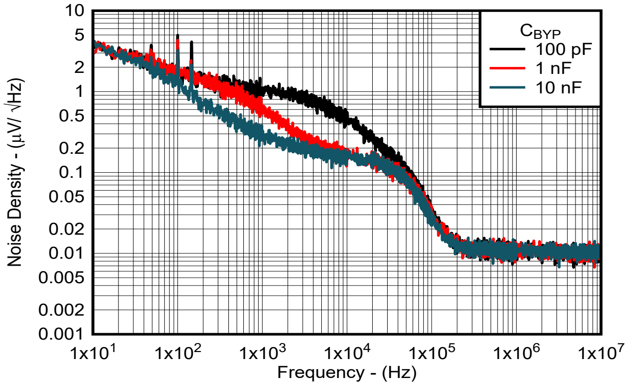


図 5-24. Output Noise Density vs Frequency for New Chip

5.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, $V_{IN} = V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin (unless otherwise noted)

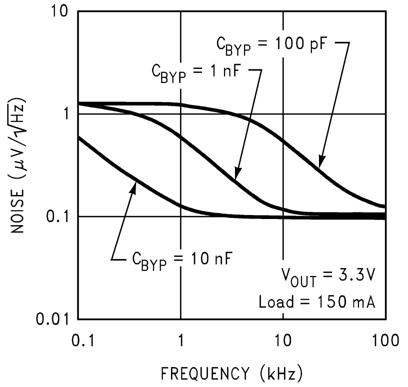
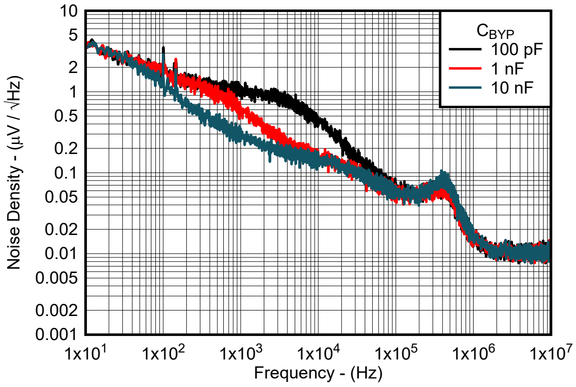


図 5-25. Output Noise Density for Legacy Chip



V_{OUT} = 3.3 V, I_{OUT} = 150 mA

図 5-26. Output Noise Density vs Frequency for New Chip

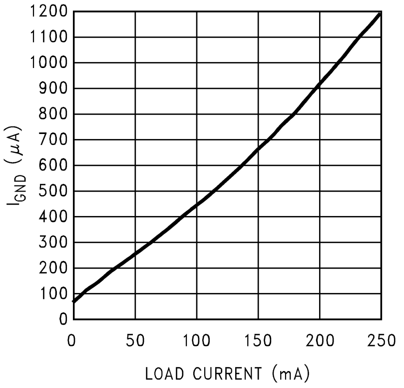


図 5-27. GND Pin vs Load Current for Legacy Chip

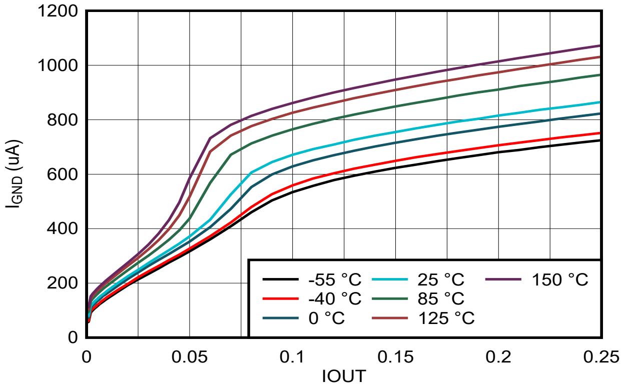


図 5-28. GND Pin vs Load Current for New Chip

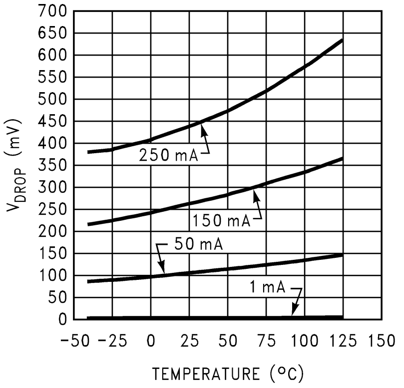


図 5-29. Dropout Voltage vs Temperature for Legacy Chip

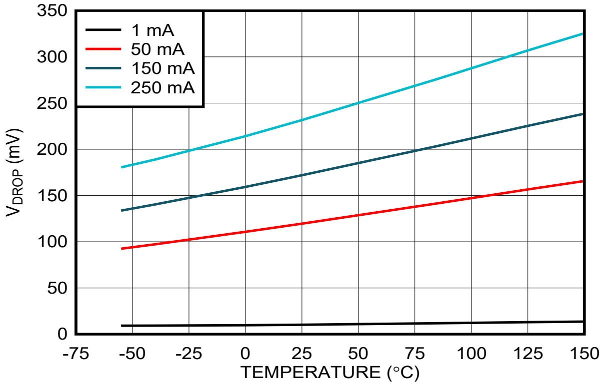


図 5-30. Dropout Voltage vs Temperature for New Chip

5.6 Typical Characteristics (continued)

C_{IN} = 1 μF, C_{OUT} = 4.7 μF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin (unless otherwise noted)

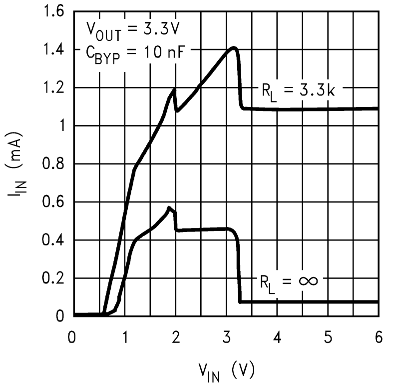


図 5-31. Input Current vs Input Voltage for Legacy Chip

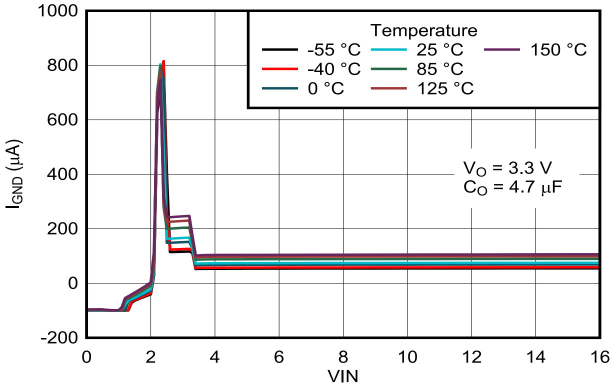


図 5-32. Input Current vs Input Voltage for New Chip

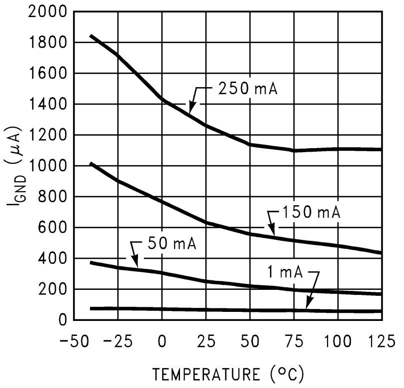


図 5-33. I_{GND} vs Load and Temperature for Legacy Chip

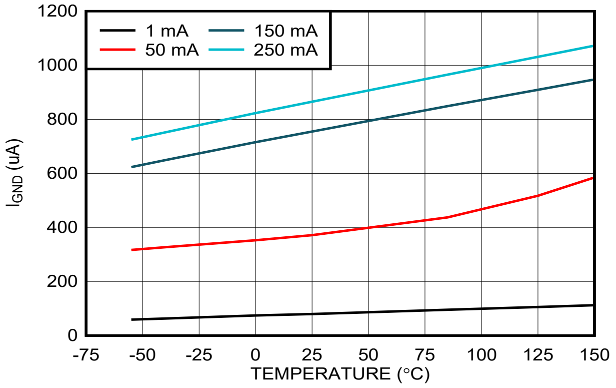


図 5-34. I_{GND} vs Load and Temperature for New Chip

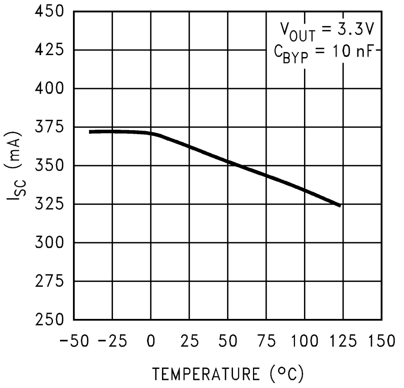


図 5-35. Short-Circuit Current vs Temperature for Legacy Chip

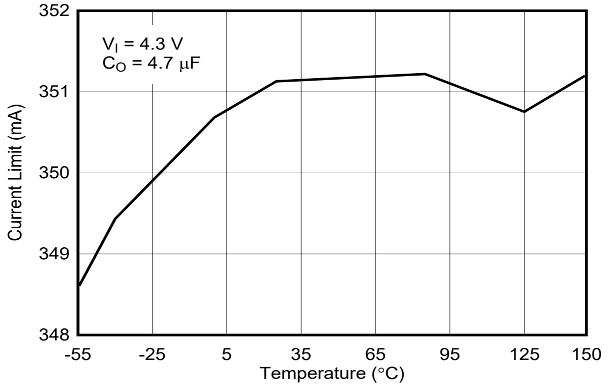


図 5-36. Short-Circuit Current vs Temperature for New Chip

5.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, $V_{IN} = V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{\text{OFF}}$ pin is tied to the IN pin (unless otherwise noted)

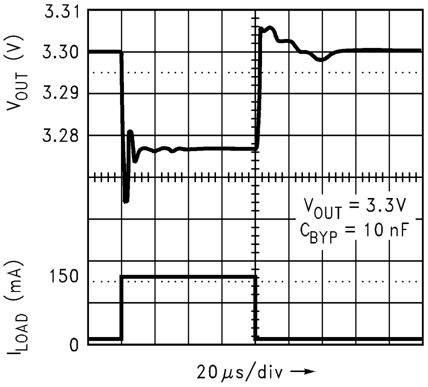
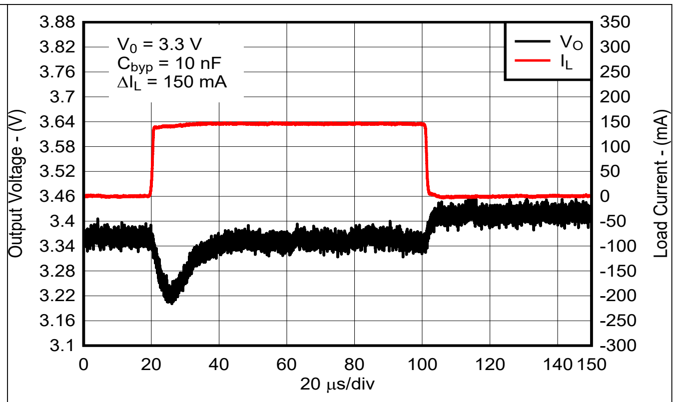


図 5-37. Load Transient Response for Legacy Chip



dI/dt = 1 A/µ

図 5-38. Load Transient for New Chip

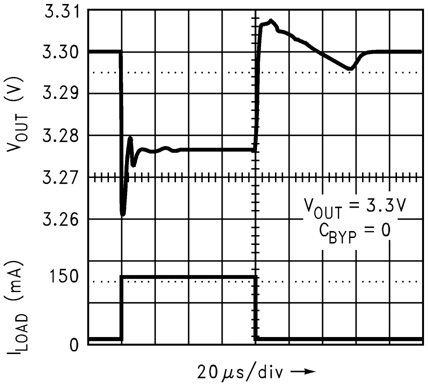
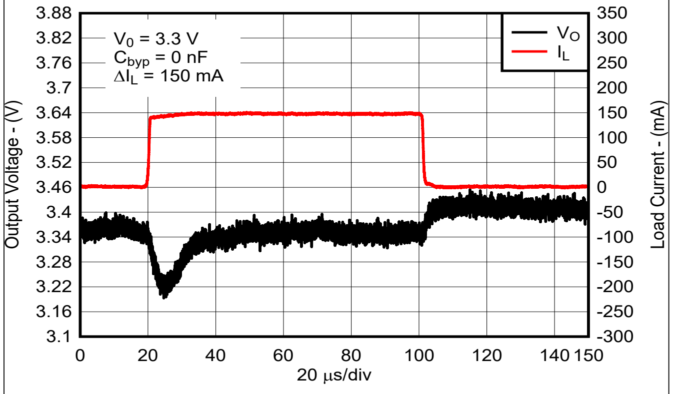


図 5-39. Load Transient Response for Legacy Chip



dI/dt = 1 A/µ

図 5-40. Load Transient Response for New Chip

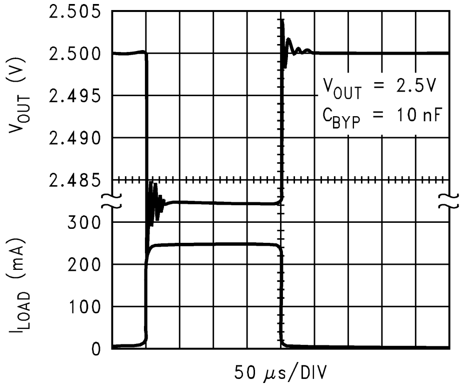
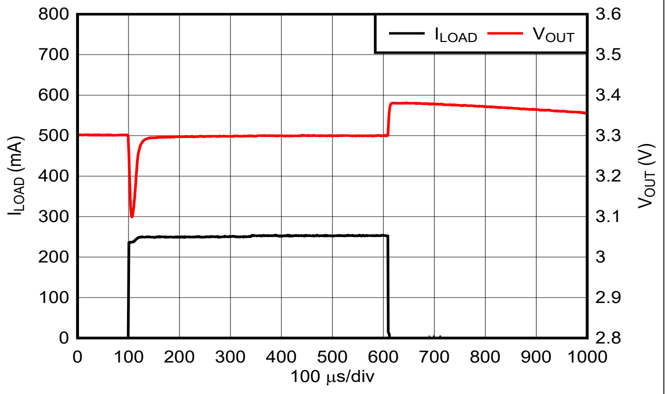


図 5-41. Load Transient Response for Legacy Chip



V_{OUT} = 3.3 V,
dI/dt = 1 A/µs

図 5-42. Load Transient Response for New Chip

5.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin (unless otherwise noted)

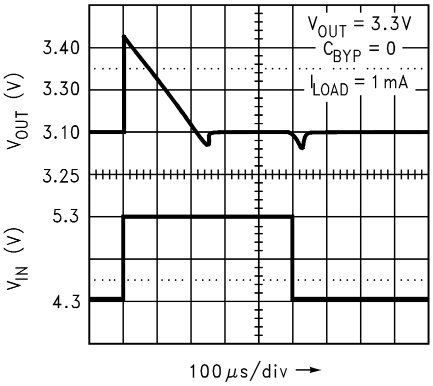
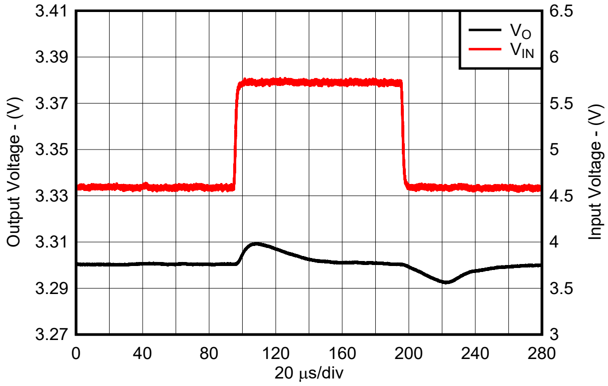


図 5-43. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 0 nF, ΔV_{IN} = 1 V, I_{OUT} = 1 mA, dV/dt = 1 V/µ

図 5-44. Line Transient Response for New Chip

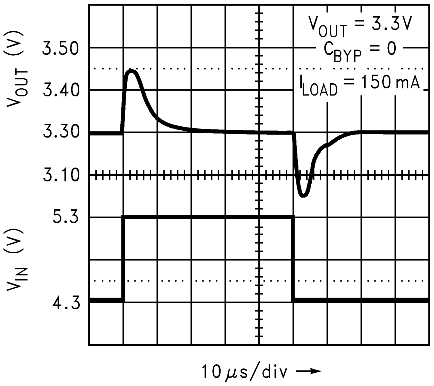
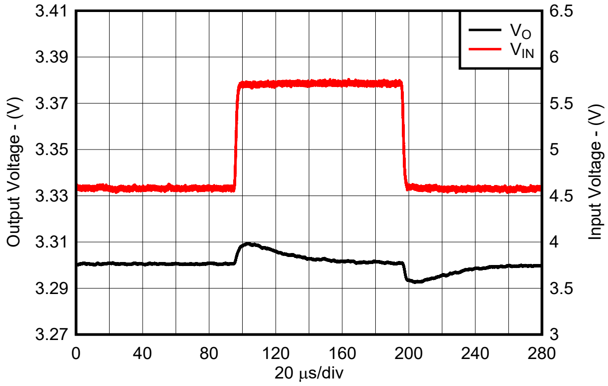


図 5-45. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 0 nF, ΔV_{IN} = 1 V, I_{OUT} = 150 mA, dV/dt = 1 V/µ

図 5-46. Line Transient Response for New Chip

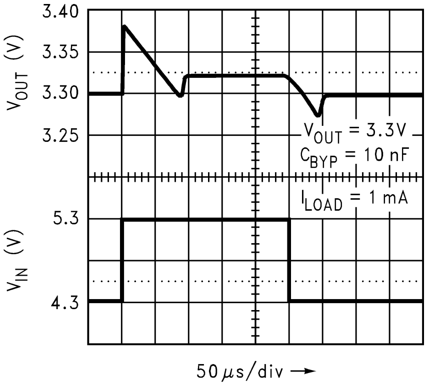
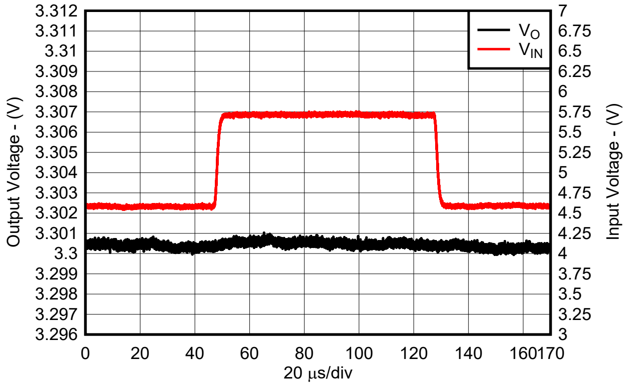


図 5-47. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 10 nF, ΔV_{IN} = 1 V, I_{OUT} = 1 mA, dV/dt = 1 V/µ

図 5-48. Line Transient Response for New Chip

5.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, $V_{IN} = V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{\text{OFF}}$ pin is tied to the IN pin (unless otherwise noted)

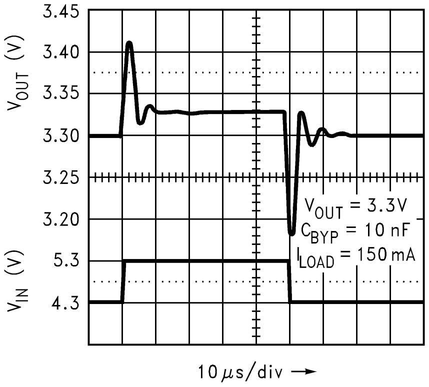
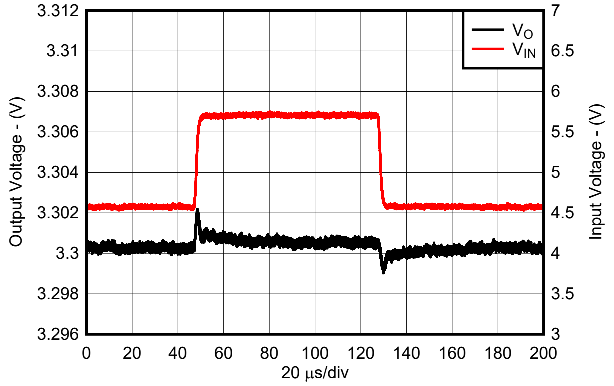


図 5-49. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 10 nF, ΔV_{IN} = 1 V, I_{OUT} = 150 mA, dV/dt = 1 V/µ

図 5-50. Line Transient Response for New Chip

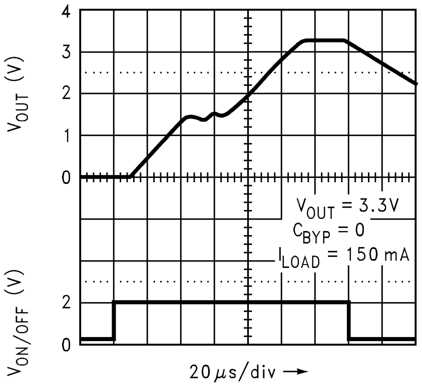


図 5-51. Turn-on Time for Legacy Chip

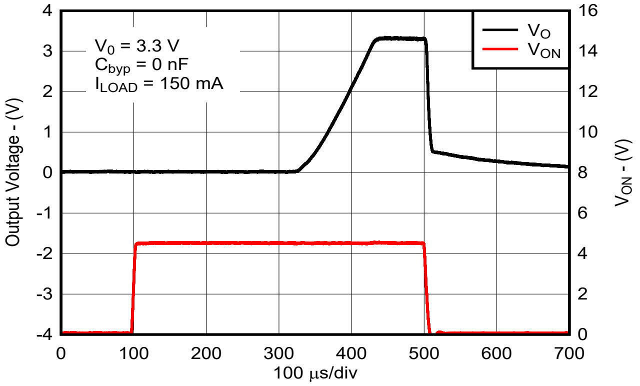


図 5-52. Turn-on Time for New Chip

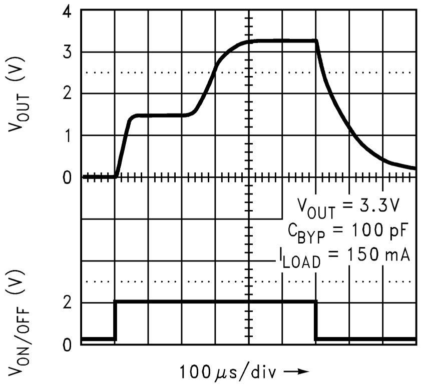


図 5-53. Turn-on Time for Legacy Chip

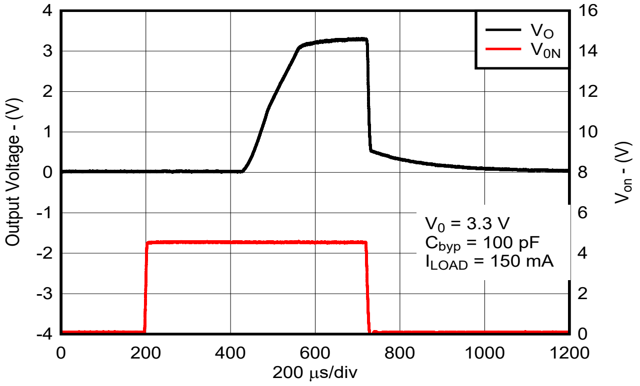


図 5-54. Turn-on Time for New Chip

5.6 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin (unless otherwise noted)

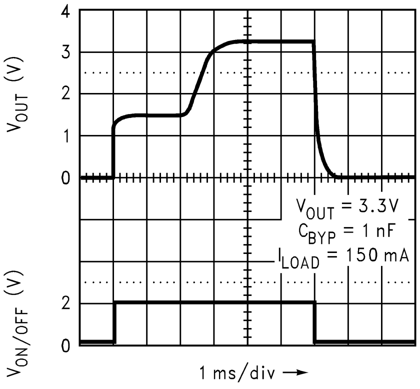


図 5-55. Turn-on Time for Legacy Chip

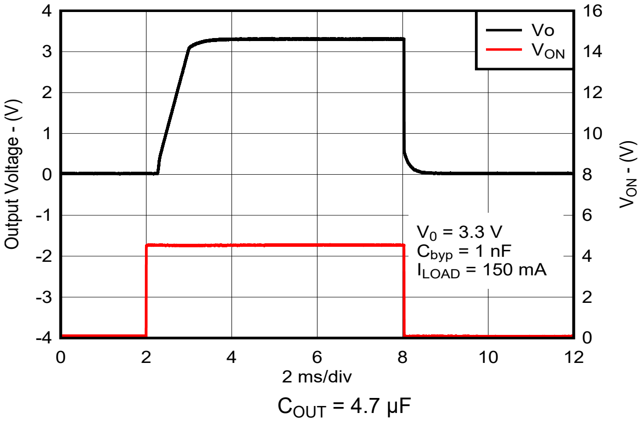


図 5-56. Turn-on Time for New Chip

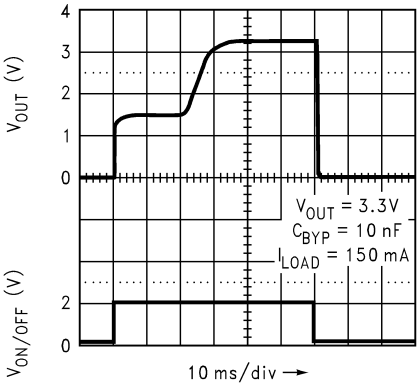


図 5-57. Turn-on Time for Legacy Chip

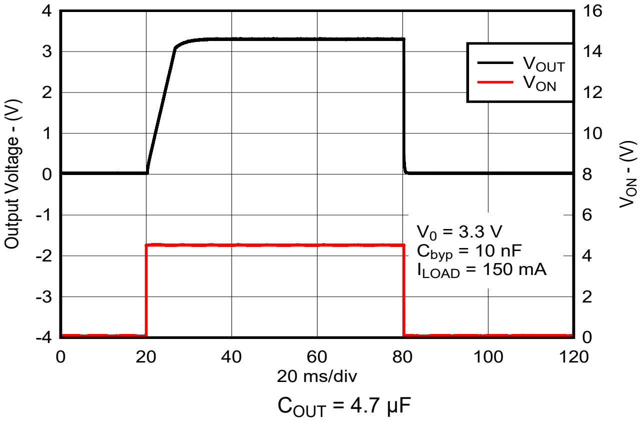


図 5-58. Turn-on Time for New Chip

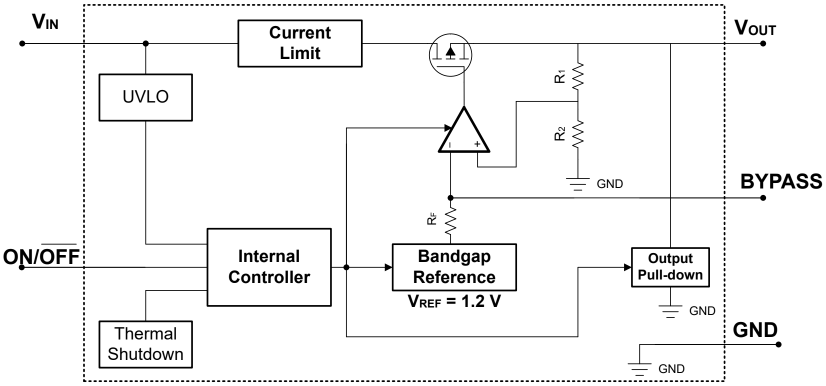
6 Detailed Description

6.1 Overview

The LP2991 is a fixed-output, low-noise, high PSRR, low-dropout regulator that offers exceptional, cost-effective performance for both portable and nonportable applications. The LP2991 has an output tolerance of 1% across line, load, and temperature variation (for the new chip) and is capable of delivering 250 mA of continuous load current.

This device features integrated overcurrent protection, thermal shutdown, output enable, and internal output pulldown and has a built-in soft-start mechanism for controlled inrush current. This device delivers excellent line and load transient performance. The operating ambient temperature range of the device is –40°C to 125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Output Enable

The ON/$\overline{\text{OFF}}$ pin for the device is an active-high pin. The output voltage is enabled when the voltage of the ON/$\overline{\text{OFF}}$ pin is greater than the high-level input voltage of the ON/$\overline{\text{OFF}}$ pin and disabled with the ON/$\overline{\text{OFF}}$ pin voltage is less than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin. If independent control of the output voltage is not needed, connect the ON/$\overline{\text{OFF}}$ pin to the input of the device.

The device has an internal pulldown circuit that activates when the device is disabled by pulling the ON/$\overline{\text{OFF}}$ pin voltage lower than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin, to actively discharge the output voltage.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *セクション 5.3* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *セクション 5.4* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) × I_{CL}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

図 6-1 shows a diagram of the current limit.

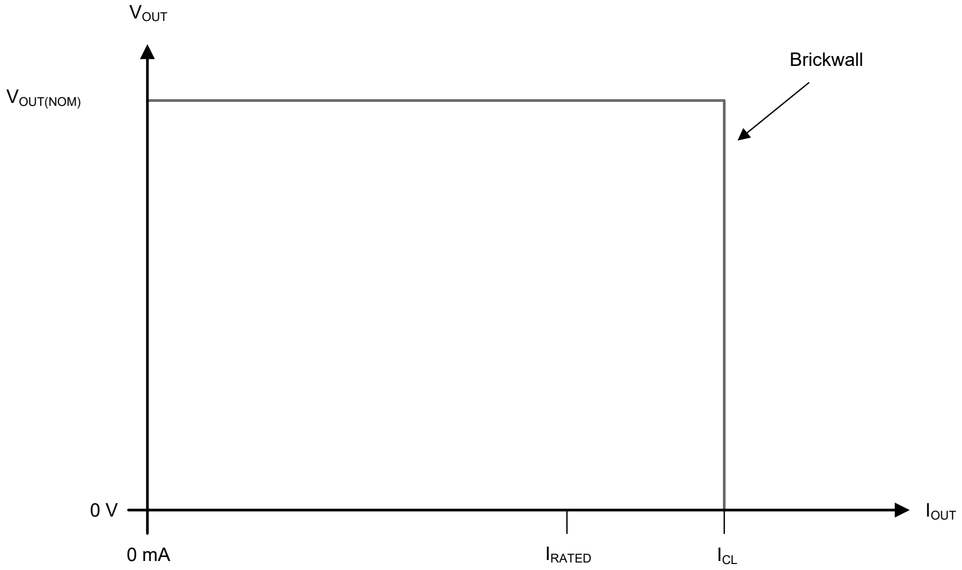


図 6-1. Current Limit

6.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *セクション 5.4* table.

6.3.5 Output Pulldown

The new chip has an output pulldown circuit. The output pulldown activates in the following conditions:

- When the device is disabled ($V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$)
- If 1.0 V < $V_{IN} < V_{UVLO}$

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *セクション 7.1.6* section for more details.

6.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis resets (turns on) the device when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large $V_{IN} - V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the セクション 5.3 table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

表 6-1 shows the conditions that lead to the different modes of operation. See セクション 5.4 for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$V_{ON/\overline{OFF}}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The ON/$\overline{\text{OFF}}$ voltage has previously exceeded the ON/$\overline{\text{OFF}}$ rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the ON/$\overline{\text{OFF}}$ pin to less than the maximum ON/$\overline{\text{OFF}}$ pin low-level input voltage (see the *セクション 5.4* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. セクション 5.5 lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{2}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \tag{3}$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *セクション 5.3* table for stability.

7.1.3 Noise Bypass Capacitor (C_{BYPASS})

The LP2992 allows for low-noise performance with the use of a bypass capacitor that is connected to the internal band-gap reference with the BYPASS pin. This high-impedance band-gap circuitry is biased in the microampere range and, thus, cannot be loaded significantly, otherwise, the output (and, correspondingly, the output of the regulator) changes. Thus, for best output accuracy, dc leakage current through C_{BYPASS} must be minimized as much as possible and must never exceed 100 nA. The C_{BYPASS} capacitor also impacts the start-up behavior of the regulator. Inrush current and start-up time increase with larger bypass capacitor values.

Use a 10-nF capacitor for C_{BYPASS}. Ceramic and film capacitors are good choices for this purpose.

7.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \tag{4}$$

注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{θJA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{θJA} \times P_D) \tag{5}$$

Thermal resistance ($R_{θJA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in セクション 5.5 table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.1.5 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in セクション 5.3 account for an effective capacitance of approximately 50% of the nominal value.

7.1.6 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \le V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

図 7-1 shows one approach for protecting the device.

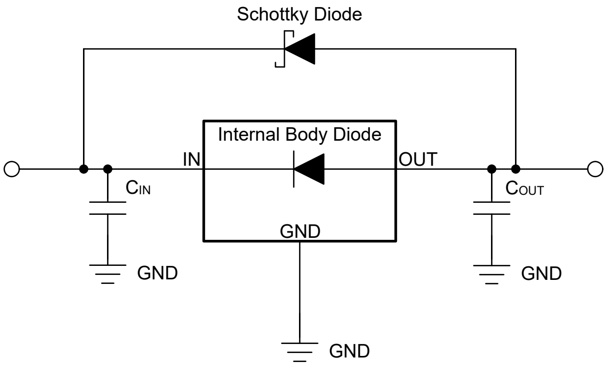


図 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2 Typical Application

図 7-2 shows the standard usage of the LP2992 as a low-dropout regulator.

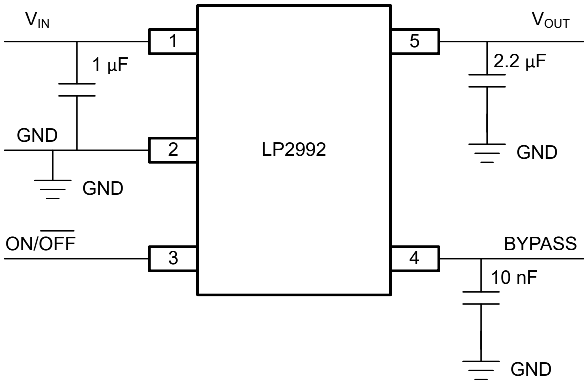


図 7-2. LP2992 Typical Application

7.2.1 Design Requirements

Minimum C_{OUT} value for stability (can be increased without limit for improved stability and transient response)

ON/$\overline{OFF}$ must be actively terminated. Connect to V_{IN} if shutdown feature is not used.

Optional BYPASS capacitor for low-noise operation.

7.2.2 Detailed Design Procedure

7.2.2.1 ON/$\overline{OFF}$ Operation

The LP2992 allows for a shutdown mode using the ON/$\overline{OFF}$ pin. Driving the pin LOW (≤ 0.4 V) turns the device OFF; conversely, a HIGH (≥ 1.2 V) turns the device ON. If the shutdown feature is not used, connect ON/$\overline{OFF}$ to the input so that the regulator is on at all times. For proper operation, do not leave ON/$\overline{OFF}$ unconnected.

7.2.3 Application Curves

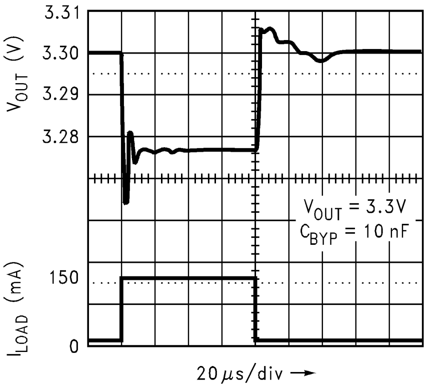
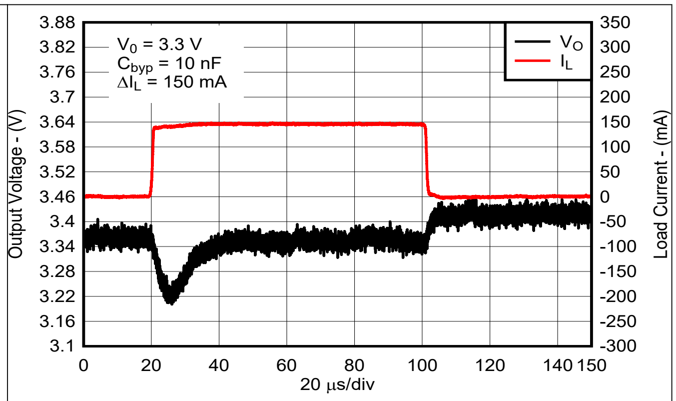


図 7-3. Load Transient Response for Legacy Chip



dI/dt = 1 A/µ

図 7-4. Load Transient for New Chip

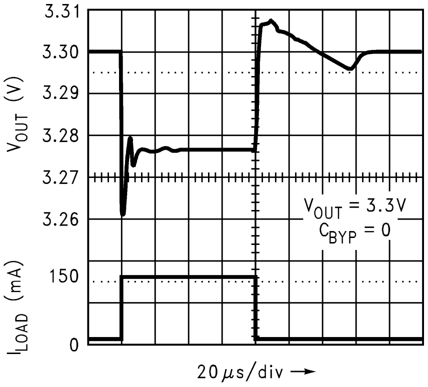
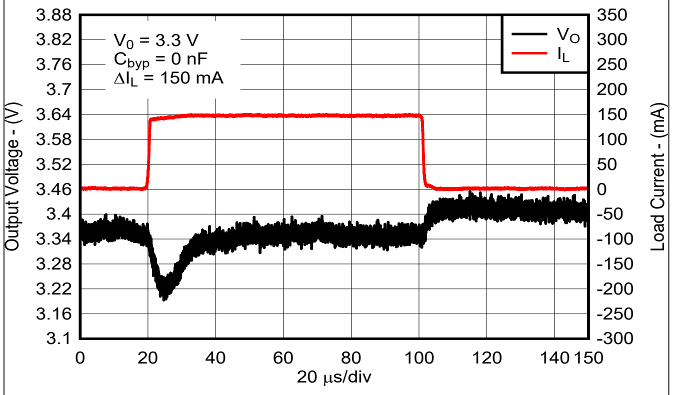


図 7-5. Load Transient Response for Legacy Chip



dI/dt = 1 A/µ

図 7-6. Load Transient Response for New Chip

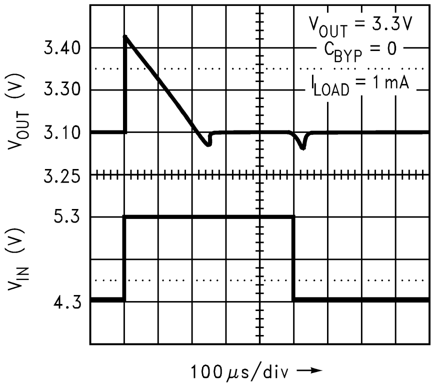
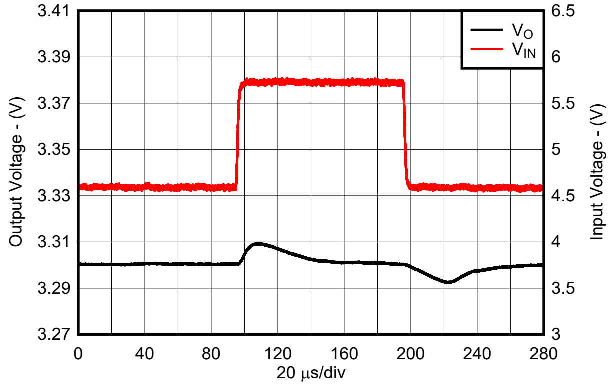


図 7-7. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 0 nF, ΔV_{IN} = 1 V, I_{OUT} = 1 mA,
dV/dt = 1 V/µ

図 7-8. Line Transient Response for New Chip

7.2.3 Application Curves (continued)

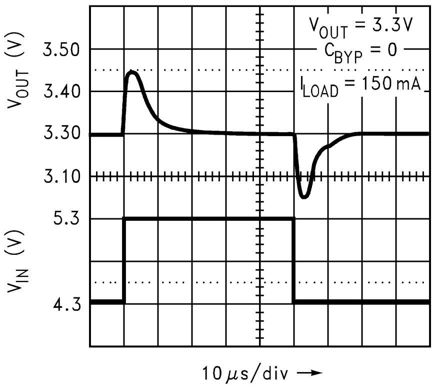
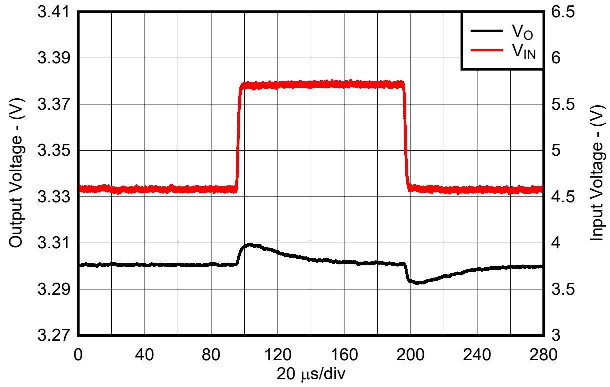


図 7-9. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 0 nF, ΔV_{IN} = 1 V, I_{OUT} = 150 mA, dV/dt = 1 V/µ

図 7-10. Line Transient Response for New Chip

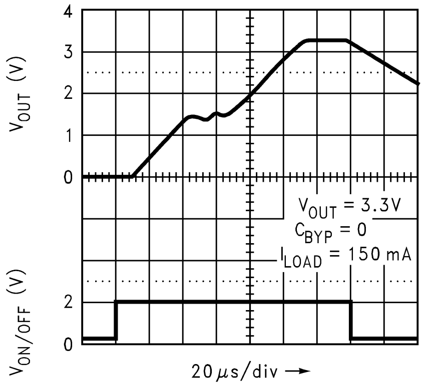


図 7-11. Turn-on Time for Legacy Chip

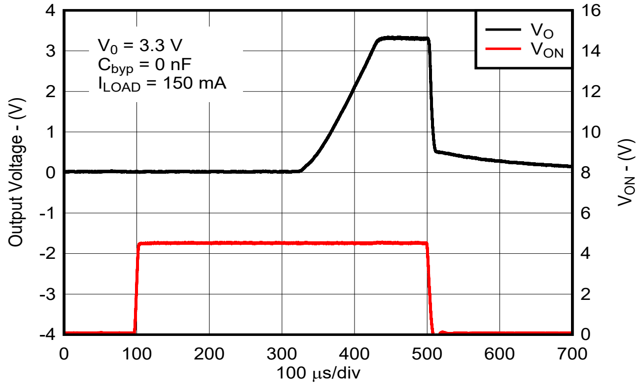


図 7-12. Turn-on Time for New Chip

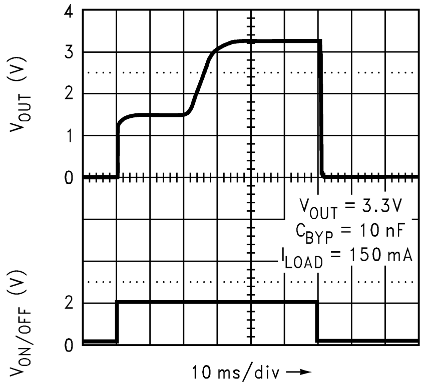
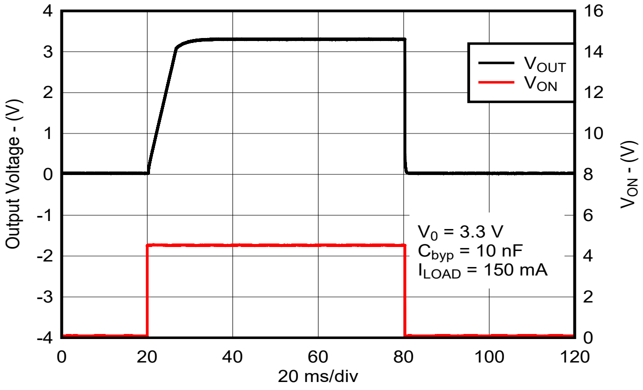


図 7-13. Turn-on Time for Legacy Chip



C_{OUT} = 4.7 µF

図 7-14. Turn-on Time for New Chip

8 Power Supply Recommendations

A power supply can be used at the input voltage within the ranges given in the *Recommended Operating Conditions* table. Use bypass capacitors as described in the *セクション 9.1* section.

9 Layout

9.1 Layout Guidelines

- Bypass the input pin to ground with a bypass capacitor.
- The optimum placement of the bypass capacitor is closest to the V_{IN} of the device and GND of the system. Care must be taken to minimize the loop area formed by the bypass capacitor connection, the V_{IN} pin, and the GND pin of the system.
- For operation at full-rated load, use wide trace lengths to eliminate IR drop and heat dissipation.

9.2 Layout Examples

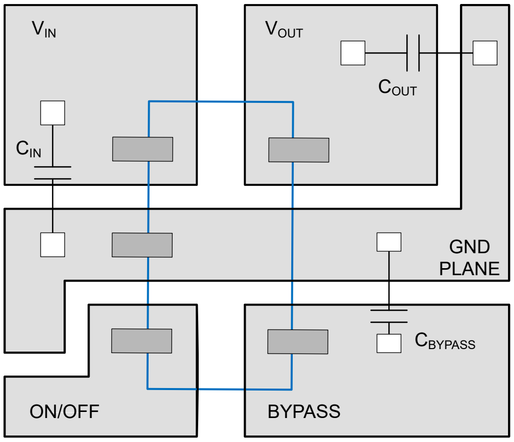


図 9-1. Layout Diagram

10 Device and Documentation Support

10.1 Device Nomenclature

表 10-1. Available Options

PRODUCT(1)	V_{OUT}
LP2992-**xxyyyz** Legacy chip	**xx** is the nominal output voltage (for example, 33 = 3.3 V; 50 = 5.0 V). **yyy** is the package designator. **z** is the package quantity. R is for large quantity reel, T is for small quantity reel.
LP2992-**xxyyyz*M3*** New chip	**xx** is the nominal output voltage (for example, 33 = 3.3 V; 50 = 5.0 V). **yyy** is the package designator. **z** is the package quantity. R is for large quantity reel, T is for small quantity reel. **M3** is a suffix designator for newer chip redesigns, fabricated on the latest TI process technology.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *AN-1187 Leadless Leadframe Package (LLP)*, application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics*, application note
- Texas Instruments, *Using New Thermal Metrics*, application note
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*, application note

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 サポート・リソース

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リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

10.5 Trademarks

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10.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.7 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision J (January 2017) to Revision K (December 2023) — Page

- 文書全体にわたって表、図、相互参照の採番方法を更新 1
- 現在のファミリのフォーマットに合わせてドキュメント全体を変更 1
- ドキュメントに M3 デバイスを追加 1
- 文書全体にわたって表、図、相互参照の採番方法を更新 1
- Updated Absolute Maximum Ratings, Recommended Operating Conditions, Electrical Characteristics and Thermal Information for M3-suffix(new chip) 5
- Added *Device Nomenclature* section 29

Changes from Revision I (November 2015) to Revision J (January 2017) — Page

- 「概略回路」図のコンデンサから具体的な値を削除 1
- Added *Receiving Notification of Documentation Updates* 29

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2992AILD-1.5/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L011A	Samples
LP2992AILD-1.8/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L012A	Samples
LP2992AILD-3.3/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L014A	Samples
LP2992AILD-5.0/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L015A	Samples
LP2992AILDX-3.3/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L014A	Samples
LP2992AILDX-5.0/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L015A	Samples
LP2992AIM5-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFBA	Samples
LP2992AIM5-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFCA	Samples
LP2992AIM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFDA	Samples
LP2992AIM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LFEA	Samples
LP2992AIM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFFA	Samples
LP2992AIM5X-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFBA	Samples
LP2992AIM5X-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFCA	Samples
LP2992AIM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFDA	Samples
LP2992AIM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LFEA	Samples
LP2992AIM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFFA	Samples
LP2992ILD-1.8/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L012A B	Samples
LP2992ILD-2.5/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L013A B	Samples
LP2992ILD-3.3/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L014A B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2992ILD-5.0/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L015A B	Samples
LP2992ILDX-1.5/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L011A B	Samples
LP2992ILDX-3.3/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L014A B	Samples
LP2992ILDX-5.0/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L015A B	Samples
LP2992IM5-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFBB	Samples
LP2992IM5-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFCB	Samples
LP2992IM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFDB	Samples
LP2992IM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LF8B	Samples
LP2992IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LFEB	Samples
LP2992IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFFB	Samples
LP2992IM5X-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFBB	Samples
LP2992IM5X-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFCB	Samples
LP2992IM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFDB	Samples
LP2992IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LFEB	Samples
LP2992IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFFB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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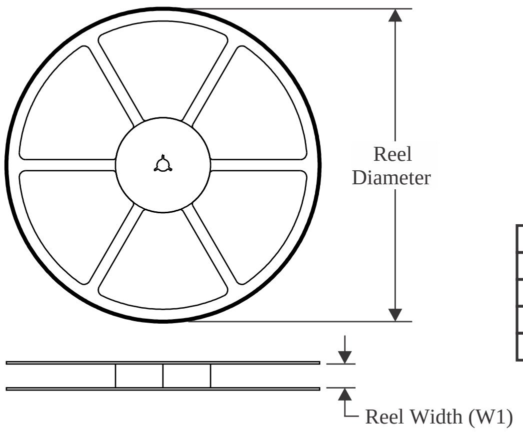
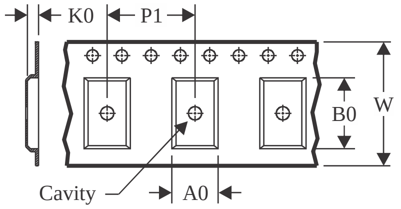
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

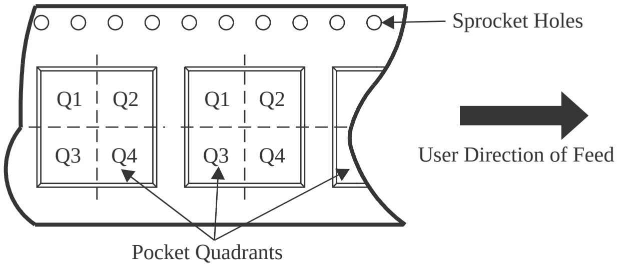


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

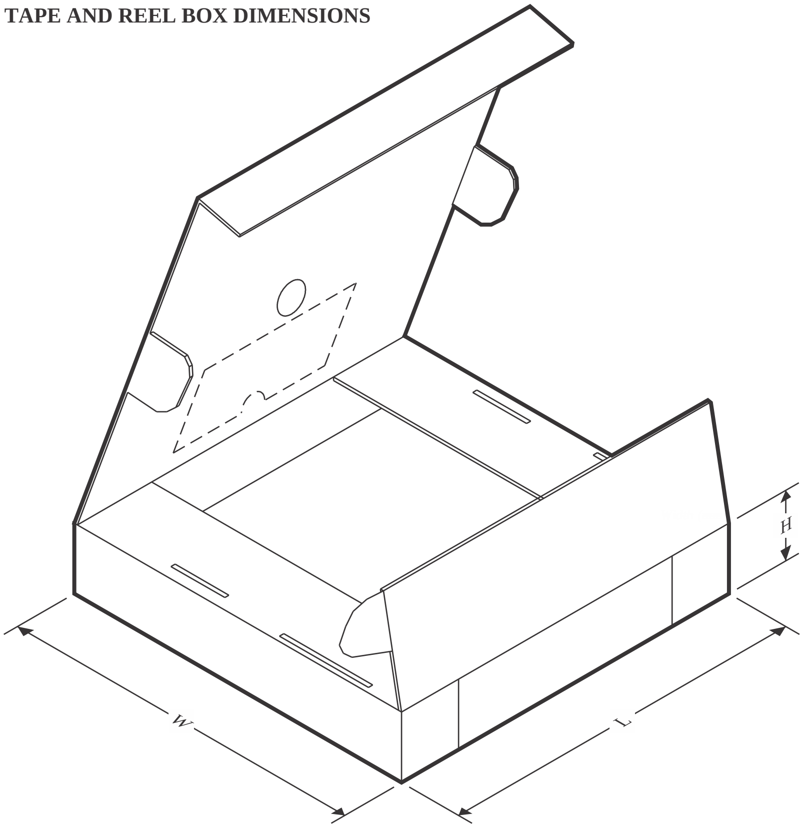


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2992AILD-1.5/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-1.8/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-3.3/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-5.0/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILDX-3.3/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILDX-5.0/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AIM5-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-1.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-2.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2992ILD-1.8/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-2.5/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-3.3/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-5.0/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILDX-1.5/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILDX-3.3/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILDX-5.0/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992IM5-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-1.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-1.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

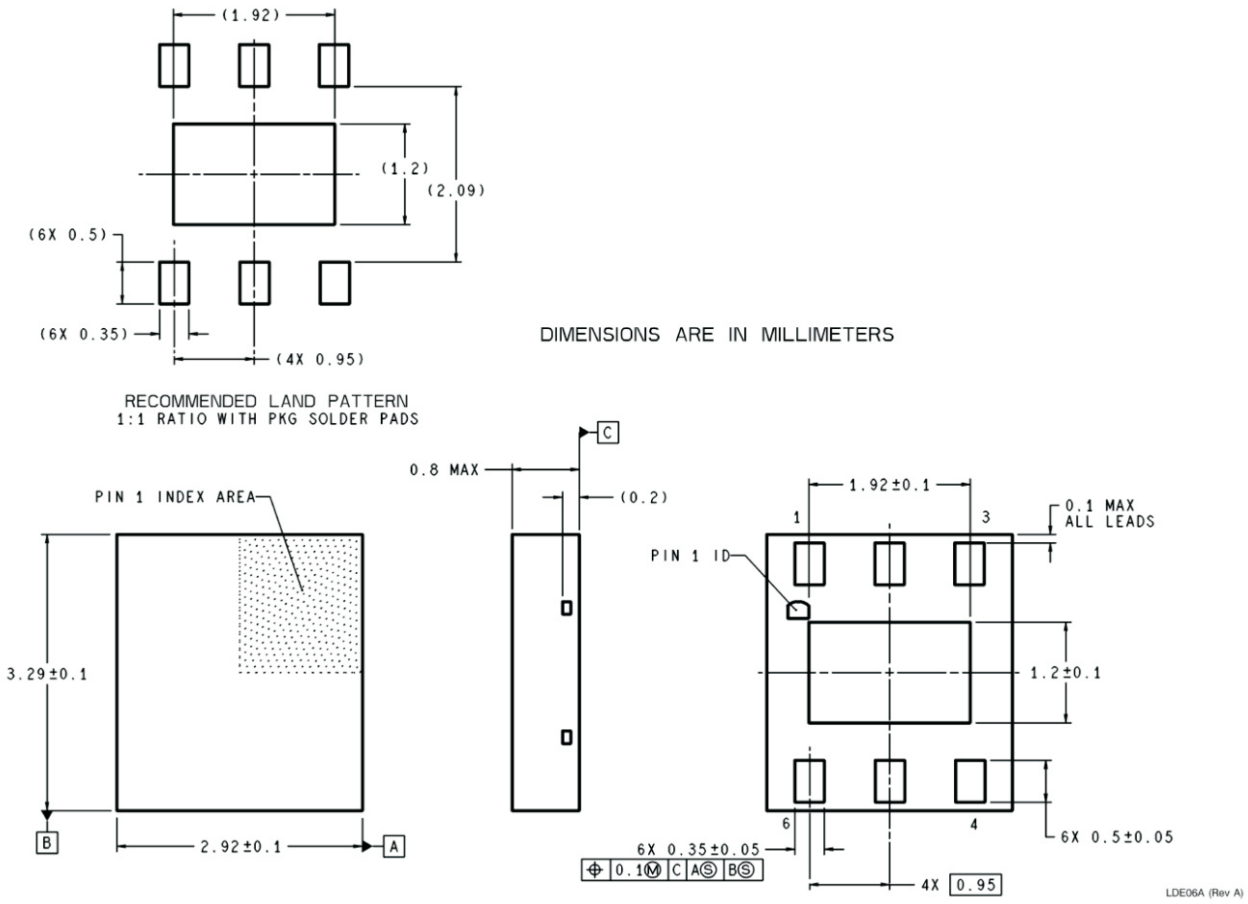
TAPE AND REEL BOX DIMENSIONS

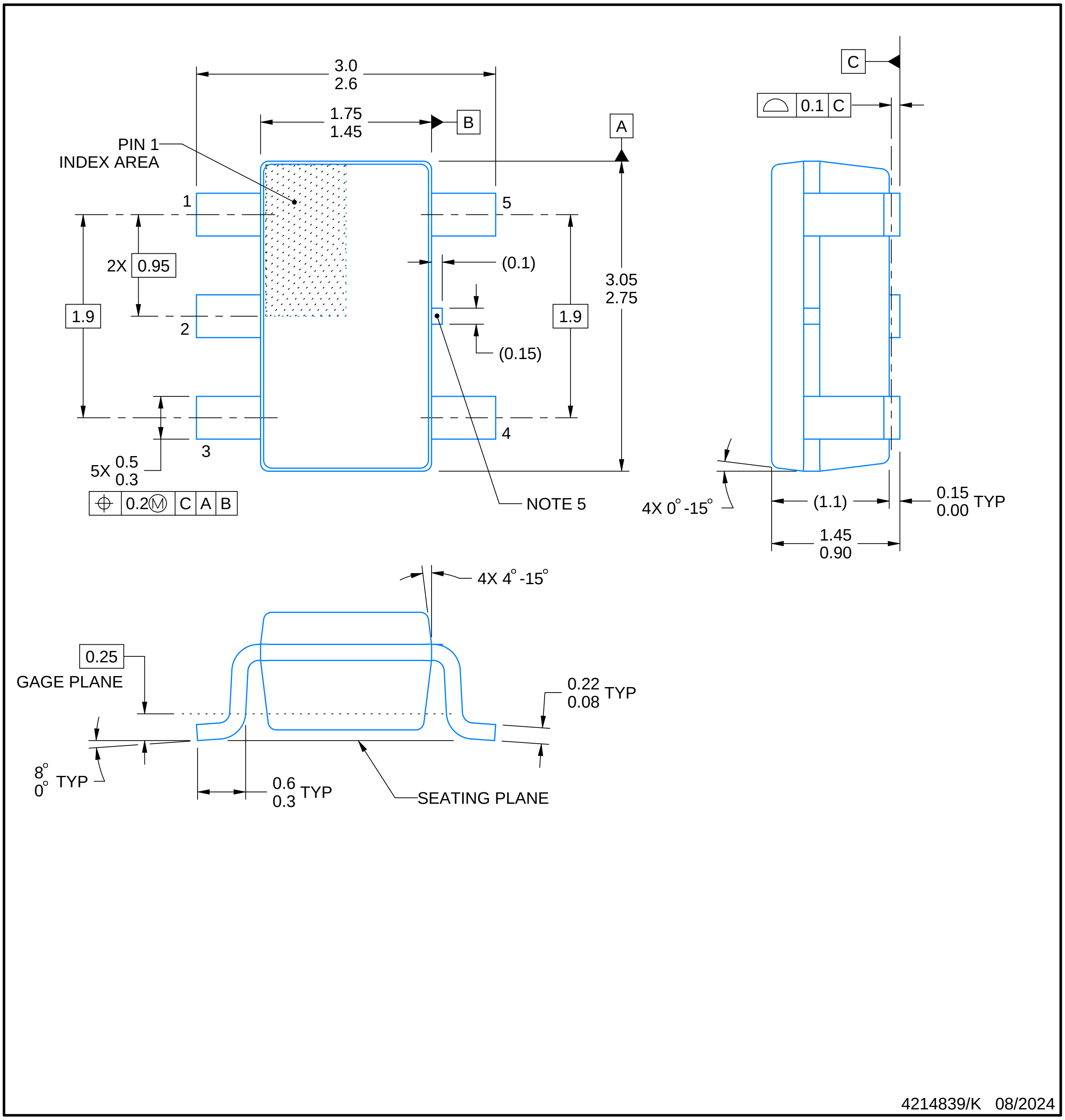


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2992AILD-1.5/NOPB	WSON	NGD	6	1000	208.0	191.0	35.0
LP2992AILD-1.8/NOPB	WSON	NGD	6	1000	208.0	191.0	35.0
LP2992AILD-3.3/NOPB	WSON	NGD	6	1000	208.0	191.0	35.0
LP2992AILD-5.0/NOPB	WSON	NGD	6	1000	213.0	191.0	35.0
LP2992AILDX-3.3/NOPB	WSON	NGD	6	4500	356.0	356.0	36.0
LP2992AILDX-5.0/NOPB	WSON	NGD	6	4500	356.0	356.0	36.0
LP2992AIM5-1.5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2992AIM5-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5X-1.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2992AIM5X-1.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2992AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2992AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992ILD-1.8/NOPB	WSON	NGD	6	1000	208.0	191.0	35.0
LP2992ILD-2.5/NOPB	WSON	NGD	6	1000	208.0	191.0	35.0

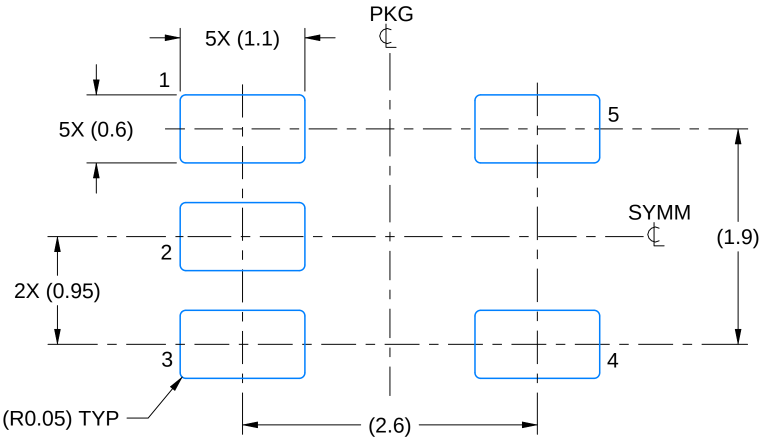
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2992ILD-3.3/NOPB	WSON	NGD	6	1000	208.0	191.0	35.0
LP2992ILD-5.0/NOPB	WSON	NGD	6	1000	213.0	191.0	35.0
LP2992ILDX-1.5/NOPB	WSON	NGD	6	4500	367.0	367.0	38.0
LP2992ILDX-3.3/NOPB	WSON	NGD	6	4500	356.0	356.0	36.0
LP2992ILDX-5.0/NOPB	WSON	NGD	6	4500	356.0	356.0	36.0
LP2992IM5-1.5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2992IM5-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5-2.5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2992IM5-3.0/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2992IM5-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-1.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2992IM5X-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-2.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2992IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0


(1.92)
(1.2)
(2.09)
(6X 0.5)
(6X 0.35)
(4X 0.95)
RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS
DIMENSIONS ARE IN MILLIMETERS
PIN 1 INDEX AREA
3.29±0.1
B
2.92±0.1
A
C
0.8 MAX
(0.2)
1.92±0.1
1
3
0.1 MAX
ALL LEADS
PIN 1 ID
1.2±0.1
6
4
6X 0.5±0.05
6X 0.35±0.05
⌖ 0.1Ⓜ C AⓈ BⓈ
4X 0.95
LDE06A (Rev A)

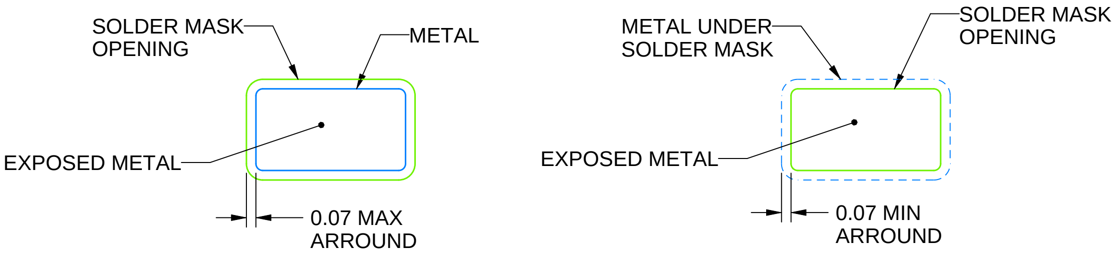


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

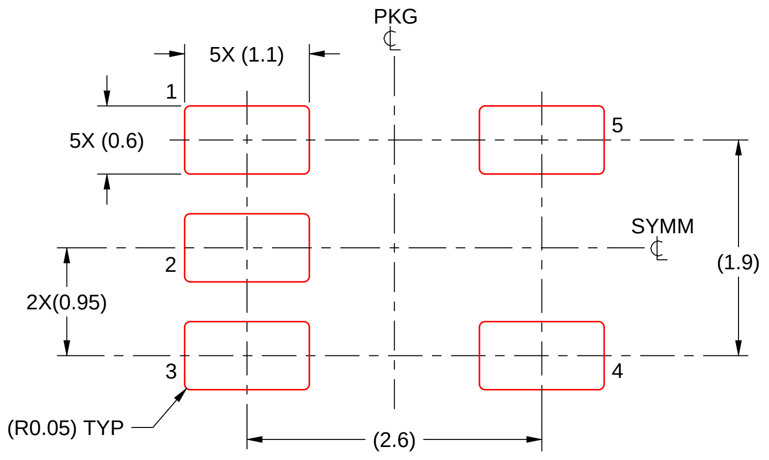
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265