LP5907-Q1 車載用250mA、超低ノイズ、低I_Q LDO

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み:
  - デバイス温度グレード 1: 動作時周囲温度範囲 –40℃～125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC6
- 入力電圧範囲: 2.2V～5.5V
- 出力電圧範囲: 1.2V～4.5V
- 1µFのセラミック入力/出力コンデンサで安定動作
- ノイズ・バイパス・コンデンサが不要
- 出力コンデンサのリモート配置
- 過熱および短絡保護
- 出力電流: 250mA
- 低い出力電圧ノイズ: 6.5μV_{RMS}未満
- PSRR: 82dB (1kHz時)
- 出力電圧公差: ±2%
- ほぼゼロのI_Q (ディセーブル時): 1µA未満
- 超低I_Q (イネーブル時): 12µA
- スタートアップ時間: 80µs
- 低いドロップアウト: 120mV (標準値)
- 動作時接合部温度範囲: -40℃～125℃

2 アプリケーション

- 車載インフォテインメント
- テレマティクス・システム
- ADASのカメラとレーダー
- ナビゲーション・システム

3 概要

LP5907-Q1は低ノイズLDOで、250mAの出力電流を供給できます。RF/アナログ回路の要件を満たすよう設計されたLP5907-Q1は、低ノイズ、高PSRR、低静止電流、低ライン/負荷過渡応答といった特徴を備えています。新しい革新的な設計手法の採用により、ノイズ・バイパス用コンデンサなしでクラス最高レベルの優れたノイズ特性を実現し、出力コンデンサのリモート配置にも対応します。

このデバイスは、入力および出力に1µFのセラミック・コンデンサを使用して動作するよう設計されています(個別にノイズ・バイパス・コンデンサを用意する必要はありません)。

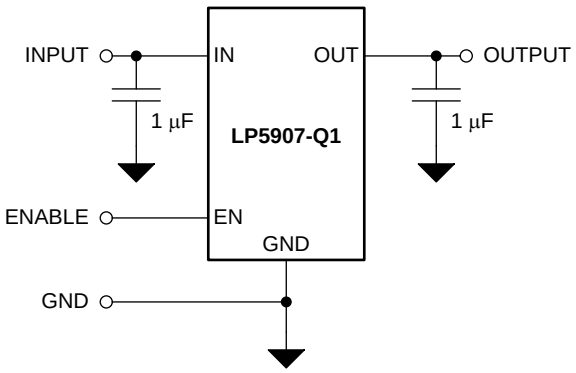
このデバイスでは、1.2V～4.5V (25mVステップ)の固定出力電圧を使用できます。具体的な電圧オプションについては、テキサス・インスツルメンツの販売部門までお問い合わせください。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LP5907-Q1	SOT-23 (5)	2.90mm×1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (September 2016) から **Revision C** に変更 **Page**

- 「*特長*」セクションにESD分類レベルの箇条書き副項目を 追加 ... 1
- Changed DBV values in *Thermal Information* table ... 4
- Deleted footnote 1 from *Thermal Information* table ... 4
- Added *Overshoot on start-up with EN* row to *Electrical Characteristics* table ... 6
- Changed *Device Comparison* table: changed table title, added new rows and new data, moved to new sub-section ... 12

Revision A (June 2016) から **Revision B** に変更 **Page**

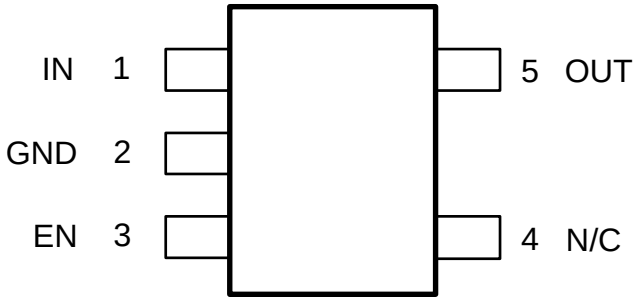
- タイトルの表現 変更 ... 1
- 「低い出力電圧ノイズ: 10μV_{RMS}未満」を「低い出力電圧ノイズ: 6.5μV_{RMS}未満」に 変更 ... 1
- 「*アプリケーション*」の一覧の項目 変更 ... 1
- 「*概要*」の最初の文について表現を 変更 ... 1

2014年9月発行のものから更新 **Page**

- 「*特長*」に車載関連の箇条書き項目を 追加 ... 1
- TI Designs用の上端のナビゲーション・アイコン 追加 ... 1
- 「リニア・レギュレータ」を「LDO」に 変更 ... 1
- Changed storage temperature from *Handling Ratings* to *Abs Max* table; replaced *Handling Ratings* with *ESD Ratings* per new format ... 4

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOT23-5		
IN	1	I	Input voltage supply. Connect a 1-µF capacitor at this input.
GND	2	–	Common ground
EN	3	I	Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off and discharges the output pin to GND through an internal 230-Ω pulldown resistor. A high voltage (> V_{IH}) on this pin enables the regulator output. This pin has an internal 1-MΩ pulldown resistor to hold the regulator off by default.
N/C	4	–	No internal electrical connection.
OUT	5	O	Regulated output voltage. Connect a minimum 1-µF low-ESR capacitor to this pin. Connect this output to the load circuit. An internal 230-Ω (typical) pulldown resistor prevents a charge remaining on V_{OUT} when the regulator is in the shutdown mode (V_{EN} low).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	See (3)	V
V_{EN}	Enable input voltage	–0.3	6	V
	Continuous power dissipation(4)	Internally limited		W
T_{JMAX}	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND pin.
(3) Abs Max V_{OUT} is the lessor of V_{IN} + 0.3 V, or 6 V.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged-device model (CDM), per AEC Q100-011	Corner pins (1,3,4,5)	±1000	
			Other pin (2)	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage	2.2	5.5	V
V_{EN}	Enable input voltage	0	5.5	V
I_{OUT}	Output current	0	250	mA
$T_{J\text{-}MAX\text{-}OP}$	Operating junction temperature(3)	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND pin.
(3) $T_{J\text{-}MAX\text{-}OP} = [T_{A(MAX)} + (P_{D(MAX)} \times R_{\theta JA})]$.

6.4 Thermal Information

THERMAL METRIC(1)		LP5907-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	112.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted)(1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GENERAL							
V_{IN}	Input voltage	T_A = 25°C		2.2		5.5	V
ΔV_{OUT}	Output voltage tolerance	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA to 250 mA, V_{OUT} ≥ 1.8 V		–2		2	%V_{OUT}
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA to 250 mA, V_{OUT} < 1.8 V		–3		3	
	Line regulation	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 5.5 V, I_{OUT} = 1 mA			0.02		%/V
	Load regulation	I_{OUT} = 1 mA to 250 mA			0.001		%/mA
I_{LOAD}	Output load current			0		250	mA
I_Q	Quiescent current(4)	V_{EN} = 1.2 V, I_{OUT} = 0 mA			12	25	µA
		V_{EN} = 1.2 V, I_{OUT} = 250 mA			250	425	
		V_{EN} = 0.3 V (Disabled)			0.2	1	
I_G	Ground current(5)	V_{EN} = 1.2 V, I_{OUT} = 0 mA			14		µA
V_{DO}	Dropout voltage(6)	I_{OUT} = 100 mA			50		mV
		I_{OUT} = 250 mA				250	
I_{SC}	Short-circuit current limit	T_A = 25°C(7)		250	500		mA
PSRR	Power-supply rejection ratio(8)	f = 100 Hz, I_{OUT} = 20 mA			90		dB
		f = 1 kHz, I_{OUT} = 20 mA			82		
		f = 10 kHz, I_{OUT} = 20 mA			65		
		f = 100 kHz, I_{OUT} = 20 mA			60		
e_N	Output noise voltage(8)	BW = 10 Hz to 100 kHz	I_{OUT} = 1 mA		10		μV_{RMS}
			I_{OUT} = 250 mA		6.5		
R_{AD}	Output automatic discharge pulldown resistance	V_{EN} < V_{IL} (output disabled)			230		Ω
T_{SD}	Thermal shutdown	T_J rising			160		°C
	Thermal hysteresis	T_J falling from shutdown			15		
LOGIC INPUT THRESHOLDS							
V_{IL}	Low input threshold	V_{IN} = 2.2 V to 5.5 V, V_{EN} falling until the output is disabled				0.4	V
V_{IH}	High input threshold	V_{IN} = 2.2 V to 5.5 V, V_{EN} rising until the output is enabled		1.2			V
I_{EN}	Input current at EN pin(9)	V_{EN} = 5.5 V and V_{IN} = 5.5 V			5.5		µA
		V_{EN} = 0 V and V_{IN} = 5.5 V			0.001		

(1) All voltages are with respect to the device GND terminal, unless otherwise stated.
(2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application $R_{\theta JA}$), as given by the following equation: T_{A-MAX} = $T_{J-MAX-OP}$ – ($R_{\theta JA}$ × P_{D-MAX}). See *Application and Implementation*.
(4) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
(5) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
(6) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
(7) Short-circuit current (I_{SC}) for the LP5907-Q1 is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.
(8) This specification is verified by design.
(9) There is a 1-MΩ resistor between EN and ground on the device.

Electrical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF (unless otherwise noted)(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSIENT CHARACTERISTICS						
ΔV_{OUT}	Line transient(8)	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 1.6 V) in 30 µs	–1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6 V) to ($V_{OUT(NOM)}$ + 1.6 V) in 30 µs			1	
	Load transient(8)	I_{OUT} = 1 mA to 250 mA in 10 µs	–40			
		I_{OUT} = 250 mA to 1 mA in 10 µs			40	
	Overshoot on start-up(8)	Stated as a percentage of $V_{OUT(NOM)}$			5%	
	Overshoot on start-up with EN(8)	Stated as a percentage of $V_{OUT(NOM)}$, V_{IN} = V_{OUT} + 1 V to 5.5 V, 0.7 µF < C_{OUT} < 10 µF, 0 mA < I_{OUT} < 250 mA, EN rising until the output is enabled			1%	
t_{ON}	Turnon time	From V_{EN} > V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$, T_A = 25°C		80	150	µs

6.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX	UNIT
C_{IN}	Input capacitance(2)	Capacitance for stability	0.7	1		µF
C_{OUT}	Output capacitance(2)		0.7	1	10	
ESR	Output/input capacitance(2)		5		500	mΩ

(1) The minimum capacitance should be greater than 0.5 µF over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.
(2) This specification is verified by design.

6.7 Typical Characteristics

V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C (unless otherwise noted)

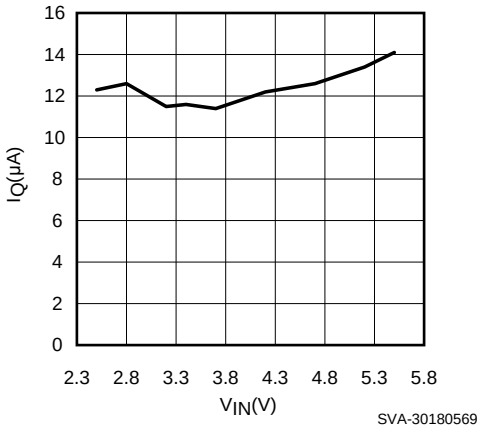


Figure 1. Quiescent Current vs Input Voltage

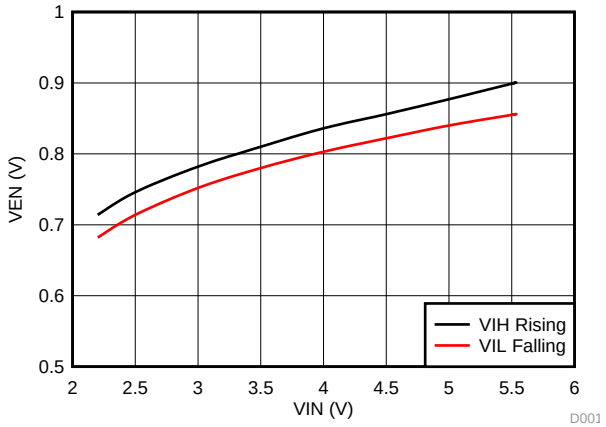
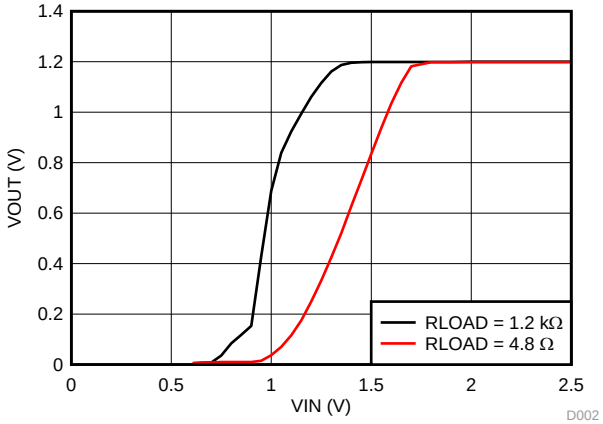
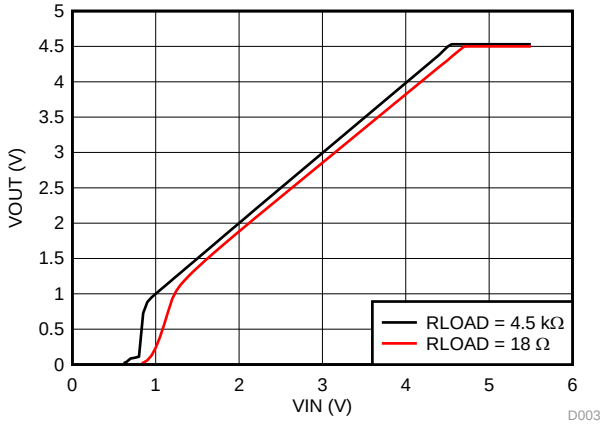


Figure 2. V_{EN} Thresholds vs V_{IN}



V_{OUT} = 1.2 V, V_{EN} = V_{IN}

Figure 3. V_{OUT} vs V_{IN}



V_{OUT} = 4.5 V, V_{EN} = V_{IN}

Figure 4. V_{OUT} vs V_{IN}

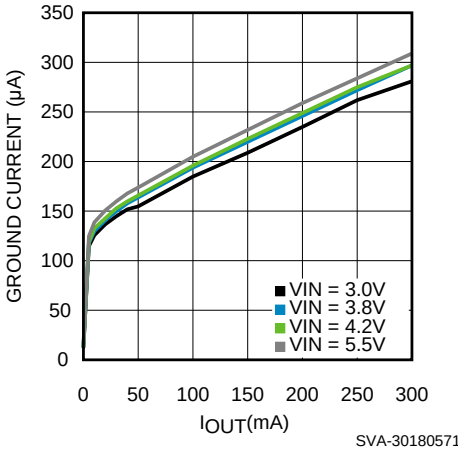


Figure 5. Ground Current vs Output Current

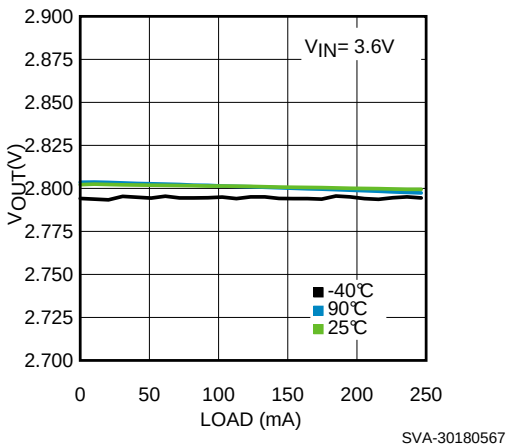


Figure 6. Load Regulation

Typical Characteristics (continued)

V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C (unless otherwise noted)

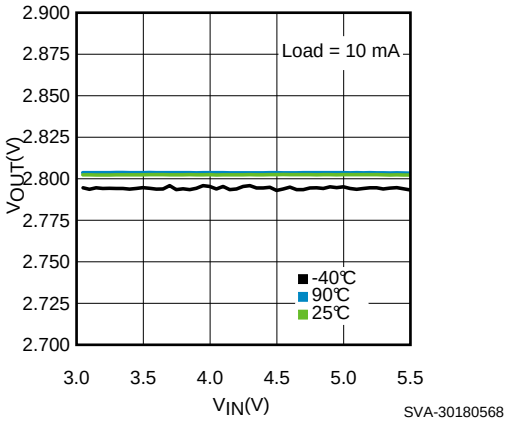


Figure 7. Line Regulation

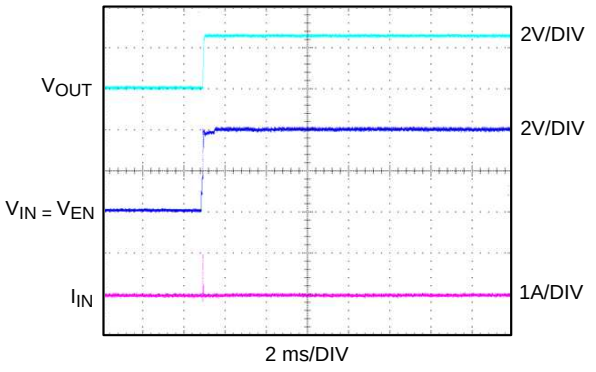
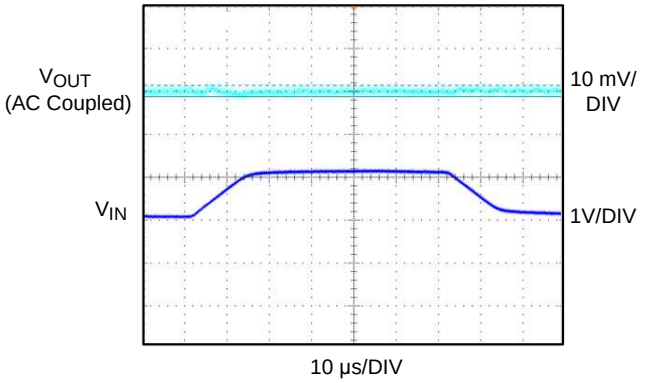
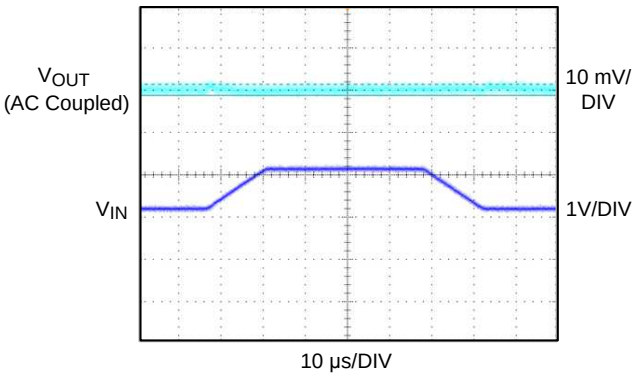


Figure 8. Inrush Current



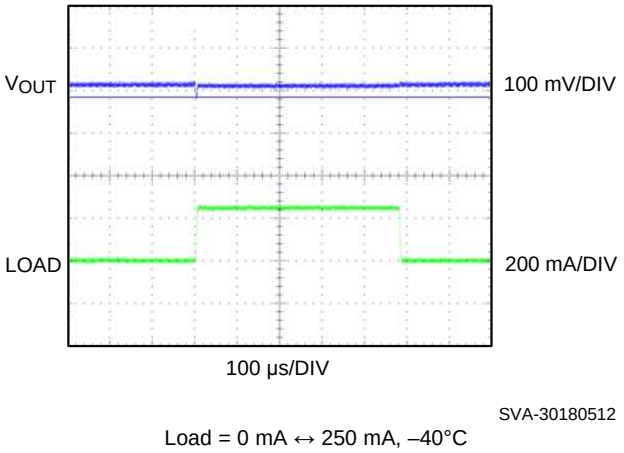
V_{IN} = 3.2 V ↔ 4.2 V, load = 1 mA

Figure 9. Line Transient



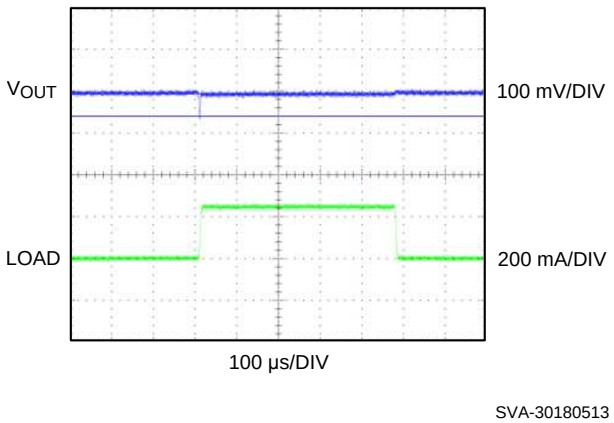
V_{IN} = 3.2 V ↔ 4.2 V, load = 250 mA

Figure 10. Line Transient



Load = 0 mA ↔ 250 mA, –40°C

Figure 11. Load Transient

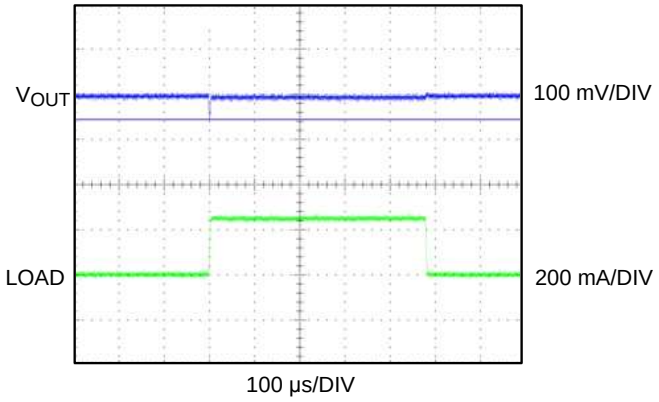


Load = 0 mA ↔ 250 mA, 90°C

Figure 12. Load Transient

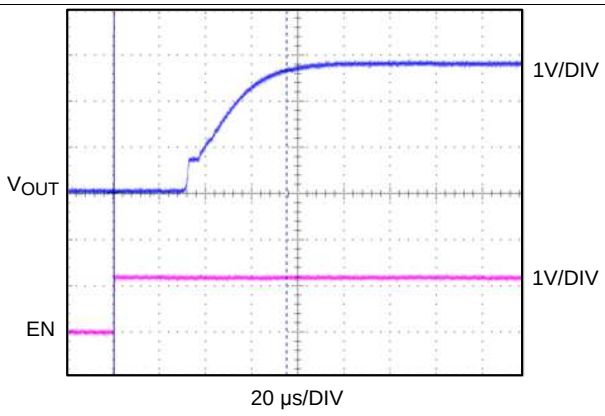
Typical Characteristics (continued)

V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C (unless otherwise noted)



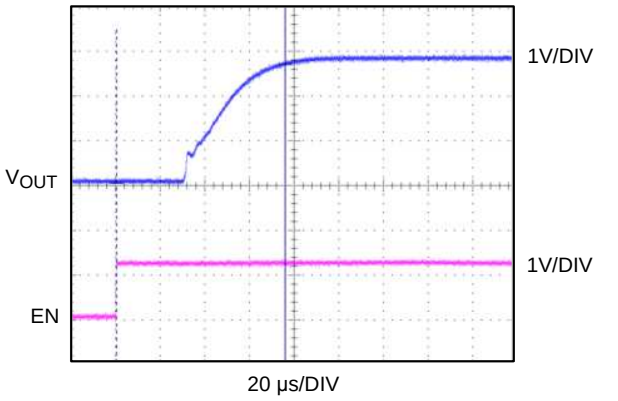
Load = 0 mA ↔ 250 mA, 25°C

Figure 13. Load Transient



0 mA

Figure 14. Start-Up



250 mA

Figure 15. Start-Up

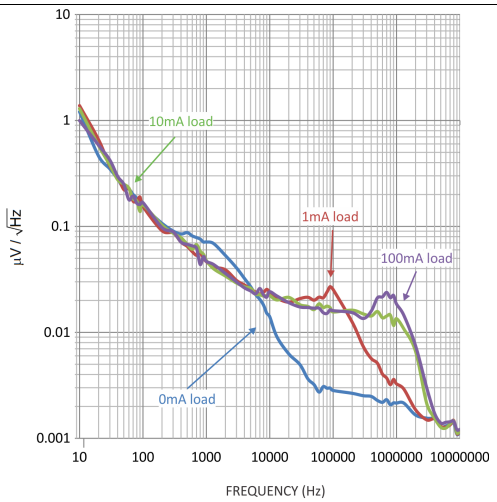


Figure 16. Noise Density Test

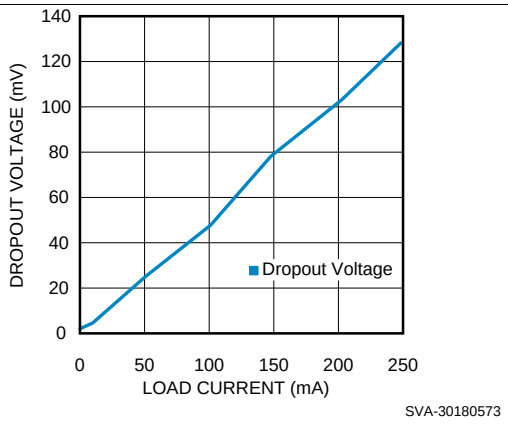


Figure 17. Dropout Voltage vs Load Current

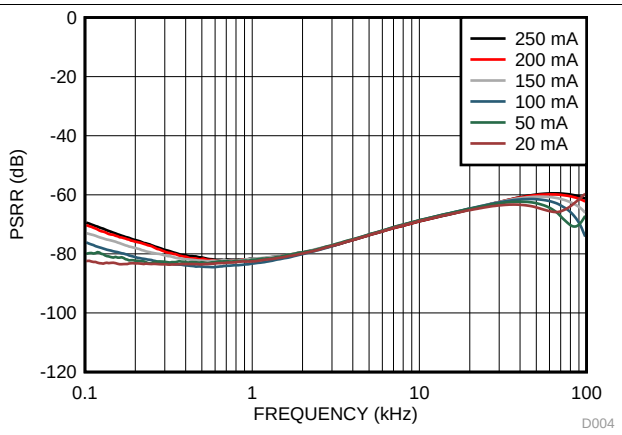


Figure 18. PSRR Loads Averaged 100 Hz To 100 KHz

Typical Characteristics (continued)

V_{IN} = 3.7 V, V_{OUT} = 2.8 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, T_A = 25°C (unless otherwise noted)

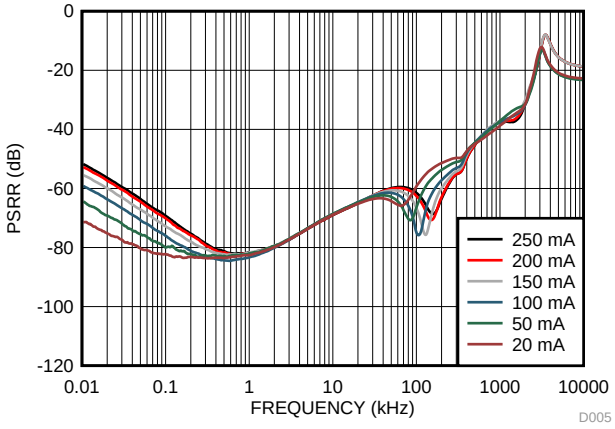


Figure 19. PSRR Loads Averaged 10 Hz To 10 MHz

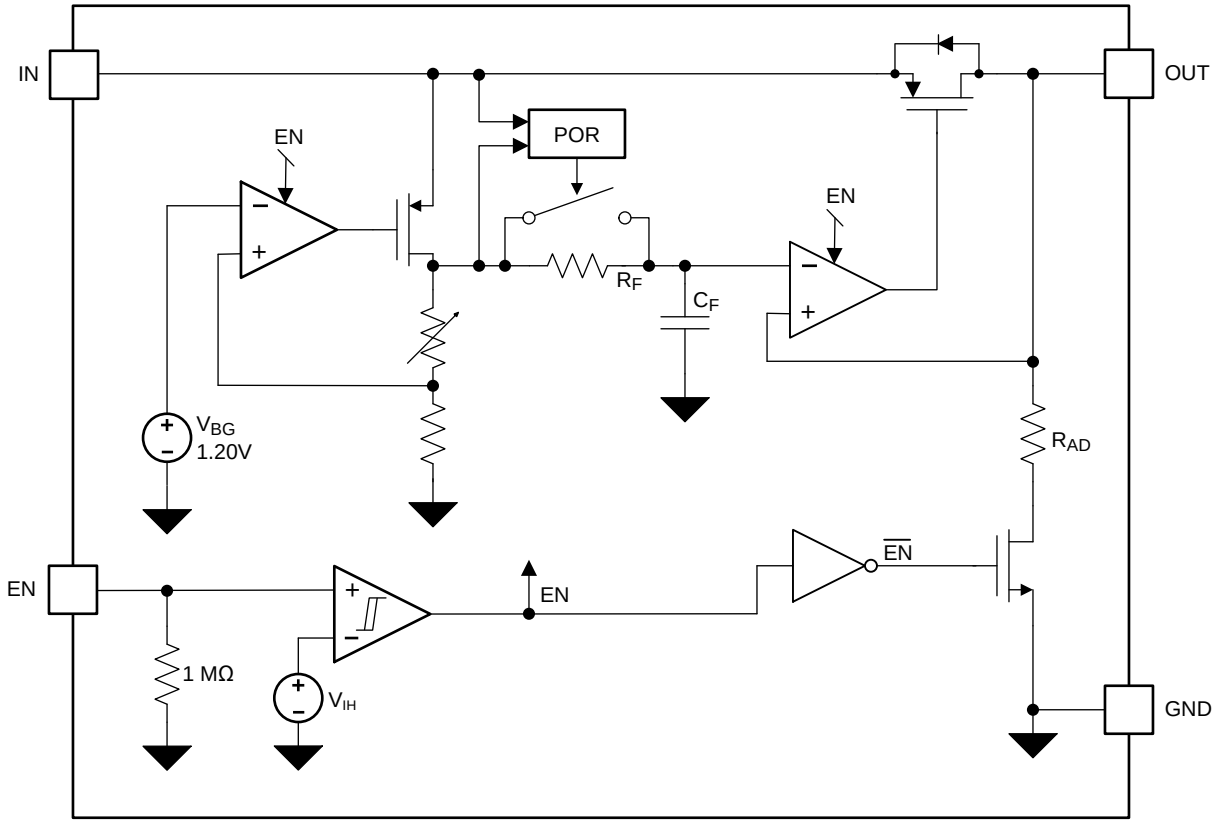
7 Detailed Description

7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the LP5907-Q1 provides low noise, high PSRR, low quiescent current, as well as low line and load transient response figures. Using new innovative design techniques, the LP5907-Q1 offers class leading noise performance without the need for a separate noise filter capacitor.

The LP5907-Q1 is designed to perform with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor. With a reasonable PCB layout, the single 1-µF ceramic output capacitor can be placed up to 10 cm away from the LP5907-Q1 package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 LP5907-Q1 Voltage Options

Table 1 lists the available voltage options for the LP5907-Q1 SOT-23 package.

Table 1. Voltage Options

SOT-23 PACKAGE ORDER NUMBER	VOLTAGE OPTION (V)
LP5907QMFX-1.2Q1	1.2
—	1.3
—	1.5
LP5907QMFX-1.8Q1	1.8
LP5907QMFX-2.5Q1	2.5
LP5907QMFX-2.8Q1	2.8
	2.85
	2.9
LP5907QMFX-3.0Q1	3.0
LP5907QMFX-3.3Q1	3.3
LP5907QMFX-3.8Q1	3.8
LP5907QMFX-4.5Q1	4.5

7.3.2 Enable (EN)

The LP5907-Q1 EN pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

7.3.3 Low Output Noise

Any internal noise at the LP5907-Q1 reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. The low-pass RC filter has a –3 dB cut-off frequency of approximately 0.1 Hz.

7.3.4 Output Automatic Discharge

The LP5907-Q1 output employs an internal 230-Ω (typical) pulldown resistance to discharge the output when the EN pin is low, and the device is disabled.

7.3.5 Remote Output Capacitor Placement

The LP5907-Q1 requires at least a 1-µF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10 cm away from the LDO.

7.3.6 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the LP5907-Q1 has been designed to protect against temporary thermal overload conditions. The thermal shutdown circuitry was not intended to replace proper heat-sinking. Continuously running the LP5907-Q1 device into thermal shutdown may degrade device reliability.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5907-Q1 Enable (EN) pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuitry is activated. Any charge on the OUT pin is discharged to GND through the internal 230-Ω (typical) pull-down resistance.

7.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5907-Q1 does not include any dedicated undervoltage lockout circuitry. The LP5907-Q1 internal circuitry is not fully functional until V_{IN} is at least 2.2 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2 V or (V_{OUT} + V_{DO}).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 20 shows the typical application circuit for the LP5907-Q1. Input and output capacitances may need to be increased above the 1 µF minimum for some applications.

8.2 Typical Application

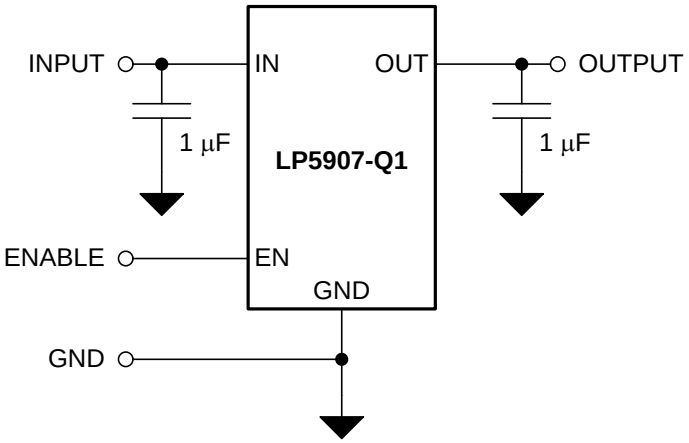


Figure 20. LP5907-Q1 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.2 to 5.5 V
Output voltage	1.8 V
Output current	200 mA
Output capacitor range	0.7 to 10 µF
Input/output capacitor ESR range	5 to 500 mΩ

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Available input voltage range
- Output voltage needed
- Output current needed
- Input and Output capacitors

8.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the device, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using Equation 1:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Equation 1 and Equation 2 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be derated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 3:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} - (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (3)$$

Alternately, if $T_{A\text{-}MAX}$ can not be derated, the P_D value must be reduced. This can be accomplished by reducing V_{IN} in the $V_{IN} - V_{OUT}$ term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

8.2.2.2 External Capacitors

Like most LDOs, the LP5907-Q1 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.3 Input Capacitor

An input capacitor is required for stability. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance. At least a 1-µF capacitor has to be connected between the LP5907-Q1 input pin and ground for stable operation over full load current range. Basically, it is acceptable to have more output capacitance than input, as long as the input is at least 1 µF.

The input capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5907-Q1, TI recommends increasing the input capacitor to at least 10 µF. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be verified by the manufacturer to have a surge current rating sufficient for the application. The initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 µF over the entire operating range.

8.2.2.4 Output Capacitor

The LP5907-Q1 is designed specifically to work with a very small ceramic output capacitor, typically 1 µF. A ceramic capacitor (dielectric types X5R or X7R) in the 1-µF to 10-µF range, and with equivalent series resistance (ESR) between 5 mΩ to 500 mΩ, is suitable in the LP5907-Q1 application circuit. For this device connect the output capacitor between the OUT pin and a good connection back to the GND pin.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 mΩ to 500 mΩ for stability. Like the input capacitor, the initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 µF over the entire operating range.

8.2.2.5 Capacitor Characteristics

The LP5907-Q1 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 10 µF, ceramic capacitors are the smallest, least expensive, and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5907-Q1.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 10 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. The ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.2.6 Remote Capacitor Operation

The LP5907-Q1 requires at least a 1-µF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor may be located up to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the output pin if there is already respective capacitors in the system (like a capacitor at the input of supplied part). The remote capacitor feature helps user to minimize the number of capacitors in the system.

As a good design practice, keep the wiring parasitic inductance at a minimum, which means to use as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

8.2.2.7 No-Load Stability

The LP5907-Q1 remains stable, and in regulation, with no external load.

8.2.2.8 Enable Control

The LP5907-Q1 may be switched ON or OFF by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, while a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1 µA. Additionally, an output pulldown circuit is activated which ensures that any charge stored on C_{OUT} is discharged to ground.

If the application does not require the use of the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1-MΩ pulldown resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turnon or turnoff voltage thresholds listed in the *Electrical Characteristics* under V_{IL} and V_{IH}.

8.2.3 Application Curves

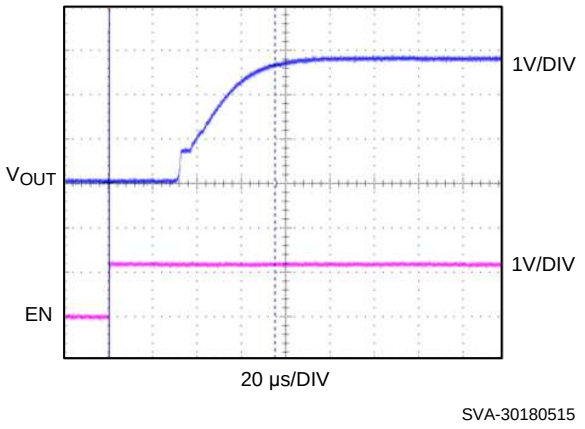


Figure 21. Start-Up

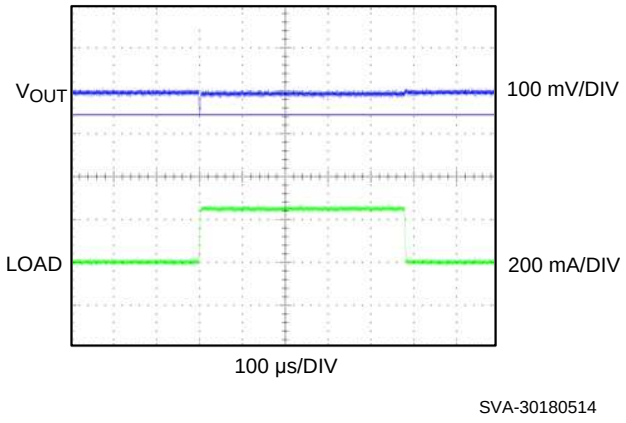


Figure 22. Load Transient Response

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.2 V to 5.5 V. The input supply must be well regulated and free of spurious noise. To ensure that the LP5907-Q1 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least V_{OUT} + 1 V. A minimum capacitor value of 1 µF is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5907-Q1 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5907-Q1.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5907-Q1, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be back to the LP5907-Q1 ground pin using as wide and short copper traces as are practical.

Avoid connections using long trace lengths, narrow trace widths, and/or connections through vias. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions

10.2 Layout Example

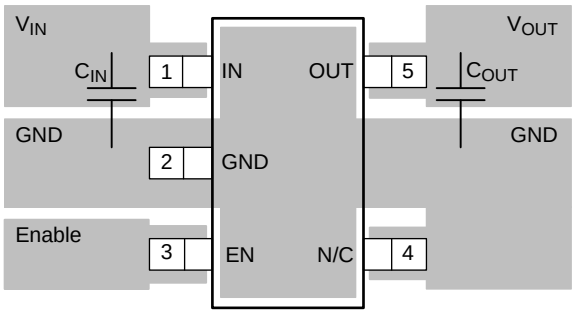


Figure 23. LP5907MF-x.x (SOT-23) Typical Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

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11.2 コミュニティ・リソース

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP590712QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D1	Samples
LP590713QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D2	Samples
LP590715QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D3	Samples
LP590718QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D4	Samples
LP590722QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FV	Samples
LP590725QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D5	Samples
LP5907285QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D7	Samples
LP590728QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D6	Samples
LP590729QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D8	Samples
LP590730QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D9	Samples
LP590733QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DA	Samples
LP590738QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DB	Samples
LP590745QDQNRQ1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DC	Samples
LP5907QMFX-1.2Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	RAFQ	Samples
LP5907QMFX-1.8Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	RAGQ	Samples
LP5907QMFX-2.5Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	RAJQ	Samples
LP5907QMFX-2.8Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	RAKQ	Samples
LP5907QMFX-3.0Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	RALQ	Samples
LP5907QMFX-3.3Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	RAHQ	Samples
LP5907QMFX-3.8Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	RAMQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907QMFX-4.5Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	RAIQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LP5907-Q1 :

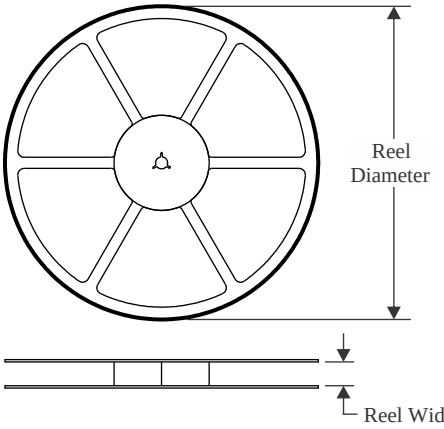
- Catalog : LP5907

NOTE: Qualified Version Definitions:

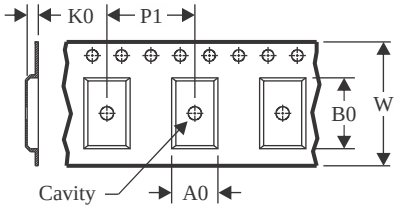
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

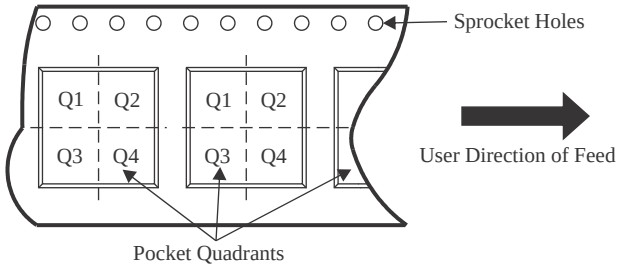


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

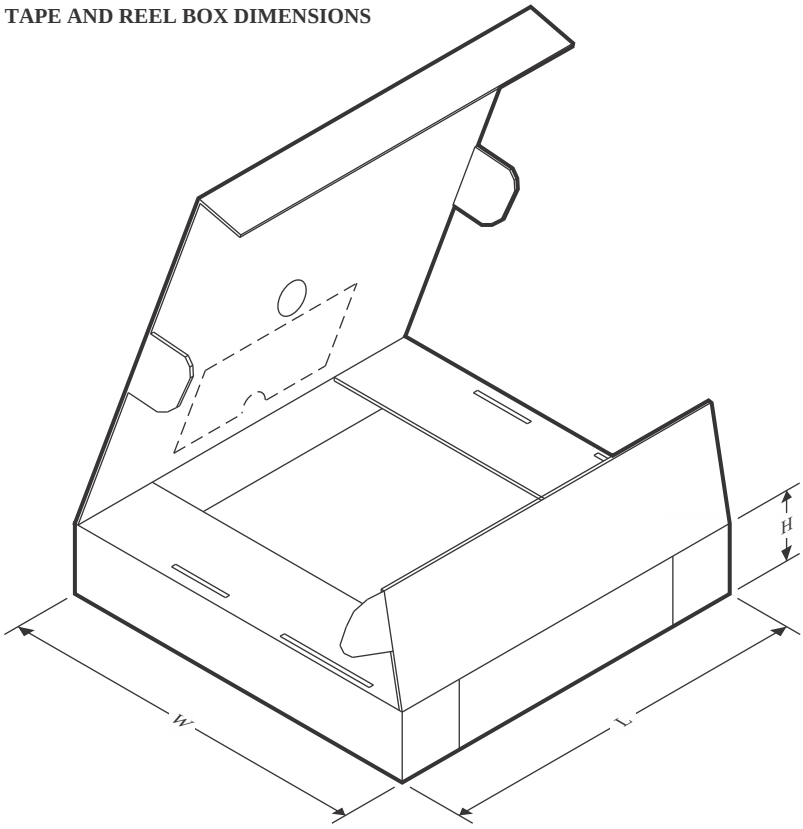


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP590712QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590713QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590715QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590718QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590722QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590725QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP5907285QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590728QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590729QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590730QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590733QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590738QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP590745QDQNRQ1	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
LP5907QMFX-1.2Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFX-1.8Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFX-2.5Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907QMFX-2.8Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFX-3.0Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFX-3.3Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFX-3.8Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907QMFX-4.5Q1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP590712QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590713QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590715QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590718QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590722QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590725QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP5907285QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590728QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590729QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590730QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590733QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590738QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP590745QDQNRQ1	X2SON	DQN	4	3000	213.0	191.0	35.0
LP5907QMFX-1.2Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFX-1.8Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFX-2.5Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFX-2.8Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFX-3.0Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0

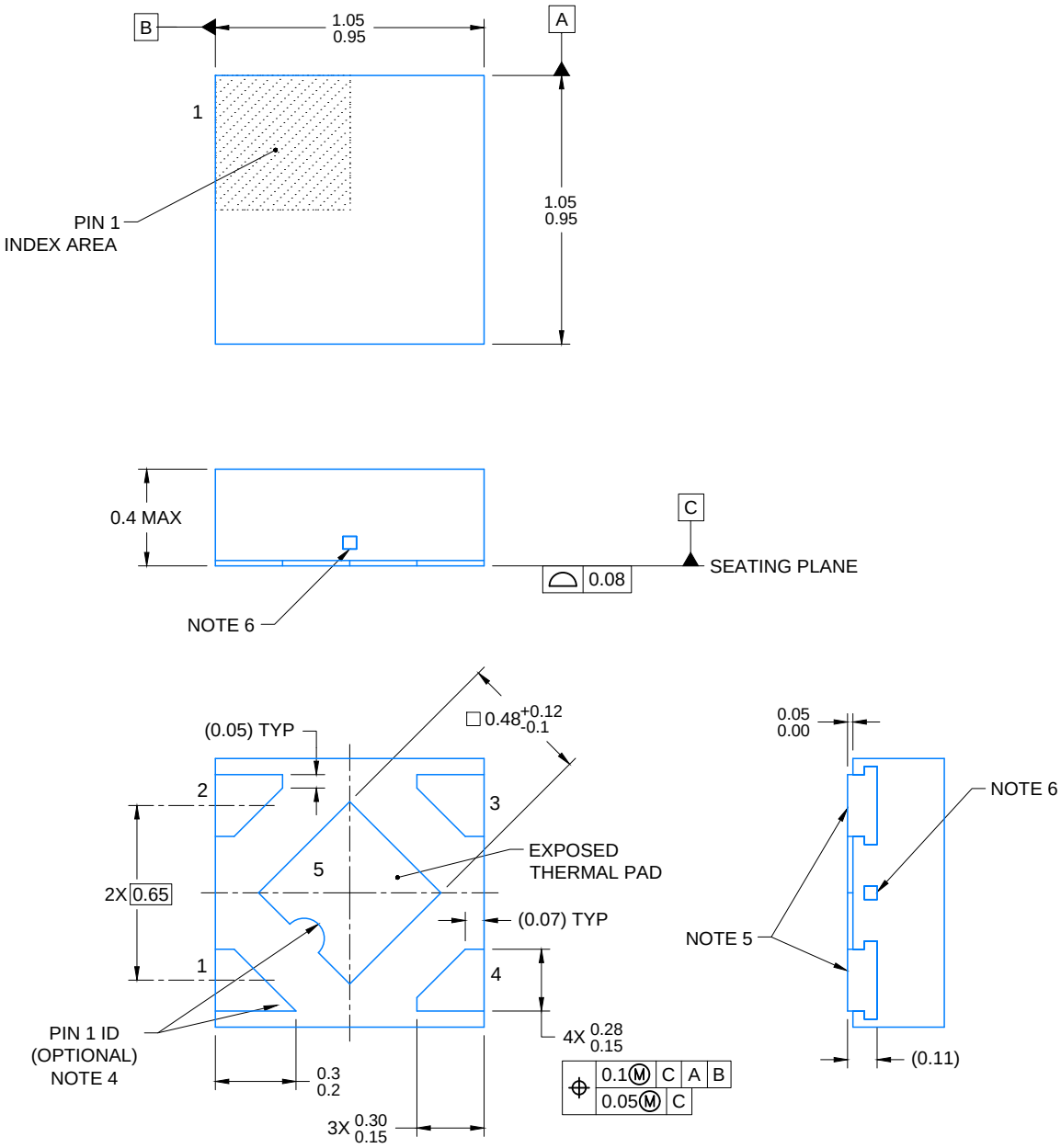
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907QMFX-3.3Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFX-3.8Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907QMFX-4.5Q1	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DQN0004A

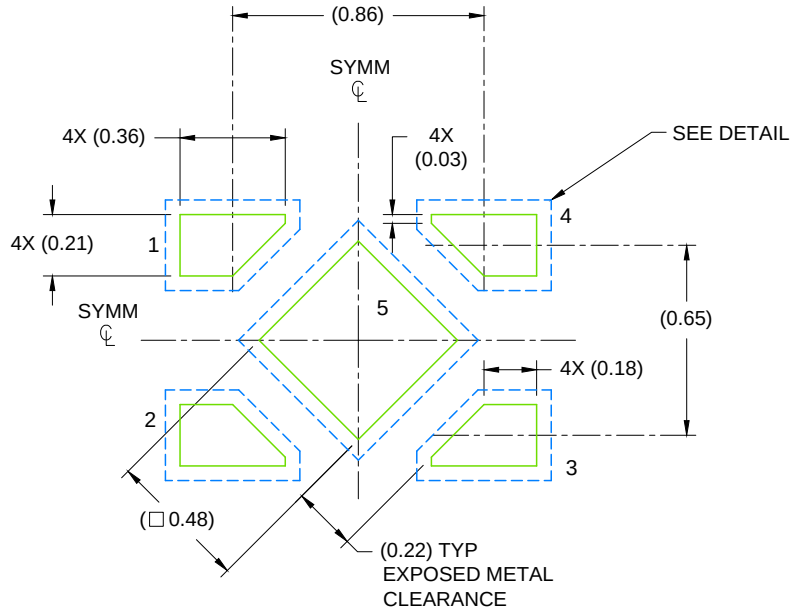
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



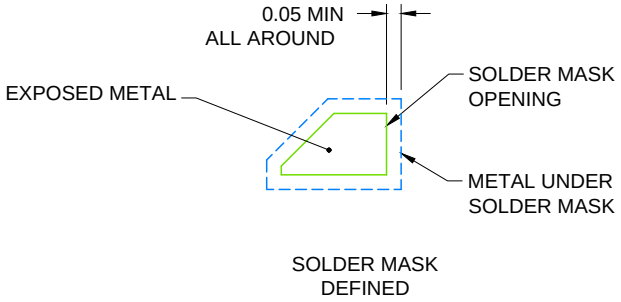
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

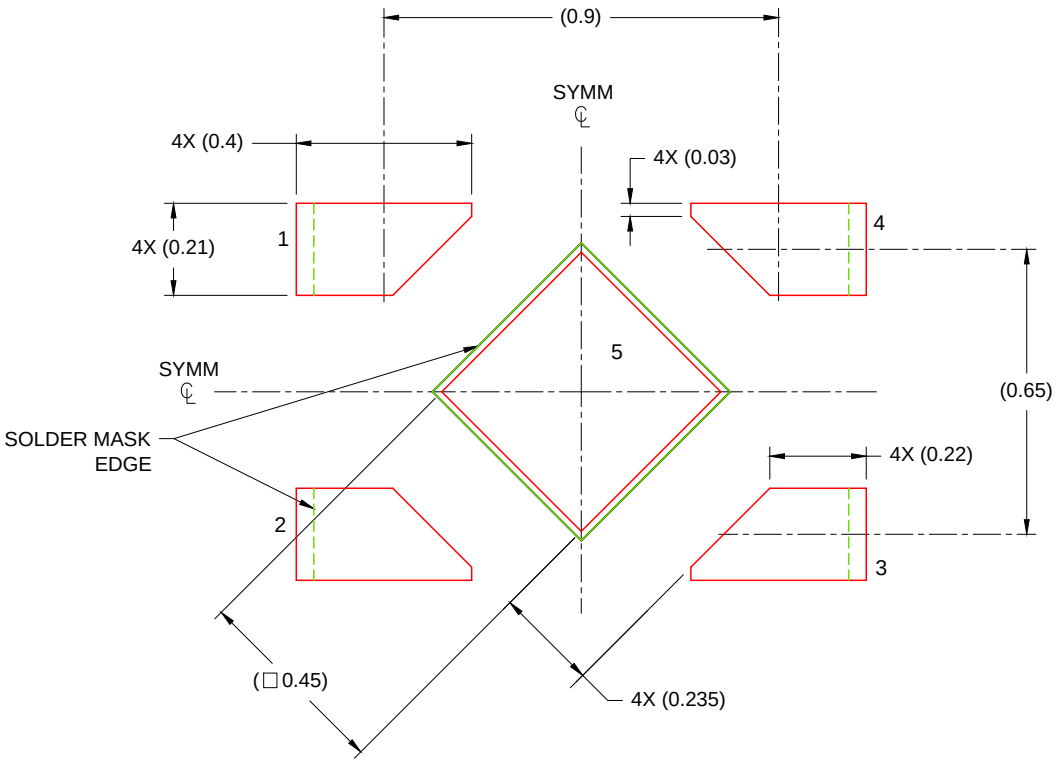


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

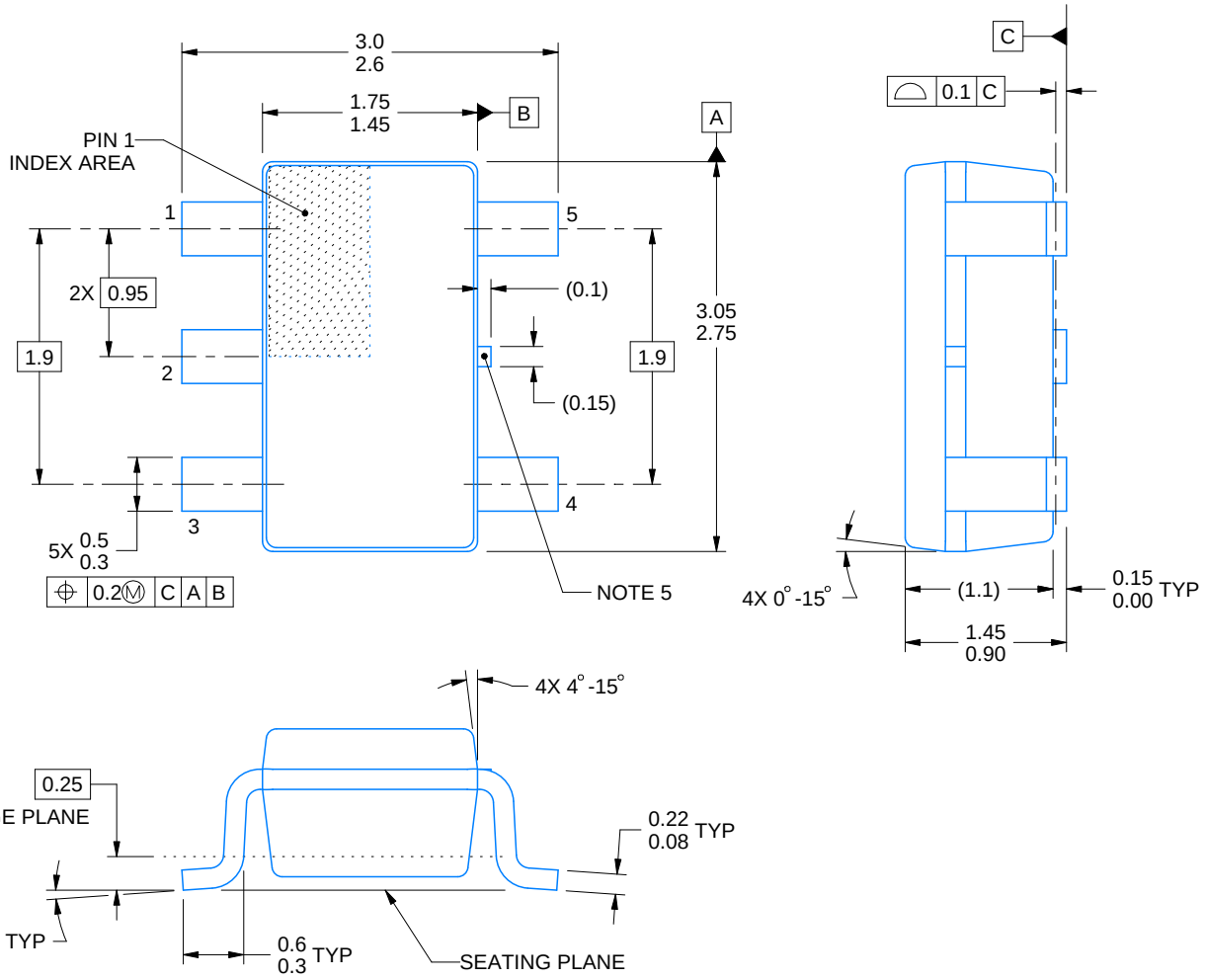
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

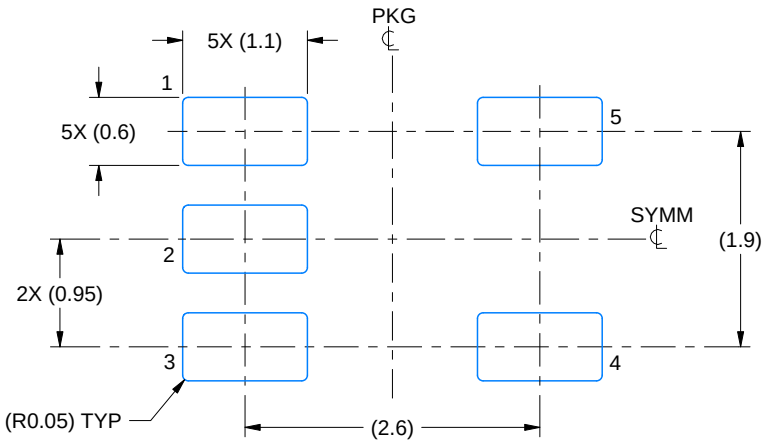
SMALL OUTLINE TRANSISTOR



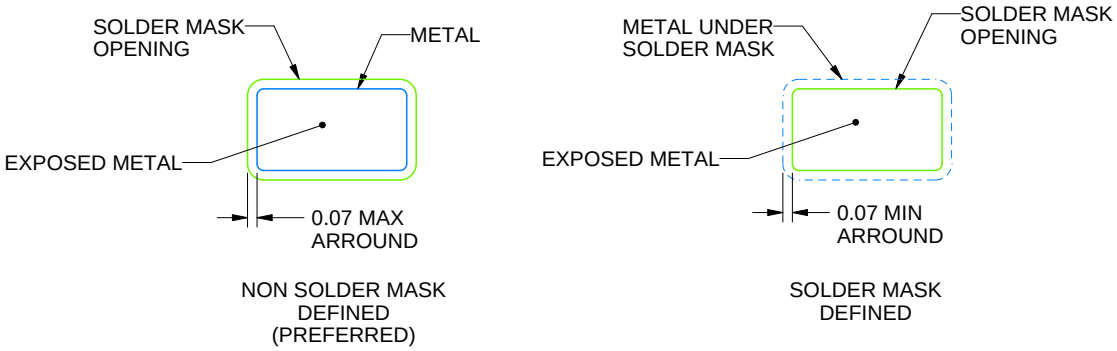
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

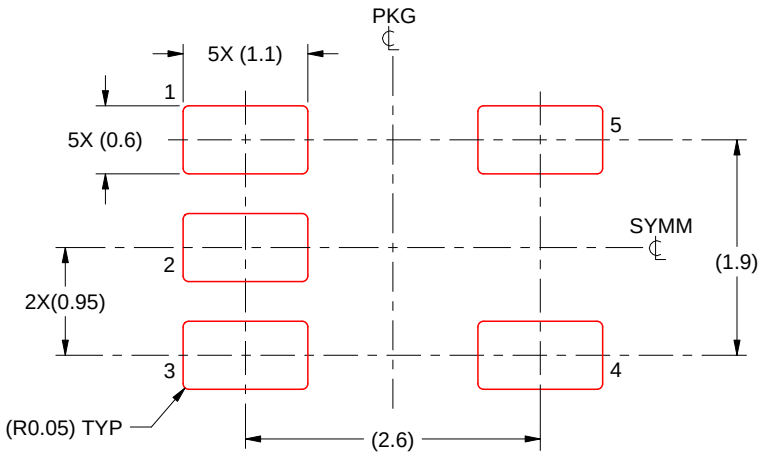


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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