TEXAS INSTRUMENTS
LPV321-N, LPV324-N, LPV358-N
JAJS630E – AUGUST 2000 – REVISED NOVEMBER 2016

LPV321-N シングル/LPV358-N デュアル/LPV324-N クワッド、汎用低電圧、低消費電力、レール・ツー・レール出力オペアンプ

1 特長

- 2.7Vおよび5Vでの性能を規定
- クロスオーバー歪みゼロ
- 省スペース型パッケージ
  - 5ピンのSC70 2×2.1×1mm
- 工業用温度範囲: -40℃～85℃
- ゲイン帯域幅積: 152kHz
- 低消費電流
  - LPV321-N: 9μA
  - LPV358-N: 15μA
  - LPV324-N: 28μA
- レール・ツー・レール出力スイング(100kΩ負荷時)
  - V^+ - 3.5mV
  - V^- + 90mV
- V_{CM}: -0.2V～V^+- 0.8V

2 アプリケーション

- アクティブ・フィルタ
- 汎用低電圧アプリケーション
- 汎用携帯機器

3 概要

LPV3xx-Nは、LMV3xxオペアンプの低消費電力バージョン(5V時にチャネルあたり9μA)です。

LMVオペアンプ製品ファミリに新たに追加された製品です。

LPV3xx-Nは、低電圧、低消費電力、省スペース、低価格が要求されるアプリケーションに、最もコスト効果の高いソリューションです。LPV3xx-Nはレール・ツー・レール出力機能を持ち、入力同相電圧範囲にグランドが含まれています。これらのオペアンプはすべて、速度/電力の比率が非常に優れており、わずか9μAの消費電流で152kHzの帯域幅を実現しています。

LPV321-Nは省スペースの5ピンSC70で供給され、5ピンSOT-23の約半分のサイズです。パッケージが小さいため、PC基板のスペースを節約でき、小型の携帯電子機器の設計が可能になります。また、デバイスを信号源に近接して配置できるため、ノイズを拾いにくくなり、シグナル・インテグリティ(信号品質)が向上します。

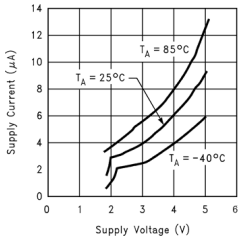
本製品は、テキサス・インスツルメンツの高度なサブミクロン・シリコンゲートBiCMOSプロセスで製造されています。LPV3xx-Nの入出力段はバイポーラ構成になっており、ノイズ性能の改善と出力電流ドライブの強化を実現しています。

製品情報(1)

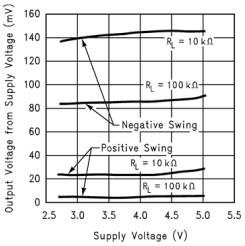
型番	パッケージ	本体サイズ(公称)
LPV321-N	SC70 (5)	2.00mm×1.25mm
	SOT-23 (5)	2.90mm×1.60mm
LPV358-N	SOIC (8)	4.90mm×3.91mm
	VSSOP (8)	3.00mm×3.00mm
LPV324-N	SOIC (14)	8.65mm×3.91mm
	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

Micropower消費電流



レール・ツー・レールの出力スイング



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (March 2013) から **Revision E** に変更 **Page**

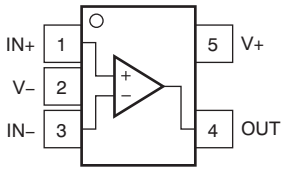
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- Deleted Soldering temperature (235°C maximum) ... 4
- Changed Thermal Resistance, $R_{\theta JA}$, values From: 478 To: 296.7 (SC70), From: 265 To: 206.6 (SOT-23), From: 190 To: 130.1 (8-Pin SOIC), From: 235 To: 187.5 (VSSOP), From: 145 To: 103.9 (14-Pin SOIC), From: 155 To: 132.7 (TSSOP) ... 4

Revision C (March 2013) から **Revision D** に変更 **Page**

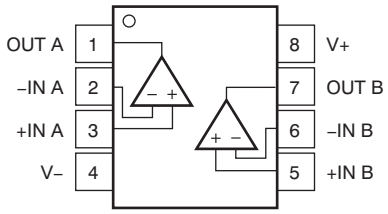
- ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更 ... 1

5 Pin Configuration and Functions

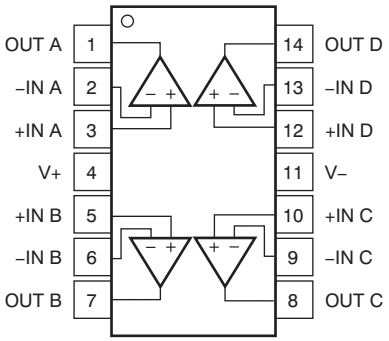
DBV or DCK Package
5-Pin SC70 or SOT-23
Top View



D or DGK Package
8-Pin SOIC or VSSOP
Top View



D or PW Package
14-Pin SOIC or TSSOP
Top View



Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	SC70 or SOT-23	SOIC or VSSOP	SOIC or TSSOP		
+IN	1	—	—	I	Noninverting input
IN A+	—	3	3	I	Noninverting input, channel A
IN B+	—	5	5	I	Noninverting input, channel B
IN C+	—	—	10	I	Noninverting input, channel C
IN D+	—	—	12	I	Noninverting input, channel D
–IN	3	—	—	I	Inverting input
IN A–	—	2	2	I	Inverting input, channel A
IN B–	—	6	6	I	Inverting input, channel B
IN C–	—	—	9	I	Inverting input, channel C
IN D–	—	—	13	I	Inverting input, channel D
OUTPUT	4	—	—	O	Output
OUT A	—	1	1	O	Output, channel A
OUT B	—	7	7	O	Output, channel B
OUT C	—	—	8	O	Output, channel C
OUT D	—	—	14	O	Output, channel D
V+	5	8	4	P	Positive (highest) power supply
V–	2	4	11	P	Negative (lowest) power supply

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Differential input voltage	±Supply voltage		
Supply voltage (V^+ – V^-)		5.5	V
Output short circuit to V^+	See(2)		
Output short circuit to V^-	See(3)		
Junction temperature, $T_{J(MAX)}$(4)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Shorting output to V^+ will adversely affect reliability.
(3) Shorting output to V^- will adversely affect reliability.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$ and $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
LPV321-N in DBV and DCK Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Machine model	±100	
LPV358-N in D and DGK Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Machine model	±100	
LPV324-N in D and PW Packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model	±100	

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage	2.7	5	V
Operating temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LPV321-N		LPV358-N		LPV324-N		UNIT
		DBV (SOT-23)	DCK (SC70)	DGK (VSSOP)	D (SOIC)	D (SOIC)	PW (TSSOP)	
		5 PINS	5 PINS	8 PINS	8 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.6	296.7	187.5	130.1	103.9	132.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	167.2	128.1	77.7	74.3	61.6	59.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.5	74.3	108	70.7	58.4	75.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	50.2	6.5	15.2	23.1	21.2	10.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.1	73.6	106.5	70.2	58.1	74.58	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics – 2.7 V

T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1 V, V_O = V^+/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input offset voltage			1.2	7	mV
TCV_{OS}	Input offset voltage average drift			2		µV/°C
I_B	Input bias current			1.7	50	nA
I_{OS}	Input offset current			0.6	40	nA
CMRR	Common mode rejection ratio	0 V ≤ V_{CM} ≤ 1.7 V	50	70		dB
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 5 V, V_O = 1 V, V_{CM} = 1 V	50	65		dB
V_{CM}	Input common-mode voltage	For CMRR ≥ 50 dB	0	−0.2		V
				1.9	1.7	
V_O	Output swing	R_L = 100 kΩ to 1.35 V	V^+ − 100	V^+ − 3		mV
				80	180	
I_S	Supply current	LPV321-N		4	8	µA
		LPV358-N, both amplifiers		8	16	
		LPV324-N, all four amplifiers		16	24	

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

6.6 AC Electrical Characteristics – 2.7 V

T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1 V, V_O = V^+/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
GBWP	Gain-bandwidth product	C_L = 22 pF		112		kHz
Φ_m	Phase margin			97		°
G_m	Gain margin			35		dB
e_n	Input-referred voltage noise	f = 1 kHz		178		nV/√Hz
i_n	Input-referred current noise	f = 1 kHz		0.5		pA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

6.7 DC Electrical Characteristics – 5 V

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2 V, V_O = V^+/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input offset voltage	T_J = 25°C		1.5	7	mV
		T_J = –40°C to 85°C			10	
TCV_{OS}	Input offset voltage average drift			2		µV/°C
I_B	Input bias current	T_J = 25°C		2	50	nA
		T_J = –40°C to 85°C			60	
I_{OS}	Input offset current	T_J = 25°C		0.6	40	nA
		T_J = –40°C to 85°C			50	
CMRR	Common mode rejection ratio	0 V ≤ V_{CM} ≤ 4 V	50	71		dB
PSRR	Power supply rejection ratio	2.7 V ≤ V^+ ≤ 5 V, V_O = 1 V, V_{CM} = 1 V	50	65		dB

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

DC Electrical Characteristics – 5 V (continued)

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2 V, V_O = V^+/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{CM}	Input common-mode voltage	For CMRR ≥ 50 dB		0	−0.2		V
					4.2	4	
A_V	Large signal voltage gain(3)	R_L = 100 kΩ	T_J = 25°C	15	100		V/mV
			T_J = –40°C to 85°C	10			
V_O	Output swing	Sourcing R_L = 100 kΩ to 2.5 V	T_J = 25°C	V^+ −100	V^+ −3.5		mV
			T_J = –40°C to 85°C	V^+ −200			
		Sinking R_L = 100 kΩ to 2.5 V	T_J = 25°C		90	180	
			T_J = –40°C to 85°C			220	
I_O	Output short circuit current sourcing	LPV3xx-N, V_O = 0 V		2	16		mA
	Output short circuit current sinking	LPV321-N, V_O = 5 V		20	60		
		LPV324-N and LPV358-N, V_O = 5 V		11	16		
I_S	Supply current	LPV321-N	T_J = 25°C		9	12	µA
			T_J = –40°C to 85°C			15	
		LPV358-N, Both amplifiers	T_J = 25°C		15	20	
			T_J = –40°C to 85°C			24	
		LPV324-N, All four amplifiers	T_J = 25°C		28	42	
			T_J = –40°C to 85°C			46	

(3) R_L is connected to V^-. The output voltage is 0.5 V ≤ V_O ≤ 4.5 V.

6.8 AC Electrical Characteristics – 5 V

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2 V, V_O = V^+/2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
SR	Slew rate(3)			0.1		V/µs
GBWP	Gain-bandwidth product	C_L = 22 pF		152		kHz
Φ_m	Phase margin			87		°
G_m	Gain margin			19		dB
e_n	Input-referred voltage noise	f = 1 kHz		146		nV/√Hz
i_n	Input-referred current noise	f = 1 kHz		0.3		pA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

6.9 Typical Characteristics

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

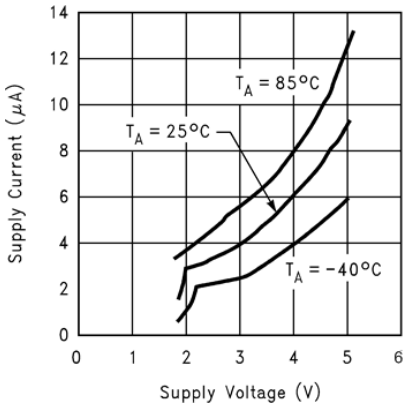


Figure 1. Supply Current vs Supply Voltage (LPV321-N)

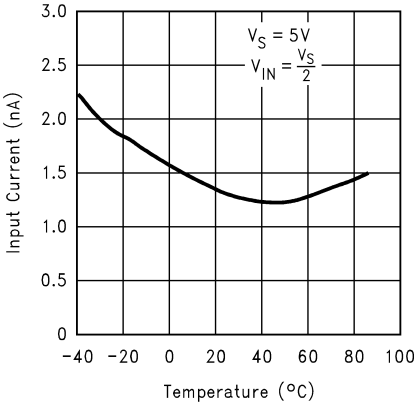


Figure 2. Input Current vs Temperature

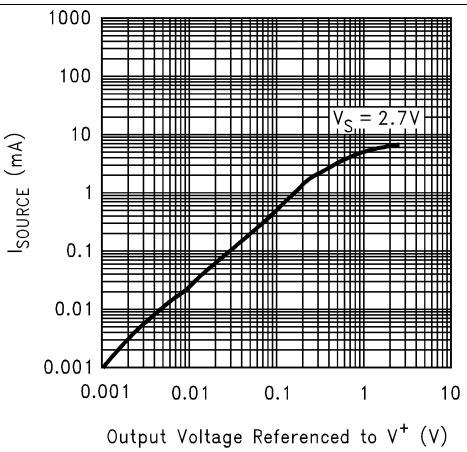


Figure 3. Sourcing Current vs Output Voltage

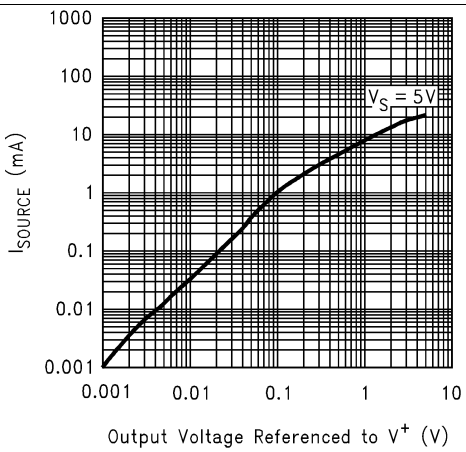


Figure 4. Sourcing Current vs Output Voltage

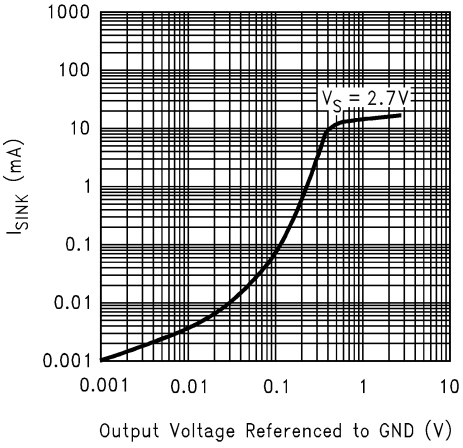


Figure 5. Sinking Current vs Output Voltage

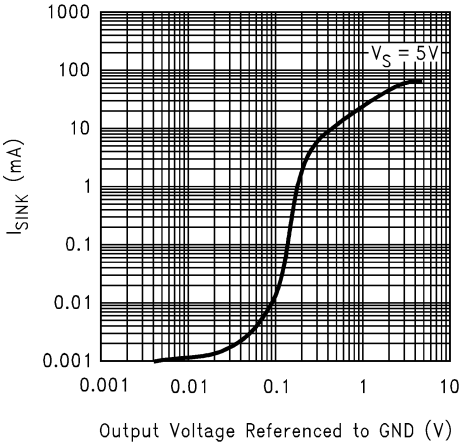


Figure 6. Sinking Current vs Output Voltage

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

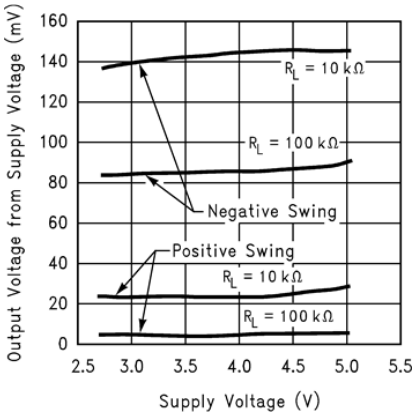


Figure 7. Output Voltage Swing vs Supply Voltage

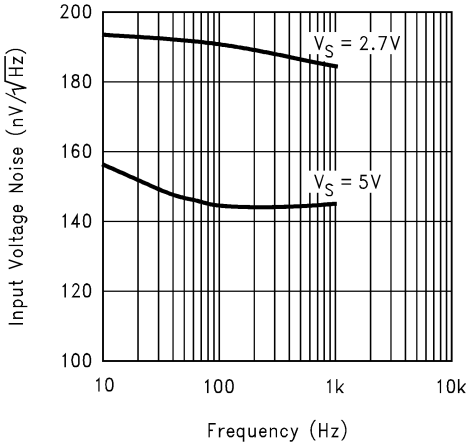


Figure 8. Input Voltage Noise vs Frequency

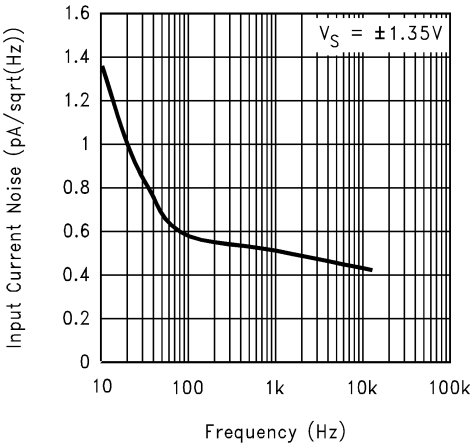


Figure 9. Input Current Noise vs Frequency

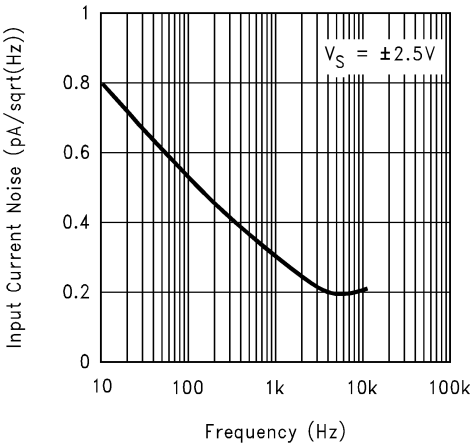


Figure 10. Input Current Noise vs Frequency

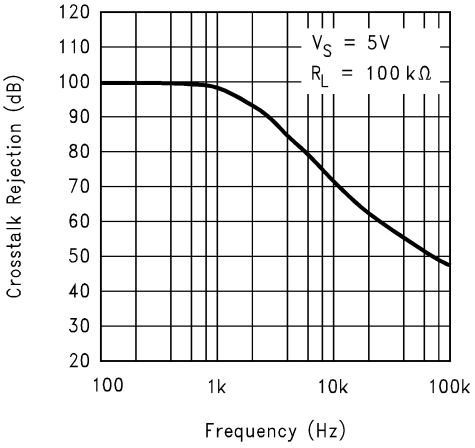


Figure 11. Crosstalk Rejection vs Frequency

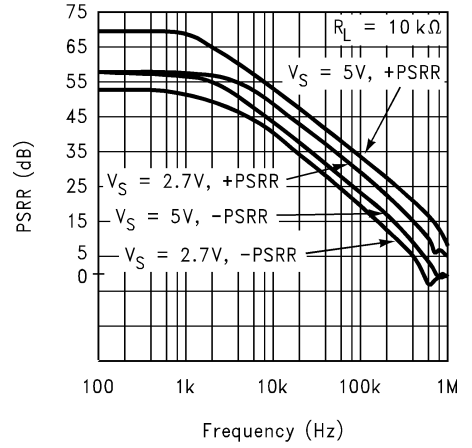


Figure 12. PSRR vs Frequency

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

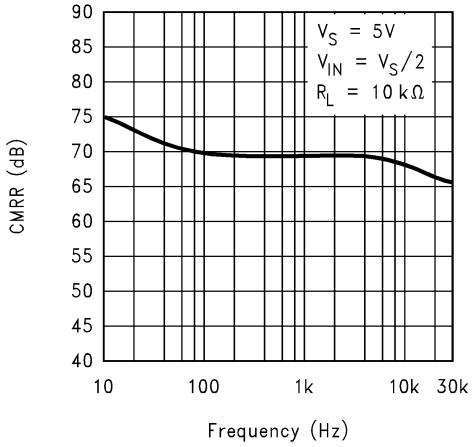


Figure 13. CMRR vs Frequency

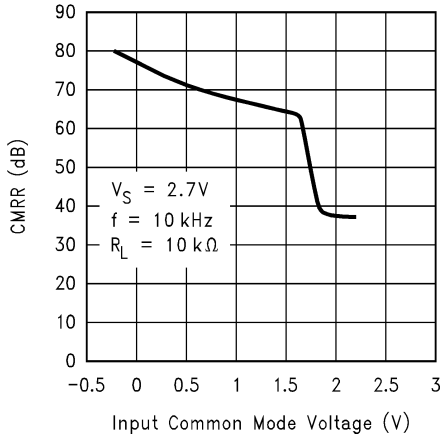


Figure 14. CMRR vs Input Common Mode Voltage

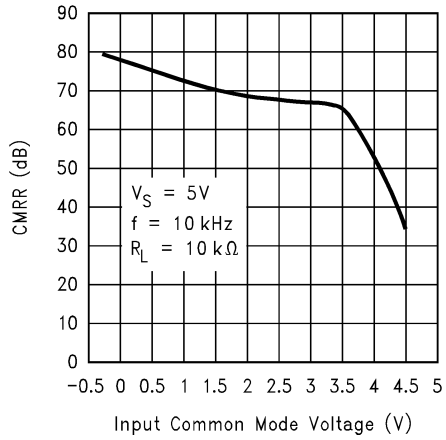


Figure 15. CMRR vs Input Common Mode Voltage

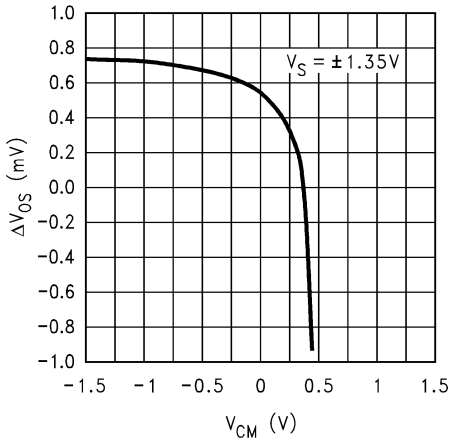


Figure 16. ΔV_{OS} vs V_{CM}

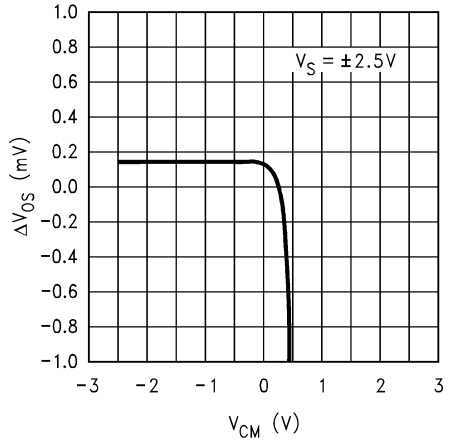


Figure 17. ΔV_{OS} vs V_{CM}

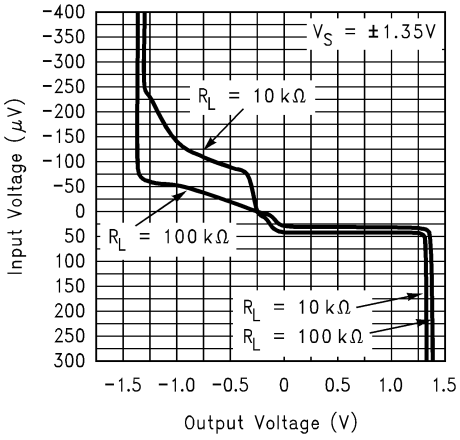


Figure 18. Input Voltage vs Output Voltage

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

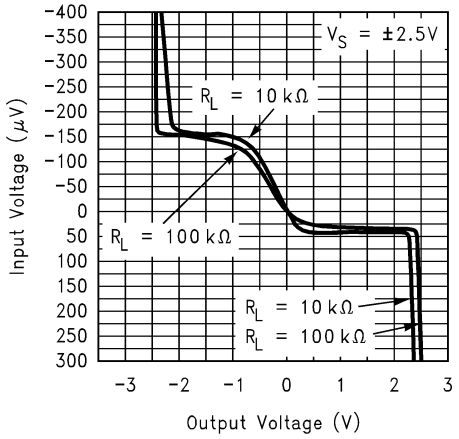


Figure 19. Input Voltage vs Output Voltage

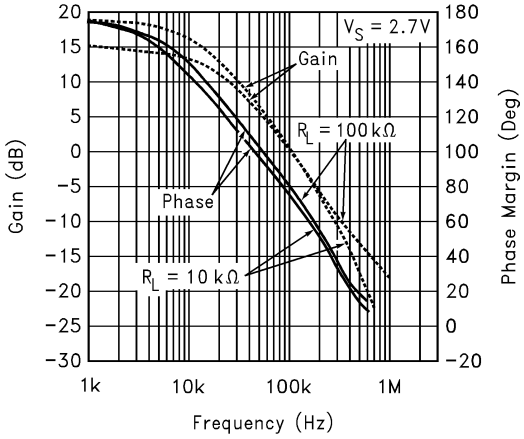


Figure 20. Open-Loop Frequency Response

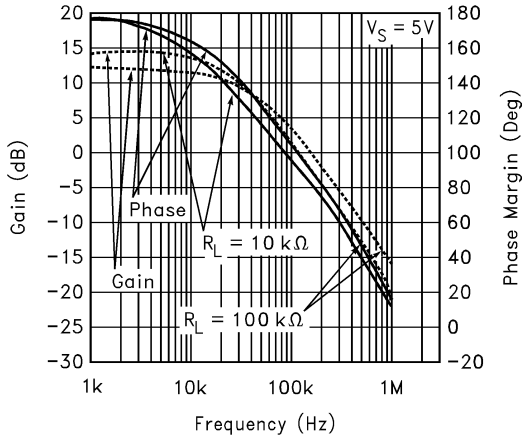


Figure 21. Open-Loop Frequency Response

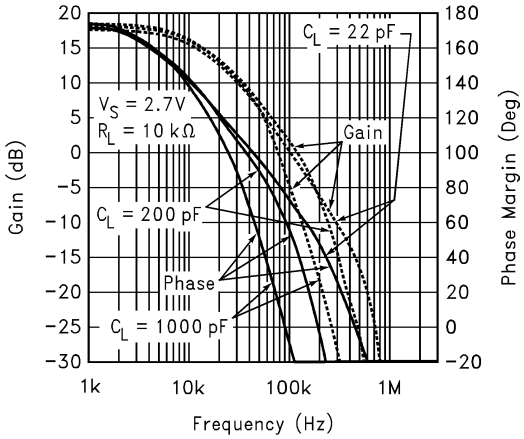


Figure 22. Gain and Phase vs Capacitive Load

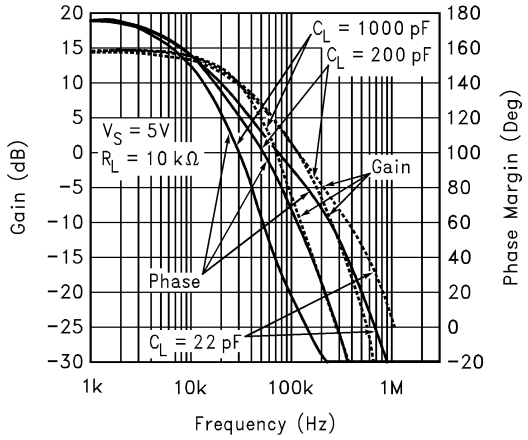


Figure 23. Gain and Phase vs Capacitive Load

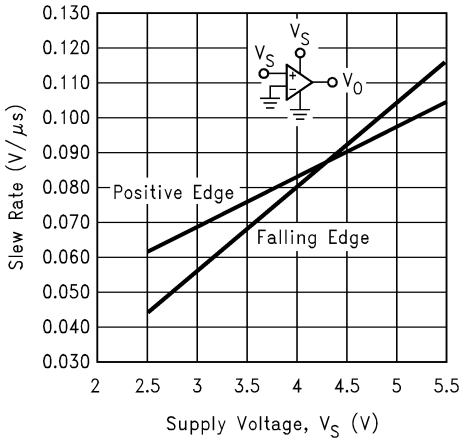


Figure 24. Slew Rate vs Supply Voltage

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

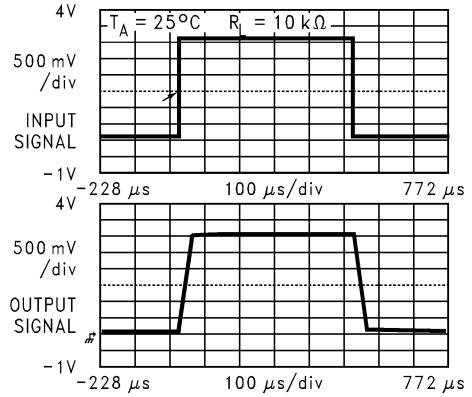


Figure 25. Noninverting Large Signal Pulse Response

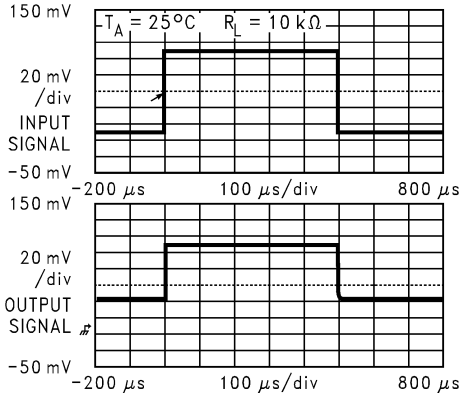


Figure 26. Noninverting Small Signal Pulse Response

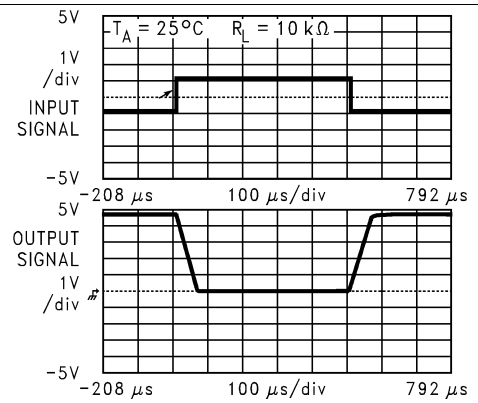


Figure 27. Inverting Large Signal Pulse Response

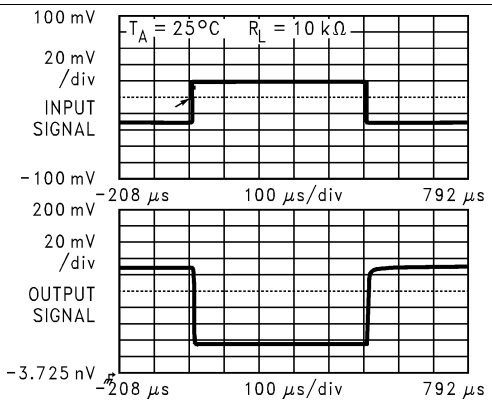


Figure 28. Inverting Small Signal Pulse Response

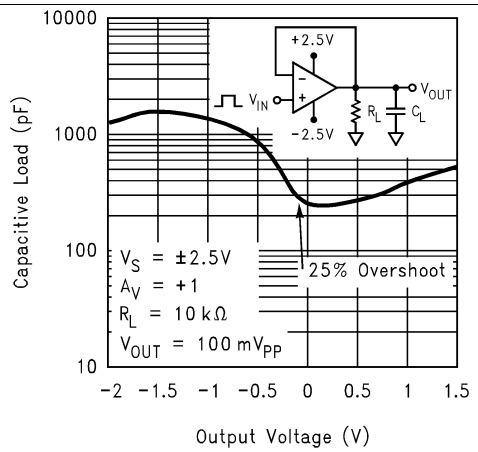


Figure 29. Stability vs Capacitive Load

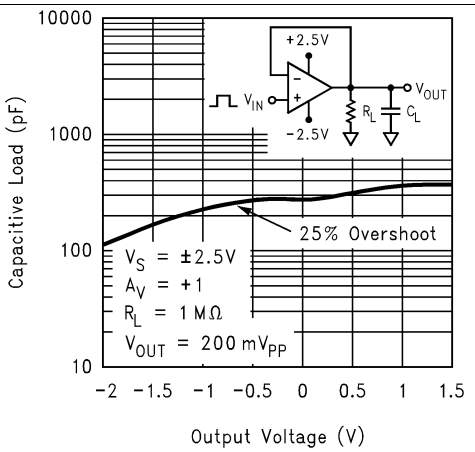


Figure 30. Stability vs Capacitive Load

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

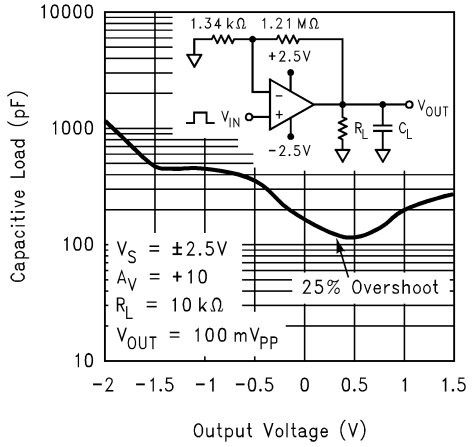


Figure 31. Stability vs Capacitive Load

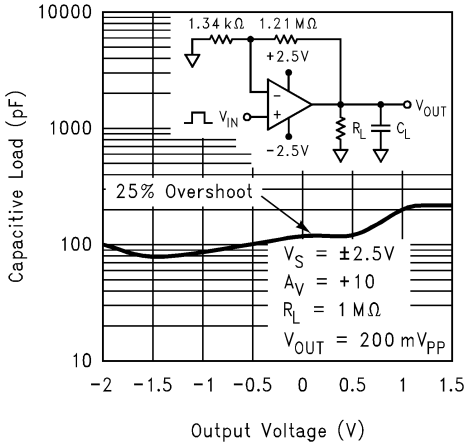


Figure 32. Stability vs Capacitive Load

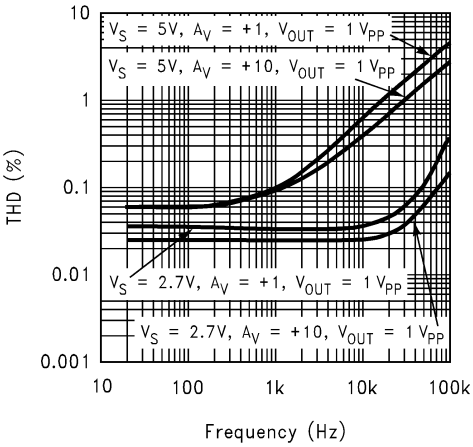


Figure 33. THD vs Frequency

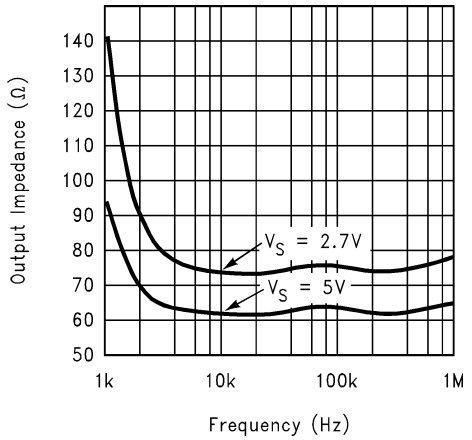


Figure 34. Open-Loop Output Impedance vs Frequency

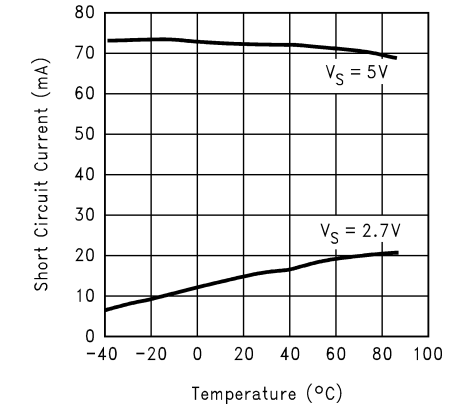


Figure 35. Short Circuit Current vs Temperature (Sinking)

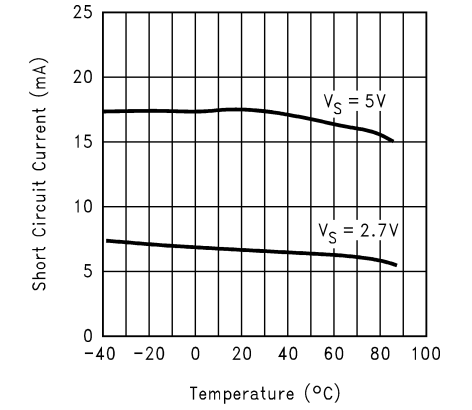


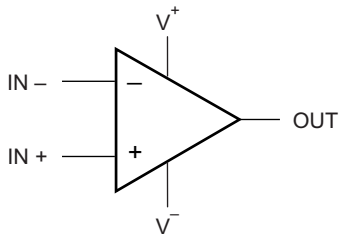
Figure 36. Short Circuit Current vs Temperature (Sourcing)

7 Detailed Description

7.1 Overview

The LPV321-N, LPV358-N, and LPV324-N devices are micropower (10-µA) versions of the popular LMV3xx-N. The LPV321-N is the single-channel version. The LPV358-N is the dual, and the LPV324-N is the quad. The LPV32x-N are the most cost effective solution for applications where low power and low voltage operation, space efficiency, and low-price are important. The LPV3x-N have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed to power ratio, achieving 152 kHz of bandwidth and 0.1-V/µs slew rate with 10 mA of supply current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Size

The small footprints of the LPV3xx-N packages save space on printed circuit boards, and enable the design of smaller electronic products (such as cellular phones, pagers, or other portable systems). The low profile of the LPV3xx-N make them possible to use in PCMCIA type III cards.

7.3.2 Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the LPV3xx-N can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

7.3.3 Simplified Board Layout

These products help avoid using long printed-circuit traces in the PCB. This means no additional components, such as capacitors and resistors, are needed to filter out unwanted signals due to the interference between the long printed-circuit traces.

7.3.4 Low Supply Current

These devices help maximize battery life. They are ideal for battery powered systems.

7.3.5 Low Supply Voltage

TI provides ensured performance at 2.7 V and 5 V. These specifications ensure operation throughout the battery lifetime.

7.3.6 Rail-to-Rail Output

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low-supply voltages.

Feature Description (continued)

7.3.7 Input Includes Ground

Allows direct sensing near GND in single supply operation.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

7.4 Device Functional Modes

The LPV3xx-N can be operated as a single-supply or a dual-supply operational amplifier depending on the application.

7.4.1 Capacitive Load Tolerance

The LPV3xx-N can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, circuit in Figure 37 can be used.

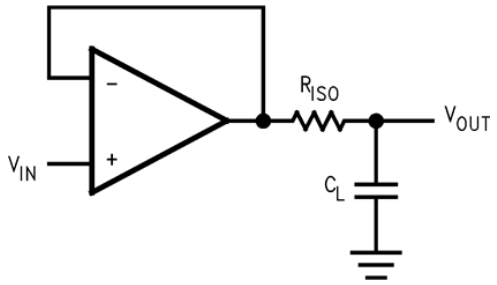


Figure 37. Indirectly Driving A Capacitive Load Using Resistive Isolation

In Figure 37, the isolation resistor (R_{ISO}) and the load capacitor (C_L) form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} is. Figure 38 is an output waveform of Figure 37 using 100 kΩ for R_{ISO} and 1000 pF for C_L.

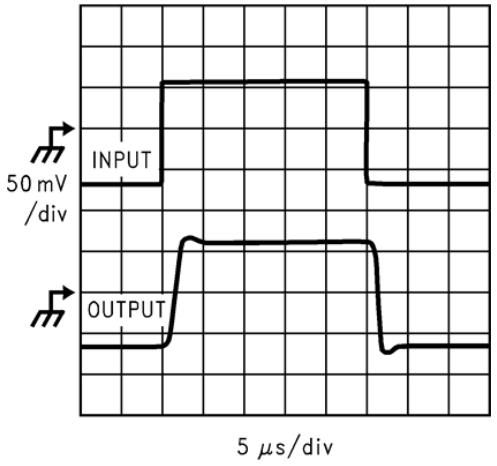


Figure 38. Pulse Response of the LPV324 Circuit in Figure 37

Device Functional Modes (continued)

The circuit in Figure 39 is an improvement to the one in Figure 37 because it provides DC accuracy as well as AC stability. If there were a load resistor in Figure 37, the output would be voltage divided by R_{ISO} and the load resistor. Instead, in Figure 39, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. Caution is needed in choosing the value of R_F due to the input bias current of the LPV3xx-N. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F. This in turn slows down the pulse response.

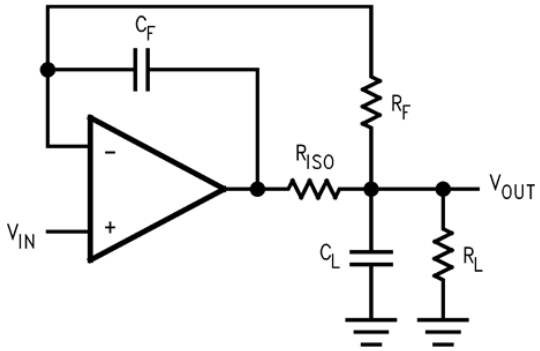


Figure 39. Indirectly Driving A Capacitive Load With DC Accuracy

7.4.2 Input Bias Current Cancellation

The LPV3xx-N family has a bipolar input stage. The typical input bias current of LPV3xx-N is 1.5 nA with 5-V supply. Thus a 100-kΩ input resistor causes 0.15 mV of error voltage. By balancing the resistor values at both inverting and noninverting inputs, the error caused by the amplifier's input bias current is reduced. The circuit in Figure 40 shows how to cancel the error caused by input bias current.

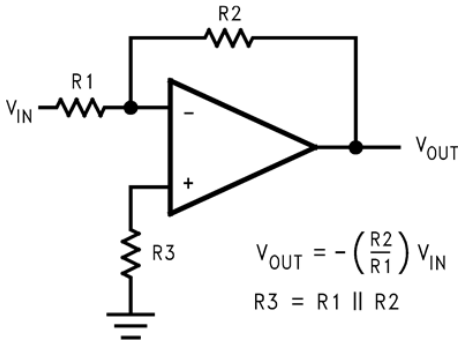


Figure 40. Cancelling the Error Caused by Input Bias Current

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LPV3xx-N family of amplifiers is specified for operation from 2.7 V to 5 V (±1.35 V to ±2.5 V). Many of the specifications apply from –40°C to 125°C. They provide ground-sensing inputs as well as rail-to-rail output swing. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

8.2 Typical Applications

8.2.1 Simple Low-Pass Active Filter

A simple low-pass filter is shown in Figure 41.

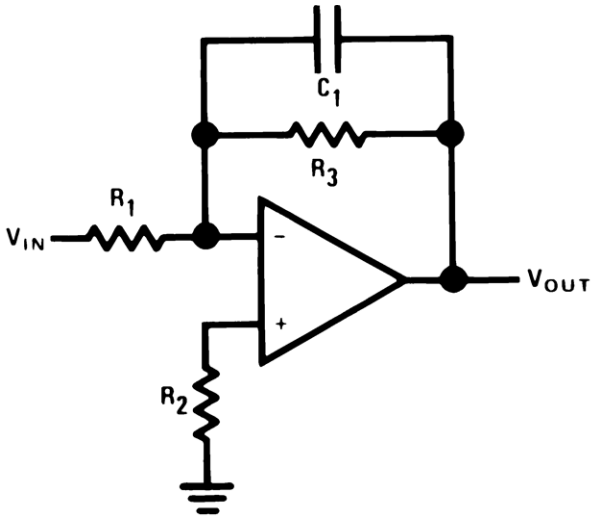


Figure 41. Simple Low-Pass Active Filter Schematic

8.2.1.1 Design Requirements

The low-pass filter is shown in Figure 41 passes low frequencies and attenuate frequencies above corner frequency (fc) at a roll-off rate of 20 dB/Decade.

8.2.1.2 Detailed Design Procedure

The low-frequency gain ($\omega \rightarrow o$) is defined by $-R_3/R_1$. This allows low-frequency gains other than unity to be obtained. The filter has a −20 dB/decade roll-off after its corner frequency fc. R_2 must be chosen equal to the parallel combination of R_1 and R_3 to minimize errors due to bais current. The frequency response of the filter is shown in Figure 42.

$$A_L = -\frac{R_3}{R_1}$$

$$f_c = \frac{1}{2\pi R_3 C_1}$$

$$R_2 = R_1 \,\text{II}\, R_3 \quad (1)$$

Typical Applications (continued)

Note that the single op amp active filters are used in to the applications that require low quality factor, Q (≤ 10), low frequency (≤ 5 kHz), and low gain (≤ 10), or a small value for the product of gain times Q (≤ 100). The op amp must have an open loop voltage gain at the highest frequency of interest at least 50 times larger than the gain of the filter at this frequency. In addition, the selected op amp must have a slew rate that meets the requirements in Equation 2.

$$\text{Slew Rate} \geq 0.5 \times (\omega_H V_{OPP}) \times 10^{-6} \text{V/µsec} \quad (2)$$

where

- ω_H is the highest frequency of interest
- V_{OPP} is the output peak-to-peak voltage

8.2.1.3 Application Curve

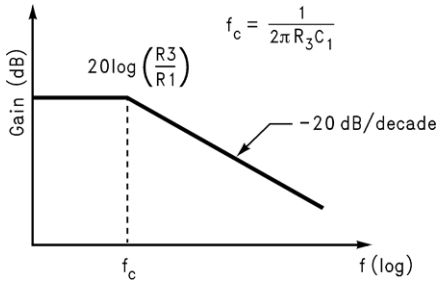


Figure 42. Frequency Response of Simple Low-pass Active Filter

8.2.2 Difference Amplifier

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier in making a differential to single-ended conversion or in rejecting a common mode signal.

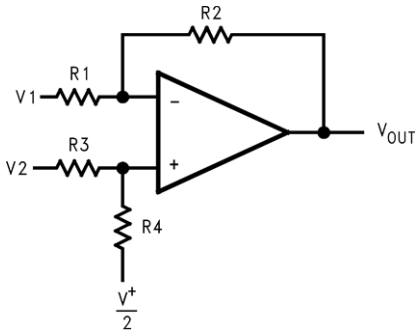


Figure 43. Difference Amplifier Schematic

$$V_{OUT} = \left(\frac{R1+R2}{R3+R4}\right)\frac{R4}{R1}V_2 - \frac{R2}{R1}V_1 + \left(\frac{R1+R2}{R3+R4}\right)\frac{R3}{R1} \times \frac{V^+}{2}$$

for $R1 = R3$ and $R2 = R4$

$$V_{OUT} = \frac{R2}{R1}(V_2 - V1) + \frac{V^+}{2} \quad (3)$$

8.2.3 Instrumentation Circuits

The input impedance of the previous difference amplifier is set by the resistor R_1, R_2, R_3, and R_4. To eliminate the problems of low input impedance, one way is to use a voltage follower ahead of each input as shown in the following two instrumentation amplifiers.

Typical Applications (continued)

8.2.3.1 Three Operating Amplifier Instrumentation

The quad LPV324 can be used to build a three-op-amp instrumentation amplifier as shown in Figure 44

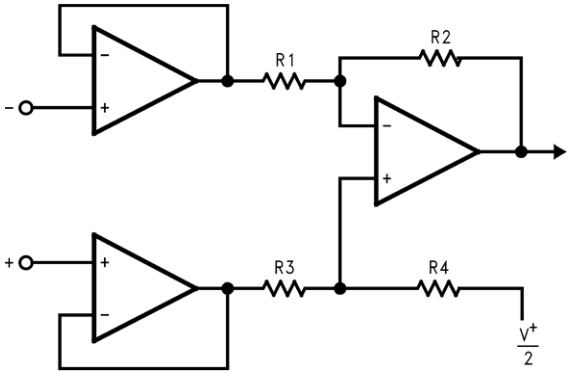


Figure 44. Three-op-amp Instrumentation Amplifier Schematic

The first stage of this instrumentation amplifier is a differential-input, differential-output amplifier, with two voltage followers. These two voltage followers assure that the input impedance is over 100 MΩ. The gain of this instrumentation amplifier is set by the ratio of R_2/R_1. R_3 should equal R_1 and R_4 equal R_2. Matching of R_3 to R_1 and R_4 to R_2 affects the CMRR. For good CMRR over temperature, low drift resistors should be used. Making R_4 Slightly smaller than R_2 and adding a trim pot equal to twice the difference between R_2 and R_4 will allow the CMRR to be adjusted for optimum.

8.2.3.2 Two Operating Amplifier Instrumentation

A two-op-amp instrumentation amplifier can also be used to make a high-input-impedance DC differential amplifier (Figure 45). As in the three-op-amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR. R_4 should equal to R_1 and R_3 must equal R_2.

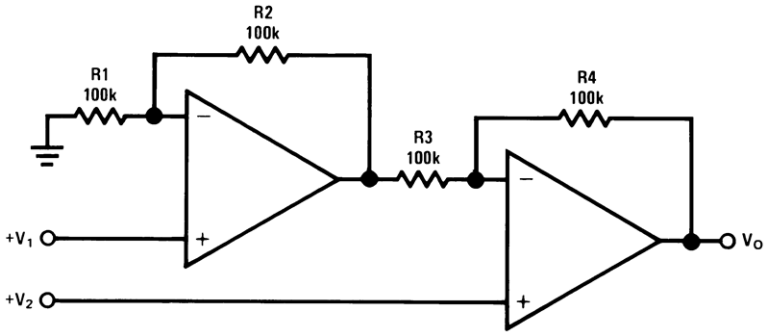


Figure 45. Two-op-amp Instrumentation Amplifier Schematic

$$V_O = \left(1 + \frac{R4}{R3}\right)(V_2 - V_1), \text{where } R1 = R4 \text{ and } R2 = R3$$

$$\text{As shown}: V_O = 2(V_2 - V_1) \quad (4)$$

8.2.3.3 Single-Supply Inverting Amplifier

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using R_3 and R_4 is implemented to bias the amplifier so the input signal is within the input common-common voltage range of the amplifier. The capacitor C_1 is placed between the inverting input and resistor R_1 to block the DC signal going into the AC signal source, V_{IN}. The values of R_1 and C_1 affect the cutoff frequency in Equation 5.

$$fc = 1/2\pi R_1 C_1 \quad (5)$$

Typical Applications (continued)

As a result, the output signal is centered around mid-supply (if the voltage divider provides $V^+/2$ at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.

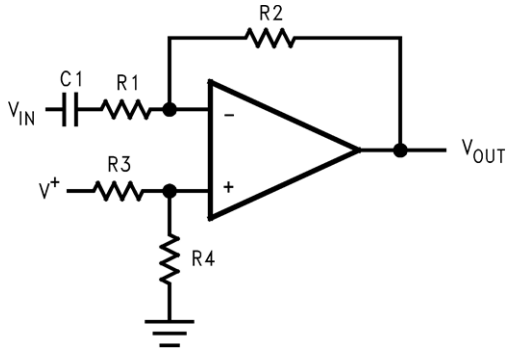


Figure 46. Single-Supply Inverting Amplifier

$$V_{OUT} = -\frac{R2}{R1} V_{IN} \quad (6)$$

9 Power Supply Recommendations

The LPV3xx-N is specified for operation from 2.7 V to 5.5 V; many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

For best operational performance, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Figure 47.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

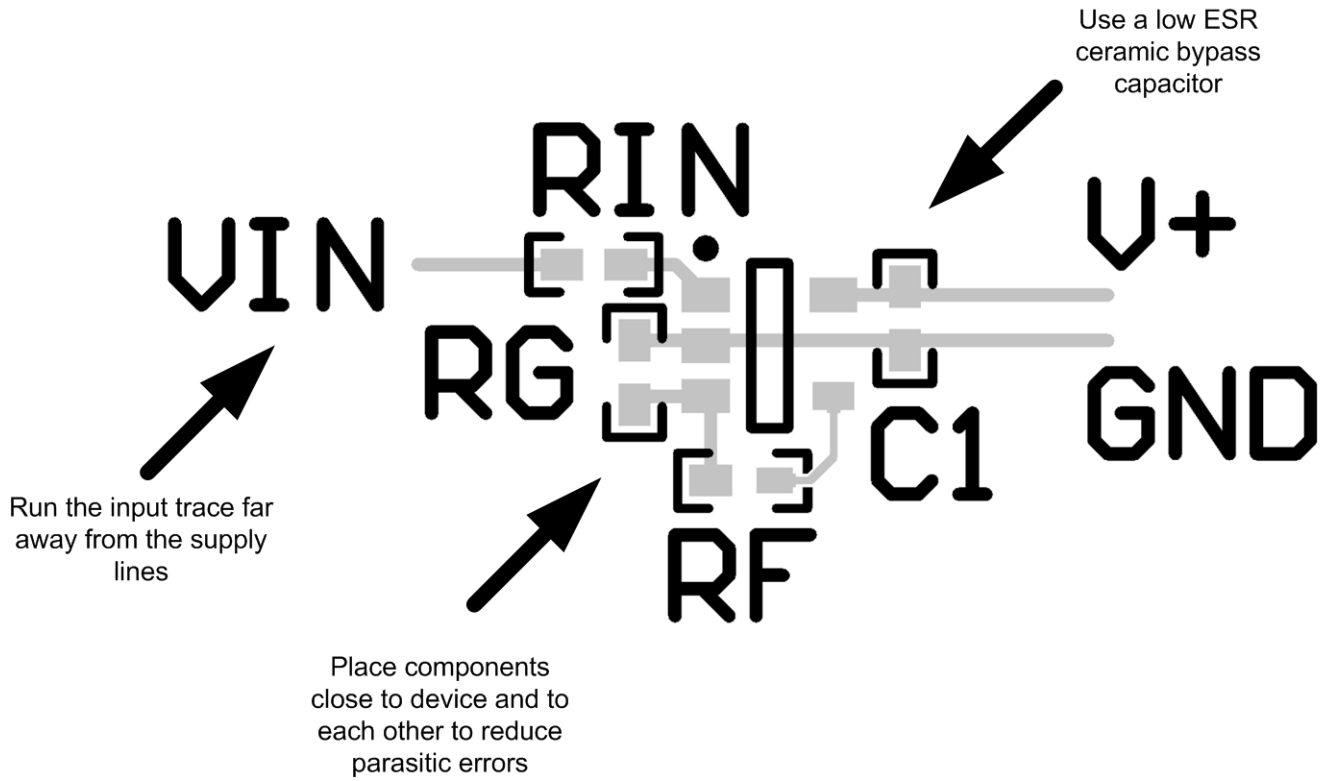


Figure 47. Operational Amplifier Board Layout for Noninverting Configuration

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

- LPV321-N PSPICEモデル(SNOM026)
- LPV358-N PSPICEモデル(SNOM022)
- LPV324-N PSPICEモデル(SNOM027)
- TINA-TI SPICEベースのアナログ・シミュレーション・プログラム
- DIP アダプタ評価モジュール
- TIユニバーサル・オペアンプ評価モジュール
- TI Filterproソフトウェア

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『オペアンプ・アプリケーション・ハンドブック』*(SBOA092)
- *『トランスインピーダンス・アンプの直感的な補正』*SBOA055
- *『基板のレイアウト技法』*(SLOA089)
- *『AN-1803 トランスインピーダンス・アンプ設計の考慮事項』*(SNOA515)

11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LPV321-N	ここをクリックしてください	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LPV324-N	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LPV358-N	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV321M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A27A	Samples
LPV321M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A27A	Samples
LPV321M7/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A19	Samples
LPV321M7X/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A19	Samples
LPV324M/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LPV324M	Samples
LPV324MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LPV324 MT	Samples
LPV324MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LPV324 MT	Samples
LPV324MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LPV324M	Samples
LPV358M/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LPV 358M	Samples
LPV358MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	P358	Samples
LPV358MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	P358	Samples
LPV358MX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LPV 358M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

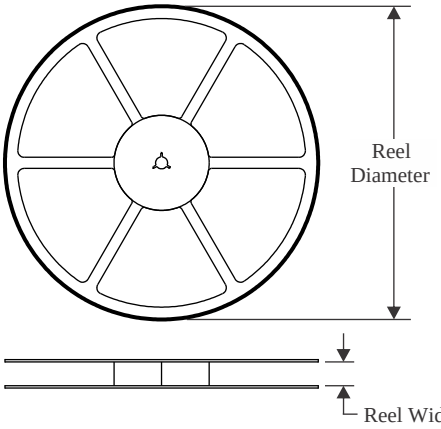
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

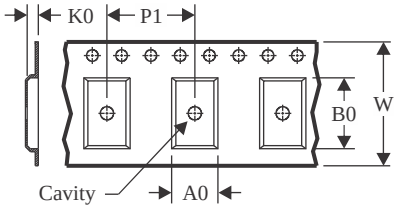
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

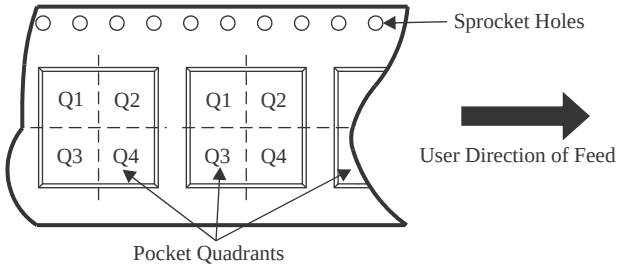


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

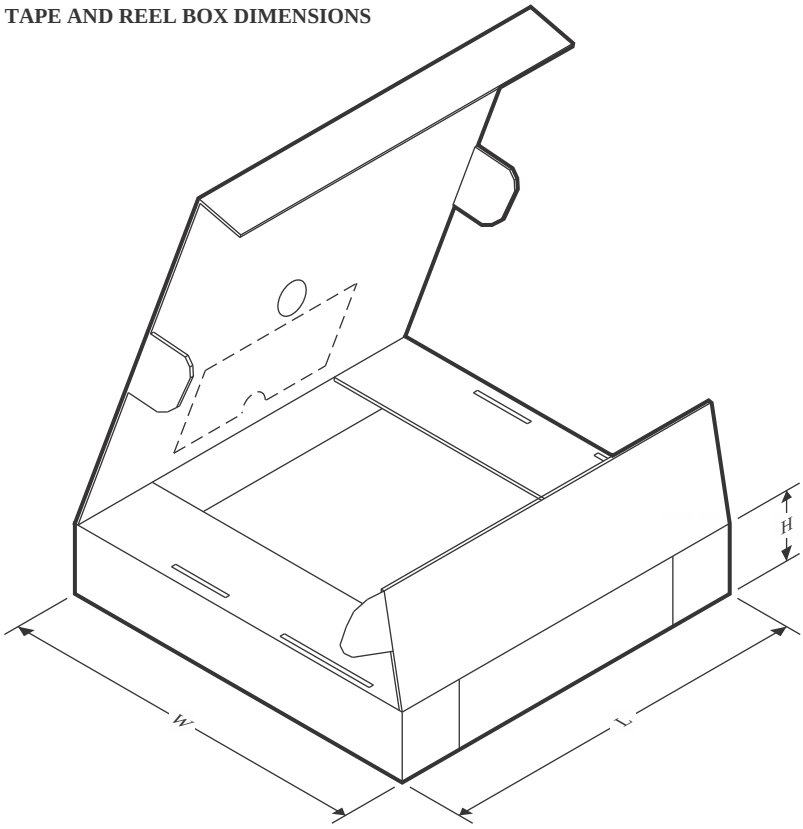
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV321M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV321M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV321M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV321M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV324MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LPV324MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LPV358MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

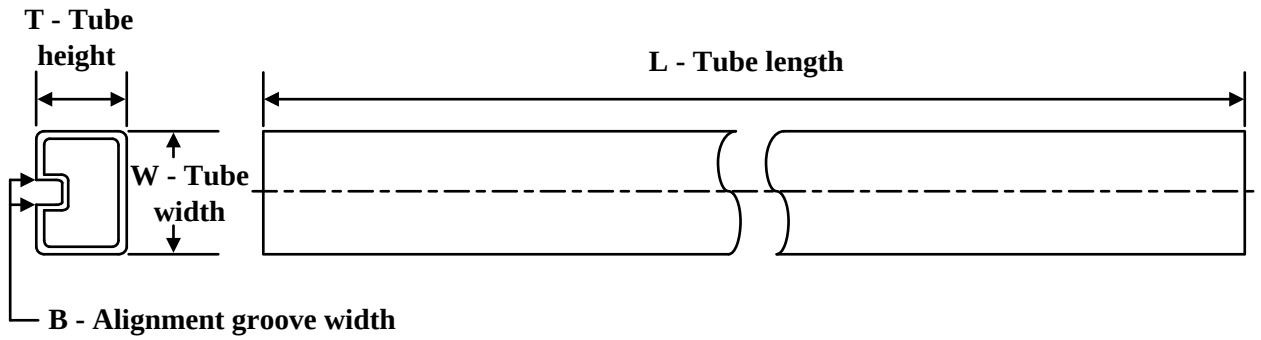
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

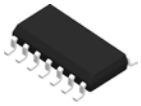
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV321M5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LPV321M5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LPV321M7/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LPV321M7X/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LPV324MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LPV324MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LPV358MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LPV358MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LPV358MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LPV324M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LPV324MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LPV358M/NOPB	D	SOIC	8	95	495	8	4064	3.05

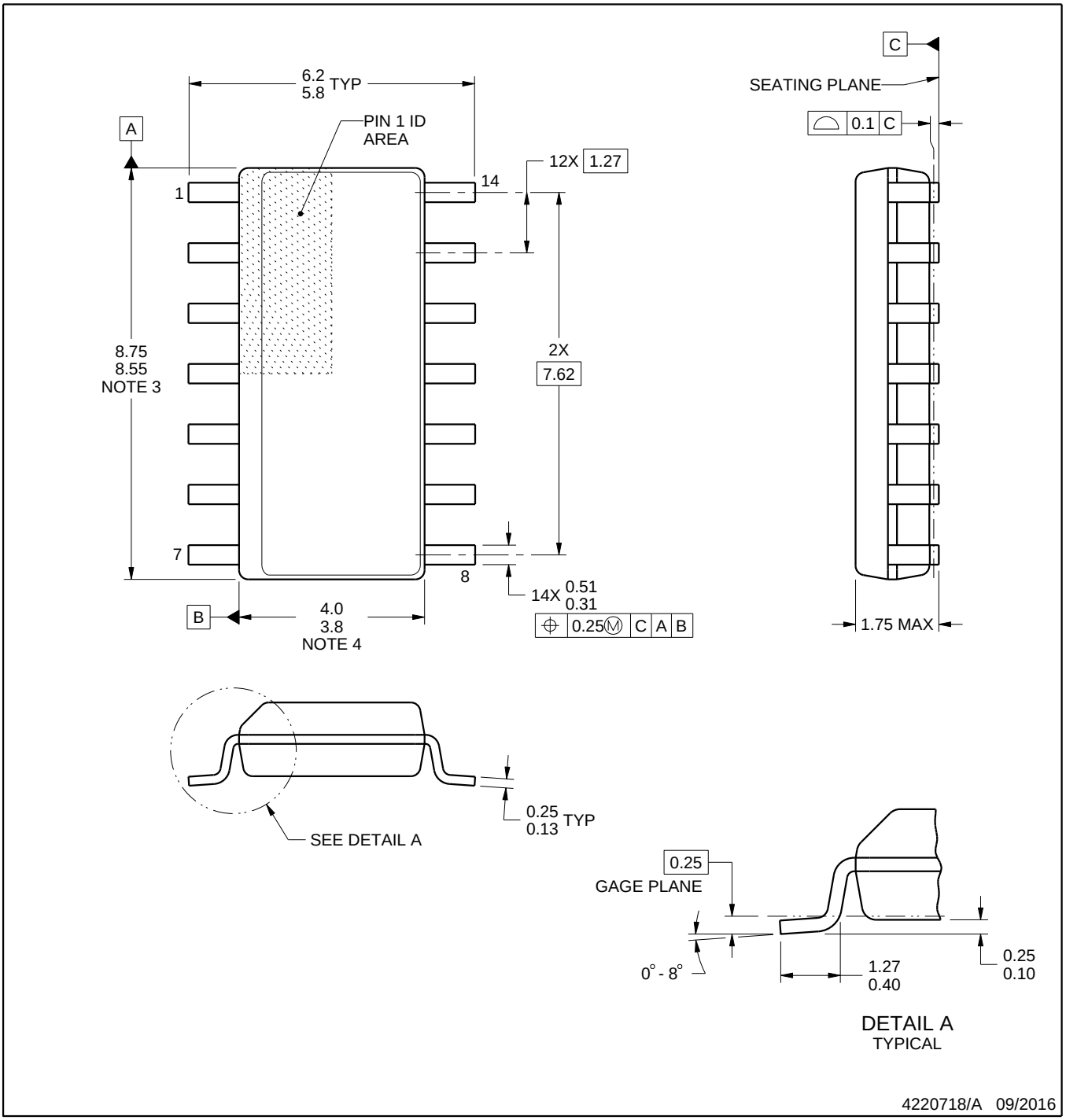


PACKAGE OUTLINE

D0014A

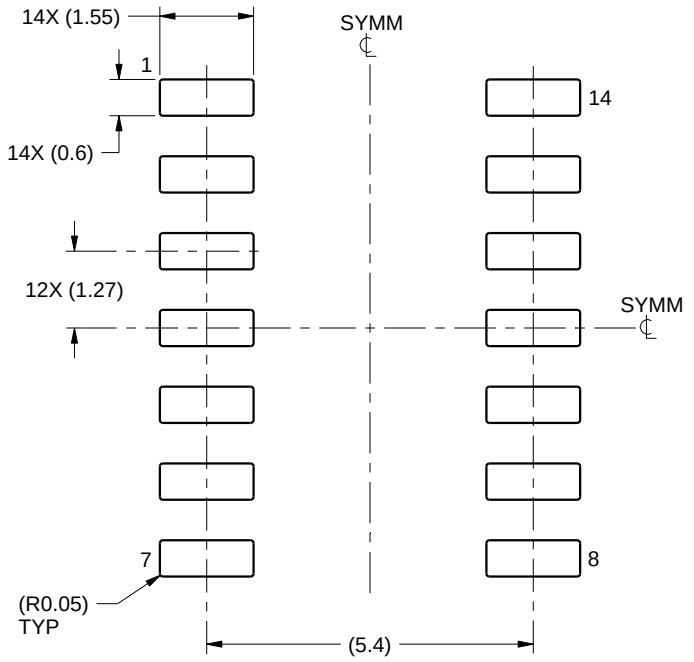
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

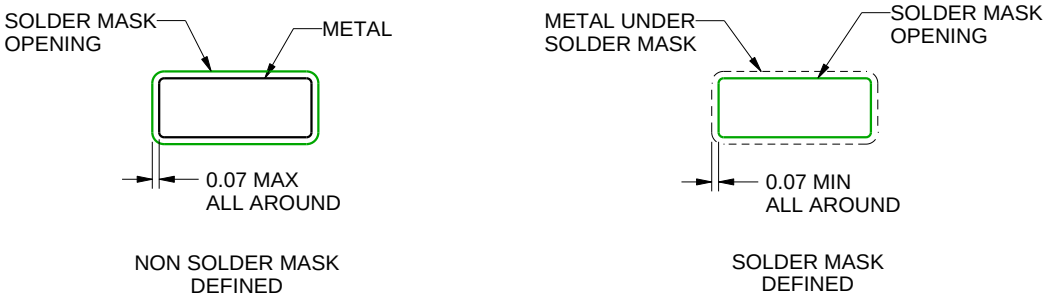


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

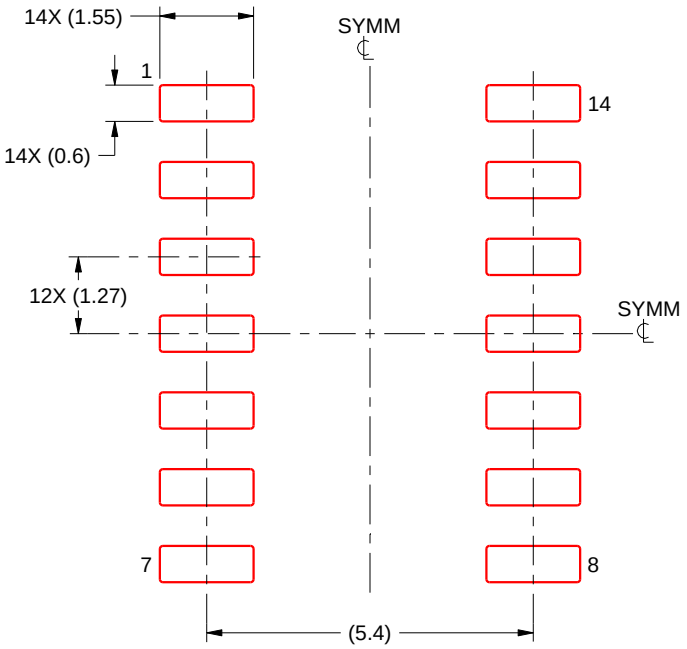
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

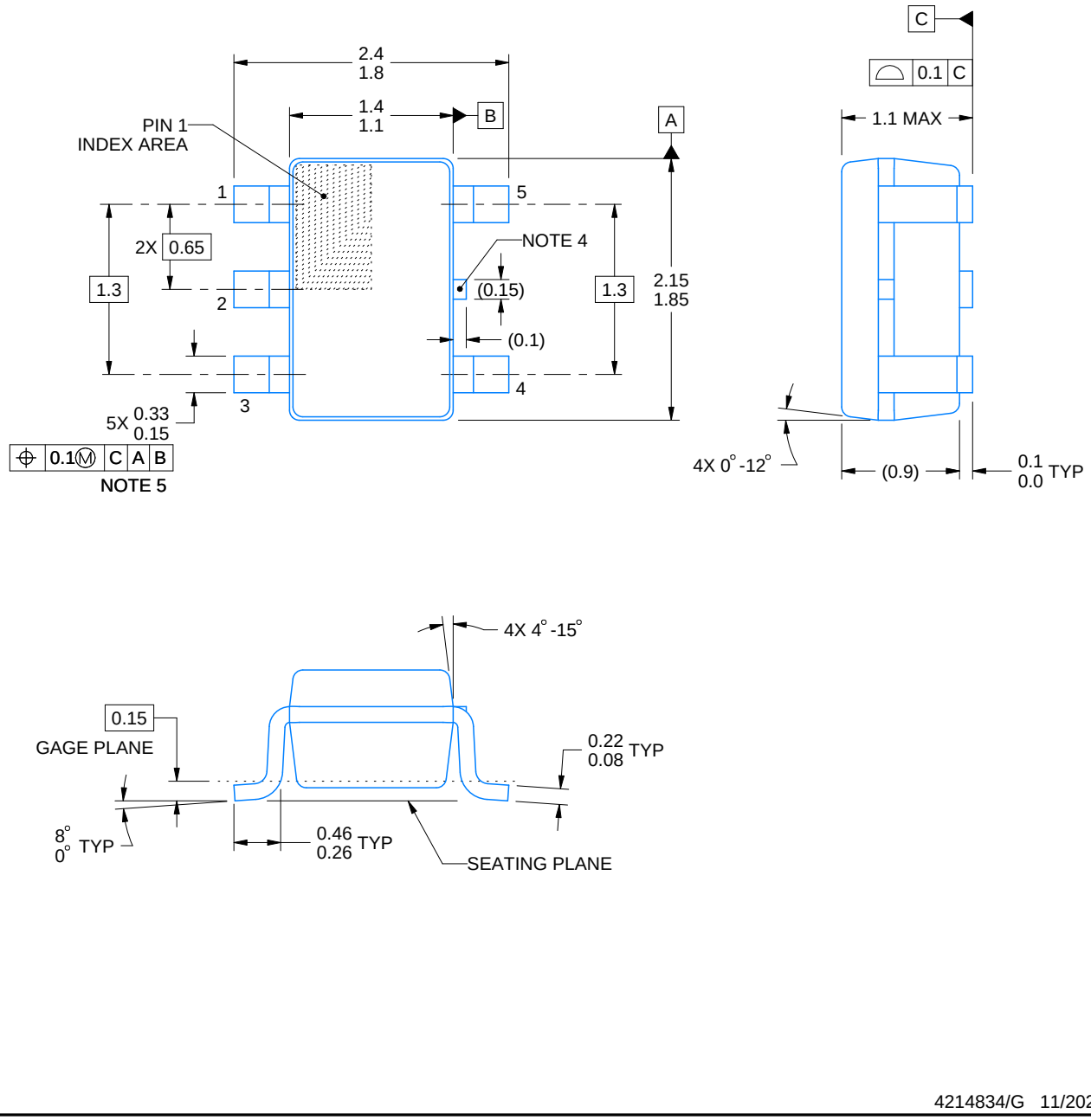
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

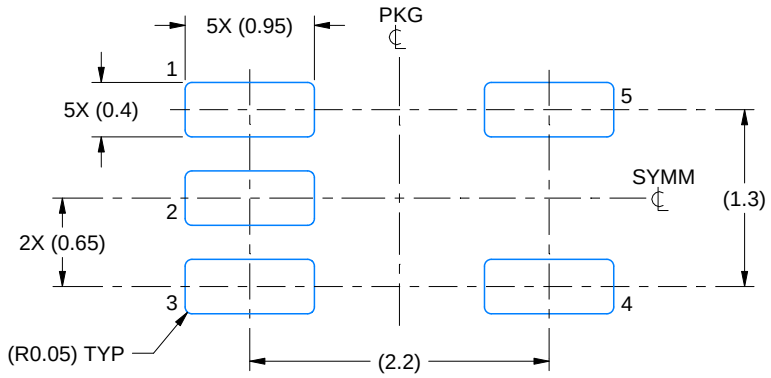
SMALL OUTLINE TRANSISTOR



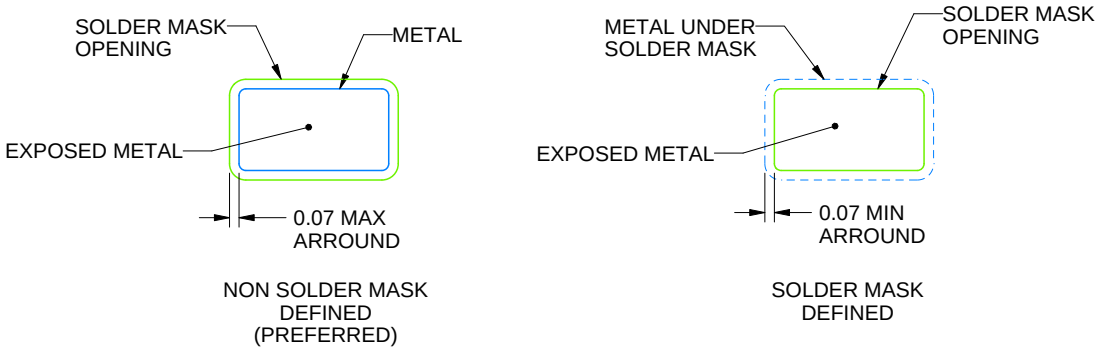
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

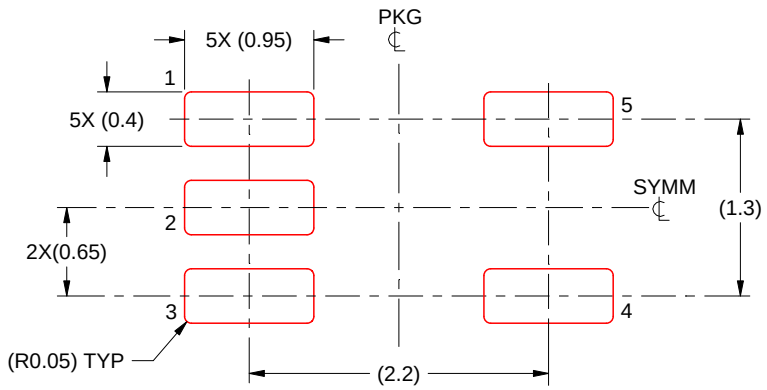


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

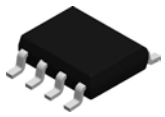


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

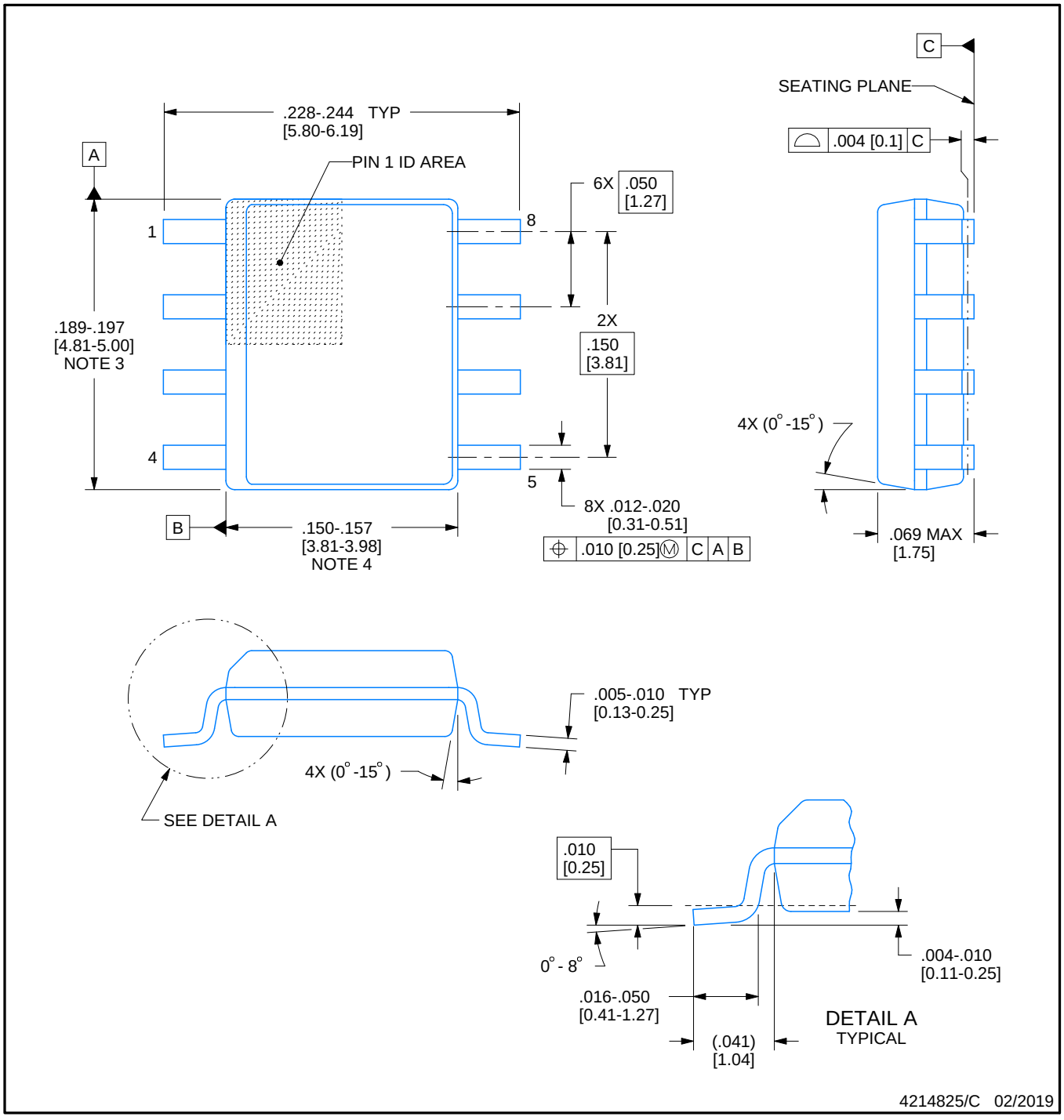


PACKAGE OUTLINE

D0008A

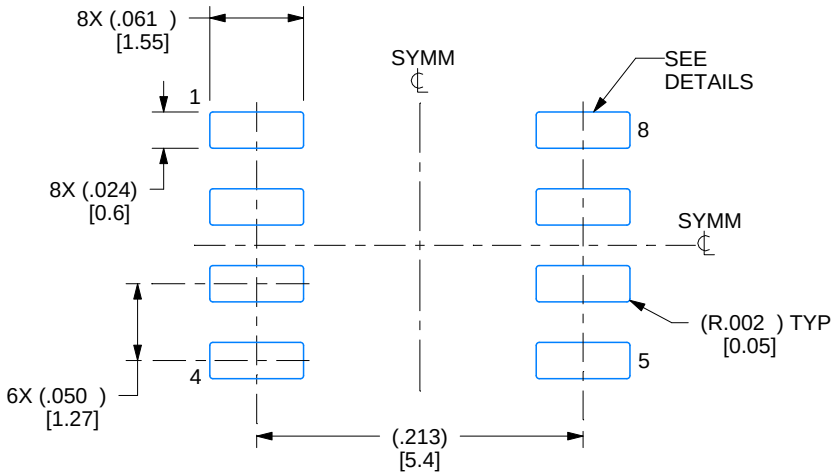
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

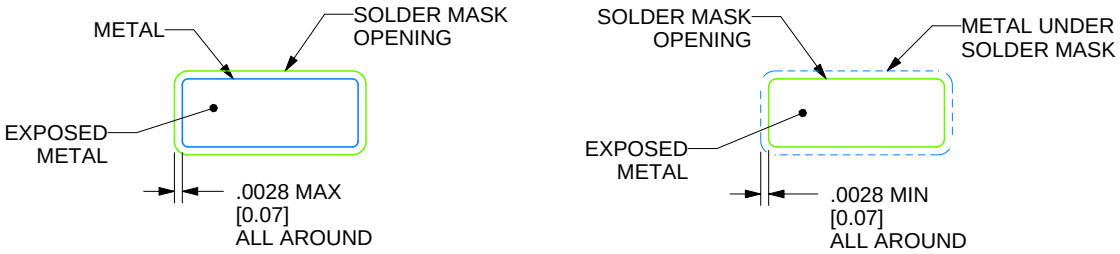


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

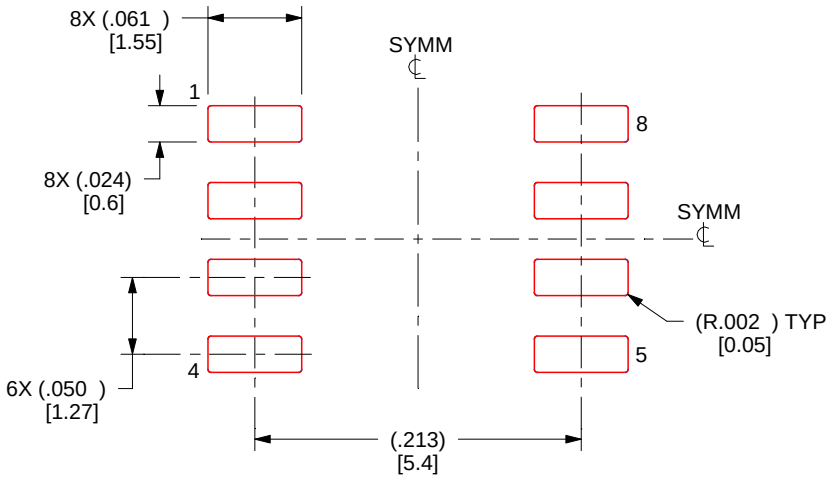
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

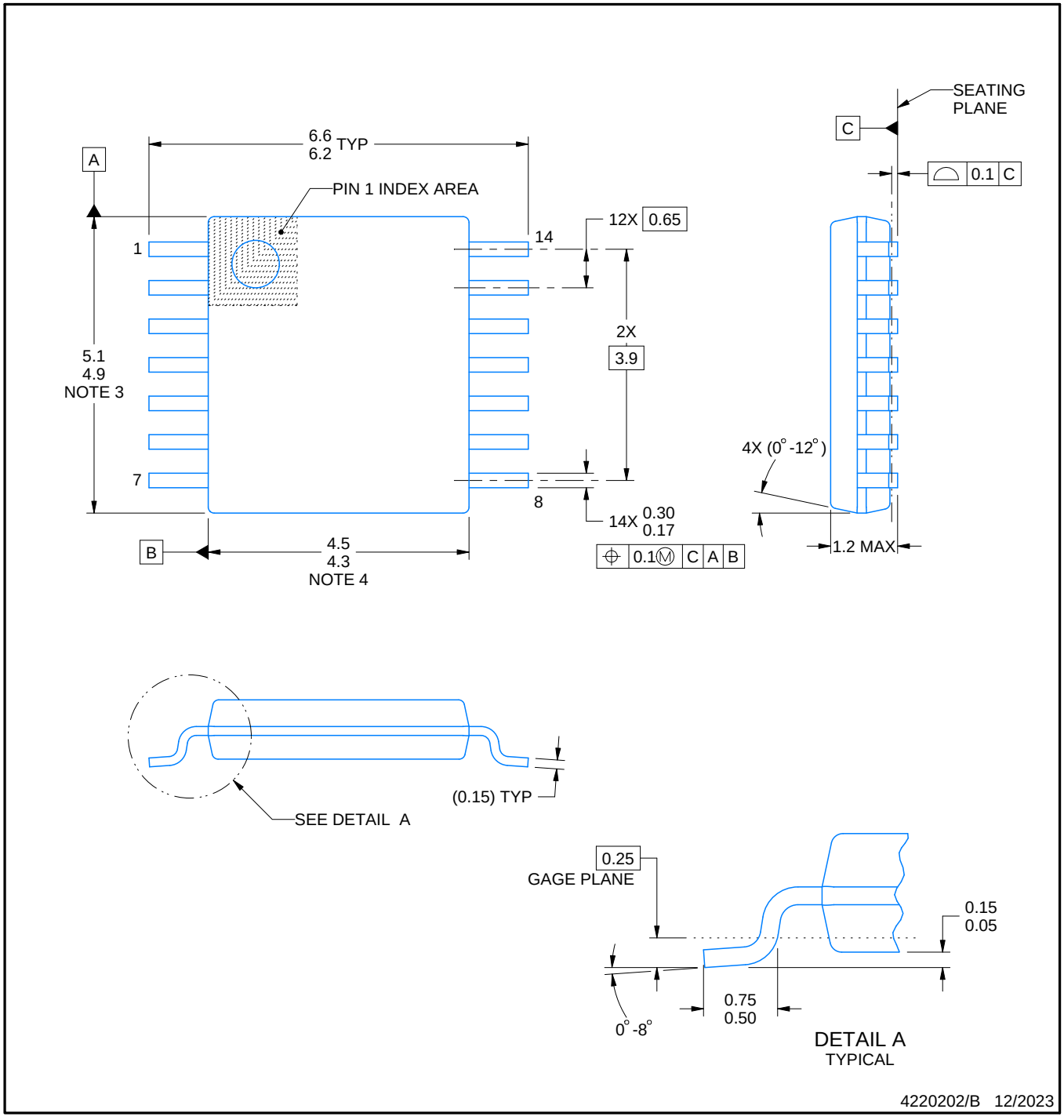
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

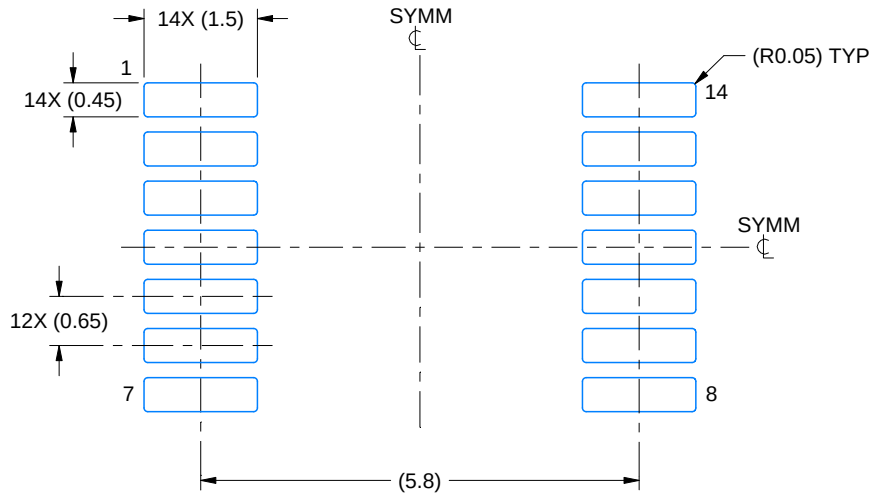
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

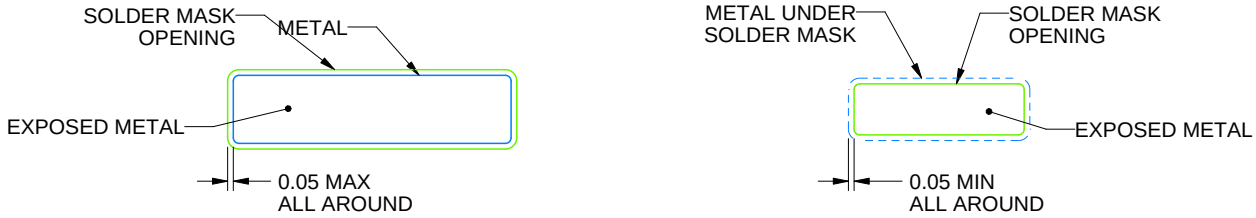


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

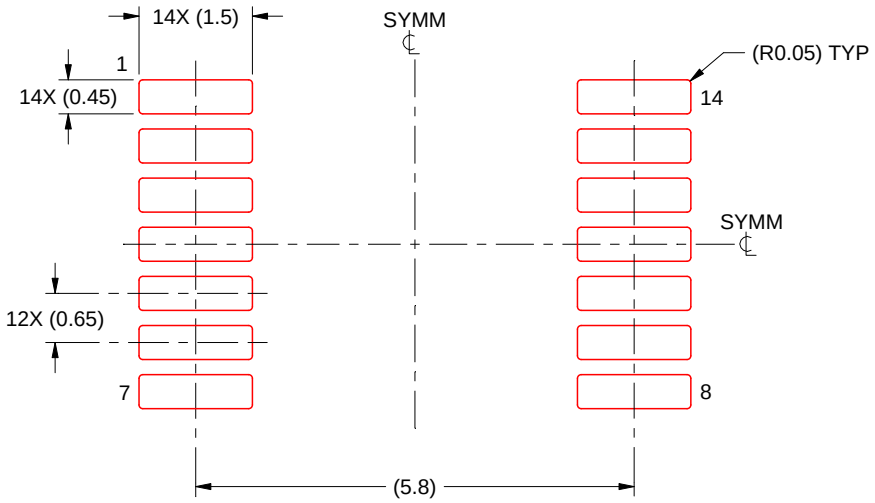


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

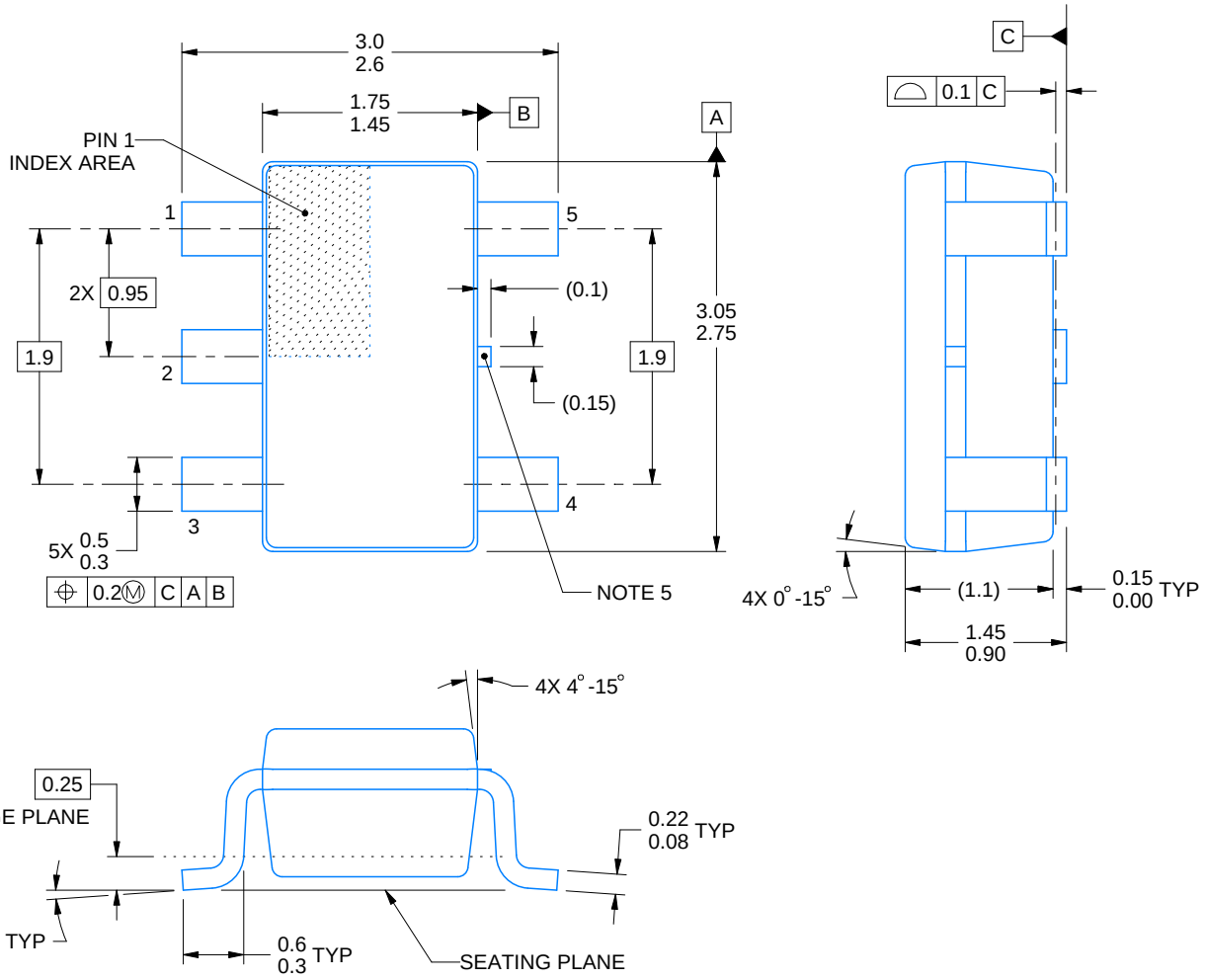
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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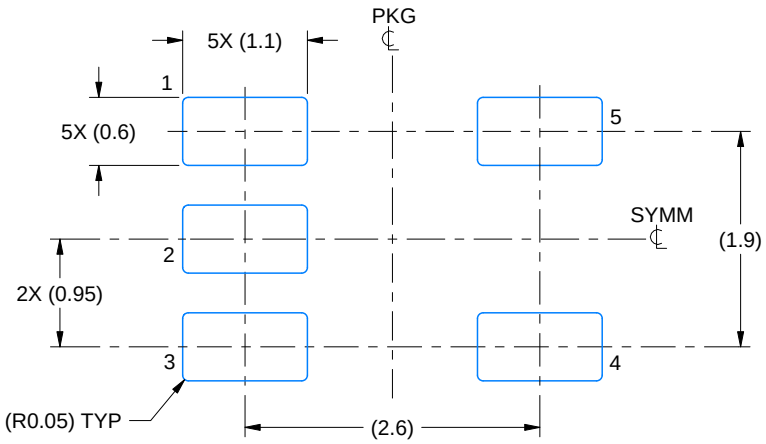
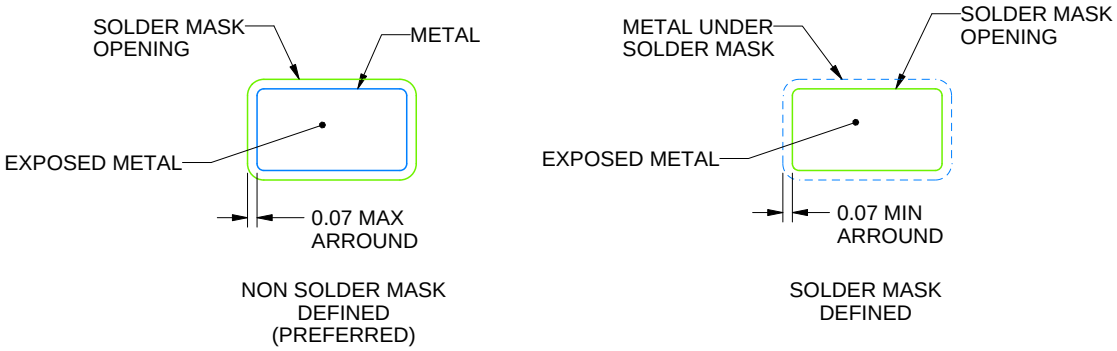
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

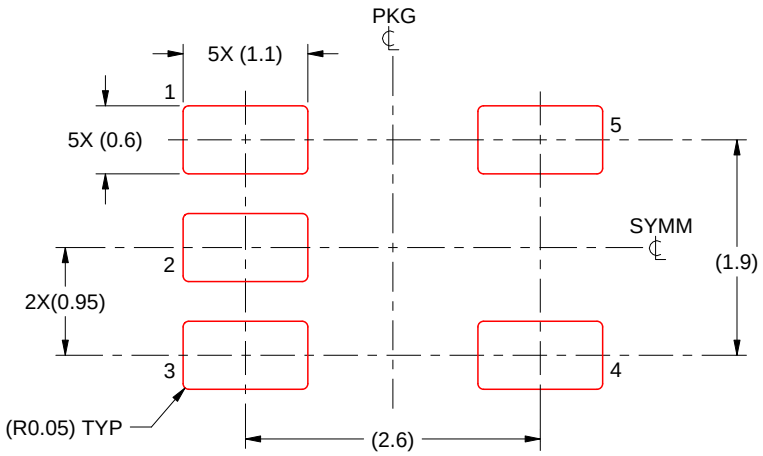


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

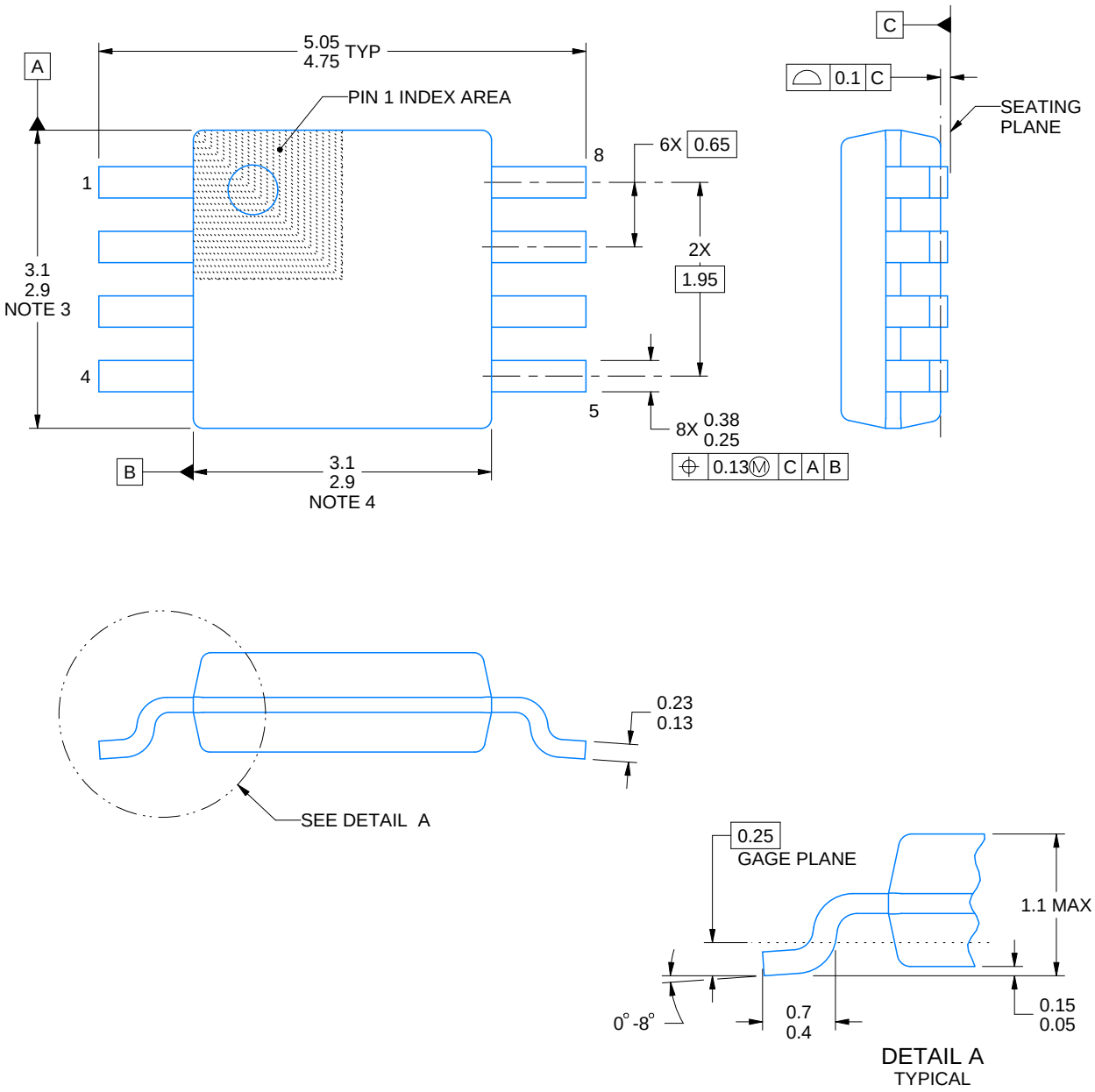
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

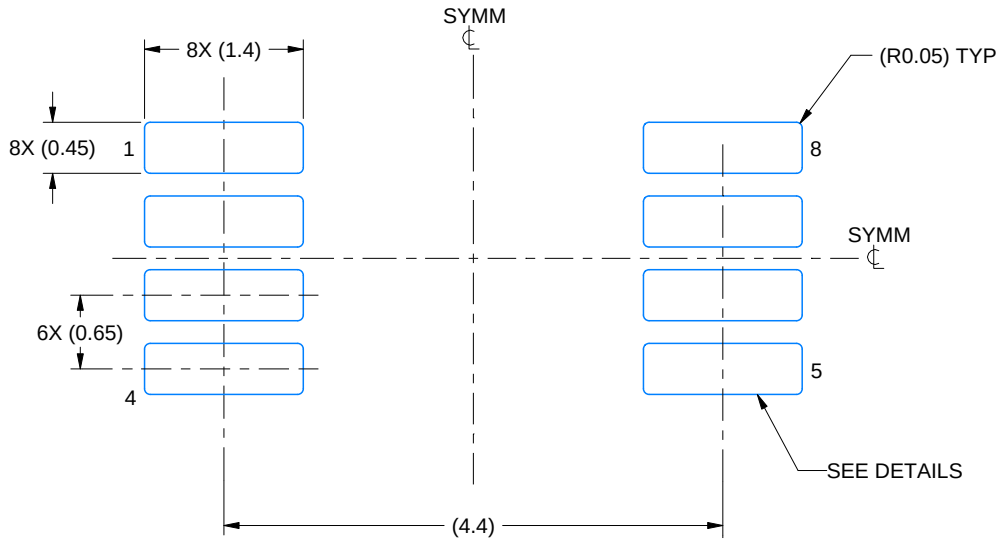
SMALL OUTLINE PACKAGE



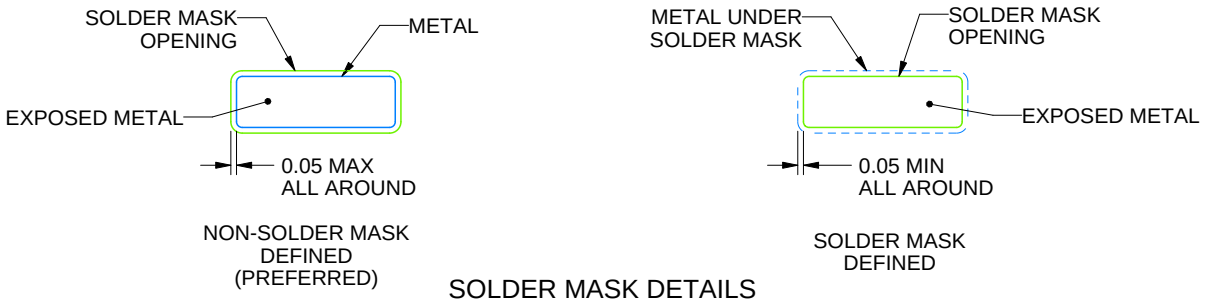
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

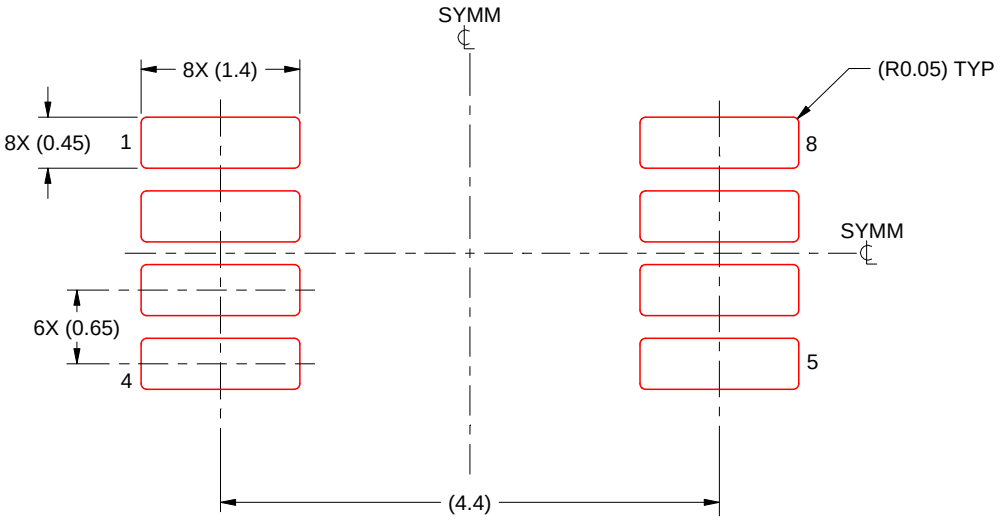


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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