参考資料

LPV511 Micropower、レール・ツー・レール入出力オペアンプ

1 特長

- 広い電源電圧範囲: 2.7V～12V
- スルーレート: 7.7V/ms
- 消費電流: 880nA
- 出力短絡電流: 1.35mA
- レール・ツー・レール入力
- レール・ツー・レール出力: 電源レールから100mV
- 帯域幅(C_L = 50pF、R_L = 1MΩ): 27kHz
- ユニティ・ゲインで安定

2 アプリケーション

- バッテリ駆動のシステム
- セキュリティ・システム
- Micropowerサーモスタット
- 太陽電池で動作するシステム
- 携帯機器
- Micropowerフィルタ
- リモート・センサ・アンプ

3 概要

LPV511は、2.7V～12Vの広い電源電圧範囲で動作するMicropowerオペアンプであり、3V、5V、12Vでの仕様が保証されています。LPV511は非常に消費電力が低く、卓越した速度/電力比を示し、27kHzの帯域幅でわずか880nAの電流しか消費しません。これらの仕様から、LPV511は計測機器、センサの条件設定、バッテリ電流監視など、バッテリ駆動で、長時間動作のため低い消費電流が要求されるシステムに理想的です。

LPV511の入力範囲には、グランドと、ハイサイドのバッテリ・センシング・アプリケーションの両方の電源レールが含まれています。LPV511の出力は、どちらのレールからも100mVの範囲内でスイングでき、電源電圧の低いアプリケーションにおいて信号のダイナミック・レンジを最大化できます。さらに、出力は12Vバッテリによる駆動の場合、650µAの電流を供給できます。

LPV511は、TIの先進のVIP50Cプロセスで製造されます。

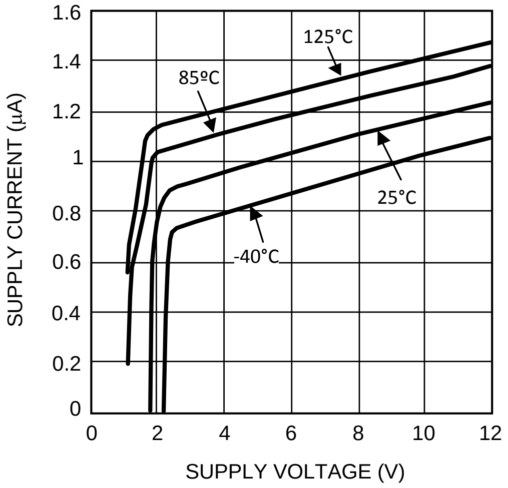
LPV511は省スペースのSC70パッケージで供給されるため、PCボードのサイズが制限される携帯用電子機器に理想的です。

製品情報(1)

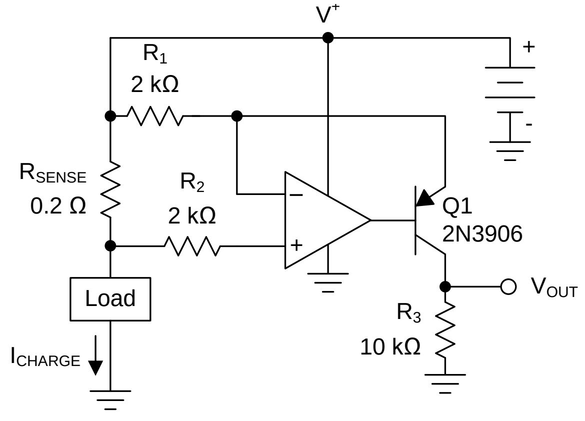
型番	パッケージ	本体サイズ(公称)
LPV511	SC70 (5)	2.00mm×1.25mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

標準消費電流



ハイサイド・バッテリ・電流センサ



$$V_{OUT} = \frac{R_{SENSE} \times R_3}{R_1} \times I_{CHARGE} = 1\Omega \times I_{CHARGE}$$

目次

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (March 2013) から Revision D に変更 **Page**

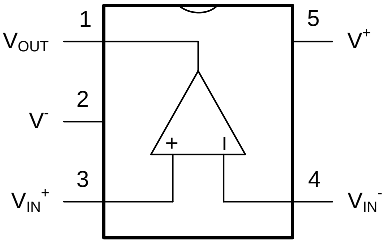
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージング、および注文情報*」セクション 追加 ... 1
- Added *Thermal Information* table ... 4

Revision B (March 2013) から Revision C に変更 **Page**

- ナショナル セミコンダクターのデータシートのレイアウトをTIフォーマットに 変更 ... 1

5 Pin Configuration and Functions

DCK Package
5-Pin SC70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{OUT}	O	Output
2	V^-	P	Negative supply voltage
3	V_{IN}^+	I	Noninverting input
4	V_{IN}^-	I	Inverting input
5	V^+	P	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
V_{IN} Differential		2.1	V
Supply voltage (V^+ - V^-)		13.2	V
Voltage at input and output pins	$V^+ + 0.3$	$V^- - 0.3$	V
Short-circuit duration	See[3]		
Junction temperature, T_J[4]		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Output short-circuit duration is infinite for $V^+ < 6$ V at room temperature and below. For $V^+ > 6$ V, allowable short-circuit duration is 1.5 ms.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1][2]	±2000	V
		Machine model (MM)[3]	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human Body Model: 1.5 kΩ in series with 100 pF.
(3) Machine Model: 0 Ω in series with 200 pF.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Temperature[1]	–40	85	°C
Supply voltage (V^+ – V^-)	2.7	12	V

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.4 Thermal Information

THERMAL METRIC[1]		LPV511	UNIT
		DCK (SC70)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	105.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: 3 V

Unless otherwise specified, all limits are specified for T_J = 25°C, V^+ = 3 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L = 100 kΩ to $V^+/2$.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input offset voltage	T_J = 25°C			±0.2	±3	mV
		T_J = –40°C to 85°C				±3.8	
TC V_{OS}	Input offset voltage drift(4)	T_J = 25°C			±0.3		µV/°C
		T_J = –40°C to 85°C				±15	
I_B	Input bias current(5)	V_{CM} = 0.5 V	T_J = 25°C	–1000	–320		pA
			T_J = –40°C to 85°C	–1600			
		V_{CM} = 2.5 V	T_J = 25°C		110	800	
			T_J = –40°C to 85°C			1900	
I_{OS}	Input offset current				±10		pA
CMRR	Common mode rejection ratio	V_{CM} Stepped from 0 V to 1.5 V	T_J = 25°C	77	100		dB
			T_J = –40°C to 85°C	70			
		V_{CM} Stepped from 2.4 V to 3 V	T_J = 25°C	75	115		
			T_J = –40°C to 85°C	68			
		V_{CM} Stepped from 0.5 V to 2.5 V	T_J = 25°C	60	80		
			T_J = –40°C to 85°C	56			
PSRR	Power supply rejection ratio	V^+ = 2.7 V to 5 V, V_{CM} = 0.5 V	T_J = 25°C	72	114		dB
			T_J = –40°C to 85°C	68			
		V^+ = 3 V to 5 V, V_{CM} = 0.5 V	T_J = 25°C	76	115		
			T_J = –40°C to 85°C	72			
		V^+ = 5 V to 12 V, V_{CM} = 0.5 V	T_J = 25°C	84	117		
			T_J = –40°C to 85°C	80			
CMVR	Input common-mode voltage	CMRR ≥ 50 dB	T_J = 25°C	−0.1		3.1	V
			T_J = –40°C to 85°C	0		3	
A_{VOL}	Large signal voltage gain	Sinking, V_O = 2.5 V	T_J = 25°C	75	105		dB
			T_J = –40°C to 85°C	70			
		Sourcing, V_O = 0.5 V	T_J = 25°C	75	105		
			T_J = –40°C to 85°C	70			
V_O	Output swing high	V_{ID} = 100 mV	T_J = 25°C	2.85	2.9		V
			T_J = –40°C to 85°C	2.8			
	Output swing low	V_{ID} = −100 mV	T_J = 25°C		100	150	
			T_J = –40°C to 85°C			200	
I_{SC}	Output short circuit current(6)	Sourcing V_{ID} = 100 mV			−500	−225	µA
		Sinking V_{ID} = −100 mV		225	1350		
I_S	Supply current	T_J = 25°C			0.88	1.2	µA
		T_J = –40°C to 85°C				1.5	
SR	Slew rate(7)	A_V = 1, V_O ramps from 0.5 V to 2.5 V	T_J = 25°C	5.25	7.7		V/ms
			T_J = –40°C to 85°C	3.10			

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm at the time of characterization.
(4) Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in VOS at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) The Short-Circuit Test is a momentary test. See Note 3 in *Absolute Maximum Ratings*.
(7) Slew rate is the average of the rising and falling slew rates.

Electrical Characteristics: 3 V (continued)

Unless otherwise specified, all limits are specified for T_J = 25°C, V^+ = 3 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L = 100 kΩ to $V^+/2$.(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
GBW	Gain bandwidth product	R_L = 1 MΩ, C_L= 50 pF		27		kHz
	Phase margin	R_L = 1 MΩ, C_L= 50 pF		53		º
e_n	Input-referred voltage noise	f = 100 Hz		320		nV/√Hz
i_n	Input-referred current noise	f = 10 Hz		0.02		pA/√Hz
		f = 1 kHz		0.01		

6.6 Electrical Characteristics: 5 V

Unless otherwise specified, all limits are specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L = 100 kΩ to $V^+/2$.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input offset voltage	T_J = 25°C			±0.2	±3	mV
		T_J = –40°C to 85°C				±3.8	
TC V_{OS}	Input offset voltage drift(4)	T_J = 25°C			±0.3		µV/°C
		T_J = –40°C to 85°C				±15	
I_B	Input bias current(5)	V_{CM} = 0.5 V	T_J = 25°C	–1000	–320		pA
			T_J = –40°C to 85°C	–1600			
		V_{CM} = 4.5 V	T_J = 25°C		110	800	
			T_J = –40°C to 85°C			1900	
I_{OS}	Input offset current				±10		pA
CMRR	Common mode rejection ratio	V_{CM} Stepped from 0 V to 2.5 V	T_J = 25°C	80	115		dB
			T_J = –40°C to 85°C	73			
		V_{CM} Stepped from 4.4 to 5 V	T_J = 25°C	75	107		
			T_J = –40°C to 85°C	68			
		V_{CM} Stepped from 0.5 to 4.5 V	T_J = 25°C	65	87		
			T_J = –40°C to 85°C	62			
PSRR	Power supply rejection ratio	V^+ = 2.7 V to 5 V, V_{CM} = 0.5 V	T_J = 25°C	72	114		dB
			T_J = –40°C to 85°C	68			
		V^+ = 3 V to 5 V, V_{CM} = 0.5 V	T_J = 25°C	76	115		
			T_J = –40°C to 85°C	72			
		V^+ = 5 V to 12 V, V_{CM} = 0.5 V	T_J = 25°C	84	117		
			T_J = –40°C to 85°C	80			
CMVR	Input common-mode voltage	CMRR ≥ 50 dB	T_J = 25°C	—0.1		5.1	V
			T_J = –40°C to 85°C	0		5	
A_{VOL}	Large signal voltage gain	Sinking, V_O = 4.5 V	T_J = 25°C	78	110		dB
			T_J = –40°C to 85°C	73			
		Sourcing, V_O = 0.5 V	T_J = 25°C	78	110		
			T_J = –40°C to 85°C	73			

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(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm at the time of characterization.
(4) Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in VOS at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

Electrical Characteristics: 5 V (continued)

Unless otherwise specified, all limits are specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L = 100 kΩ to $V^+/2$.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_O	Output swing high	V_{ID} = 100 mV	T_J = 25°C	4.8	4.89		V
			T_J = –40°C to 85°C	4.75			
	Output swing low	V_{ID} = −100 mV	T_J = 25°C		110	200	mV
			T_J = –40°C to 85°C			250	
I_{SC}	Output short circuit current(6)	Sourcing to V^- V_{ID} = 100 mV			–550	–225	µA
		Sinking to V^+ V_{ID} = −100 mV		225	1350		
I_S	Supply current	T_J = 25°C			0.97	1.2	µA
		T_J = –40°C to 85°C				1.5	
SR	Slew rate(7)	A_V = 1, V_O ramps from 0.5 V to 4.5 V	T_J = 25°C	5.25	7.5		V/ms
			T_J = –40°C to 85°C	3.1			
GBW	Gain bandwidth product	R_L = 1 MΩ, C_L= 50 pF			27		kHz
	Phase margin	R_L = 1 MΩ, C_L= 50 pF			53		°
e_n	Input-referred voltage noise	f = 100 Hz			320		nV/√Hz
i_n	Input-referred current noise	f = 10 Hz			0.02		pA/√Hz
		f = 1 kHz			0.01		

(6) The Short-Circuit Test is a momentary test. See Note 3 in *Absolute Maximum Ratings*.
(7) Slew rate is the average of the rising and falling slew rates.

6.7 Electrical Characteristics: 12 V

Unless otherwise specified, all limits are specified for T_J = 25°C, V^+ = 12 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L = 100 kΩ to $V^+/2$.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input offset voltage	T_J = 25°C			±0.2	±3	mV
		T_J = –40°C to 85°C				±3.8	
TC V_{OS}	Input offset voltage drift(4)	T_J = 25°C			±0.3		µV/°C
		T_J = –40°C to 85°C				±15	
I_B	Input bias current(5)	V_{CM} = 0.5 V	T_J = 25°C	−1000	−320		pA
			T_J = –40°C to 85°C	−1600			
		V_{CM} = 11.5 V	T_J = 25°C		110	800	
			T_J = –40°C to 85°C			1900	
I_{OS}	Input offset current				±10		pA
CMRR	Common mode rejection ratio	V_{CM} Stepped from 0 V to 6 V	T_J = 25°C	75	115		dB
			T_J = –40°C to 85°C	70			
		V_{CM} Stepped from 11.4 V to 12 V	T_J = 25°C	75	110		
			T_J = –40°C to 85°C	68			
		V_{CM} Stepped from 0.5 V to 11.5 V	T_J = 25°C	70	97		
			T_J = –40°C to 85°C	65			

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm at the time of characterization.
(4) Offset voltage drift is specified by design and/or characterization and is not tested in production. Offset voltage drift is determined by dividing the change in VOS at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

Electrical Characteristics: 12 V (continued)

Unless otherwise specified, all limits are specified for T_J = 25°C, V^+ = 12 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L = 100 kΩ to $V^+/2$.(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
PSRR	Power supply rejection ratio	V^+ = 2.7 V to 5 V, V_{CM} = 0.5 V	T_J = 25°C	72	114		
			T_J = –40°C to 85°C	68			
		V^+ = 3 V to 5 V, V_{CM} = 0.5 V	T_J = 25°C	76	115		
			T_J = –40°C to 85°C	72			
		V^+ = 5 V to 12 V, V_{CM} = 0.5 V	T_J = 25°C	84	117		
			T_J = –40°C to 85°C	80			
CMVR	Input common-mode voltage	CMRR ≥ 50 dB	T_J = 25°C	−0.1		12.1	V
			T_J = –40°C to 85°C	0		12	
A_{VOL}	Large signal voltage gain	Sinking, V_O = 0.5 V	T_J = 25°C	89	110		dB
			T_J = –40°C to 85°C	84			
		Sourcing, V_O = 11.5 V	T_J = 25°C	89	110		
			T_J = –40°C to 85°C	84			
V_O	Output swing high	V_{ID} = 100 mV	T_J = 25°C	11.8	11.85		V
			T_J = –40°C to 85°C	11.72			
	Output swing low	V_{ID} = −100 mV	T_J = 25°C		150	200	mV
			T_J = –40°C to 85°C			280	
I_{SC}	Output short circuit current (6)	Sourcing V_{ID} = 100 mV			−650	−200	µA
		Sinking V_{ID} = −100 mV		200	1300		
I_S	Supply current	T_J = 25°C			1.2	1.75	µA
		T_J = –40°C to 85°C				2.5	
SR	Slew rate (7)	A_V = 1, V_O ramped from 1 V to 11 V		5.25	7		V/ms
				3.1			
GBW	Gain bandwidth product	R_L = 1 MΩ, C_L= 50 pF			25		kHz
	Phase margin	R_L = 1 MΩ, C_L= 50 pF			52		°
e_n	Input-referred voltage noise	f = 100 Hz			320		$nV/\sqrt{Hz}$
i_n	Input-referred current noise	f = 10 Hz			0.02		$pA/\sqrt{Hz}$
		f = 1 kHz			0.01		

(6) The Short-Circuit Test is a momentary test. See Note 3 in *Absolute Maximum Ratings*.
(7) Slew rate is the average of the rising and falling slew rates.

6.8 Typical Characteristics

At T_J = 25°C, unless otherwise specified.

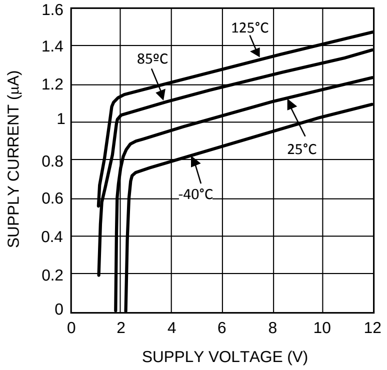


Figure 1. Supply Current vs Supply Voltage

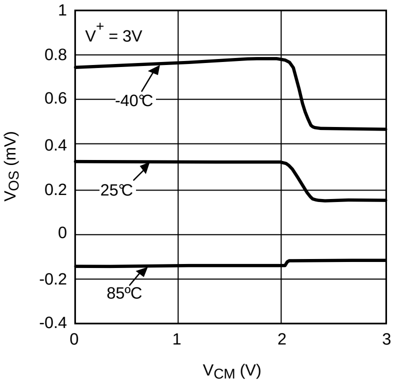


Figure 2. Input Offset Voltage vs Input Common Mode

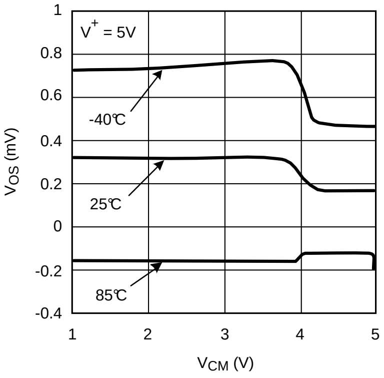


Figure 3. Input Offset Voltage vs Input Common Mode

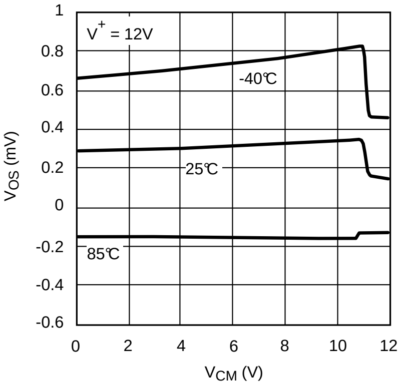


Figure 4. Input Offset Voltage vs Input Common Mode

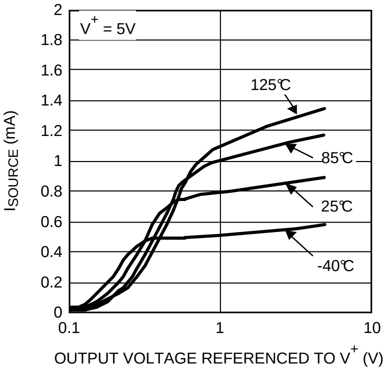


Figure 5. Sourcing Current vs Output Voltage

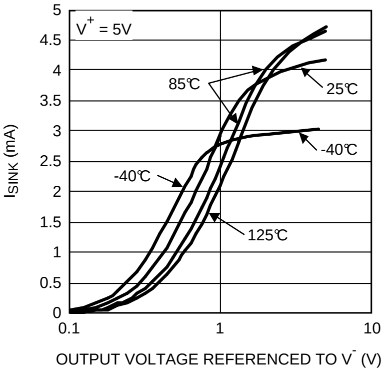


Figure 6. Sinking Current vs Output Voltage

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

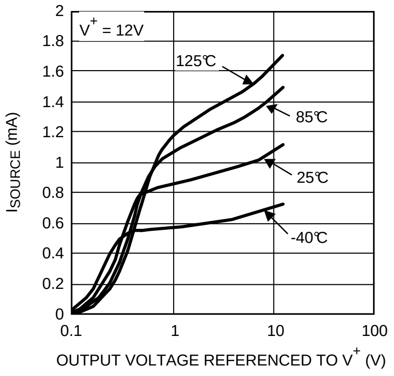


Figure 7. Sourcing Current vs Output Voltage

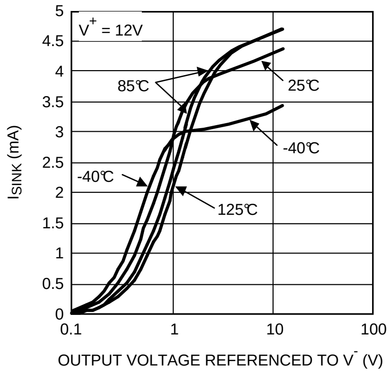


Figure 8. Sinking Current vs Output Voltage

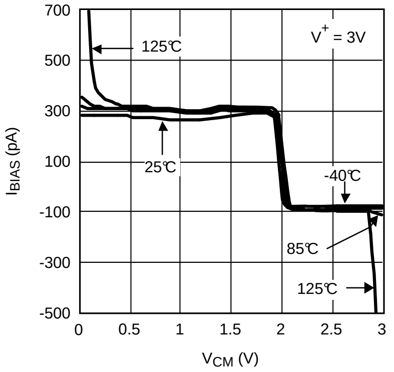


Figure 9. Input Bias Current vs Common Mode Voltage

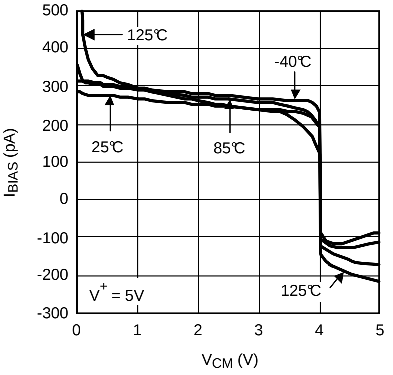


Figure 10. Input Bias Current vs Common Mode Voltage

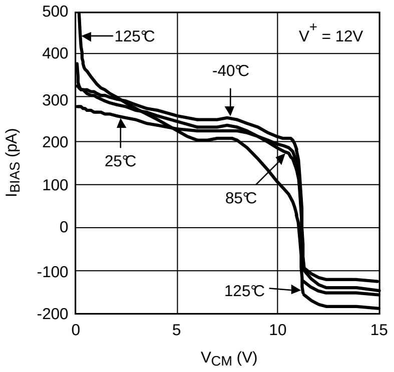


Figure 11. Input Bias Current vs Common Mode Voltage

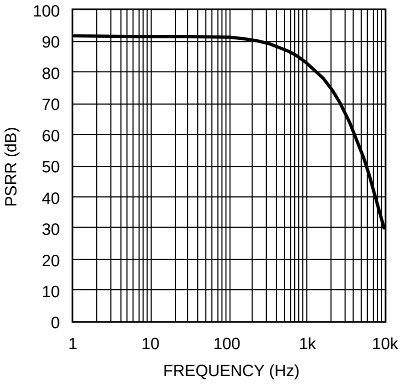


Figure 12. PSRR vs Frequency

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

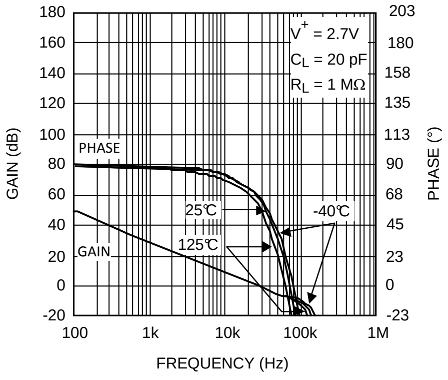


Figure 13. Frequency Response vs Temperature

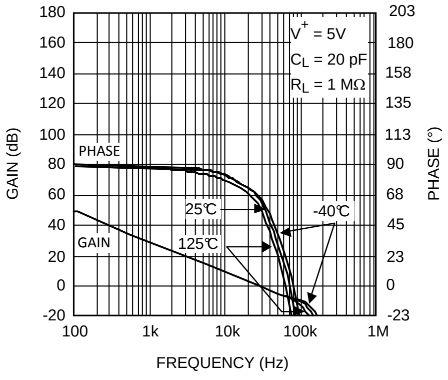


Figure 14. Frequency Response vs Temperature

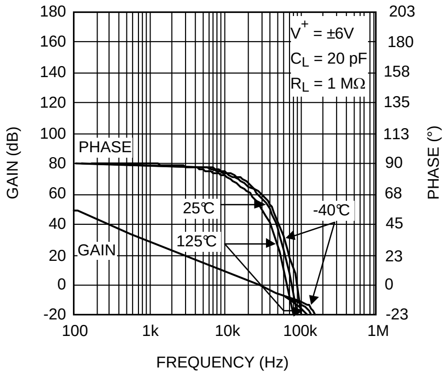


Figure 15. Frequency Response vs Temperature

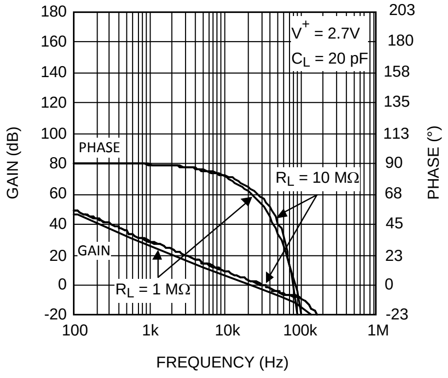


Figure 16. Frequency Response vs R_L

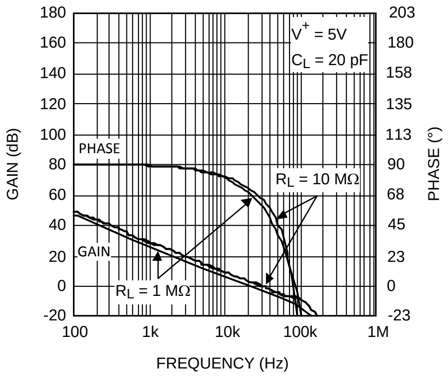


Figure 17. Frequency Response vs R_L

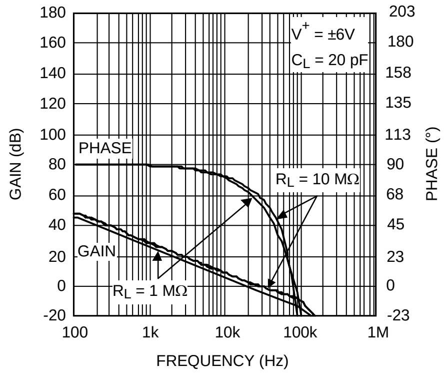


Figure 18. Frequency Response vs R_L

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

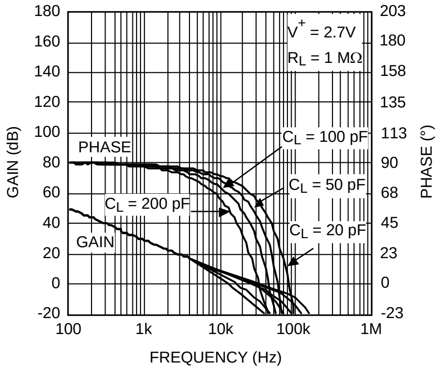


Figure 19. Frequency Response vs C_L

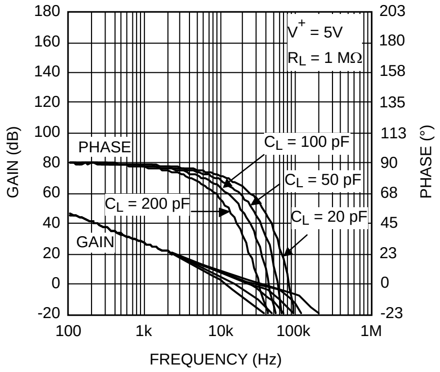


Figure 20. Frequency Response vs C_L

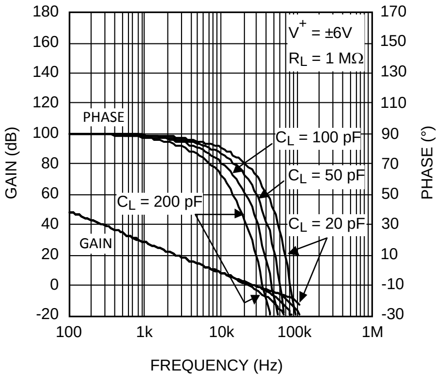


Figure 21. Frequency Response vs C_L

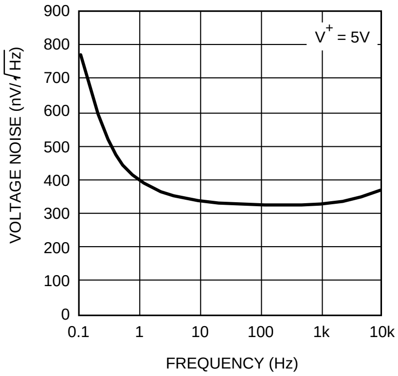


Figure 22. Voltage Noise vs Frequency

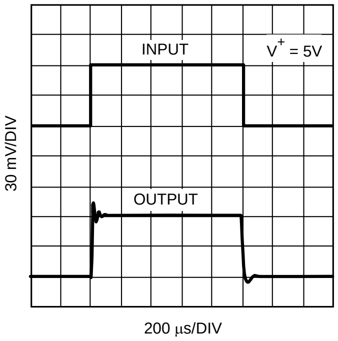


Figure 23. Noninverting Small-Signal Pulse Response

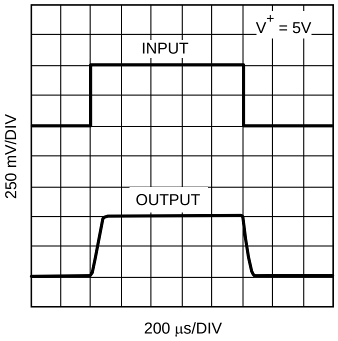


Figure 24. Noninverting Large-Signal Pulse Response

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

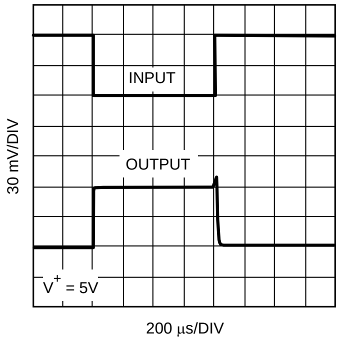


Figure 25. Inverting Small-Signal Pulse Response

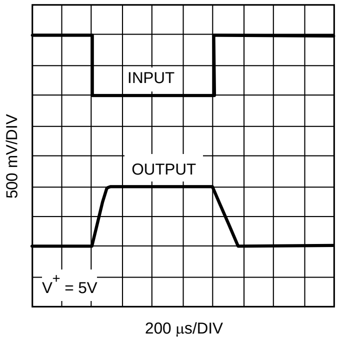


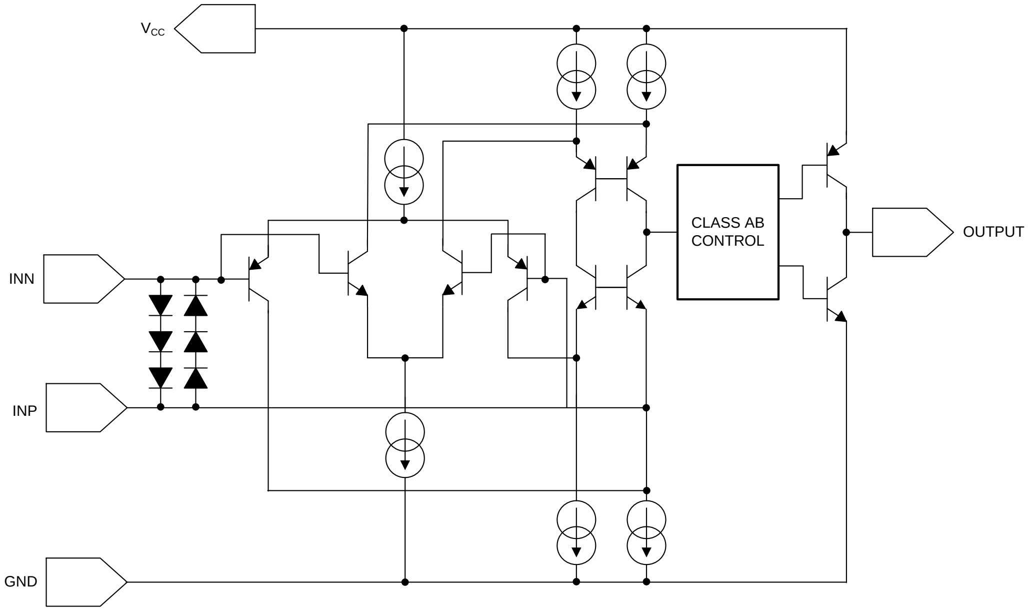
Figure 26. Inverting Large-Signal Pulse Response

7 Detailed Description

7.1 Overview

The LPV511 is a micropower operational amplifier that operates from a voltage supply range as wide as 2.7 V to 12 V with ensured specifications at 3 V, 5 V, and 12 V. The LPV511 exhibits an excellent speed-to-power ratio, drawing only 880 nA of supply current with a bandwidth of 27 kHz.

7.2 Functional Block Diagram



7.3 Feature Description

The LPV511 has a rail-to-rail input which provides more flexibility for the system designer. As can be seen from *Functional Block Diagram*, rail-to-rail input is achieved by using in parallel, one PNP differential pair and one NPN differential pair. When the common mode input voltage (V_{CM}) is near V^+, the NPN pair is on and the PNP pair is off. When V_{CM} is near V^-, the NPN pair is off and the PNP pair is on. When V_{CM} is between V^+ and V^-, internal logic decides how much current each differential pair will get. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

7.4 Device Functional Modes

7.4.1 Input Stage

Because both input stages have their own offset voltage (V_{OS}) characteristic, the offset voltage of the LPV511 becomes a function of V_{CM}. V_{OS} has a crossover point at 1 V below V^+. See the *V_{OS} vs V_{CM}* curve in *Typical Characteristics*. Caution must be taken in situations where the input signal amplitude is comparable to the V_{OS} value and/or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point.

The input bias current, I_B will change in value and polarity as the input crosses the transition region. In addition, parameters such as PSRR and CMRR which involve the input offset voltage will also be affected by changes in V_{CM} across the differential pair transition region.

Differential input voltage is the difference in voltage between the noninverting (+) input and the inverting input (−) of the op amp. Due to the three series diodes across the two inputs, the absolute maximum differential input voltage is ±2.1 V. This may not be a problem to most conventional op amp designs; however, designers **must avoid using the LPV511 as a comparator**.

Device Functional Modes (continued)

7.4.2 Output Stage

The LPV511 output voltage swing 100 mV from rails at 3-V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV511 maximum output voltage swing defines the maximum swing possible under a particular output load. The LPV511 output swings 110 mV from the rail at 5-V supply with an output load of 100 kΩ.

7.4.3 Driving Capacitive Load

The LPV511 is internally compensated for stable unity gain operation, with a 27-kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of the op amp. When the output is required to drive a large capacitive load, greater than 100 pF, a small series resistor at the output of the amplifier improves the phase margin (see Figure 27).

In Figure 27, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. But the DC accuracy is degraded when the R_{ISO} gets bigger. If there were a load resistor in Figure 27, the output voltage would be divided by R_{ISO} and the load resistor.

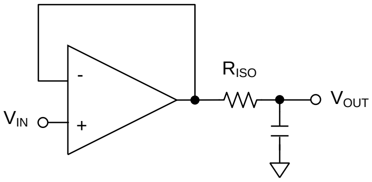


Figure 27. Resistive Isolation of Capacitive Load

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

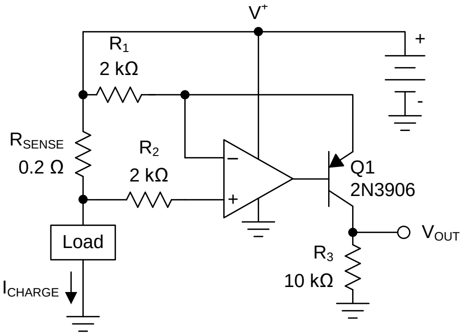
8.1 Application Information

The LPV511 is fabricated with Texas Instrument's state-of-the-art VIP50C process.

8.2 Typical Applications

8.2.1 Battery Current Sensing

The rail-to-rail common mode input range and the very low quiescent current make the LPV511 ideal to use in high-side and low-side battery current sensing applications. The high-side current sensing circuit in Figure 28 is commonly used in a battery charger to monitor the charging current to prevent over charging. A sense resistor R_{SENSE} is connected to the battery directly.



$$V_{OUT} = \frac{R_{SENSE} \times R_3}{R_1} \times I_{CHARGE} = 1\Omega \times I_{CHARGE}$$

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Figure 28. High Side Current Sensing

8.2.1.1 Design Requirements

The high-side current-sensing circuit (Figure 28) is commonly used in a battery charger to monitor charging current to prevent overcharging. A sense resistor RSENSE is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LPV511 ideal for this application because its common-mode input range extends up to the positive supply.

8.2.1.2 Detailed Design Procedure

As seen in Figure 28, the I_{CHARGE} current flowing through sense resistor R_{SENSE} develops a voltage drop equal to V_{SENSE}. The voltage at the negative sense point will now be less than the positive sense point by an amount proportional to the V_{SENSE} voltage.

The low-bias currents of the LPV511 cause little voltage drop through R_2, so the negative input of the LPV551 amplifier is at essentially the same potential as the negative sense input.

The LPV511 will detect this voltage error between its inputs and servo the transistor base to conduct more current through Q1, increasing the voltage drop across R_1 until the LPV511 inverting input matches the noninverting input. At this point, the voltage drop across R_1 now matches V_{SENSE}.

I_G, a current proportional to I_{CHARGE}, will flow according to the following relation to:

$$I_G = V_{RSENSE} / R_1 = (R_{SENSE} \times I_{CHARGE}) / R_1 \qquad (1)$$

Typical Applications (continued)

I_G also flows through the gain resistor R_3 developing a voltage drop equal to:

$$V_3 = I_G \times R_3 = (V_{RSENSE} / R_1) \times R_3 = ((R_{SENSE} \times I_{CHARGE}) / R_2) \times R_3 \quad (2)$$

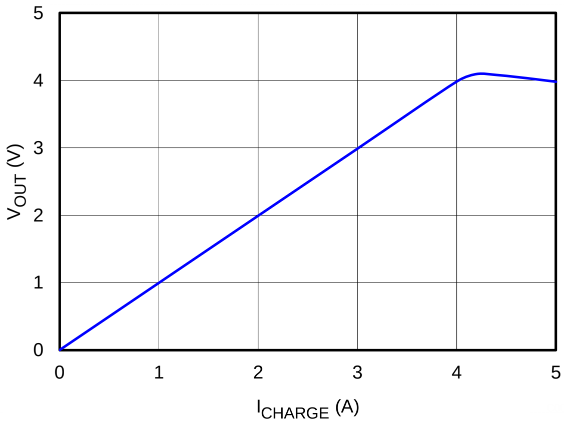
$$V_{OUT} = (R_{SENSE} \times I_{CHARGE}) \times G$$

where

- $G = R_3 / R_1$ (3)

8.2.1.3 Application Curve

Figure 29 shows the results of the example current sense circuit.



The error after 4 V where transistor Q1 runs out of headroom and saturates, limiting the upper output swing.

Figure 29. Current Sense Amplifier Results

8.2.2 Summing Amplifier

The LPV511 operational amplifier is a perfect fit in a summing amplifier circuit because of the rail-to-rail input and output and the sub-micro Amp quiescent current. In this configuration, the amplifier outputs the sum of the three input voltages.

Equation 4 shows the ratio of the sum and the output voltage is defined using feedback and input resistors.

$$V_{OUT} = R_F \left(\frac{V_{REF} - V_1}{R_1} + \frac{V_{REF} - V_2}{R_2} + \frac{V_{REF} - V_3}{R_3} \right) + V_{REF} \quad (4)$$

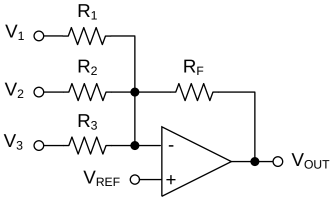


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Figure 30. Summing Amplifier Circuit

8.3 Dos and Don'ts

Do properly bypass the power supplies.

Do add series resistence to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external Schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 kΩ per volt).

9 Power Supply Recommendations

The LPV80x is specified for operation from 1.6 V to 5.5 V (±0.8 V to ±2.75 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Electrical Characteristics: 3 V*.

CAUTION

Supply voltages larger than 13.2 V can permanently damage the device.

For proper operation, the power supplies bust be properly decoupled. For decoupling the supply lines it is suggested that 100 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

- The V^+ pin should be bypassed to ground with a low-ESR capacitor.
- The optimum placement is closest to the V^+ and ground pins.
- Take care to minimize the loop area formed by the bypass capacitor connection between V^+ and ground.
- The ground pin should be connected to the PCB ground plane at the pin of the device.
- The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

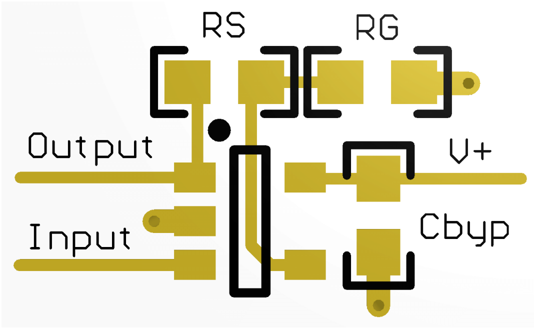

Figure 31. SOT-23 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

LPV511 PSPICEモデル、http://www.ti.com/lit/zip/snom023

TINA-TI SPICEベース・アナログ・シミュレータ・プログラム、http://www.ti.com/tool/tina-ti

DIPアダプタ評価モジュール、http://www.ti.com/tool/dip-adapter-evm

TIユニバーサル・オペアンプ評価モジュール、http://www.ti.com/tool/opampevm

TI Filterproソフトウェア、http://www.ti.com/tool/filterpro

11.2 ドキュメントのサポート

11.2.1 関連資料

- *『オペアンプ・アプリケーション・ハンドブック』*(SBOA092)
- *『トランスインピーダンス・アンプの直感的な補正』*SBOA055
- *『基板のレイアウト技法』*(SLOA089)
- *『AN-1803 トランスインピーダンス・アンプ設計の考慮事項』*(SNOA515)

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商標

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV511MG/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A91	Samples
LPV511MGX/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A91	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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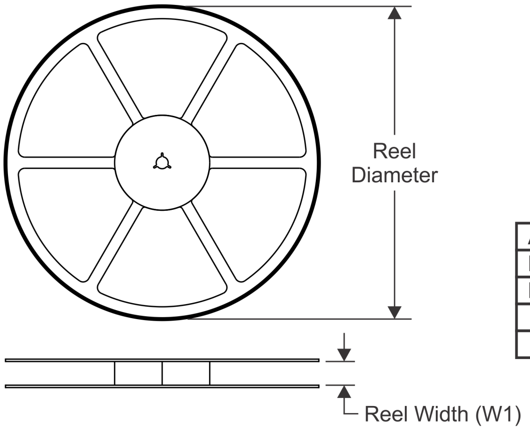
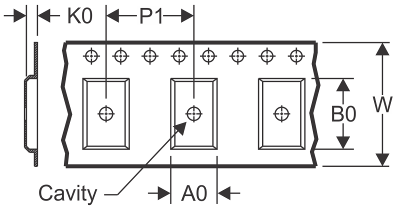
TAPE AND REEL INFORMATION

REEL DIMENSIONS

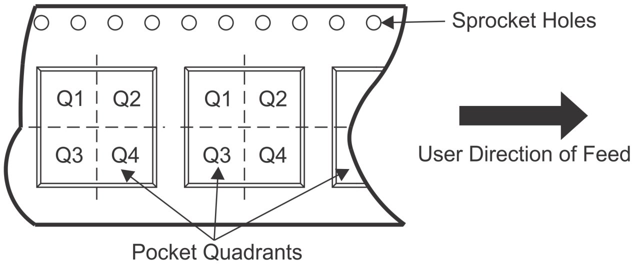


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

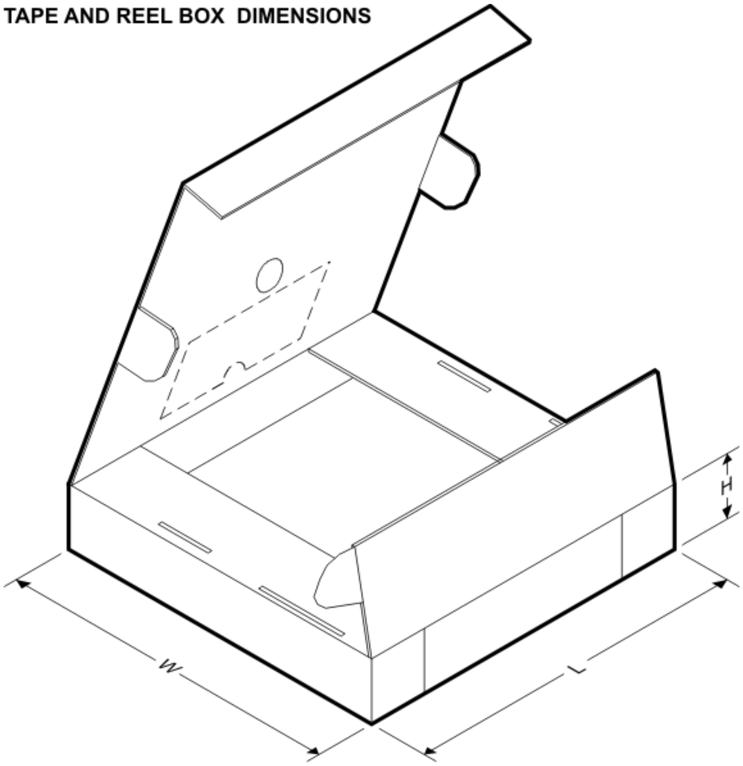
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

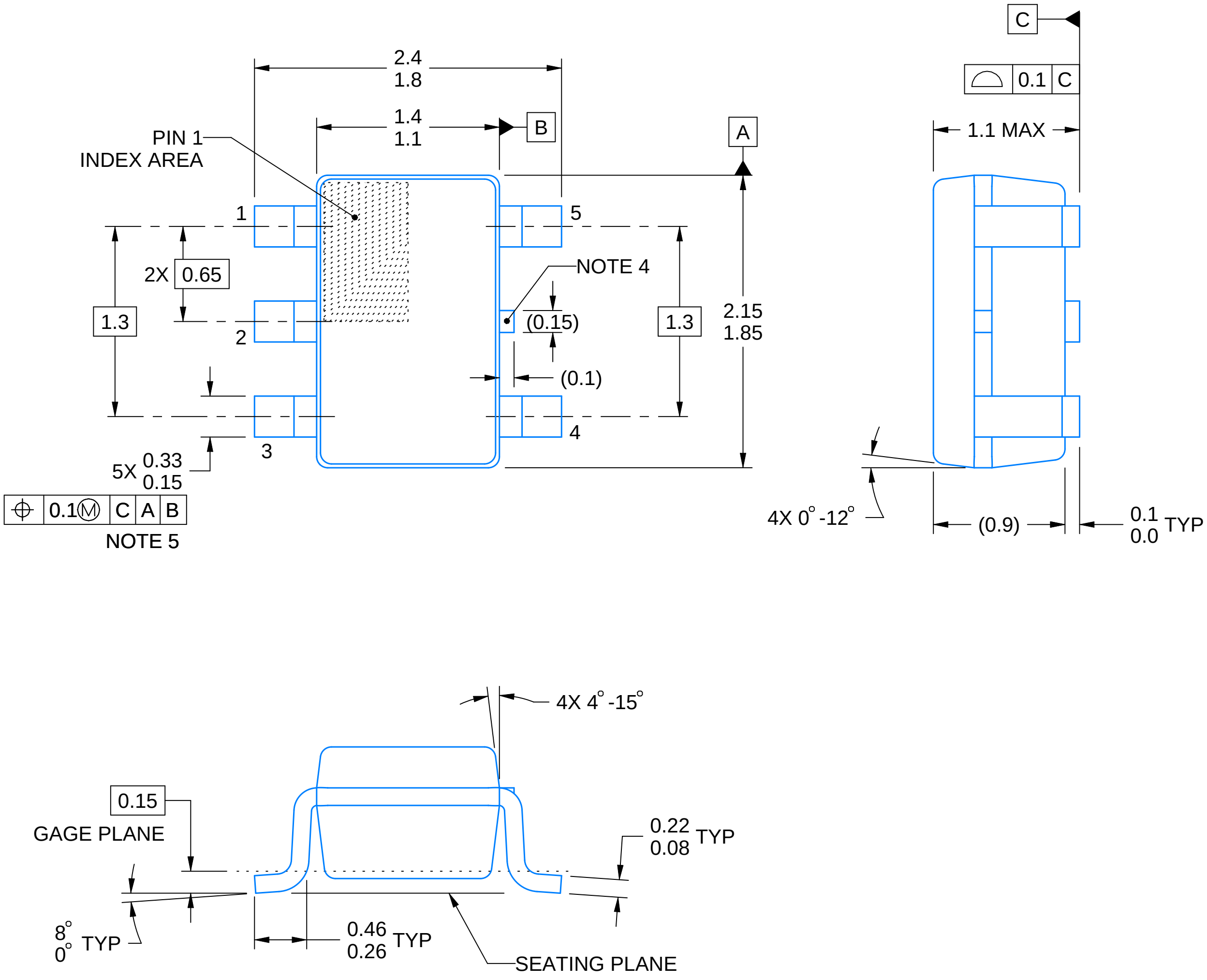
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV511MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV511MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV511MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LPV511MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0



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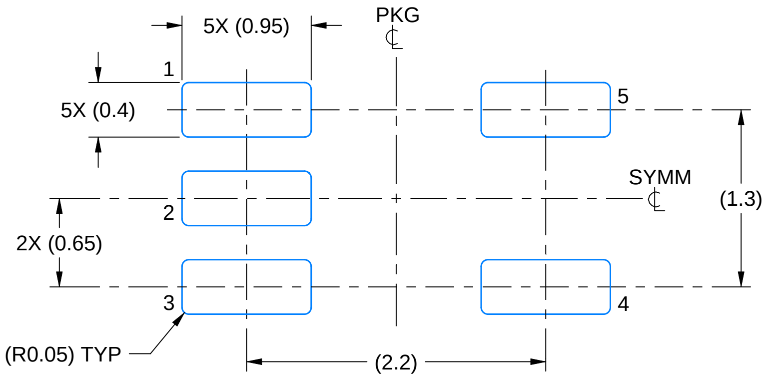
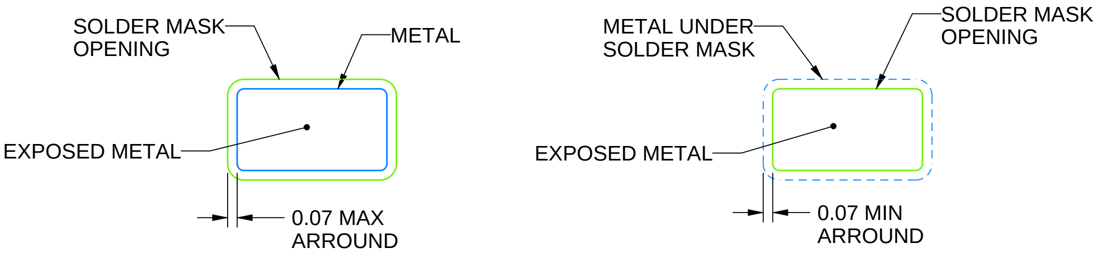
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



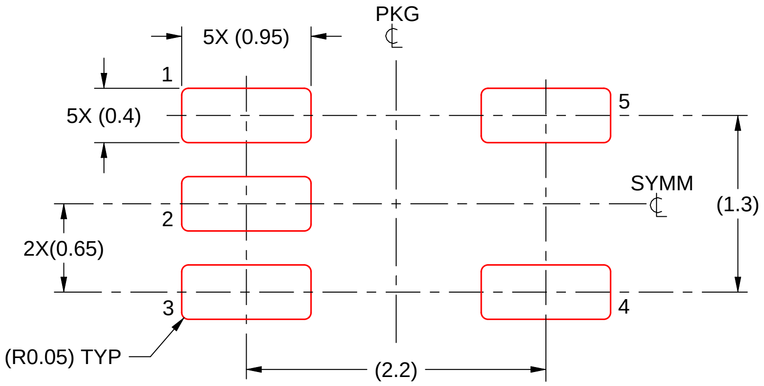
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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