

MSP430F534x ミクスト・シグナル・マイクロコントローラ

1 デバイスの概要

1.1 特長

- 低い電源電圧範囲: 3.6Vから最低1.8Vまで
- 超低消費電力
 - アクティブ・モード(AM): すべてのシステム・クロックがアクティブ
 - 290 μ A/MHz (8MHz, 3V)、フラッシュ・プログラム実行時(標準値)
 - 150 μ A/MHz (8MHz, 3V)、RAMプログラム実行時(標準値)
 - スタンバイ・モード(LPM3)
 - リアルタイム・クロック(RTC)(水晶振動子を使用)、ウォッチドッグ、および電源スーパーバイザが動作、RAMデータ完全保持、高速ウェークアップ:
 - 1.9 μ A (2.2V)、2.1 μ A (3V)(標準値)
 - 低消費電力発振器(VLO)、汎用カウンタ、ウォッチドッグ、および電源スーパーバイザが動作、RAMデータ完全保持、高速ウェークアップ:
 - 1.4 μ A (3V)(標準値)
 - オフ・モード(LPM4)
 - RAMデータ完全保持、電源スーパーバイザが動作、高速ウェークアップ:
 - 1.1 μ A (3V)(標準値)
 - シャットダウン・モード(LPM4.5)
 - 0.18 μ A (3V)(標準値)
- スタンバイ・モードから3.5 μ sでウェークアップ(標準値)
- 16ビットRISCアーキテクチャ、拡張メモリ、最大25MHzのシステム・クロック
- 柔軟な電力管理システム
 - プログラム可能な、レギュレートされたコア電源電圧を持つ、完全に統合されたLDO
 - 電源電圧の管理、監視、およびブラウンアウト
- 統合クロック・システム
 - FLL制御ループによる周波数安定化
 - 低電力、低周波数の内部クロック・ソース(VLO)
 - 低周波数のトリムされた内部基準ソース(REFO)
 - 32kHzの時計用水晶振動子(XT1)
 - 最高32MHzの高周波数水晶振動子(XT2)
- 16ビット・タイマ TA0: 5個のキャプチャ/コンペア・レジスタを備えたTimer_A
- 16ビット・タイマ TA1: 3個のキャプチャ/コンペア・レジスタを備えたTimer_A
- 16ビット・タイマ TA2: 3個のキャプチャ/コンペア・レジスタを備えたTimer_A
- 16ビット・タイマTB0: 7個のキャプチャ/コンペア・シャドウ・レジスタを備えたTimer_B
- 2つのユニバーサル・シリアル通信インターフェイス(USCI)
 - USCI_A0、USCI_A1がそれぞれ次の機能をサポート
 - 自動ボーレート検出機能付きの拡張UART
 - IrDAエンコーダおよびデコーダ
 - 同期SPI
 - USCI_B0、USCI_B1がそれぞれ次の機能をサポート
 - I²C
 - 同期SPI
- 内部リファレンス、サンプル・アンド・ホールド、オートスキャン機能搭載の12ビットのA/Dコンバータ(ADC)
- コンパレータ
- ハードウェア乗算器で32ビットの演算をサポート
- シリアルのオンボード・プログラミング、外部からのプログラミング電圧は不要
- 3チャンネルの内蔵DMA
- RTC機能付き基本タイマ
- [デバイスの比較](#) に、供給中の製品ファミリを掲載

1.2 アプリケーション

- アナログ・センサ・システム
- デジタル・センサ・システム
- データ・ロギング
- 汎用アプリケーション

1.3 概要

TIのMSP超低消費電力マイクロコントローラ・ファミリは、各種アプリケーションを対象とするそれぞれ異なるペリフェラルを備えた複数のデバイスで構成されています。アーキテクチャに多様な低消費電力モードを組み合わせ、携帯型測定機器で長いバッテリー駆動時間を実現するように最適化しています。強力な16ビットRISC CPU、16ビット・レジスタ、および定数ジェネレータが搭載されているため、最高水準のコード効率を実現できます。デジタル制御発振器(DCO)により、低消費電力モードからアクティブ・モードへ3.5 μ s(標準値)でウェークアップできます。

MSP430F534x MCUは、4つの16ビット・タイマ、高性能の12ビットADC、2つのUSCI、ハードウェア乗算器、DMA、アラーム機能付きのRTCモジュール、38本のI/Oピンを搭載しています。



モジュールの完全な説明については、『MSP430FR5xxおよびMSP430FR6xxファミリー ユーザー・ガイド』を参照してください。

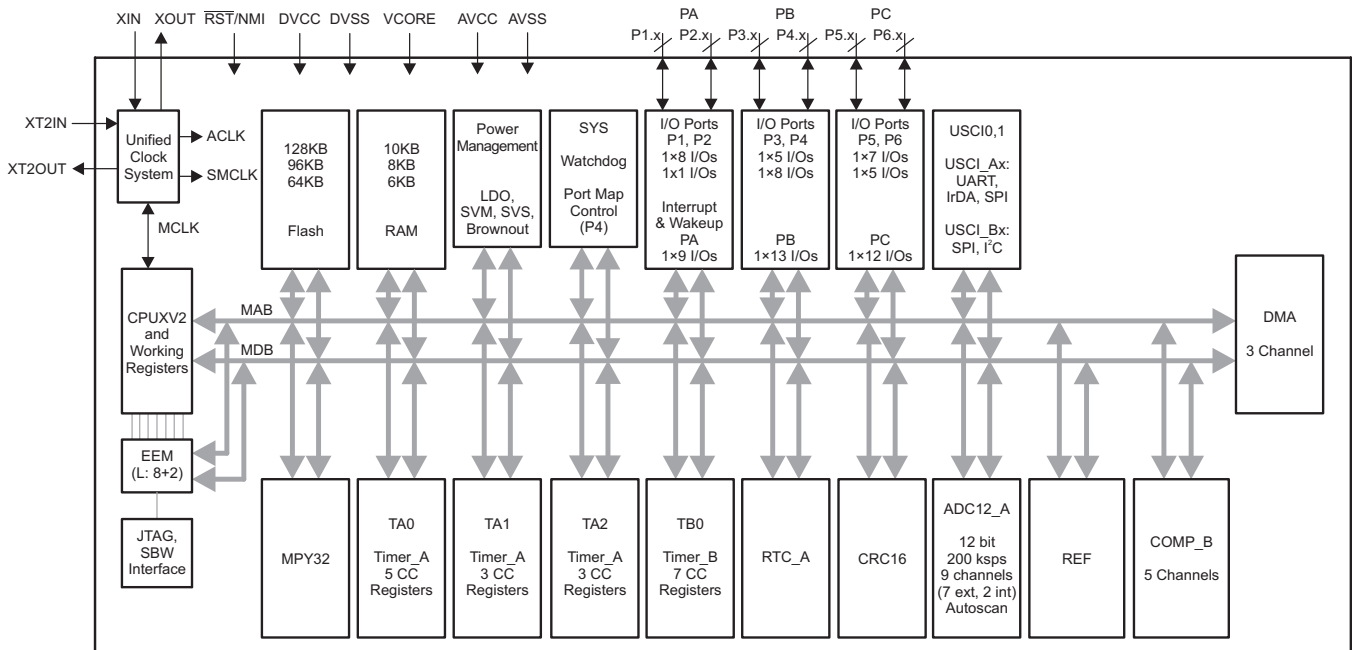
製品情報⁽¹⁾

型番	パッケージ	本体サイズ ⁽²⁾
MSP430F5342IRGZ	VQFN (48)	7mm×7mm
MSP430F5341IRGZ	VQFN (48)	7mm×7mm
MSP430F5340IRGZ	VQFN (48)	7mm×7mm

- (1) 最新の製品、パッケージ、および注文情報については、8の「付録:パッケージ・オプション」、または www.ti.com のTI Webサイトを参照してください。
- (2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、8の「メカニカル・データ」を参照してください。

1.4 機能ブロック図

機能ブロック図を、図 1-1に示します。



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図 1-1. MSP430F534xのブロック図

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2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2013年10月1日発行分から2018年09月26日発行分への変更	Page
• 全体を通してドキュメントのフォーマットと構成を変更、セクションの番号追加も含む	1
• 「製品情報」表を追加	2
• 機能ブロック図を 1.4に移動.....	2
• Added Section 3.1, Related Products	5
• Added typical conditions statements at the beginning of Section 5, Specifications	11
• Added Section 5.2, ESD Ratings	11
• Added note to $C_{V_{CORE}}$ in Section 5.3, Recommended Operating Conditions	11
• Moved Section 5.6, Thermal Resistance Characteristics	13
• Changed the TYP value of the $C_{L,eff}$ parameter with Test Conditions of "XTS = 0, XCAPx = 0" from 2 pF to 1 pF in Section 5.15, Crystal Oscillator, XT1, Low-Frequency Mode	18
• Changed the MIN value of $V_{(DVCC_BOR_hys)}$ from 60 mV to 50 mV in Section 5.20, PMM, Brownout Reset (BOR)	22
• Updated notes (1) and (2) and added note (3) in Section 5.26, Wake-up Times From Low-Power Modes and Reset	25
• Removed ADC12DIV from the formula for the TYP value in the second row of the $t_{CONVERT}$ parameter in Section 5.36, 12-Bit ADC, Timing Parameters , because ADC12CLK is after division	31
• Added second row for the t_{EN_CMP} parameter with Test Conditions of "CBPWRMD = 10" and MAX value of 100 μ s and removed option for "CBPWRMD = 10" from first row of Test Conditions in Section 5.42, Comparator_B	36
• Changed all instances of "bootstrap loader" to "bootloader" throughout document	42
• 7 を追加して、「ツールのサポート」、「デバイスの項目表記」、「静電気放電に関する注意事項」、「商標」セクションをそこに移動.....	84
• 従来の「ツールのサポート」を 7.3 「ツールとソフトウェア」に置き換え	86
• 8 「メカニカル、パッケージ、および注文情報」を追加	90

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison⁽¹⁾⁽²⁾

DEVICE	FLASH (KB)	SRAM (KB)	Timer_A ⁽³⁾	Timer_B ⁽⁴⁾	USCI		ADC12_A (Ch)	Comp_B (Ch)	I/Os	PACKAGE
					CHANNEL A: UART, IrDA, SPI	CHANNEL B: SPI, I ² C				
MSP430F5342	128	10	5, 3 ⁽⁵⁾ , 3 ⁽⁶⁾	7	2	2	7 ext, 2 int	5	38	48 RGZ
MSP430F5341	96	8	5, 3 ⁽⁵⁾ , 3 ⁽⁶⁾	7	2	2	7 ext, 2 int	5	38	48 RGZ
MSP430F5340	64	6	5, 3 ⁽⁵⁾ , 3 ⁽⁶⁾	7	2	2	7 ext, 2 int	5	38	48 RGZ

- (1) For the most current package and ordering information, see the *Package Option Addendum* in 8, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
- (3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (5) Only one PWM output and one external capture input available at pin.
- (6) No PWM outputs or external capture inputs available at pins.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI Microcontrollers TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

Products for MSP430 Ultra-Low-Power Microcontrollers One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

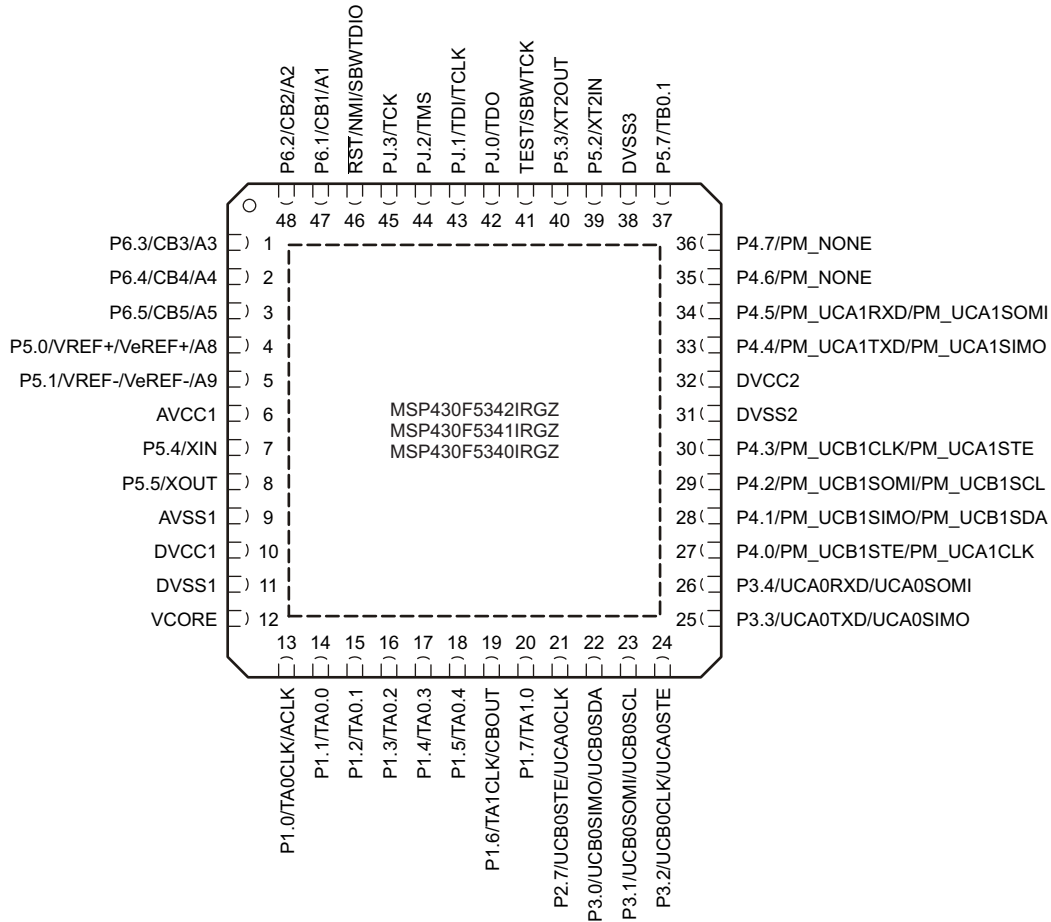
Companion Products for MSP430F5342 Review products that are frequently purchased or used in conjunction with this product.

TI Reference Designs Find reference designs that leverage the best in TI technology to solve your system-level challenges.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pinout of the 48-pin RGZ package.



NOTE: TI recommends connecting the exposed thermal pad connection to V_{SS} .

Figure 4-1. 48-Pin RGZ Package (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals.

Table 4-1. Signal Descriptions

TERMINAL		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
P6.3/CB3/A3	1	I/O	General-purpose digital I/O Comparator_B input CB3 Analog input A3 for the ADC
P6.4/CB4/A4	2	I/O	General-purpose digital I/O Comparator_B input CB4 Analog input A4 for the ADC
P6.5/CB5/A5	3	I/O	General-purpose digital I/O Comparator_B input CB5 Analog input A5 for the ADC
P5.0/A8/VREF+/VeREF+	4	I/O	General-purpose digital I/O Analog input A8 for the ADC Output of reference voltage to the ADC Input for an external reference voltage to the ADC
P5.1/A9/VREF-/VeREF-	5	I/O	General-purpose digital I/O Analog input A9 for the ADC Negative terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
AVCC1	6		Analog power supply
P5.4/XIN	7	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
P5.5/XOUT	8	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
AVSS1	9		Analog ground supply
DVCC1	10		Digital power supply
DVSS1	11		Digital ground supply
VCORE ⁽²⁾	12		Regulated core power supply output (internal use only, no external current loading)
P1.0/TA0CLK/ACLK	13	I/O	General-purpose digital I/O with port interrupt TA0 clock signal TA0CLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P1.1/TA0.0	14	I/O	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	15	I/O	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input
P1.3/TA0.2	16	I/O	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output

(1) I = input, O = output, N/A = not available

(2) VCORE is for internal use only. No external current loading is possible. VCORE should be connected to only the recommended capacitor value, C_{VCORE}.

Table 4-1. Signal Descriptions (continued)

TERMINAL		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
P1.4/TA0.3	17	I/O	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4	18	I/O	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/TA1CLK/CBOUT	19	I/O	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input Comparator_B output
P1.7/TA1.0	20	I/O	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output
P2.7/UCB0STE/UCA0CLK	21	I/O	General-purpose digital I/O with port interrupt Slave transmit enable for USCI_B0 SPI mode Clock signal input for USCI_A0 SPI slave mode Clock signal output for USCI_A0 SPI master mode
P3.0/UCB0SIMO/UCB0SDA	22	I/O	General-purpose digital I/O Slave in, master out for USCI_B0 SPI mode I ² C data for USCI_B0 I ² C mode
P3.1/UCB0SOMI/UCB0SCL	23	I/O	General-purpose digital I/O Slave out, master in for USCI_B0 SPI mode I ² C clock for USCI_B0 I ² C mode
P3.2/UCB0CLK/UCA0STE	24	I/O	General-purpose digital I/O Clock signal input for USCI_B0 SPI slave mode Clock signal output for USCI_B0 SPI master mode Slave transmit enable for USCI_A0 SPI mode
P3.3/UCA0TXD/UCA0SIMO	25	I/O	General-purpose digital I/O Transmit data for USCI_A0 UART mode Slave in, master out for USCI_A0 SPI mode
P3.4/UCA0RXD/UCA0SOMI	26	I/O	General-purpose digital I/O Receive data for USCI_A0 UART mode Slave out, master in for USCI_A0 SPI mode
P4.0/PM_UCB1STE/ PM_UCA1CLK	27	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave transmit enable for USCI_B1 SPI mode Default mapping: Clock signal input for USCI_A1 SPI slave mode Default mapping: Clock signal output for USCI_A1 SPI master mode
P4.1/PM_UCB1SIMO/ PM_UCB1SDA	28	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out for USCI_B1 SPI mode Default mapping: I ² C data for USCI_B1 I ² C mode
P4.2/PM_UCB1SOMI/ PM_UCB1SCL	29	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in for USCI_B1 SPI mode Default mapping: I ² C clock for USCI_B1 I ² C mode

Table 4-1. Signal Descriptions (continued)

TERMINAL		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
P4.3/PM_UCB1CLK/ PM_UCA1STE	30	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input for USCI_B1 SPI slave mode Default mapping: Clock signal output for USCI_B1 SPI master mode Default mapping: Slave transmit enable for USCI_A1 SPI mode
DVSS2	31		Digital ground supply
DVCC2	32		Digital power supply
P4.4/PM_UCA1TXD/ PM_UCA1SIMO	33	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data for USCI_A1 UART mode Default mapping: Slave in, master out for USCI_A1 SPI mode
P4.5/PM_UCA1RXD/ PM_UCA1SOMI	34	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data for USCI_A1 UART mode Default mapping: Slave out, master in for USCI_A1 SPI mode
P4.6/PM_NONE	35	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
P4.7/PM_NONE	36	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
P5.7/TB0.1	37	I/O	General-purpose digital I/O TB0 CCR1 capture: CCI1A input, compare: Out1 output
DVSS3	38		Digital ground supply
P5.2/XT2IN	39	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P5.3/XT2OUT	40	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTK ⁽³⁾	41	I	Test mode pin – Selects 4-wire JTAG operation. Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated
PJ.0/TDO ⁽⁴⁾	42	I/O	General-purpose digital I/O JTAG test data output port
PJ.1/TDI/TCLK ⁽⁴⁾	43	I/O	General-purpose digital I/O JTAG test data input or test clock input
PJ.2/TMS ⁽⁴⁾	44	I/O	General-purpose digital I/O JTAG test mode select
PJ.3/TCK ⁽⁴⁾	45	I/O	General-purpose digital I/O JTAG test clock
$\overline{\text{RST}}$ /NMI/SBWDIO ⁽³⁾	46	I/O	Reset input active low ⁽⁵⁾ Nonmaskable interrupt input Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated.
P6.1/CB1/A1	47	I/O	General-purpose digital I/O Comparator_B input CB1 Analog input A1 for the ADC

(3) See [Section 6.5](#) and [Section 6.6](#) for use with BSL and JTAG functions

(4) See [Section 6.6](#) for use with JTAG function.

(5) When this pin is configured as reset, the internal pullup resistor is enabled by default.

Table 4-1. Signal Descriptions (continued)

TERMINAL		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
P6.2/CB2/A2	48	I/O	General-purpose digital I/O Comparator_B input CB2 Analog input A2 for the ADC
Thermal Pad			QFN package pad. TI recommends connecting to V _{SS} .

5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

5.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}	-0.3	4.1	V
Voltage applied to any pin (excluding V _{CORE}) ⁽²⁾	-0.3	$V_{CC} + 0.3$	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg} ⁽³⁾	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . V_{CORE} is for internal device use only. No external DC loading or voltage should be applied.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

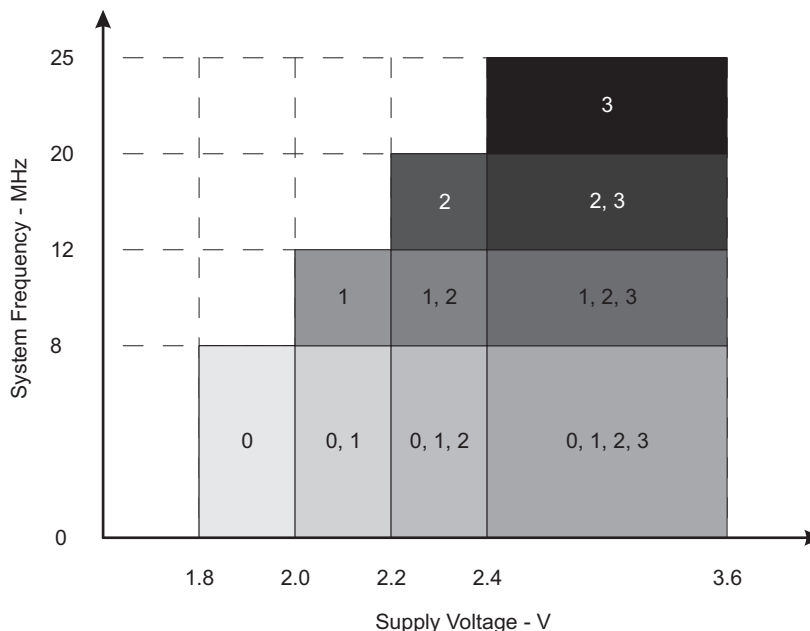
	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming ($AV_{CCx} = DV_{CCx} = V_{CC}$) ⁽¹⁾⁽²⁾	PMMCOREV _x = 0	1.8	3.6	V
		PMMCOREV _x = 0, 1	2.0	3.6	
		PMMCOREV _x = 0, 1, 2	2.2	3.6	
		PMMCOREV _x = 0, 1, 2, 3	2.4	3.6	
V_{SS}	Supply voltage ($AV_{SSx} = DV_{SSx} = V_{SS}$)		0		V
T_A	Operating free-air temperature	-40		85	°C
T_J	Operating junction temperature	-40		85	°C
$C_{V_{CORE}}$	Recommended capacitor at V _{CORE} ⁽³⁾		470		nF
$C_{DV_{CC}}/C_{V_{CORE}}$	Capacitor ratio of DV _{CC} to V _{CORE}		10		
f_{SYSTEM}	Processor frequency (maximum MCLK frequency) ⁽⁴⁾ (see Figure 5-1)	PMMCOREV _x = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V (default condition)	0	8.0	MHz
		PMMCOREV _x = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V	0	12.0	
		PMMCOREV _x = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0	20.0	
		PMMCOREV _x = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V	0	25.0	

- (1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
- (2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the Section 5.22 threshold parameters for the exact values and further details.
- (3) A capacitor tolerance of ±20% or better is required.
- (4) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-1. Maximum System Frequency

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)^{(1) (2) (3)}

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)										UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, Flash}$	Flash	3 V	0	0.36	0.47	2.32	2.60							mA
			1	0.40		2.65		4.0	4.4					
			2	0.44		2.90		4.3		7.1	7.7			
			3	0.46		3.10		4.6		7.6	10.1	11.0		
$I_{AM, RAM}$	RAM	3 V	0	0.20	0.24	1.20	1.30						mA	
			1	0.22		1.35		2.0	2.2					
			2	0.24		1.50		2.2		3.7	4.2			
			3	0.26		1.60		2.4		3.9	5.3	6.2		

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Characterized with program executing typical data processing.
 $f_{ACLK} = 32786$ Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
 XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

PARAMETER	V_{CC}	PMMCOREVx	TEMPERATURE (T_A)								UNIT
			-40°C		25°C		60°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$ Low-power mode 0 ^{(3) (4)}	2.2 V	0	73	77	85	80	85	97	μA		
	3 V	3	79	83	92	88	95	105			
I_{LPM2} Low-power mode 2 ^{(5) (4)}	2.2 V	0	6.5	6.5	12	10	11	17	μA		
	3 V	3	7.0	7.0	13	11	12	18			
$I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode ^{(6) (4)}	2.2 V	0	1.60	1.90		2.6	5.6		μA		
		1	1.65	2.00		2.7	5.9				
		2	1.75	2.15		2.9	6.1				
	3 V	0	1.8	2.1	2.9	2.8	5.8	8.3			
		1	1.9	2.3		2.9	6.1				
		2	2.0	2.4		3.0	6.3				
$I_{LPM3,VLO}$ Low-power mode 3, VLO mode ^{(7) (4)}	3 V	3	2.0	2.5	3.9	3.1	6.4	9.3			
		0	1.1	1.4	2.7	1.9	4.9	7.4			
		1	1.1	1.4		2.0	5.2				
		2	1.2	1.5		2.1	5.3				
I_{LPM4} Low-power mode 4 ^{(8) (4)}	3 V	3	1.3	1.6	3.0	2.2	5.4	8.5			
		0	0.9	1.1	1.5	1.8	4.8	7.3			
		1	1.1	1.2		2.0	5.1				
		2	1.2	1.2		2.1	5.2				
$I_{LPM4.5}$ Low-power mode 4.5 ⁽⁹⁾	3 V		0.15	0.18	0.35	0.26	0.5	1.0	μA		

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK} = 32768$ Hz, $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO} = 1$ MHz

(4) Current for brownout, high-side supervisor (SVSH) normal mode included. Low-side supervisor (SVSL) and low-side monitor (SVM_L) disabled. High-side monitor (SVM_H) disabled. RAM retention enabled.

(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), $f_{ACLK} = 32768$ Hz, $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO} = 0$ MHz, DCO setting = 1-MHz operation, DCO bias generator enabled.)

(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO} = 0$ MHz

(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK} = f_{DCO} = 0$ MHz

(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

(9) Internal regulator disabled. No data retention.

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

5.6 Thermal Resistance Characteristics, VQFN (RGZ) Package

THERMAL METRIC			VALUE	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	High-K board (JESD51-7)	27.8	°C/W
$R\theta_{JC}$	Junction-to-case thermal resistance		13.6	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance		4.7	°C/W

5.7 Schmitt-Trigger Inputs – General-Purpose I/O⁽¹⁾ (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V _{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V _{hys}	Input voltage hysteresis (V _{IT+} – V _{IT-})		1.8 V	0.3		0.8	V
			3 V	0.4		1.0	
R _{Pull}	Pullup/pulldown resistor ⁽²⁾	For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC}		20	35	50	kΩ
C _I	Input capacitance	V _{IN} = V _{SS} or V _{CC}			5		pF

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

(2) Also applies to RST pin when pullup or pulldown resistor is enabled.

5.8 Inputs – Ports P1 and P2⁽¹⁾ (P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
t _(int)	External interrupt timing ⁽²⁾	External trigger pulse duration to set interrupt flag	2.2 V, 3 V	20	ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

5.9 Leakage Current – General-Purpose I/O (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
I _{lkg(Px.y)}	High-impedance leakage current	(1) (2)	1.8 V, 3 V	±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

5.10 Outputs – General-Purpose I/O (Full Drive Strength) (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Section 5.14](#))

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{OH}	High-level output voltage	I _(OHmax) = -3 mA ⁽¹⁾	1.8 V	V _{CC} - 0.25	V _{CC}	V
		I _(OHmax) = -10 mA ⁽²⁾		V _{CC} - 0.60	V _{CC}	
		I _(OHmax) = -5 mA ⁽¹⁾	3 V	V _{CC} - 0.25	V _{CC}	
		I _(OHmax) = -15 mA ⁽²⁾		V _{CC} - 0.60	V _{CC}	
V _{OL}	Low-level output voltage	I _(OLmax) = 3 mA ⁽¹⁾	1.8 V	V _{SS}	V _{SS} + 0.25	V
		I _(OLmax) = 10 mA ⁽²⁾		V _{SS}	V _{SS} + 0.60	
		I _(OLmax) = 5 mA ⁽¹⁾	3 V	V _{SS}	V _{SS} + 0.25	
		I _(OLmax) = 15 mA ⁽²⁾		V _{SS}	V _{SS} + 0.60	

- (1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

5.11 Outputs – General-Purpose I/O (Reduced Drive Strength) (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see [Section 5.13](#))

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{OH}	High-level output voltage	I _(OHmax) = -1 mA ⁽²⁾	1.8 V	V _{CC} - 0.25	V _{CC}	V
		I _(OHmax) = -3 mA ⁽³⁾		V _{CC} - 0.60	V _{CC}	
		I _(OHmax) = -2 mA ⁽²⁾	3 V	V _{CC} - 0.25	V _{CC}	
		I _(OHmax) = -6 mA ⁽³⁾		V _{CC} - 0.60	V _{CC}	
V _{OL}	Low-level output voltage	I _(OLmax) = 1 mA ⁽²⁾	1.8 V	V _{SS}	V _{SS} + 0.25	V
		I _(OLmax) = 3 mA ⁽³⁾		V _{SS}	V _{SS} + 0.60	
		I _(OLmax) = 2 mA ⁽²⁾	3 V	V _{SS}	V _{SS} + 0.25	
		I _(OLmax) = 6 mA ⁽³⁾		V _{SS}	V _{SS} + 0.60	

- (1) Selecting reduced drive strength may reduce EMI.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
- (3) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

5.12 Output Frequency – General-Purpose I/O (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3)

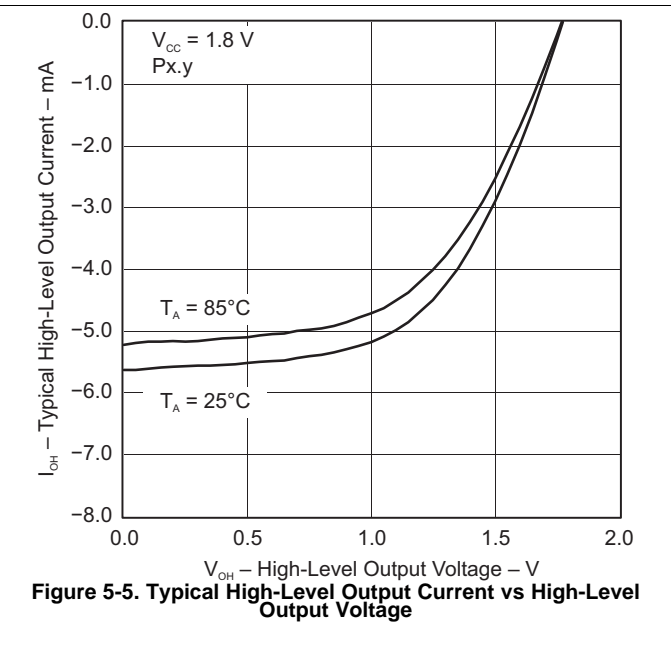
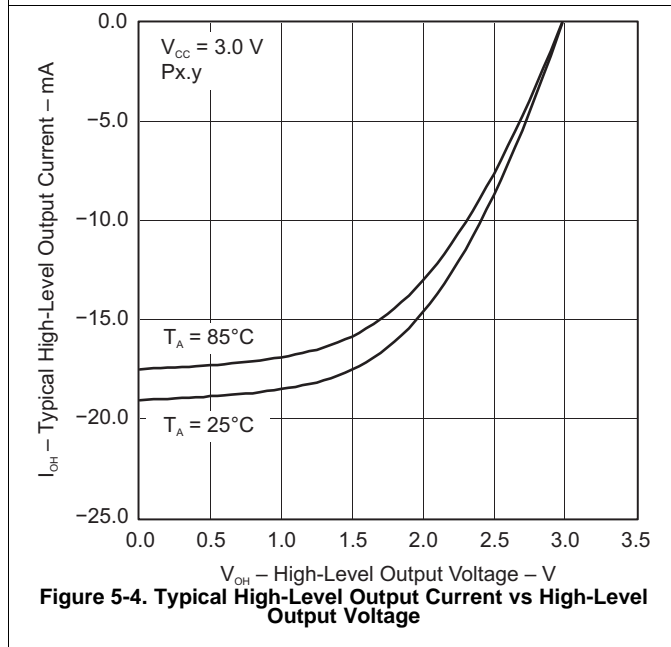
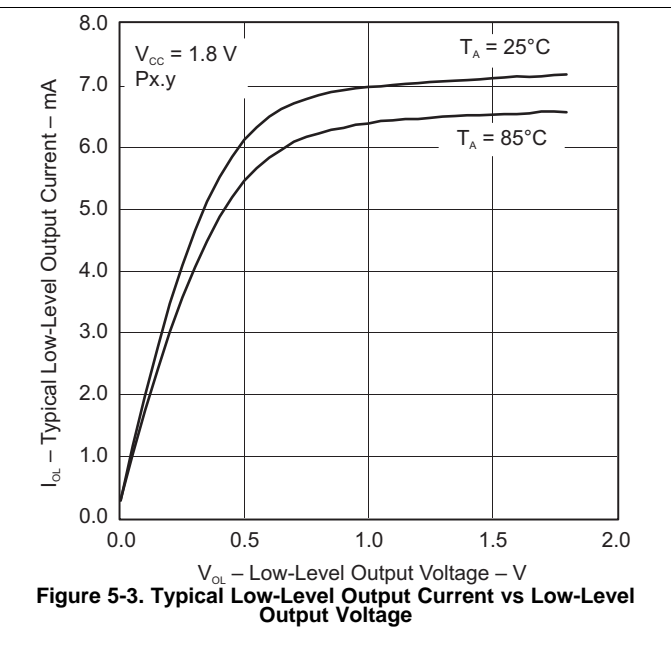
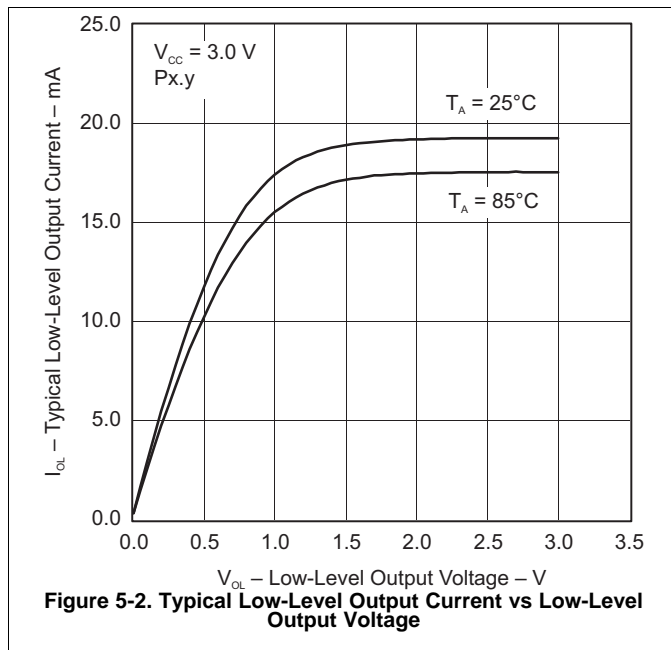
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f _{Px,y}	Port output frequency (with load)	See ⁽¹⁾ ⁽²⁾	V _{CC} = 1.8 V, PMMCOREVx = 0	16	MHz
			V _{CC} = 3 V, PMMCOREVx = 3	25	
f _{Port_CLK}	Clock output frequency	ACLK, SMCLK, or MCLK , C _L = 20 pF ⁽²⁾	V _{CC} = 1.8 V, PMMCOREVx = 0	16	MHz
			V _{CC} = 3 V, PMMCOREVx = 3	25	

- (1) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

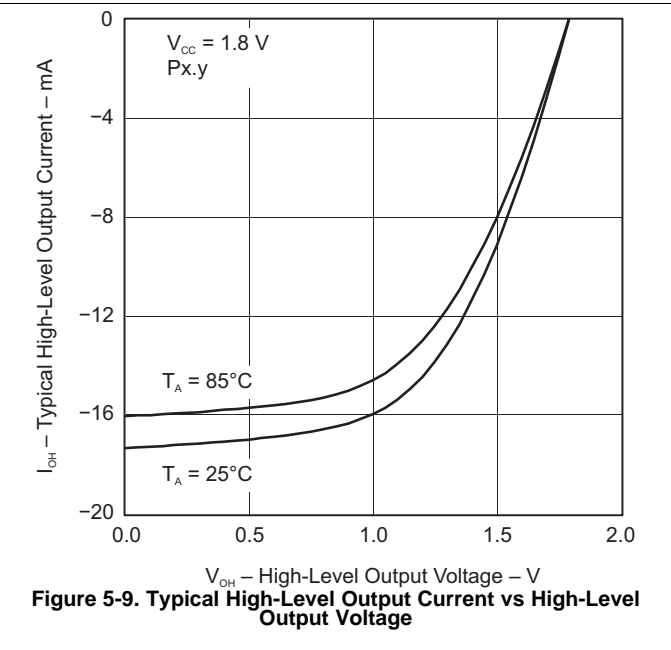
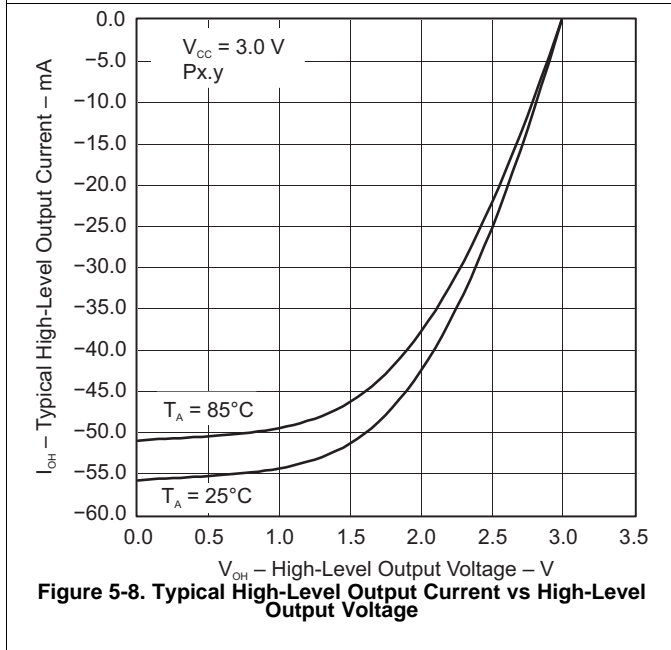
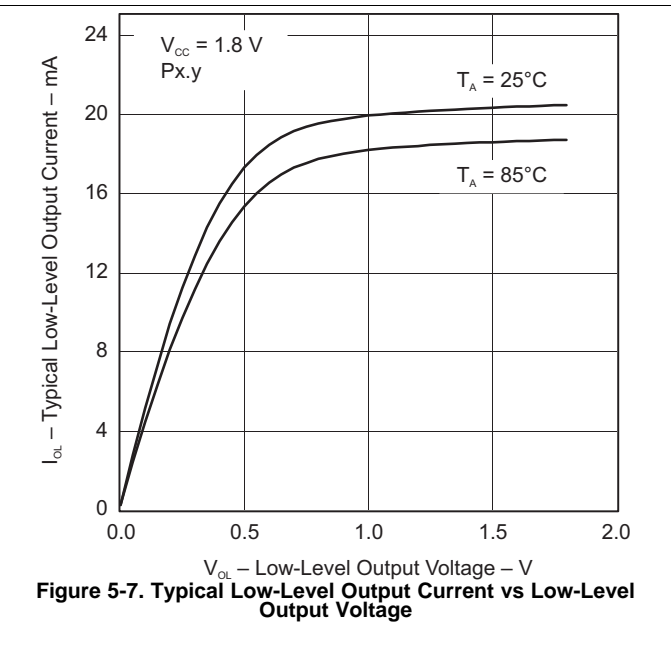
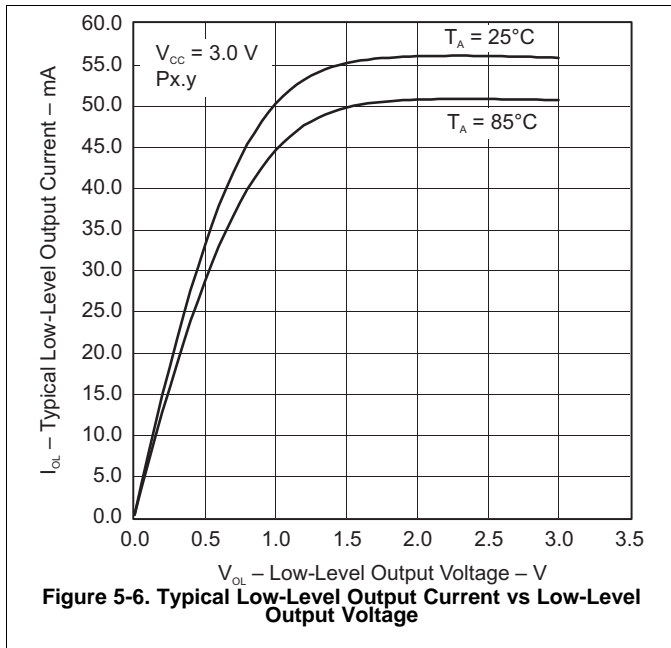
5.13 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



5.14 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



5.15 Crystal Oscillator, XT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
$\Delta I_{DVCC,LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	3 V		0.075		μA	
	$f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C						
	$f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C						
	$f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C			0.290			
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode			32768		Hz	
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode		10	32.768	50	kHz	
OA_{LF}	Oscillation allowance for LF crystals ⁽⁴⁾			210		k Ω	
							XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 6 pF
	XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 12 pF			300			
$C_{L,eff}$	Integrated effective load capacitance, LF mode ⁽⁵⁾			1		pF	
							XTS = 0, XCAP _x = 0 ⁽⁶⁾
							XTS = 0, XCAP _x = 1
							XTS = 0, XCAP _x = 2
	XTS = 0, XCAP _x = 3			12.0			
	Duty cycle, LF mode		30%		70%		
$f_{Fault,LF}$	Oscillator fault frequency, LF mode ⁽⁷⁾		10		10000	Hz	
$t_{START,LF}$	Start-up time, LF mode	3 V		1000		ms	
							$f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 6 pF
	$f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C, C _{L,eff} = 12 pF			500			

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE_x settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - For XT1DRIVE_x = 0, C_{L,eff} ≤ 6 pF.
 - For XT1DRIVE_x = 1, 6 pF ≤ C_{L,eff} ≤ 9 pF.
 - For XT1DRIVE_x = 2, 6 pF ≤ C_{L,eff} ≤ 10 pF.
 - For XT1DRIVE_x = 3, C_{L,eff} ≥ 6 pF.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

5.16 Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{DVCC,XT2}	XT2 oscillator crystal current consumption	f _{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C	3 V		200		μA
		f _{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 1, T _A = 25°C			260		
		f _{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C			325		
		f _{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 3, T _A = 25°C			450		
f _{XT2,HF0}	XT2 oscillator crystal frequency, mode 0	XT2DRIVE _x = 0, XT2BYPASS = 0 ⁽³⁾		4		8	MHz
f _{XT2,HF1}	XT2 oscillator crystal frequency, mode 1	XT2DRIVE _x = 1, XT2BYPASS = 0 ⁽³⁾		8		16	MHz
f _{XT2,HF2}	XT2 oscillator crystal frequency, mode 2	XT2DRIVE _x = 2, XT2BYPASS = 0 ⁽³⁾		16		24	MHz
f _{XT2,HF3}	XT2 oscillator crystal frequency, mode 3	XT2DRIVE _x = 3, XT2BYPASS = 0 ⁽³⁾		24		32	MHz
f _{XT2,HF,SW}	XT2 oscillator logic-level square-wave input frequency, bypass mode	XT2BYPASS = 1 ^{(4) (3)}		0.7		32	MHz
O _{AHF}	Oscillation allowance for HF crystals ⁽⁵⁾	XT2DRIVE _x = 0, XT2BYPASS = 0, f _{XT2,HF0} = 6 MHz, C _{L,eff} = 15 pF			450		Ω
		XT2DRIVE _x = 1, XT2BYPASS = 0, f _{XT2,HF1} = 12 MHz, C _{L,eff} = 15 pF			320		
		XT2DRIVE _x = 2, XT2BYPASS = 0, f _{XT2,HF2} = 20 MHz, C _{L,eff} = 15 pF			200		
		XT2DRIVE _x = 3, XT2BYPASS = 0, f _{XT2,HF3} = 32 MHz, C _{L,eff} = 15 pF			200		
t _{START,HF}	Start-up time	f _{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 15 pF	3 V		0.5		ms
		f _{OSC} = 20 MHz, XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C, C _{L,eff} = 15 pF			0.3		
C _{L,eff}	Integrated effective load capacitance, HF mode ^{(6) (1)}				1		pF
	Duty cycle	Measured at ACLK, f _{XT2,HF2} = 20 MHz		40%	50%	60%	
f _{Fault,HF}	Oscillator fault frequency ⁽⁷⁾	XT2BYPASS = 1 ⁽⁸⁾		30		300	kHz

- (1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. In general, an effective load capacitance of up to 18 pF can be supported.
- (2) To improve EMI on the XT2 oscillator the following guidelines should be observed.
 - Keep the traces between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
 - Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.
- (4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
- (5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
- (6) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

5.17 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df _{VLO} /dT	VLO frequency temperature drift	Measured at ACLK ⁽¹⁾	1.8 V to 3.6 V		0.5		%/°C
df _{VLO} /dV _{CC}	VLO frequency supply voltage drift	Measured at ACLK ⁽²⁾	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.18 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{REFO}	REFO oscillator current consumption	T _A = 25°C	1.8 V to 3.6 V		3		μA
f _{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5%	
		T _A = 25°C	3 V			±1.5%	
df _{REFO} /dT	REFO frequency temperature drift	Measured at ACLK ⁽¹⁾	1.8 V to 3.6 V		0.01		%/°C
df _{REFO} /dV _{CC}	REFO frequency supply voltage drift	Measured at ACLK ⁽²⁾	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	
t _{START}	REFO start-up time	40%/60% duty cycle	1.8 V to 3.6 V		25		μs

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.19 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0) ⁽¹⁾	DCORSELx = 0, DCOx = 0, MODx = 0	0.07	0.20	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31) ⁽¹⁾	DCORSELx = 0, DCOx = 31, MODx = 0	0.70	1.70	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0) ⁽¹⁾	DCORSELx = 1, DCOx = 0, MODx = 0	0.15	0.36	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31) ⁽¹⁾	DCORSELx = 1, DCOx = 31, MODx = 0	1.47	3.45	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0) ⁽¹⁾	DCORSELx = 2, DCOx = 0, MODx = 0	0.32	0.75	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31) ⁽¹⁾	DCORSELx = 2, DCOx = 31, MODx = 0	3.17	7.38	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0) ⁽¹⁾	DCORSELx = 3, DCOx = 0, MODx = 0	0.64	1.51	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31) ⁽¹⁾	DCORSELx = 3, DCOx = 31, MODx = 0	6.07	14.0	MHz
$f_{DCO(4,0)}$	DCO frequency (4, 0) ⁽¹⁾	DCORSELx = 4, DCOx = 0, MODx = 0	1.3	3.2	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31) ⁽¹⁾	DCORSELx = 4, DCOx = 31, MODx = 0	12.3	28.2	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0) ⁽¹⁾	DCORSELx = 5, DCOx = 0, MODx = 0	2.5	6.0	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31) ⁽¹⁾	DCORSELx = 5, DCOx = 31, MODx = 0	23.7	54.1	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0) ⁽¹⁾	DCORSELx = 6, DCOx = 0, MODx = 0	4.6	10.7	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31) ⁽¹⁾	DCORSELx = 6, DCOx = 31, MODx = 0	39.0	88.0	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0) ⁽¹⁾	DCORSELx = 7, DCOx = 0, MODx = 0	8.5	19.6	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31) ⁽¹⁾	DCORSELx = 7, DCOx = 31, MODx = 0	60	135	MHz
$S_{DCORSEL}$	Frequency step (ratio) between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)} / f_{DCO(DCORSEL,DCO)}$	1.2	2.3	
S_{DCO}	Frequency step (ratio) between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)} / f_{DCO(DCORSEL,DCO)}$	1.02	1.12	
	Duty cycle	Measured at SMCLK	40%	50%	60%
df_{DCO}/dT	DCO frequency temperature drift ⁽²⁾	$f_{DCO} = 1 \text{ MHz}$		0.1	%/°C
df_{DCO}/dV_{CC}	DCO frequency voltage drift ⁽³⁾	$f_{DCO} = 1 \text{ MHz}$		1.9	%/V

- (1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO} , should be set to reside within the range of $f_{DCO(n,0),MAX} \leq f_{DCO} \leq f_{DCO(n,31),MIN}$, where $f_{DCO(n,0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. If the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.
- (2) Calculated using the box method: $(MAX(-40^\circ\text{C} \text{ to } 85^\circ\text{C}) - MIN(-40^\circ\text{C} \text{ to } 85^\circ\text{C})) / MIN(-40^\circ\text{C} \text{ to } 85^\circ\text{C}) / (85^\circ\text{C} - (-40^\circ\text{C}))$
- (3) Calculated using the box method: $(MAX(1.8 \text{ V to } 3.6 \text{ V}) - MIN(1.8 \text{ V to } 3.6 \text{ V})) / MIN(1.8 \text{ V to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$



Figure 5-10. Typical DCO Frequency

5.20 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DVCC_BOR_IT-)}$	BOR _H on voltage, DV _{CC} falling level	$ dDV_{CC}/dt < 3 \text{ V/s}$			1.45	V
$V_{(DVCC_BOR_IT+)}$	BOR _H off voltage, DV _{CC} rising level	$ dDV_{CC}/dt < 3 \text{ V/s}$	0.80	1.30	1.50	V
$V_{(DVCC_BOR_hys)}$	BOR _H hysteresis		50		250	mV
t_{RESET}	Pulse duration required at the $\overline{\text{RST/NMI}}$ pin to accept a reset		2			μs

5.21 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{CORE3(AM)}}$	Core voltage, active mode, PMMCOREV = 3	$2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.90		V
$V_{\text{CORE2(AM)}}$	Core voltage, active mode, PMMCOREV = 2	$2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.80		V
$V_{\text{CORE1(AM)}}$	Core voltage, active mode, PMMCOREV = 1	$2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.60		V
$V_{\text{CORE0(AM)}}$	Core voltage, active mode, PMMCOREV = 0	$1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.40		V
$V_{\text{CORE3(LPM)}}$	Core voltage, low-current mode, PMMCOREV = 3	$2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.94		V
$V_{\text{CORE2(LPM)}}$	Core voltage, low-current mode, PMMCOREV = 2	$2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.84		V
$V_{\text{CORE1(LPM)}}$	Core voltage, low-current mode, PMMCOREV = 1	$2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.64		V
$V_{\text{CORE0(LPM)}}$	Core voltage, low-current mode, PMMCOREV = 0	$1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$		1.44		V

5.22 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV _{CC} = 3.6 V		0		nA
		SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 0		200		
		SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 1		1.5		μA
$V_{(SVSH_IT-)}$	SVS _H on voltage level ⁽¹⁾	SVSHE = 1, SVSHRVL = 0	1.57	1.68	1.78	V
		SVSHE = 1, SVSHRVL = 1	1.79	1.88	1.98	
		SVSHE = 1, SVSHRVL = 2	1.98	2.08	2.21	
		SVSHE = 1, SVSHRVL = 3	2.10	2.18	2.31	
$V_{(SVSH_IT+)}$	SVS _H off voltage level ⁽¹⁾	SVSHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	V
		SVSHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	
		SVSHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	
		SVSHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
		SVSHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	
		SVSHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
		SVSHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
		SVSHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
$t_{pd(SVSH)}$	SVS _H propagation delay	SVSHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVSHFP = 1		2.5		μs
		SVSHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVSHFP = 0		20		
$t_{(SVSH)}$	SVS _H on or off delay time	SVSHE = 0 → 1, dV _{DVCC} /dt = 10 mV/μs, SVSHFP = 1		12.5		μs
		SVSHE = 0 → 1, dV _{DVCC} /dt = 1 mV/μs, SVSHFP = 0		100		
dV _{DVCC} /dt	DV _{CC} rise time		0		1000	V/s

(1) The SVS_H settings available depend on the VCore (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) on recommended settings and use.

5.23 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM _H current consumption	SVMHE = 0, DV _{CC} = 3.6 V		0		nA
		SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 0		200		
		SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 1		1.5		μA
$V_{(SVMH)}$	SVM _H on or off voltage level ⁽¹⁾	SVMHE = 1, SVSMHRRRL = 0	1.62	1.74	1.85	V
		SVMHE = 1, SVSMHRRRL = 1	1.88	1.94	2.07	
		SVMHE = 1, SVSMHRRRL = 2	2.07	2.14	2.28	
		SVMHE = 1, SVSMHRRRL = 3	2.20	2.30	2.42	
		SVMHE = 1, SVSMHRRRL = 4	2.32	2.40	2.55	
		SVMHE = 1, SVSMHRRRL = 5	2.52	2.70	2.88	
		SVMHE = 1, SVSMHRRRL = 6	2.90	3.10	3.23	
		SVMHE = 1, SVSMHRRRL = 7	2.90	3.10	3.23	
$t_{pd(SVMH)}$	SVM _H propagation delay	SVMHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1		2.5		μs
		SVMHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0		20		
$t_{(SVMH)}$	SVM _H on or off delay time	SVMHE = 0 → 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1		12.5		μs
		SVMHE = 0 → 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0		100		

(1) The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervision* chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) on recommended settings and use.

5.24 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS _L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		1.5		μA
$t_{pd(SVSL)}$	SVS _L propagation delay	SVSLE = 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1		2.5		μs
		SVSLE = 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0		20		
$t_{(SVSL)}$	SVS _L on or off delay time	SVSLE = 0 → 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1		12.5		μs
		SVSLE = 0 → 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0		100		

5.25 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM _L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 0		200		
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 1		1.5		μA
$t_{pd(SVML)}$	SVM _L propagation delay	SVMLE = 1, dV _{CORE} /dt = 10 mV/μs, SVMLFP = 1		2.5		μs
		SVMLE = 1, dV _{CORE} /dt = 1 mV/μs, SVMLFP = 0		20		
$t_{(SVML)}$	SVM _L on or off delay time	SVMLE = 0 → 1, dV _{CORE} /dt = 10 mV/μs, SVMLFP = 1		12.5		μs
		SVMLE = 0 → 1, dV _{CORE} /dt = 1 mV/μs, SVMLFP = 0		100		

5.26 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{WAKE-UP-FAST}	Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽¹⁾	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	f _{MCLK} ≥ 4.0 MHz	3.5	7.5	μs
				1.0 MHz < f _{MCLK} < 4.0 MHz	4.5	
t _{WAKE-UP-SLOW}	Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽²⁾⁽³⁾	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0		150	165	μs
t _{WAKE-UP-LPM5}	Wake-up time from LPM4.5 to active mode ⁽⁴⁾			2	3	ms
t _{WAKE-UP-RESET}	Wake-up time from \overline{RST} or BOR event to active mode ⁽⁴⁾			2	3	ms

- (1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). t_{WAKE-UP-FAST} is possible with SVS_L and SVM_L in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430F5xx and MSP430F6xx Family User's Guide*.
- (2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). t_{WAKE-UP-SLOW} is set with SVS_L and SVM_L in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430F5xx and MSP430F6xx Family User's Guide*.
- (3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.
- (4) This value represents the time from the wake-up event to the reset vector execution.

5.27 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	1.8 V, 3 V		25	MHz
t _{TA,cap}	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	1.8 V, 3 V	20		ns

5.28 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	1.8 V, 3 V		25	MHz
t _{TB,cap}	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	1.8 V, 3 V	20		ns

5.29 USCI (UART Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% \pm 10%		f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			1	MHz

5.30 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
t_r	UART receive deglitch time ⁽¹⁾	2.2 V	50	600	ns
		3 V	50	600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

5.31 USCI (SPI Master Mode) Clock Frequency

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% \pm 10%		f_{SYSTEM}	MHz

5.32 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

(see [Figure 5-11](#) and [Figure 5-12](#))

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK or ACLK, Duty cycle = 50% \pm 10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time	PMMCOREV = 0	1.8 V	55	ns	
			3 V	38		
		PMMCOREV = 3	2.4 V	30		
			3 V	25		
$t_{HD,MI}$	SOMI input data hold time	PMMCOREV = 0	1.8 V	0	ns	
			3 V	0		
		PMMCOREV = 3	2.4 V	0		
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time ⁽²⁾	UCLK edge to SIMO valid, $C_L = 20$ pF, PMMCOREV = 0	1.8 V		20	ns
			3 V		18	
		UCLK edge to SIMO valid, $C_L = 20$ pF, PMMCOREV = 3	2.4 V		16	
			3 V		15	
$t_{HD,MO}$	SIMO output data hold time ⁽³⁾	$C_L = 20$ pF, PMMCOREV = 0	1.8 V	-10	ns	
			3 V	-8		
		$C_L = 20$ pF, PMMCOREV = 3	2.4 V	-10		
			3 V	-8		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave))$

For the slave parameters $t_{SU,SI}(Slave)$ and $t_{VALID,SO}(Slave)$, see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-11](#) and [Figure 5-12](#).

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 5-11](#) and [Figure 5-12](#).

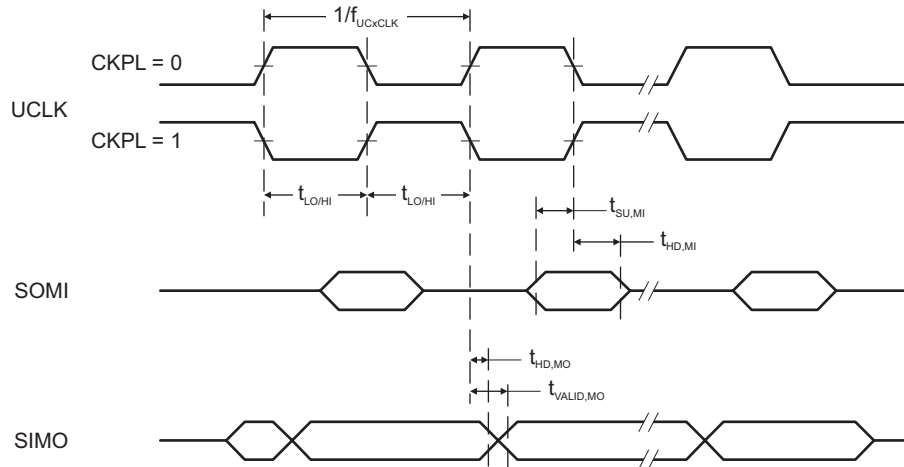


Figure 5-11. SPI Master Mode, CKPH = 0

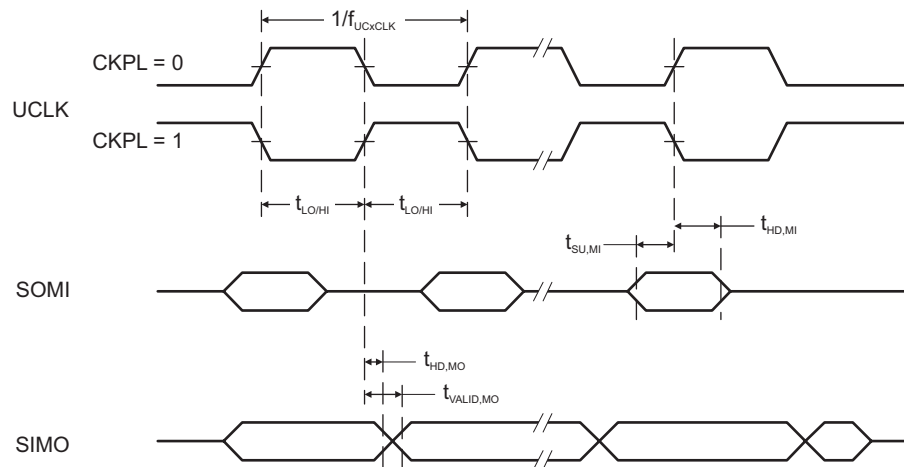


Figure 5-12. SPI Master Mode, CKPH = 1

5.33 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾
(see [Figure 5-13](#) and [Figure 5-14](#))

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
t _{STE,LEAD}	STE lead time, STE low to clock	PMMCOREV = 0	1.8 V	11	ns	
			3 V	8		
		PMMCOREV = 3	2.4 V	7		
			3 V	6		
t _{STE,LAG}	STE lag time, last clock to STE high	PMMCOREV = 0	1.8 V	3	ns	
			3 V	3		
		PMMCOREV = 3	2.4 V	3		
			3 V	3		
t _{STE,ACC}	STE access time, STE low to SOMI data out	PMMCOREV = 0	1.8 V	66	ns	
			3 V	50		
		PMMCOREV = 3	2.4 V	36		
			3 V	30		
t _{STE,DIS}	STE disable time, STE high to SOMI high impedance	PMMCOREV = 0	1.8 V	30	ns	
			3 V	23		
		PMMCOREV = 3	2.4 V	16		
			3 V	13		
t _{SU,SI}	SIMO input data setup time	PMMCOREV = 0	1.8 V	5	ns	
			3 V	5		
		PMMCOREV = 3	2.4 V	2		
			3 V	2		
t _{HD,SI}	SIMO input data hold time	PMMCOREV = 0	1.8 V	5	ns	
			3 V	5		
		PMMCOREV = 3	2.4 V	5		
			3 V	5		
t _{VALID,SO}	SOMI output data valid time ⁽²⁾	UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 0	1.8 V	76	ns	
			3 V	60		
		UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 3	2.4 V	44		
			3 V	40		
t _{HD,SO}	SOMI output data hold time ⁽³⁾	C _L = 20 pF, PMMCOREV = 0	1.8 V	18	ns	
			3 V	12		
		C _L = 20 pF, PMMCOREV = 3	2.4 V	10		
			3 V	8		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$

For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.

- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-13](#) and [Figure 5-14](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-13](#) and [Figure 5-14](#).

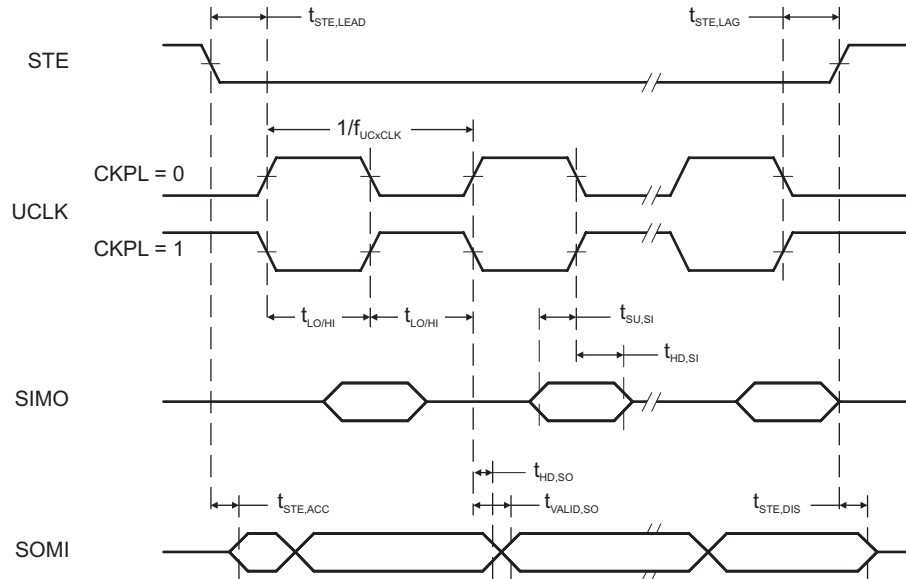


Figure 5-13. SPI Slave Mode, CKPH = 0

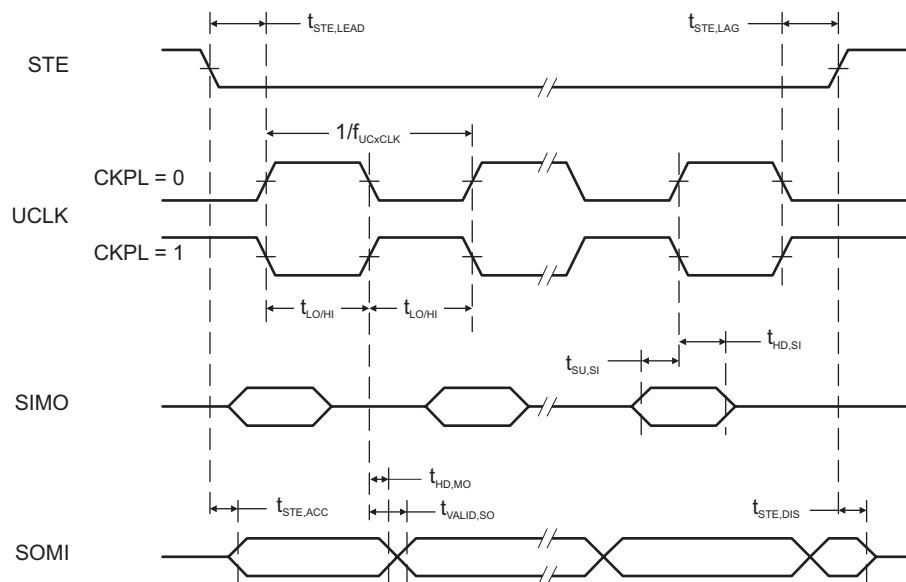


Figure 5-14. SPI Slave Mode, CKPH = 1

5.34 USCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-15](#))

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%		f _{SYSTEM}		MHz
f _{SCL}	SCL clock frequency		2.2 V, 3 V	0	400	kHz
t _{HD,STA}	Hold time (repeated) START	f _{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0		μs
		f _{SCL} > 100 kHz		0.6		
t _{SU,STA}	Setup time for a repeated START	f _{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7		μs
		f _{SCL} > 100 kHz		0.6		
t _{HD,DAT}	Data hold time		2.2 V, 3 V	0		ns
t _{SU,DAT}	Data setup time		2.2 V, 3 V	250		ns
t _{SU,STO}	Setup time for STOP	f _{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0		μs
		f _{SCL} > 100 kHz		0.6		
t _{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50	600	ns
			3 V	50	600	

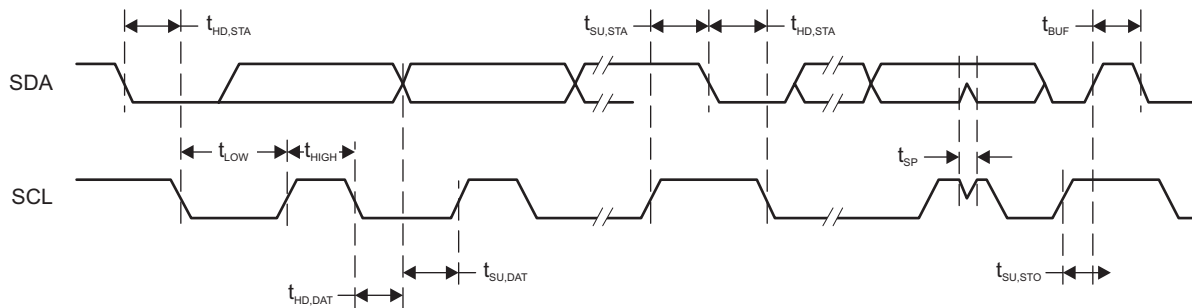


Figure 5-15. I²C Mode Timing

5.35 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
AV _{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, V _(AVSS) = V _(DVSS) = 0 V		2.2		3.6	V
V _(Ax)	Analog input voltage range ⁽²⁾	All ADC12 analog input pins Ax		0		AV _{CC}	V
I _{ADC12_A}	Operating supply current into AVCC terminal ⁽³⁾	f _{ADC12CLK} = 5.0 MHz ⁽⁴⁾	2.2 V		125	155	μA
			3 V		150	220	
C _I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20	25	pF
R _I	Input MUX ON resistance	0 V ≤ V _{Ax} ≤ AVCC		10	200	1900	Ω

(1) The leakage current is specified by the digital I/O input leakage.

(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See Section 5.40 and Section 5.41.

(3) The internal reference supply current is not included in current consumption parameter I_{ADC12_A}.

(4) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0.

5.36 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{ADC12CLK}	ADC conversion clock	For specified performance of ADC12 linearity parameters using an external reference voltage or AVCC as reference ⁽¹⁾	2.2 V, 3 V	0.45	4.8	5.0	MHz
		For specified performance of ADC12 linearity parameters using the internal reference ⁽²⁾		0.45	2.4	4.0	
		For specified performance of ADC12 linearity parameters using the internal reference ⁽³⁾		0.45	2.4	2.7	
f _{ADC12OSC}	Internal ADC12 oscillator ⁽⁴⁾	ADC12DIV = 0, f _{ADC12CLK} = f _{ADC12OSC}	2.2 V, 3 V	4.2	4.8	5.4	MHz
t _{CONVERT}	Conversion time	REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock	2.2 V, 3 V	2.4		3.1	μs
		External f _{ADC12CLK} from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			13 × 1 / f _{ADC12CLK}		
t _{Sample}	Sampling time	R _S = 400 Ω, R _I = 1000 Ω, C _I = 20 pF, τ = (R _S + R _I) × C _I ⁽⁵⁾	2.2 V, 3 V	1000			ns

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The performance of the ADC12 linearity is specified when using the ADC12OSC. For other clock sources, the performance of the ADC12 linearity is specified with f_{ADC12CLK} maximum of 5.0 MHz.

(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1

(3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.

(4) The ADC12OSC is sourced directly from MODOSC inside the UCS.

(5) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB:

$$t_{\text{Sample}} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800 \text{ ns, where } n = \text{ADC resolution} = 12, R_S = \text{external source resistance}$$

5.37 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
E _I	Integral linearity error ⁽¹⁾	1.4 V ≤ dVREF ≤ 1.6 V ⁽²⁾	2.2 V, 3 V			±2.0	LSB
		1.6 V < dVREF ⁽²⁾				±1.7	
E _D	Differential linearity error ⁽¹⁾	See ⁽²⁾	2.2 V, 3 V			±1.0	LSB
E _O	Offset error ⁽³⁾	dVREF ≤ 2.2 V ⁽²⁾	2.2 V, 3 V		±1.0	±2.0	LSB
		dVREF > 2.2 V ⁽²⁾	2.2 V, 3 V		±1.0	±2.0	
E _G	Gain error ⁽³⁾	See ⁽²⁾	2.2 V, 3 V		±1.0	±2.0	LSB
E _T	Total unadjusted error	dVREF ≤ 2.2 V ⁽²⁾	2.2 V, 3 V		±1.4	±3.5	LSB
		dVREF > 2.2 V ⁽²⁾	2.2 V, 3 V		±1.4	±3.5	

(1) Parameters are derived using the histogram method.

(2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = V_{R+} - V_{R-}, V_{R+} < AVCC, V_{R-} > AVSS. Unless otherwise noted, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω and two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current. Also see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

(3) Parameters are derived using a best fit curve.

5.38 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	V _{CC}	MIN	TYP	MAX	UNIT
E _I	Integral linearity error ⁽²⁾	ADC12SR = 0, REFOUT = 1, f _{ADC12CLK} ≤ 4.0 MHz	2.2 V, 3 V			±1.7	LSB
		ADC12SR = 0, REFOUT = 0, f _{ADC12CLK} ≤ 2.7 MHz				±2.5	
E _D	Differential linearity error ⁽²⁾	ADC12SR = 0, REFOUT = 1, f _{ADC12CLK} ≤ 4.0 MHz	2.2 V, 3 V	-1.0		+2.0	LSB
		ADC12SR = 0, REFOUT = 1, f _{ADC12CLK} ≤ 2.7 MHz		-1.0		+1.5	
		ADC12SR = 0, REFOUT = 0, f _{ADC12CLK} ≤ 2.7 MHz		-1.0		+2.5	
E _O	Offset error ⁽³⁾	ADC12SR = 0, REFOUT = 1, f _{ADC12CLK} ≤ 4.0 MHz	2.2 V, 3 V		±1.0	±2.0	LSB
		ADC12SR = 0, REFOUT = 0, f _{ADC12CLK} ≤ 2.7 MHz			±1.0	±2.0	
E _G	Gain error ⁽³⁾	ADC12SR = 0, REFOUT = 1, f _{ADC12CLK} ≤ 4.0 MHz	2.2 V, 3 V		±1.0	±2.0	LSB
		ADC12SR = 0, REFOUT = 0, f _{ADC12CLK} ≤ 2.7 MHz				±1.5% ⁽⁴⁾	
E _T	Total unadjusted error	ADC12SR = 0, REFOUT = 1, f _{ADC12CLK} ≤ 4.0 MHz	2.2 V, 3 V		±1.4	±3.5	LSB
		ADC12SR = 0, REFOUT = 0, f _{ADC12CLK} ≤ 2.7 MHz				±1.5% ⁽⁴⁾	

(1) The internal reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 1. dVREF = V_{R+} - V_{R-}.

(2) Parameters are derived using the histogram method.

(3) Parameters are derived using a best fit curve.

(4) The gain error and total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode, the reference voltage used by the ADC12_A is not available on a pin.

5.39 12-Bit ADC, Temperature Sensor and Built-In V_{MID} ⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	See ⁽²⁾ and Figure 5-16	ADC12ON = 1, INCH = 0Ah, $T_A = 0^\circ\text{C}$	2.2 V	680			mV
			3 V	680			
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V	2.25			mV/ $^\circ\text{C}$
			3 V	2.25			
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected ⁽³⁾	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	100			μs
			3 V	100			
V_{MID}	AV_{CC} divider at channel 11, V_{AVCC} factor	ADC12ON = 1, INCH = 0Bh		0.48	0.5	0.52	V_{AVCC}
	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh	2.2 V	1.06	1.1	1.14	V
			3 V	1.44	1.5	1.56	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected ⁽⁴⁾	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V, 3 V	1000			ns

- (1) The temperature sensor is provided by the REF module. See the REF module parametric, I_{REF+} , regarding the current consumption of the temperature sensor.
- (2) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor. The TLV structure contains calibration values for $30^\circ\text{C} \pm 3^\circ\text{C}$ and $85^\circ\text{C} \pm 3^\circ\text{C}$ for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature}, ^\circ\text{C}) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy. Also see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).
- (3) The typical equivalent impedance of the sensor is 51 k Ω . The sample time required includes the sensor on-time $t_{SENSOR(on)}$.
- (4) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

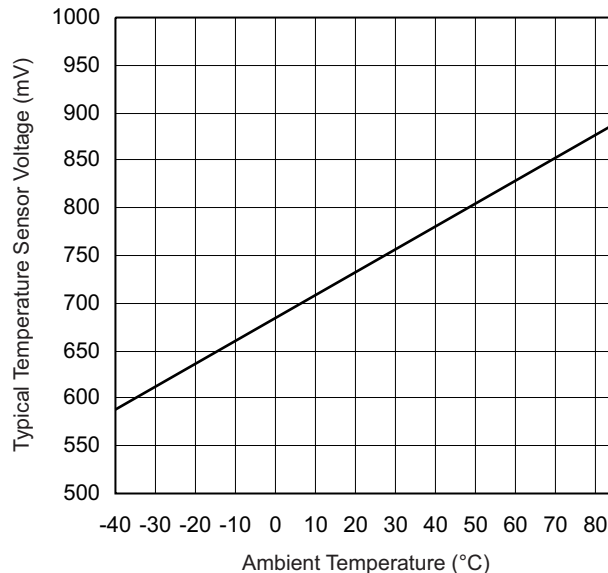


Figure 5-16. Typical Temperature Sensor Voltage

5.40 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{eREF+}	Positive external reference voltage input	V _{eREF+} > V _{REF} /V _{eREF-} ⁽²⁾		1.4	AV _{CC}	V
V _{REF} /V _{eREF-}	Negative external reference voltage input	V _{eREF+} > V _{REF} /V _{eREF-} ⁽³⁾		0	1.2	V
(V _{eREF+} – V _{REF} /V _{eREF-})	Differential external reference voltage input	V _{eREF+} > V _{REF} /V _{eREF-} ⁽⁴⁾		1.4	AV _{CC}	V
I _{VeREF+} , I _{VREF-/VeREF-}	Static input current	1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF-} = 0 V, f _{ADC12CLK} = 5 MHz, ADC12SHTx = 1h, Conversion rate 200 kpsps	2.2 V, 3 V	-26	26	μA
		1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF-} = 0 V, f _{ADC12CLK} = 5 MHz, ADC12SHTx = 8h, Conversion rate 20 kpsps	2.2 V, 3 V	-1	1	
C _{VREF+/-}	Capacitance at VREF+ or VREF- terminal			⁽⁵⁾ 10		μF

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- (5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. Also see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

5.41 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{REF+}	REFVSEL = {2} for 2.5 V, REFON = REFOUT = 1, I _{VREF+} = 0 A	3 V	2.4625	2.50	2.5375	V
	REFVSEL = {1} for 2.0 V, REFON = REFOUT = 1, I _{VREF+} = 0 A	3 V	1.9503	1.98	2.0097	
	REFVSEL = {0} for 1.5 V, REFON = REFOUT = 1, I _{VREF+} = 0 A	2.2 V, 3 V	1.4677	1.49	1.5124	
AV _{CC(min)}	REFVSEL = {0} for 1.5 V		2.2			V
	REFVSEL = {1} for 2.0 V		2.3			
	REFVSEL = {2} for 2.5 V		2.8			
I _{REF+}	ADC12SR = 1 ⁽⁴⁾ , REFON = 1, REFOUT = 0, REFBURST = 0	3 V		70	100	μA
	ADC12SR = 1 ⁽⁴⁾ , REFON = 1, REFOUT = 1, REFBURST = 0			0.45	0.75	mA
	ADC12SR = 0 ⁽⁴⁾ , REFON = 1, REFOUT = 0, REFBURST = 0			210	310	μA
	ADC12SR = 0 ⁽⁴⁾ , REFON = 1, REFOUT = 1, REFBURST = 0			0.95	1.7	mA
I _{L(VREF+)}	REFVSEL = {0, 1, 2}, I _{VREF+} = +10 μA or -1000 μA, AV _{CC} = AV _{CC(min)} for each reference level, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1				2500	μV/mA
C _{VREF+}	REFON = REFOUT = 1		20		100	pF
TC _{REF+}	I _{VREF+} = 0 A, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1			30	50	ppm/ °C
PSRR _{DC}	AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1			120	300	μV/V
PSRR _{AC}	AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, f = 1 kHz, ΔV _{pp} = 100 mV, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1			6.4		mV/V
t _{SETTLE}	AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , REFVSEL = {0, 1, 2}, REFOUT = 0, REFON = 0 → 1			75		μs
	AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , C _{VREF} = C _{VREF(max)} , REFVSEL = {0, 1, 2}, REFOUT = 1, REFON = 0 → 1			75		

- The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger, for driving the VREF+ terminal. When REFOUT = 1, the reference is available at the VREF+ terminal and is used as the reference for the conversion and uses the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and uses the smaller buffer.
- The internal reference current is supplied from the AVCC terminal. Consumption is independent of the ADC12ON control bit, unless a conversion is active. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.
- The temperature sensor is provided by the REF module. Its current is supplied from the AVCC terminal and is equivalent to I_{REF+} with REFON = 1 and REFOUT = 0.
- For devices without the ADC12, the parametric with ADC12SR = 0 are applicable.
- Contribution only due to the reference and buffer including package. This does not include resistance due to factors such as PCB traces.
- Calculated using the box method: (MAX(-40°C to 85°C) – MIN(-40°C to 85°C)) / MIN(-40°C to 85°C)/(85°C – (-40°C)).
- The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.

5.42 Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage			1.8		3.6	V
I _{AVCC_COMP}	Comparator operating supply current into AVCC, Excludes reference resistor ladder	CBPWRMD = 00	1.8 V			40	μA
			2.2 V		30	50	
			3 V		40	65	
		CBPWRMD = 01	2.2 V, 3 V		10	30	
		CBPWRMD = 10	2.2 V, 3 V		0.1	0.5	
I _{AVCC_REF}	Quiescent current of local reference voltage amplifier into AVCC	CBREFACC = 1, CBREFLx = 01				22	μA
V _{IC}	Common mode input range			0		V _{CC} - 1	V
V _{OFFSET}	Input offset voltage	CBPWRMD = 00				±20	mV
		CBPWRMD = 01, 10				±10	
C _{IN}	Input capacitance				5		pF
R _{SIN}	Series input resistance	ON, switch closed			3	4	kΩ
		OFF, switch opened		30			MΩ
t _{PD}	Propagation delay, response time	CBPWRMD = 00, CBF = 0				450	ns
		CBPWRMD = 01, CBF = 0				600	
		CBPWRMD = 10, CBF = 0				50	μs
t _{PD,filter}	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 00		0.35	0.6	1.0	μs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 01		0.6	1.0	1.8	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 10		1.0	1.8	3.4	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBF _{DLY} = 11		1.8	3.4	6.5	
t _{EN_CMP}	Comparator enable time	CBON = 0 to CBON = 1, CBPWRMD = 00, 01			1	2	μs
		CBON = 0 to CBON = 1, CBPWRMD = 10				100	
t _{EN_REF}	Resistor reference enable time	CBON = 0 to CBON = 1			1	1.5	μs
V _{CB_REF}	Reference voltage for a given tap	V _{IN} = reference into resistor ladder (n = 0 to 31)			V _{IN} × (n + 1) / 32		V

5.43 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T _J	MIN	TYP	MAX	UNIT
DV _{CC(PGM/ERASE)}	Program or erase supply voltage		1.8		3.6	V
I _{PGM}	Average supply current from DVCC during program			3	5	mA
I _{ERASE}	Average supply current from DVCC during erase			6	11	mA
I _{MERASE} , I _{BANK}	Average supply current from DVCC during mass erase or bank erase			6	11	mA
t _{CPT}	Cumulative program time ⁽¹⁾				16	ms
	Program and erase endurance		10 ⁴	10 ⁵		cycles
t _{Retention}	Data retention duration	25°C	100			years
t _{Word}	Word or byte program time ⁽²⁾		64		85	μs
t _{Block, 0}	Block program time for first byte or word ⁽²⁾		49		65	μs
t _{Block, 1–(N–1)}	Block program time for each additional byte or word, except for last byte or word ⁽²⁾		37		49	μs
t _{Block, N}	Block program time for last byte or word ⁽²⁾		55		73	μs
t _{Erase}	Erase time for segment, mass erase, and bank erase (when available) ⁽²⁾		23		32	ms
f _{MCLK,MGR}	MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.

(2) These values are hardwired into the state machine of the flash controller.

5.44 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V _{CC}	MIN	TYP	MAX	UNIT
f _{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
t _{SBW,Low}	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	μs
t _{SBW,En}	Spy-Bi-Wire enable time, TEST high to acceptance of first clock edge ⁽¹⁾	2.2 V, 3 V			1	μs
t _{SBW,Rst}	Spy-Bi-Wire return to normal operation time		15		100	μs
f _{TCK}	TCK input frequency, 4-wire JTAG ⁽²⁾	2.2 V	0		5	MHz
		3 V	0		10	
R _{Internal}	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see [Figure 6-1](#)).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

Figure 6-1. CPU Registers

6.2 Operating Modes

These microcontrollers have one active mode and six software-selectable low-power modes of operation. An interrupt event can wake the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active
 - MCLK is disabled
 - FLL loop control remains active
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - FLL loop control is disabled
 - ACLK and SMCLK remain active
 - MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO is disabled
 - Crystal oscillator is stopped
 - Complete data retention
- Low-power mode 4.5 (LPM4.5)
 - Internal regulator disabled
 - No data retention
 - Wake-up input from $\overline{\text{RST}}$ /NMI, P1, and P2

6.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see [Table 6-1](#)). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-1. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up External reset Watchdog time-out, password violation Flash memory password violation PMM password violation	WDTIFG, KEYV (SYSRSTIV) ^{(1) (2)}	Reset	0FFFEh	63, highest
System NMI PMM Vacant memory access JTAG mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBINIFG, JMBOUTIFG (SYSSNIV) ⁽¹⁾	(Non)maskable	0FFFCCh	62
User NMI NMI Oscillator fault Flash memory access violation	NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV) ^{(1) (2)}	(Non)maskable	0FFFAh	61
Comp_B	Comparator B interrupt flags (CBIV) ^{(1) (3)}	Maskable	0FFF8h	60
TB0	TB0CCR0 CCIFG0 ⁽³⁾	Maskable	0FFF6h	59
TB0	TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV) ^{(1) (3)}	Maskable	0FFF4h	58
Watchdog Timer_A interval timer mode	WDTIFG	Maskable	0FFF2h	57
USCI_A0 receive or transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV) ^{(1) (3)}	Maskable	0FFF0h	56
USCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG (UCB0IV) ^{(1) (3)}	Maskable	0FFEEh	55
ADC12_A	ADC12IFG0 to ADC12IFG15 (ADC12IV) ^{(1) (3) (4)}	Maskable	0FFECCh	54
TA0	TA0CCR0 CCIFG0 ⁽³⁾	Maskable	0FFEAh	53
TA0	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV) ^{(1) (3)}	Maskable	0FFE8h	52
Reserved	Reserved	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ^{(1) (3)}	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0 ⁽³⁾	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) ^{(1) (3)}	Maskable	0FFE0h	48
I/O port P1	P1IFG.0 to P1IFG.7 (P1IV) ^{(1) (3)}	Maskable	0FFDEh	47
USCI_A1 receive or transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV) ^{(1) (3)}	Maskable	0FFDCh	46
USCI_B1 receive or transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV) ^{(1) (3)}	Maskable	0FFDAh	45
TA2	TA2CCR0 CCIFG0 ⁽³⁾	Maskable	0FFD8h	44
TA2	TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV) ^{(1) (3)}	Maskable	0FFD6h	43
I/O port P2	P2IFG.0 to P2IFG.7 (P2IV) ^{(1) (3)}	Maskable	0FFD4h	42
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) ^{(1) (3)}	Maskable	0FFD2h	41

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.

(3) Interrupt flags are in the module.

(4) Only on devices with ADC, otherwise reserved.

Table 6-1. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Reserved	Reserved ⁽⁵⁾		0FFD0h	40
			⋮	⋮
			0FF80h	0, lowest

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

6.4 Memory Organization

Table 6-2 summarizes the memory map for all device variants.

Table 6-2. Memory Organization⁽¹⁾

		MSP430F5340	MSP430F5341	MSP430F5342
Memory (flash) Main: interrupt vector	Total Size	64KB 00FFFFh to 00FF80h	96KB 00FFFFh to 00FF80h	128KB 00FFFFh to 00FF80h
Main: code memory	Bank D	N/A	N/A	32KB 0243FFh to 01C400h
	Bank C	N/A	32KB 01C3FFh to 014400h	32KB 01C3FFh to 014400h
	Bank B	32KB 0143FFh to 00C400h	32KB 0143FFh to 00C400h	32KB 0143FFh to 00C400h
	Bank A	32KB 00C3FFh to 004400h	32KB 00C3FFh to 004400h	32KB 00C3FFh to 004400h
RAM	Sector 3	N/A	N/A	2 KB 0043FFh to 003C00h
	Sector 2	N/A	2KB 003BFFh to 003400h	2KB 003BFFh to 003400h
	Sector 1	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h
	Sector 0	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h
	Sector 7	2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h
Information memory (flash)	Info A	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h
	Info B	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h
	Info C	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h
	Info D	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h
Bootloader (BSL) memory (flash)	BSL 3	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h
	BSL 2	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h
	BSL 1	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h
	BSL 0	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h
Peripherals	Size	4KB 000FFFh to 0h	4KB 000FFFh to 0h	4KB 000FFFh to 0h

(1) N/A = Not available

6.5 Bootloader (BSL)

The BSL lets users program the flash memory or RAM using a UART serial interface. Access to the device memory through the BSL is protected by an user-defined password. [Table 6-3](#) lists the pins that are required to use the BSL. BSL entry requires a specific entry sequence on the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ and $\text{TEST}/\text{SBWTCK}$ pins. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For complete description of the features of the BSL and its implementation, see [MSP430 Flash Device Bootloader \(BSL\) User's Guide](#).

Table 6-3. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	Entry sequence signal
$\text{TEST}/\text{SBWTCK}$	Entry sequence signal
P1.1	Data transmit
P1.2	Data receive
VCC	Power supply
VSS	Ground supply

6.6 JTAG Operation

6.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The $\text{TEST}/\text{SBWTCK}$ pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ is required to interface with MSP430 development tools and device programmers. [Table 6-4](#) lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

Table 6-4. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
$\text{TEST}/\text{SBWTCK}$	IN	Enable JTAG pins
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	IN	External reset
VCC		Power supply
VSS		Ground supply

6.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. [Table 6-5](#) lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#).

Table 6-5. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}/\text{NMI}/\text{SBWDIO}$	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

6.7 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

6.8 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data are lost. Features of the RAM include:

- RAM has n sectors. See [Section 6.4](#) for the size of a sector.
- Each sector 0 to n can be completely disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

6.9.1 Digital I/O

Up to eight 8-bit I/O ports are implemented. For 80-pin options, P1, P2, P3, P4, P5, P6, and P7 are complete, and P8 is reduced to 3-bit I/O. For 64-pin options, P3 and P5 are reduced to 5-bit I/O and 6-bit I/O, respectively, and P7 and P8 are completely removed. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wake-up input capability available for all bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P8) or word-wise in pairs (PA through PD).

6.9.2 Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4 (see [Table 6-6](#)). [Table 6-7](#) lists the default settings for all pins that support port mapping.

Table 6-6. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_CBOU0	–	Comparator_B output
	PM_TB0CLK	TB0 clock input	–

Table 6-6. Port Mapping Mnemonics and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
2	PM_ADC12CLK	–	ADC12CLK
	PM_DMAE0	DMAE0 input	–
3	PM_SVMOUT	–	SVM output
	PM_TB0OUTH	TB0 high-impedance input TB0OUTH	–
4	PM_TB0CCR0A	TB0 CCR0 capture input CCI0A	TB0 CCR0 compare output Out0
5	PM_TB0CCR1A	TB0 CCR1 capture input CCI1A	TB0 CCR1 compare output Out1
6	PM_TB0CCR2A	TB0 CCR2 capture input CCI2A	TB0 CCR2 compare output Out2
7	PM_TB0CCR3A	TB0 CCR3 capture input CCI3A	TB0 CCR3 compare output Out3
8	PM_TB0CCR4A	TB0 CCR4 capture input CCI4A	TB0 CCR4 compare output Out4
9	PM_TB0CCR5A	TB0 CCR5 capture input CCI5A	TB0 CCR5 compare output Out5
10	PM_TB0CCR6A	TB0 CCR6 capture input CCI6A	TB0 CCR6 compare output Out6
11	PM_UCA1RXD	USCI_A1 UART RXD (Direction controlled by USCI – input)	
	PM_UCA1SOMI	USCI_A1 SPI slave out master in (direction controlled by USCI)	
12	PM_UCA1TXD	USCI_A1 UART TXD (Direction controlled by USCI – output)	
	PM_UCA1SIMO	USCI_A1 SPI slave in master out (direction controlled by USCI)	
13	PM_UCA1CLK	USCI_A1 clock input/output (direction controlled by USCI)	
	PM_UCB1STE	USCI_B1 SPI slave transmit enable (direction controlled by USCI)	
14	PM_UCB1SOMI	USCI_B1 SPI slave out master in (direction controlled by USCI)	
	PM_UCB1SCL	USCI_B1 I ² C clock (open drain and direction controlled by USCI)	
15	PM_UCB1SIMO	USCI_B1 SPI slave in master out (direction controlled by USCI)	
	PM_UCB1SDA	USCI_B1 I ² C data (open drain and direction controlled by USCI)	
16	PM_UCB1CLK	USCI_B1 clock input/output (direction controlled by USCI)	
	PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI)	
17	PM_CBOUT1	None	Comparator_B output
18	PM_MCLK	None	MCLK
19-30	Reserved	None	DVSS
31 (0FFh) ⁽¹⁾	PM_ANALOG	Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is 0FFh. The port mapping registers are 5 bits wide, and the upper bits are ignored, which results in a read out value of 31.

Table 6-7. Default Mapping

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P4.0/P4MAP0	PM_UCB1STE/PM_UCA1CLK	USCI_B1 SPI slave transmit enable (direction controlled by USCI) USCI_A1 clock input/output (direction controlled by USCI)	
P4.1/P4MAP1	PM_UCB1SIMO/PM_UCB1SDA	USCI_B1 SPI slave in master out (direction controlled by USCI) USCI_B1 I ² C data (open drain and direction controlled by USCI)	
P4.2/P4MAP2	PM_UCB1SOMI/PM_UCB1SCL	USCI_B1 SPI slave out master in (direction controlled by USCI) USCI_B1 I ² C clock (open drain and direction controlled by USCI)	
P4.3/P4MAP3	PM_UCB1CLK/PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI) USCI_B1 clock input/output (direction controlled by USCI)	
P4.4/P4MAP4	PM_UCA1TXD/PM_UCA1SIMO	USCI_A1 UART TXD (Direction controlled by USCI – output) USCI_A1 SPI slave in master out (direction controlled by USCI)	
P4.5/P4MAP5	PM_UCA1RXD/PM_UCA1SOMI	USCI_A1 UART RXD (Direction controlled by USCI – input) USCI_A1 SPI slave out master in (direction controlled by USCI)	
P4.6/P4MAP6	PM_NONE	None	DVSS
P4.7/P4MAP7	PM_NONE	None	DVSS

6.9.3 Oscillator and System Clock

The clock system is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (XT1 LF mode; XT1 HF mode not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features a digital frequency-locked loop (FLL) that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3.5 μ s (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally controlled oscillator (DCO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by the same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by the same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

6.9.4 Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

6.9.5 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

6.9.6 Real-Time Clock (RTC_A)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer or counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

6.9.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.8 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, as well as configuration management (device descriptors). The SYS module also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. [Table 6-8](#) lists the interrupt vector registers of the SYS module.

Table 6-8. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		$\overline{\text{RST}}$ /NMI (POR)	04h	
		PMMSWBOR (BOR)	06h	
		Wakeup from LPMx.5	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		PMMSWPOR (POR)	14h	
		WDT time-out (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		Reserved	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
Reserved	22h to 3Eh	Lowest		
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		SVSMLDLYIFG	06h	
		SVSMHDLYIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		SVMLVLRIFG	10h	
		SVMHVLRFIFG	12h	
		Reserved	14h to 1Eh	Lowest
		SYSUNIV, User NMI	019Ah	No interrupt pending
NMIIFG	02h			Highest
OFIFG	04h			
ACCVIFG	06h			
Reserved	08h			
Reserved	0Ah to 1Eh			Lowest

6.9.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can move data from the ADC12_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. [Table 6-9](#) lists the available DMA triggers.

Table 6-9. DMA Trigger Assignments⁽¹⁾

TRIGGER	CHANNEL		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA2CCR2 CCIFG	TA2CCR2 CCIFG	TA2CCR2 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG
24	ADC12IFGx	ADC12IFGx	ADC12IFGx
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) If a reserved trigger source is selected, no trigger is generated.

6.9.10 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3- or 4-pin) or I²C.

The MSP430F534x MCUs include two complete USCI modules (n = 0, 1).

6.9.11 TA0

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 6-10](#)). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-10. TA0 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
13-P1.0	TA0CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
13-P1.0	TA0CLK	$\overline{\text{TACLK}}$				
14-P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	14-P1.1
	DV _{SS}	CCI0B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
15-P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	15-P1.2
	CBOUT (internal)	CCI1B				ADC12 (internal) ADC12SHSx = {1}
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
16-P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	16-P1.3
	ACLK (internal)	CCI2B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
17-P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	17-P1.4
	DV _{SS}	CCI3B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
18-P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	18-P1.5
	DV _{SS}	CCI4B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				

6.9.12 TA1

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 6-11](#)). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-11. TA1 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
19-P1.6	TA1CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
19-P1.6	TA1CLK	$\overline{\text{TACLK}}$				
20-P1.7	TA1.0	CCI0A	CCR0	TA0	TA1.0	20-P1.7
	DV _{SS}	CCI0B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
Not available	TA1.1	CCI1A	CCR1	TA1	TA1.1	Not available
	CBOUT (internal)	CCI1B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
Not available	TA1.2	CCI2A	CCR2	TA2	TA1.2	Not available
	ACLK (internal)	CCI2B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				

6.9.13 TA2

TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA2 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 6-12](#)). TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. TA2 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
Not available	TA2CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
Not available	TA2CLK	\overline{TACLK}				
Not available	TA2.0	CCI0A	CCR0	TA0	TA2.0	Not available
	DV _{SS}	CCI0B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
Not available	TA2.1	CCI1A	CCR1	TA1	TA2.1	Not available
	CBOUT (internal)	CCI1B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
Not available	TA2.2	CCI2A	CCR2	TA2	TA2.2	Not available
	ACLK (internal)	CCI2B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				

6.9.14 TB0

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. TB0 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 6-13](#)). TB0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-13. TB0 Signal Connections

INPUT PIN NUMBER ⁽¹⁾	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER ⁽¹⁾
	TB0CLK	TBCLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
	TB0CLK	$\overline{\text{TBCLK}}$				
	TB0.0	CCIOA	CCR0	TB0	TB0.0	
	TB0.0	CCIOB				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
37-P5.7	TB0.1	CCI1A	CCR1	TB1	TB0.1	37-P5.7
	CBOUT (internal)	CCI1B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
	TB0.2	CCI2A	CCR2	TB2	TB0.2	
	TB0.2	CCI2B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
	TB0.3	CCI3A	CCR3	TB3	TB0.3	
	TB0.3	CCI3B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
	TB0.4	CCI4A	CCR4	TB4	TB0.4	
	TB0.4	CCI4B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
	TB0.5	CCI5A	CCR5	TB5	TB0.5	
	TB0.5	CCI5B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
	TB0.6	CCI6A	CCR6	TB6	TB0.6	
	ACLK (internal)	CCI6B				
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				

(1) Timer functions selectable through the port mapping controller.

6.9.15 *Comparator_B*

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.9.16 *ADC12_A*

The ADC12_A module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

6.9.17 *CRC16*

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.9.18 *Reference (REF) Module Voltage Reference*

The REF module generates all critical reference voltages that can be used by the various analog peripherals in the device.

6.9.19 *Embedded Emulation Module (EEM)*

The EEM supports real-time in-system debugging. The L version of the EEM has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware trigger or breakpoint on CPU register write access
- Up to 10 hardware triggers can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

6.9.20 Peripheral File Map

Table 6-14 lists the base address for all of the peripherals that are available. Table 6-15 through Table 6-41 list the registers available in each peripheral.

Table 6-14. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 6-15)	0100h	000h to 01Fh
PMM (see Table 6-16)	0120h	000h to 010h
Flash Control (see Table 6-17)	0140h	000h to 00Fh
CRC16 (see Table 6-18)	0150h	000h to 007h
RAM Control (see Table 6-19)	0158h	000h to 001h
Watchdog (see Table 6-20)	015Ch	000h to 001h
UCS (see Table 6-21)	0160h	000h to 01Fh
SYS (see Table 6-22)	0180h	000h to 01Fh
Shared Reference (see Table 6-23)	01B0h	000h to 001h
Port Mapping Control (see Table 6-24)	01C0h	000h to 002h
Port Mapping Port P4 (see Table 6-24)	01E0h	000h to 007h
Port P1 and P2 (see Table 6-25)	0200h	000h to 01Fh
Port P3 and P4 (see Table 6-26)	0220h	000h to 00Bh
Port P5 and P6 (see Table 6-27)	0240h	000h to 00Bh
Port PJ (see Table 6-28)	0320h	000h to 01Fh
TA0 (see Table 6-29)	0340h	000h to 02Eh
TA1 (see Table 6-30)	0380h	000h to 02Eh
TB0 (see Table 6-31)	03C0h	000h to 02Eh
TA2 (see Table 6-32)	0400h	000h to 02Eh
Real-Time Clock (RTC_A) (see Table 6-33)	04A0h	000h to 01Bh
32-Bit Hardware Multiplier (see Table 6-34)	04C0h	000h to 02Fh
DMA General Control (see Table 6-35)	0500h	000h to 00Fh
DMA Channel 0 (see Table 6-35)	0510h	000h to 00Ah
DMA Channel 1 (see Table 6-35)	0520h	000h to 00Ah
DMA Channel 2 (see Table 6-35)	0530h	000h to 00Ah
USCI_A0 (see Table 6-36)	05C0h	000h to 01Fh
USCI_B0 (see Table 6-37)	05E0h	000h to 01Fh
USCI_A1 (see Table 6-38)	0600h	000h to 01Fh
USCI_B1 (see Table 6-39)	0620h	000h to 01Fh
ADC12_A (see Table 6-40)	0700h	000h to 03Eh
Comparator_B (see Table 6-41)	08C0h	000h to 00Fh

Table 6-15. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-16. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high-side control	SVSMHCTL	04h
SVS low-side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

Table 6-17. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 6-18. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 6-19. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 6-20. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 6-21. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 6-22. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 6-23. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

**Table 6-24. Port Mapping Registers
(Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)**

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping key/ID	P4MAPKEYID	00h
Port mapping control	P4MAPCTL	02h
Port P4.0 mapping	P4MAP0	00h
Port P4.1 mapping	P4MAP1	01h
Port P4.2 mapping	P4MAP2	02h
Port P4.3 mapping	P4MAP3	03h
Port P4.4 mapping	P4MAP4	04h
Port P4.5 mapping	P4MAP5	05h
Port P4.6 mapping	P4MAP6	06h
Port P4.7 mapping	P4MAP7	07h

Table 6-25. Port P1 and P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 resistor enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 resistor enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 6-26. Port P3 and P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 resistor enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 resistor enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

Table 6-27. Port P5 and P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 resistor enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 resistor enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 6-28. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ resistor enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 6-29. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TAOCTL	00h
Capture/compare control 0	TAOCCTL0	02h
Capture/compare control 1	TAOCCTL1	04h
Capture/compare control 2	TAOCCTL2	06h
Capture/compare control 3	TAOCCTL3	08h
Capture/compare control 4	TAOCCTL4	0Ah
TA0 counter	TAOR	10h
Capture/compare 0	TAOCCR0	12h
Capture/compare 1	TAOCCR1	14h
Capture/compare 2	TAOCCR2	16h
Capture/compare 3	TAOCCR3	18h
Capture/compare 4	TAOCCR4	1Ah
TA0 expansion 0	TAOEX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 6-30. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 6-31. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
Capture/compare 3	TB0CCR3	18h
Capture/compare 4	TB0CCR4	1Ah
Capture/compare 5	TB0CCR5	1Ch
Capture/compare 6	TB0CCR6	1Eh
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 6-32. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter	TA2R	10h
Capture/compare 0	TA2CCR0	12h
Capture/compare 1	TA2CCR1	14h
Capture/compare 2	TA2CCR2	16h
TA2 expansion 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 6-33. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds, RTC counter 1	RTCSEC, RTCNT1	10h
RTC minutes, RTC counter 2	RTCMIN, RTCNT2	11h
RTC hours, RTC counter 3	RTCHOUR, RTCNT3	12h
RTC day of week, RTC counter 4	RTCROW, RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

Table 6-34. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

Table 6-35. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

Table 6-36. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA0CTL1	00h
USCI control 0	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 6-37. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

Table 6-38. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA1CTL1	00h
USCI control 0	UCA1CTL0	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

Table 6-39. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB1CTL1	00h
USCI synchronous control 0	UCB1CTL0	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

Table 6-40. ADC12_A Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC control 0	ADC12CTL0	00h
ADC control 1	ADC12CTL1	02h
ADC control 2	ADC12CTL2	04h
ADC interrupt flag	ADC12IFG	0Ah
ADC interrupt enable	ADC12IE	0Ch
ADC interrupt vector word	ADC12IV	0Eh
ADC memory control 0	ADC12MCTL0	10h
ADC memory control 1	ADC12MCTL1	11h
ADC memory control 2	ADC12MCTL2	12h
ADC memory control 3	ADC12MCTL3	13h
ADC memory control 4	ADC12MCTL4	14h
ADC memory control 5	ADC12MCTL5	15h
ADC memory control 6	ADC12MCTL6	16h
ADC memory control 7	ADC12MCTL7	17h
ADC memory control 8	ADC12MCTL8	18h
ADC memory control 9	ADC12MCTL9	19h
ADC memory control 10	ADC12MCTL10	1Ah
ADC memory control 11	ADC12MCTL11	1Bh
ADC memory control 12	ADC12MCTL12	1Ch
ADC memory control 13	ADC12MCTL13	1Dh
ADC memory control 14	ADC12MCTL14	1Eh
ADC memory control 15	ADC12MCTL15	1Fh
Conversion memory 0	ADC12MEM0	20h
Conversion memory 1	ADC12MEM1	22h
Conversion memory 2	ADC12MEM2	24h
Conversion memory 3	ADC12MEM3	26h
Conversion memory 4	ADC12MEM4	28h
Conversion memory 5	ADC12MEM5	2Ah
Conversion memory 6	ADC12MEM6	2Ch
Conversion memory 7	ADC12MEM7	2Eh
Conversion memory 8	ADC12MEM8	30h
Conversion memory 9	ADC12MEM9	32h
Conversion memory 10	ADC12MEM10	34h
Conversion memory 11	ADC12MEM11	36h
Conversion memory 12	ADC12MEM12	38h
Conversion memory 13	ADC12MEM13	3Ah
Conversion memory 14	ADC12MEM14	3Ch
Conversion memory 15	ADC12MEM15	3Eh

Table 6-41. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control 0	CBCTL0	00h
Comp_B control 1	CBCTL1	02h
Comp_B control 2	CBCTL2	04h
Comp_B control 3	CBCTL3	06h
Comp_B interrupt	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

6.10 Input/Output Diagrams

6.10.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Figure 6-2 shows the port diagram. Table 6-42 summarizes the selection of the pin functions.

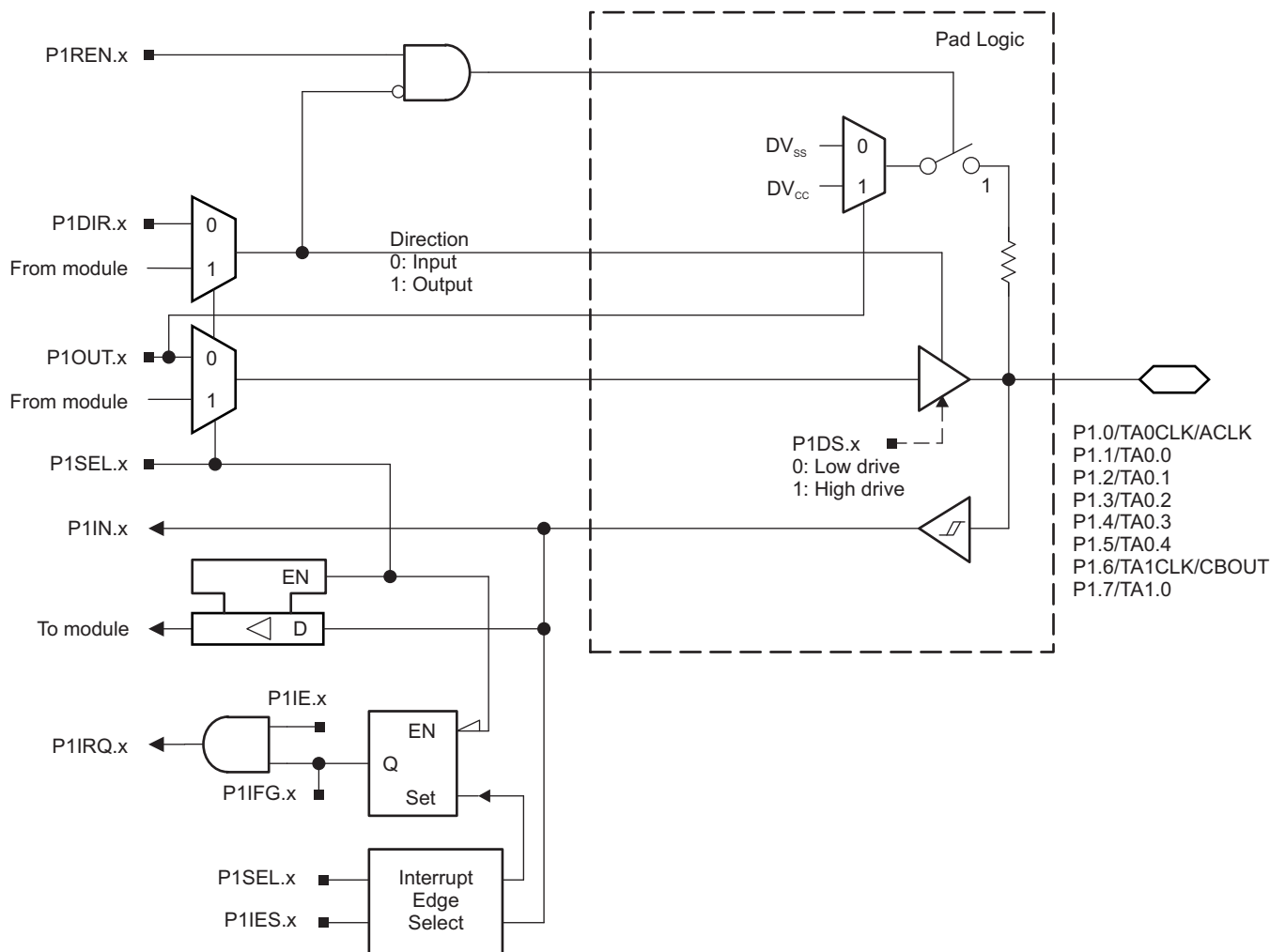


Figure 6-2. Port P1 (P1.0 to P1.7) Diagram

Table 6-42. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		TA0.CCI2A	0	1
		TA0.2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		TA0.CCI3A	0	1
		TA0.3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		TA0.CCI4A	0	1
		TA0.4	1	1
P1.6/TA1CLK/CBOUT	6	P1.6 (I/O)	I: 0; O: 1	0
		TA1CLK	0	1
		CBOUT comparator B	1	1
P1.7/TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.0	1	1

6.10.2 Port P2 (P2.7) Input/Output With Schmitt Trigger

Figure 6-3 shows the port diagram. Table 6-43 summarizes the selection of the pin functions.

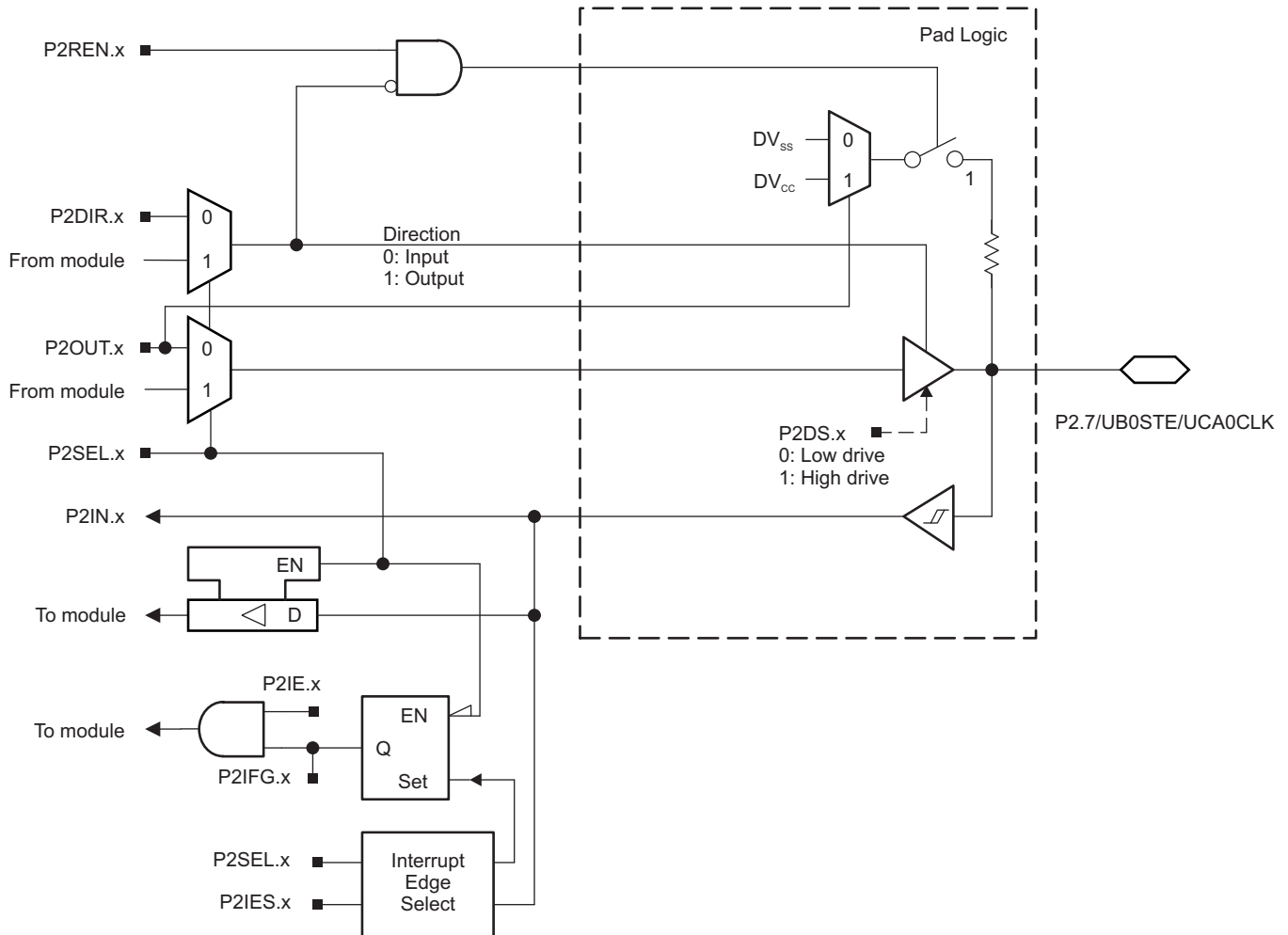


Figure 6-3. Port P2 (P2.7) Diagram

Table 6-43. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾	
			P2DIR.x	P2SEL.x
P2.7/UCB0STE/UCA0CLK	7	P2.7 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK ^{(2) (3)}	X	1

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

6.10.3 Port P3 (P3.0 to P3.4) Input/Output With Schmitt Trigger

Figure 6-4 shows the port diagram. Table 6-44 summarizes the selection of the pin functions.

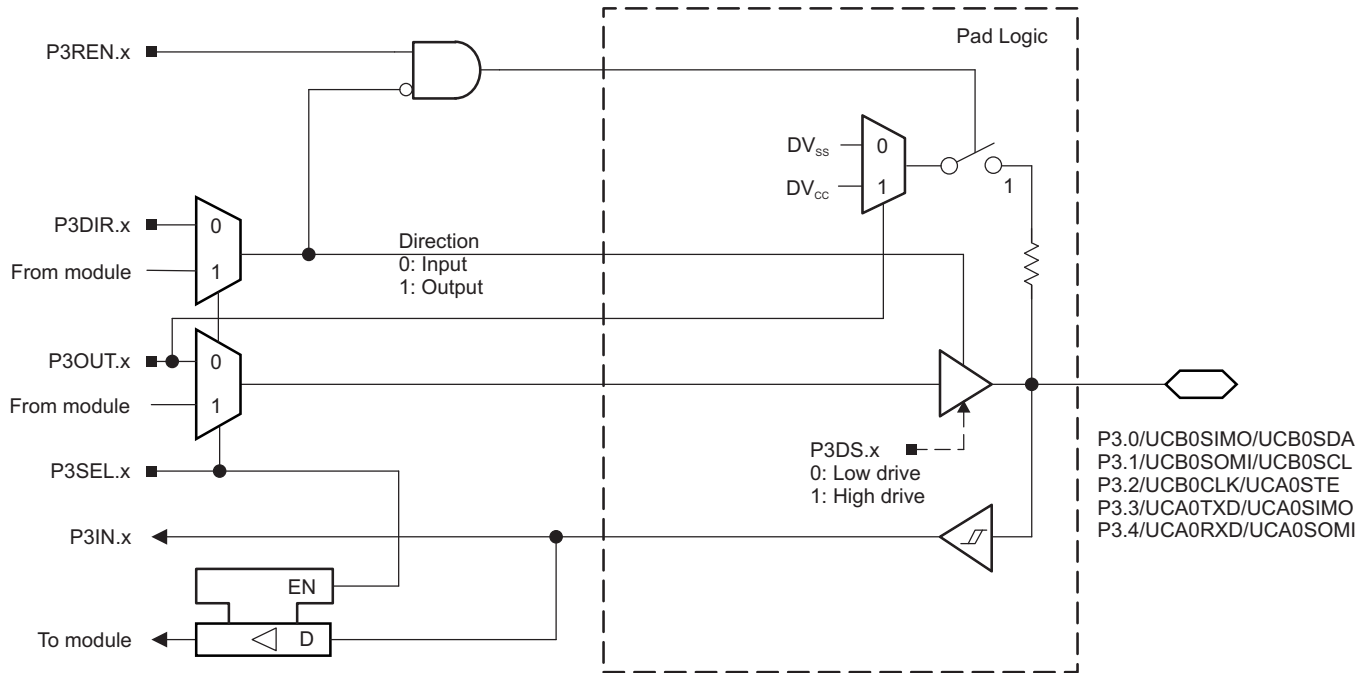


Figure 6-4. Port P3 (P3.0 to P3.4) Diagram

Table 6-44. Port P3 (P3.0 to P3.4) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾	
			P3DIR.x	P3SEL.x
P3.0/UCB0SIMO/UCB0SDA	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA ^{(2) (3)}	X	1
P3.1/UCB0SOMI/UCB0SCL	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL ^{(2) (3)}	X	1
P3.2/UCB0CLK/UCA0STE	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE ^{(2) (4)}	X	1
P3.3/UCA0TXD/UCA0SIMO	3	P3.3 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO ⁽²⁾	X	1
P3.4/UCA0RXD/UCA0SOMI	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI ⁽²⁾	X	1

- (1) X = Don't care
- (2) The pin direction is controlled by the USCI module.
- (3) If the I²C functionality is selected, the output drives only the logical 0 to V_{SS} level.
- (4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

6.10.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Figure 6-5 shows the port diagram. Table 6-45 summarizes the selection of the pin functions.

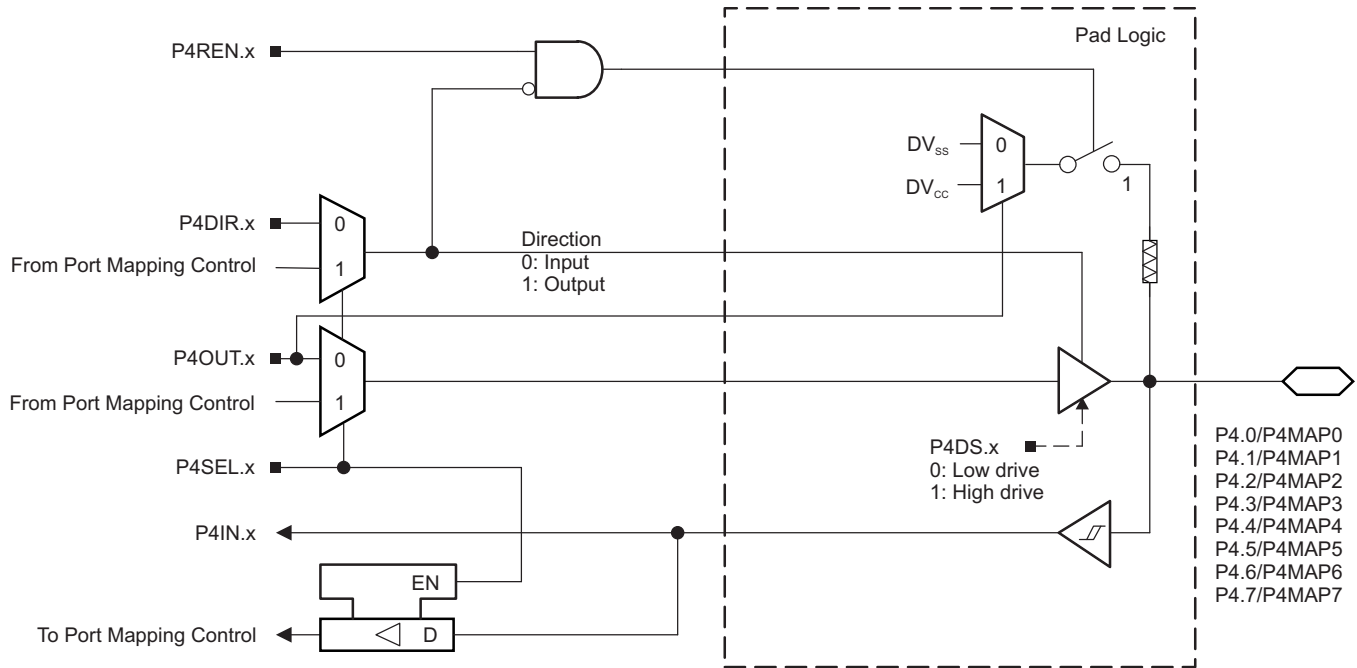


Figure 6-5. Port P4 (P4.0 to P4.7) Diagram

Table 6-45. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P4DIR.x ⁽²⁾	P4SEL.x	P4MAPx
P4.0/P4MAP0	0	P4.0 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.1/P4MAP1	1	P4.1 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.2/P4MAP2	2	P4.2 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.3/P4MAP3	3	P4.3 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.4/P4MAP4	4	P4.4 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.5/P4MAP5	5	P4.5 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.6/P4MAP6	6	P4.6 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.7/P4MAP7	7	P4.7 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30

(1) X = Don't care

(2) The direction of some mapped secondary functions are controlled directly by the module. See Table 6-6 for specific direction control information of mapped secondary functions.

6.10.5 Port P5 (P5.0 and P5.1) Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-46 summarizes the selection of the pin functions.

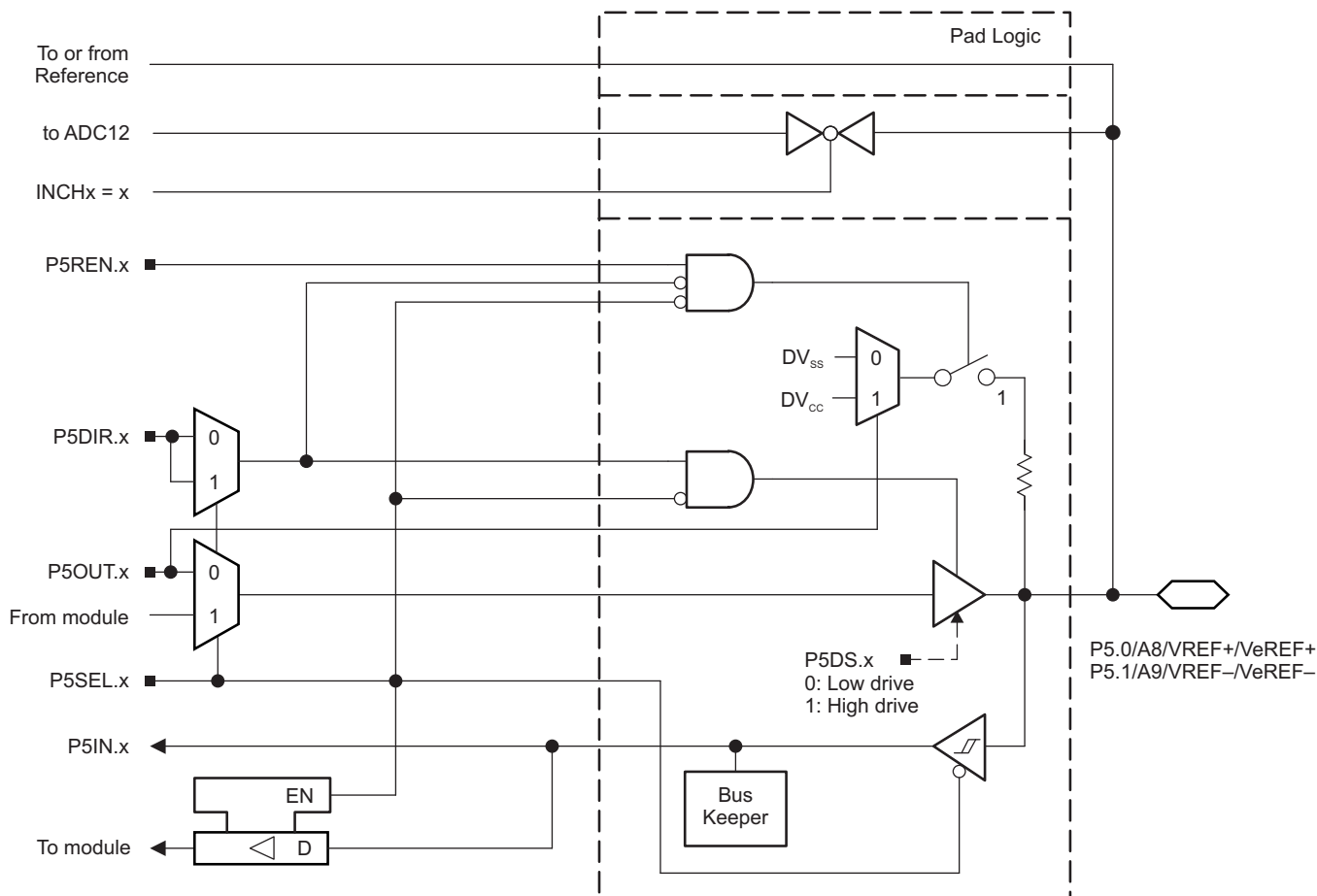


Figure 6-6. Port P5 (P5.0 and P5.1) Diagram

Table 6-46. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P5DIR.x	P5SEL.x	REFOUT
P5.0/A8/VREF+/VeREF+	0	P5.0 (I/O) ⁽²⁾	I: 0; O: 1	0	X
		A8/VeREF+ ⁽³⁾	X	1	0
		A8/VREF+ ⁽⁴⁾	X	1	1

(1) X = Don't care

(2) Default condition

(3) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12_A. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.

(4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The VREF+ reference is available at the pin. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.

Table 6-46. Port P5 (P5.0 and P5.1) Pin Functions (continued)

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P5DIR.x	P5SEL.x	REFOUT
P5.1/A9/VREF-/VeREF-	1	P5.1 (I/O) ⁽²⁾	I: 0; O: 1	0	X
		A9/VeREF- ⁽⁵⁾	X	1	0
		A9/VREF- ⁽⁶⁾	X	1	1

- (5) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12_A. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.
- (6) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The VREF- reference is available at the pin. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.

6.10.6 Port P5 (P5.2) Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-47 summarizes the selection of the pin functions.

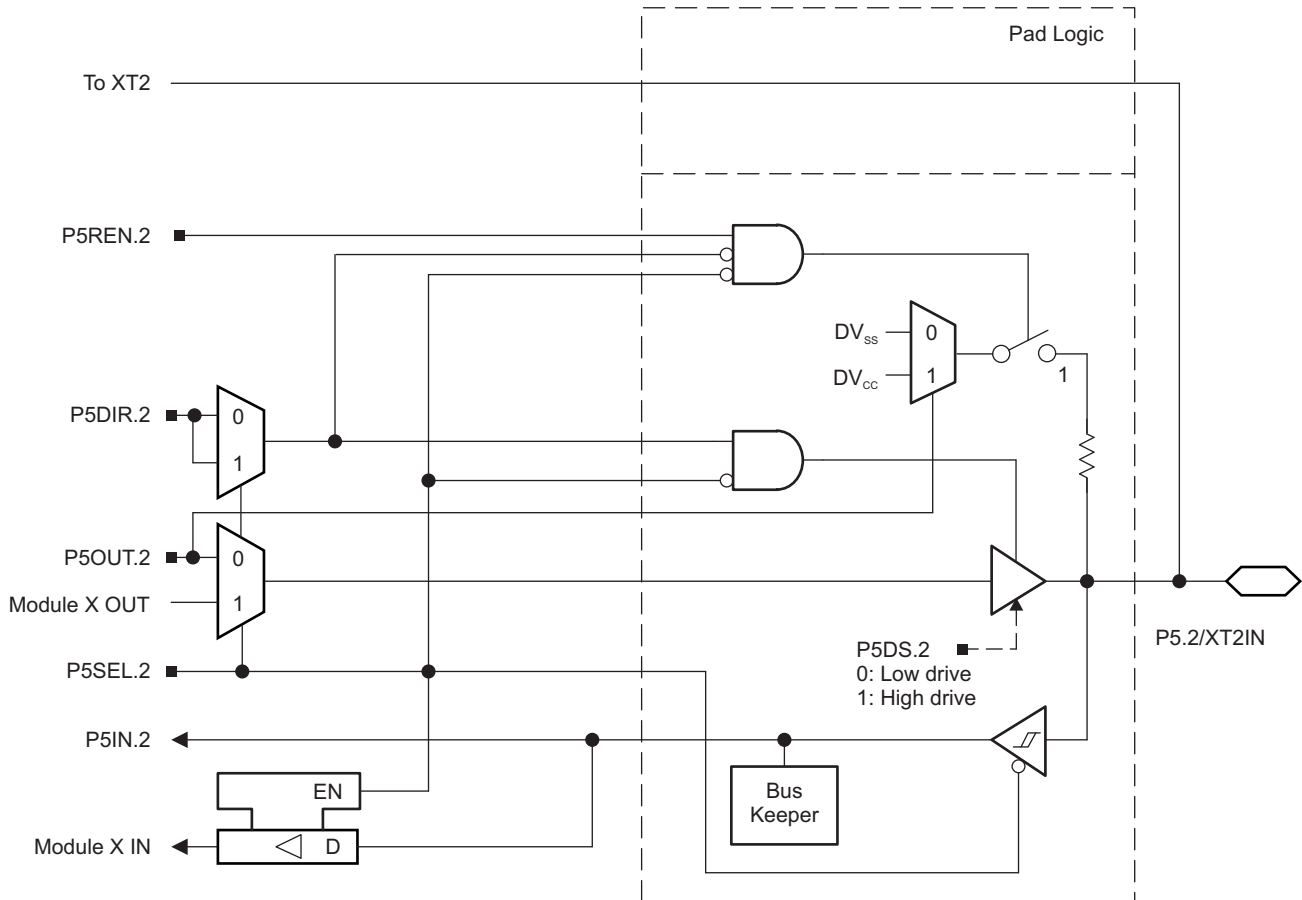


Figure 6-7. Port P5 (P5.2) Diagram

6.10.7 Port P5 (P5.3) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-47 summarizes the selection of the pin functions.

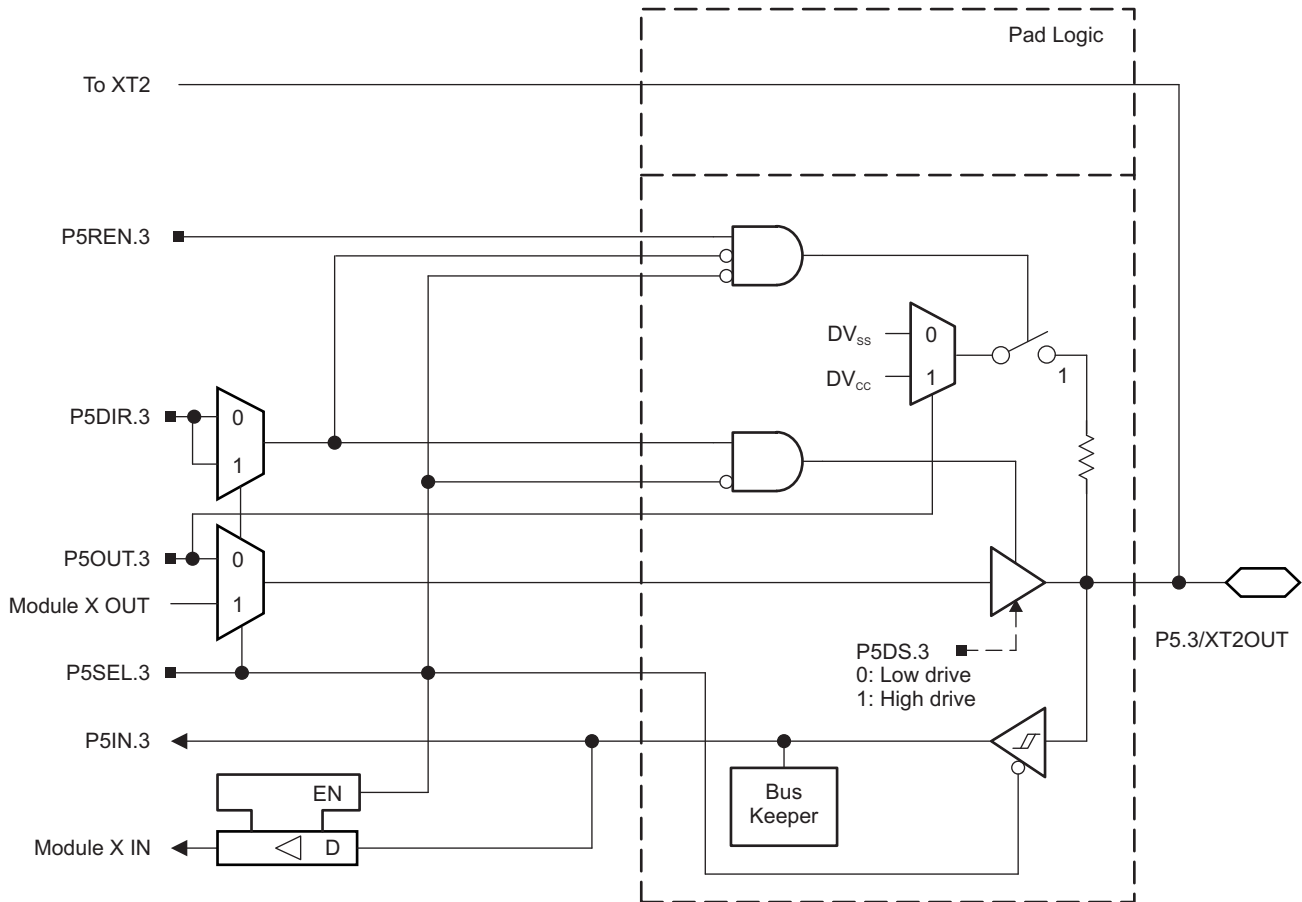


Figure 6-8. Port P5 (P5.3) Diagram

Table 6-47. Port P5 (P5.2 and 5.3) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾			
			P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode ⁽²⁾	X	1	X	0
		XT2IN bypass mode ⁽²⁾	X	1	X	1
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	X	X
		XT2OUT crystal mode ⁽³⁾	X	1	X	0
		P5.3 (I/O) ⁽³⁾	X	1	X	1

(1) X = Don't care

(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.

(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

6.10.8 Port P5 (P5.4 and P5.5) Input/Output With Schmitt Trigger

Figure 6-9 and Figure 6-10 show the port diagrams. Table 6-48 summarizes the selection of the pin functions.

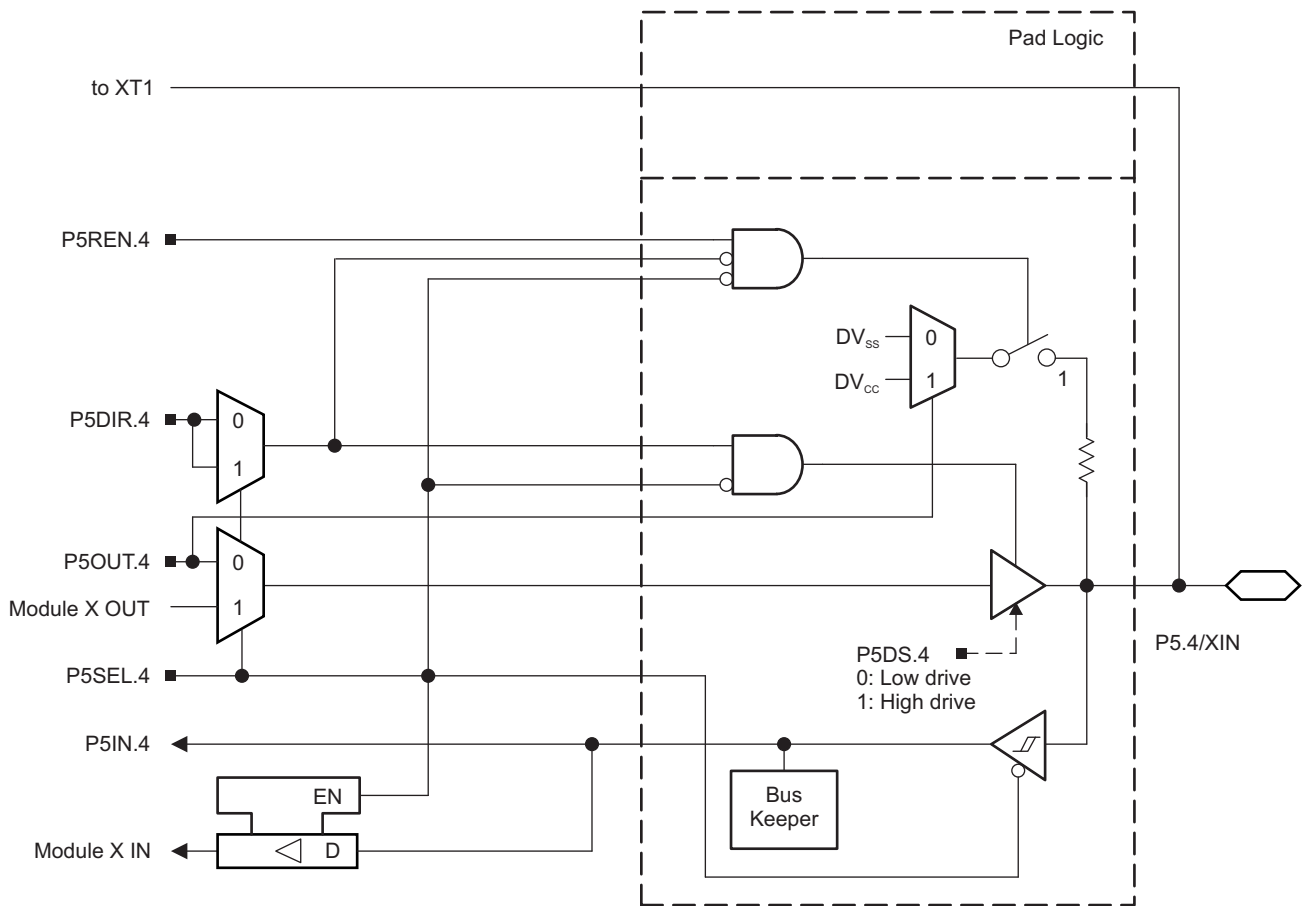


Figure 6-9. Port P5 (P5.4) Diagram

6.10.9 Port P5 (P5.7) Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 6-49 summarizes the selection of the pin functions.

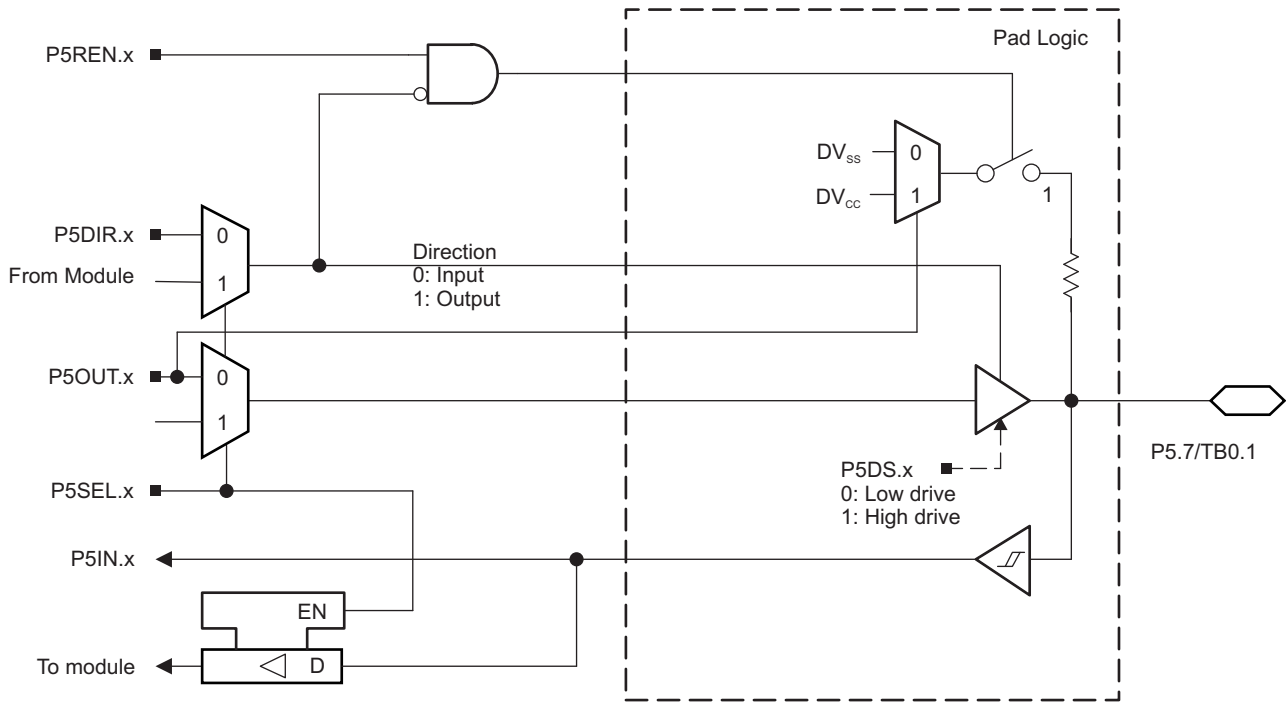


Figure 6-11. Port P5 (P5.7) Diagram

Table 6-49. Port P5 (P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P5DIR.x	P5SEL.x
P5.7/TB0.1	7	TB0.CCI1A	0	1
		TB0.1	1	1

6.10.10 Port P6 (P6.1 to P6.5) Input/Output With Schmitt Trigger

Figure 6-12 shows the port diagram. Table 6-50 summarizes the selection of the pin functions.

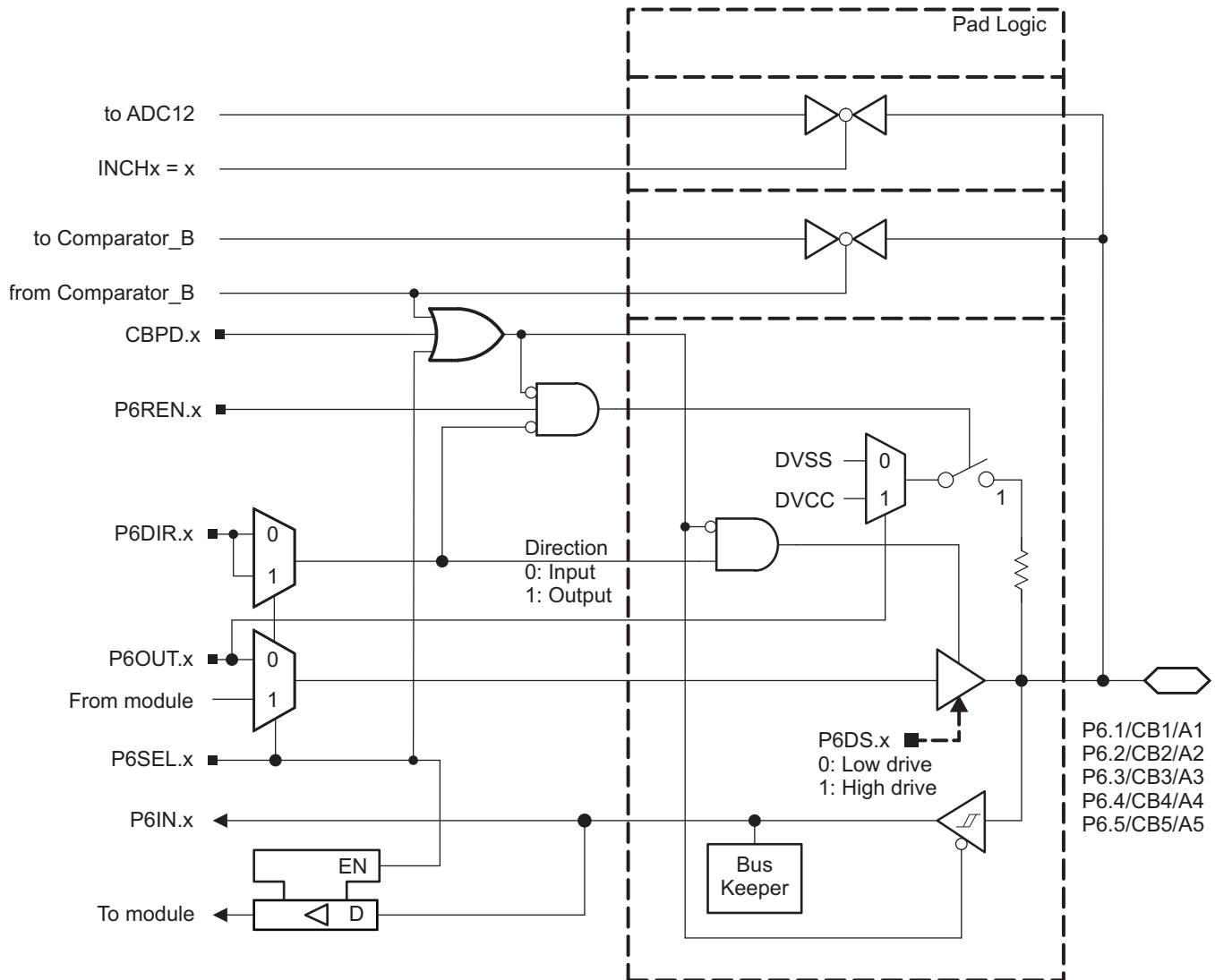


Figure 6-12. Port P6 (P6.1 to P6.5) Diagram

Table 6-50. Port P6 (P6.1 to P6.5) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P6DIR.x	P6SEL.x	CBPDx
P6.1/CB1/A1	1	P6.1 (I/O)	I: 0; O: 1	0	0
		A1	X	1	X
		CB1 ⁽²⁾	X	X	1
P6.2/CB2/A2	2	P6.2 (I/O)	I: 0; O: 1	0	0
		A2	X	1	X
		CB2 ⁽²⁾	X	X	1
P6.3/CB3/A3	3	P6.3 (I/O)	I: 0; O: 1	0	0
		A3	X	1	X
		CB3 ⁽²⁾	X	X	1
P6.4/CB4/A4	4	P6.4 (I/O)	I: 0; O: 1	0	0
		A4	X	1	X
		CB4 ⁽²⁾	X	X	1
P6.5/CB5/A5	5	P6.5 (I/O)	I: 0; O: 1	0	0
		A5	X	1	X
		CB5 ⁽²⁾	X	X	1

(1) X = Don't care

(2) Setting the CBPDx bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPDx bit.

6.10.11 Port PJ (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-13 shows the port diagram. Table 6-51 summarizes the selection of the pin functions.

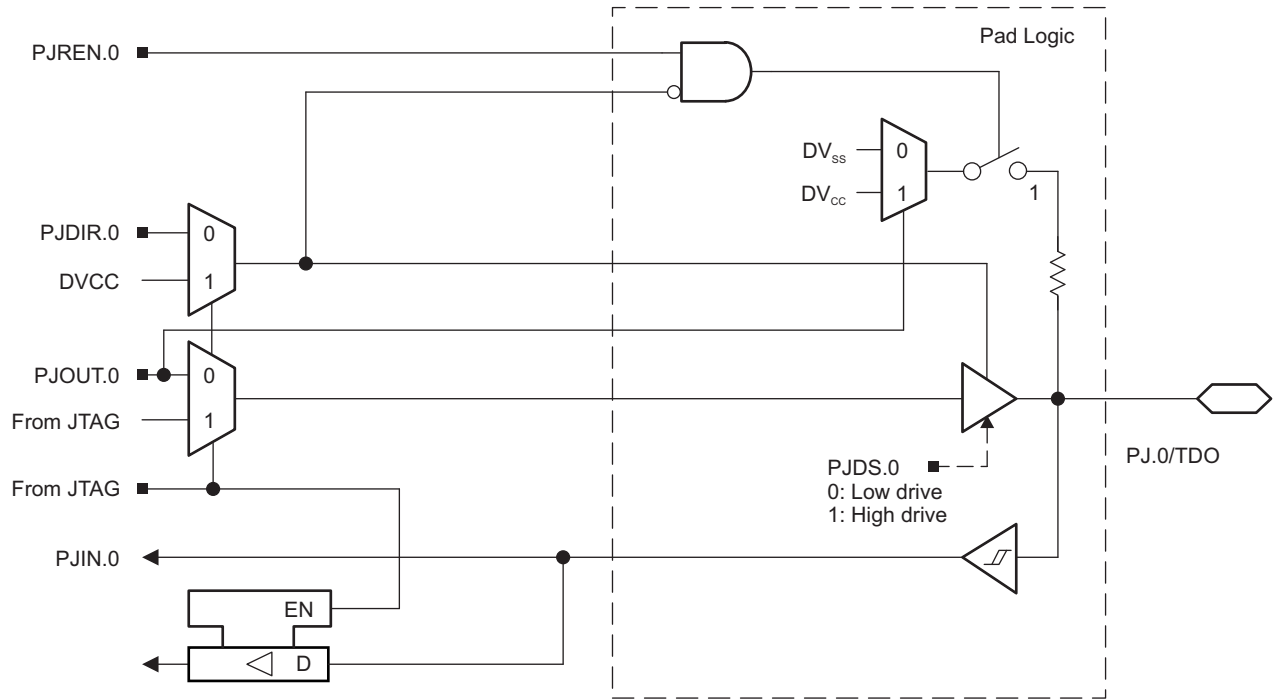


Figure 6-13. Port PJ (PJ.0) Diagram

6.10.12 Port PJ (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-14 shows the port diagram. Table 6-51 summarizes the selection of the pin functions.

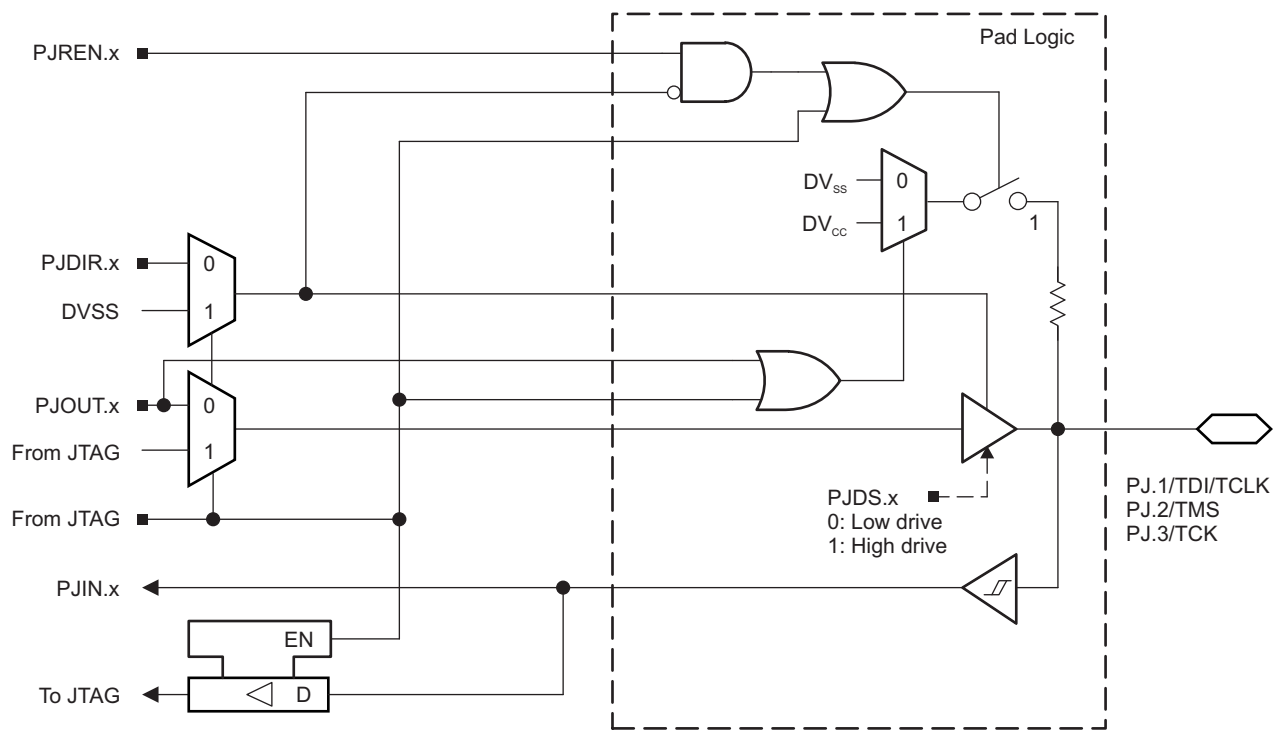


Figure 6-14. Port PJ (PJ.1 to PJ.3) Diagram

Table 6-51. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O) ⁽²⁾	I: 0; O: 1
		TDO ⁽³⁾	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O) ⁽²⁾	I: 0; O: 1
		TDI/TCLK ^{(3) (4)}	X
PJ.2/TMS	2	PJ.2 (I/O) ⁽²⁾	I: 0; O: 1
		TMS ^{(3) (4)}	X
PJ.3/TCK	3	PJ.3 (I/O) ⁽²⁾	I: 0; O: 1
		TCK ^{(3) (4)}	X

- (1) X = Don't care
- (2) Default condition
- (3) The pin direction is controlled by the JTAG module.
- (4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

6.11 Device Descriptors

Table 6-52 lists the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 6-52. Device Descriptor Table⁽¹⁾

DESCRIPTION	ADDRESS	SIZE (bytes)	VALUE			
			F5342	F5341	F5340	
Info Block	Info length	01A00h	1	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h
	CRC value	01A02h	2	Per unit	Per unit	Per unit
	Device ID	01A04h	1	1Eh	1Dh	1Ch
	Device ID	01A05h	1	81h	81h	81h
	Hardware revision	01A06h	1	Per unit	Per unit	Per unit
	Firmware revision	01A07h	1	Per unit	Per unit	Per unit
Die Record	Die record tag	01A08h	1	08h	08h	08h
	Die record length	01A09h	1	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	4	Per unit	Per unit	Per unit
	Die X position	01A0Eh	2	Per unit	Per unit	Per unit
	Die Y position	01A10h	2	Per unit	Per unit	Per unit
	Test results	01A12h	2	Per unit	Per unit	Per unit
ADC12 Calibration	ADC12 calibration tag	01A14h	1	11h	11h	11h
	ADC12 calibration length	01A15h	1	10h	10h	10h
	ADC gain factor	01A16h	2	Per unit	Per unit	Per unit
	ADC offset	01A18h	2	Per unit	Per unit	Per unit
	ADC 1.5-V reference temperature sensor 30°C	01A1Ah	2	Per unit	Per unit	Per unit
	ADC 1.5-V reference temperature sensor 85°C	01A1Ch	2	Per unit	Per unit	Per unit
	ADC 2.0-V reference temperature sensor 30°C	01A1Eh	2	Per unit	Per unit	Per unit
	ADC 2.0-V reference temperature sensor 85°C	01A20h	2	Per unit	Per unit	Per unit
	ADC 2.5-V reference temperature sensor 30°C	01A22h	2	Per unit	Per unit	Per unit
ADC 2.5-V reference temperature sensor 85°C	01A24h	2	Per unit	Per unit	Per unit	
REF Calibration	REF calibration tag	01A26h	1	12h	12h	12h
	REF calibration length	01A27h	1	06h	06h	06h
	REF 1.5-V reference factor	01A28h	2	Per unit	Per unit	Per unit
	REF 2.0-V reference factor	01A2Ah	2	Per unit	Per unit	Per unit
	REF 2.5-V reference factor	01A2Ch	2	Per unit	Per unit	Per unit

(1) N/A = Not applicable, blank = unused and reads FFh

Table 6-52. Device Descriptor Table⁽¹⁾ (continued)

DESCRIPTION	ADDRESS	SIZE (bytes)	VALUE		
			F5342	F5341	F5340
Peripheral descriptor tag	01A2Eh	1	02h	02h	02h
Peripheral descriptor length	01A2Fh	1	5Eh	5Eh	5Eh
Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah
Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h
Memory 3		2	0Eh 2Fh	0Eh 2Eh	0Eh 2Dh
Memory 4		2	2Ah 22h	22h 95h	2Ah 22h
Memory 5		1	96h	92h	94h
Delimiter		1	00h	00h	00h
Peripheral count		1	1Fh	1Fh	1Fh
MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h
JTAG		2	00h 09h	00h 09h	00h 09h
SBW		2	00h 0Fh	00h 0Fh	00h 0Fh
EEM-L		2	00h 05h	00h 05h	00h 05h
TI BSL		2	00h FCh	00h FCh	00h FCh
SFR		2	10h 41h	10h 41h	10h 41h
PMM		2	02h 30h	02h 30h	02h 30h
FCTL		2	02h 38h	02h 38h	02h 38h
CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch
CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh
RAMCTL		2	00h 44h	00h 44h	00h 44h
WDT_A		2	00h 40h	00h 40h	00h 40h
UCS		2	01h 48h	01h 48h	01h 48h
SYS		2	02h 42h	02h 42h	02h 42h
REF		2	03h A0h	03h A0h	03h A0h
Port Mapping		2	01h 10h	01h 10h	01h 10h
Port 1 and 2		2	04h 51h	04h 51h	04h 51h
Port 3 and 4		2	02h 52h	02h 52h	02h 52h
Port 5 and 6		2	02h 53h	02h 53h	02h 53h

Table 6-52. Device Descriptor Table⁽¹⁾ (continued)

DESCRIPTION	ADDRESS	SIZE (bytes)	VALUE			
			F5342	F5341	F5340	
Peripheral Descriptor (continued)	JTAG		2	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh
	TA0		2	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h
	TA2		2	04h 61h	04h 61h	04h 61h
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h
	MPY32		2	02h 85h	02h 85h	02h 85h
	DMA-3		2	04h 47h	04h 47h	04h 47h
	USCI_A, USCI_B		2	0Ch 90h	0Ch 90h	0Ch 90h
	USCI_A, USCI_B		2	04h 90h	04h 90h	04h 90h
	ADC12_A		2	10h D1h	10h D1h	10h D1h
	COMP_B		2	1Ch A8h	1Ch A8h	1Ch A8h
Interrupts	COMP_B		1	A8h	A8h	A8h
	TB0.CCIFG0		1	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h
	WDTIFG		1	40h	40h	40h
	USCI_A0		1	90h	90h	90h
	USCI_B0		1	91h	91h	91h
	ADC12_A		1	D0h	D0h	D0h
	TA0.CCIFG0		1	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h
	Reserved		1	01h	01h	01h
	DMA		1	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h
	P1		1	50h	50h	50h
	USCI_A1		1	92h	92h	92h
	USCI_B1		1	93h	93h	93h
	TA1.CCIFG0		1	66h	66h	66h
	TA1.CCIFG1..2		1	67h	67h	67h
	P2		1	51h	51h	51h
RTC_A		1	68h	68h	68h	
Delimiter		1	00h	00h	00h	

7 デバイスおよびドキュメントのサポート

7.1 はじめに

MSP430™ファミリのデバイス、および開発に役立つツールやライブラリの詳細については、「[MSP430超低消費電力センシング/測定マイコンの概要](#)」を参照してください。

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

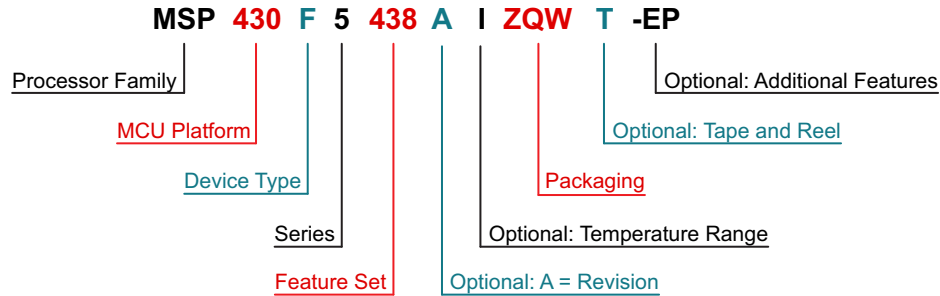
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [☒ 7-1](#) provides a legend for reading the complete device name.



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	Memory Type C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	Specialized Application AFE = Analog Front End BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD 0 = Low-Voltage Series
Feature Set	Various levels of integration within a series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced Product (-40°C to 105°C) -HT = Extreme Temperature Parts (-55°C to 150°C) -Q1 = Automotive Q100 Qualified	

☒ 7-1. Device Nomenclature

7.3 ツールとソフトウェア

すべてのMSPマイクロコントローラは、広範なソフトウェアおよびハードウェア開発ツールによりサポートされています。ツールは、TIおよびさまざまなサードパーティーから入手できます。すべての一覧は「[MSP430 超低消費電力マイコン – ツールとソフトウェア](#)」で参照できます。

MSP430F532x MCUのデバッグ機能の一覧を、表 7-1に示します。利用可能な機能の詳細については、『[MSP430用Code Composer Studio ユーザー・ガイド](#)』を参照してください。

表 7-1. ハードウェアのデバッグ機能

MSP430のアーキテクチャ	4線式JTAG	2線式JTAG	ブレイク・ポイント (N)	範囲ブレイク・ポイント	クロック制御	状態シーケンサ	トレース・バッファ	LPMx.5デバッグ・サポート
MSP430Xv2	○	○	8	○	○	○	○	×

設計キットと評価モジュール

MSP430F534x 48ピン・ターゲット・ボードのみ MSP-TS430RGZ48Bはスタンドアロンの48ピンZIFソケット・ターゲット・ボードで、これによりJTAGインターフェイスまたはSpy Bi-Wire (2線式JTAG) プロトコルを使用して、MSP430 MCUをインシステムでプログラミングおよびデバッグできます。

MSP430F5x MCU用の48ピン・ターゲット開発基板とMSP-FETプログラマ・バンドル MSP-FET430U48Bは強力なフラッシュ・エミュレーション・ツールで、MSP430 MCUによるアプリケーションの開発をすぐに開始できます。USBデバッグ・インターフェイスにより、JTAGインターフェイスまたは省ピンSpy Bi-Wire (2線式JTAG) プロトコルを使用してMSP430をインシステムでプログラミングおよびデバッグできます。MSP430のフラッシュ・メモリは、数回のキー操作により、数秒で消去およびプログラミングできます。また、極めて低消費電力であるため、外部電源は不要です。

ソフトウェア

MSP430Ware™ソフトウェア MSP430Wareソフトウェアは、すべてのMSP430デバイス向けのサンプル・コード、データシート、その他の設計リソースを、1つの便利なパッケージとしてまとめたものです。既存のMSP430 MCU 設計リソースの完全なコレクションに加えて、MSP430Ware ソフトウェアには、MSPドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSP430ハードウェアを簡単にプログラムできます。MSP430WareソフトウェアはCCSのコンポーネントとして、またはスタンドアロンのパッケージとして入手できます。

MSP430F534xサンプル・コード 各種のアプリケーションの要求に応じて、各内蔵ペリフェラルを設定するCコード・サンプルです。

MSPドライバ・ライブラリ ドライバ・ライブラリの抽象化APIで、使いやすい関数呼び出しが用意されており、MSP430ハードウェアのビットやバイトのレベルを意識せずに、より高水準の開発作業に集中できます。使いやすいAPIガイドにより包括的な技術資料が参照でき、それぞれの関数呼び出しと、認識されるパラメータの詳細が記載されています。開発者は、ドライバ・ライブラリの関数を使用して、最小限のオーバーヘッドで完全なプロジェクトを作成できます。

MSP EnergyTrace™テクノロジー MSP430マイクロコントローラ用のEnergyTraceテクノロジーは、エネルギーを基準としたコード解析ツールで、アプリケーションのエネルギー・プロファイルを測定して表示し、消費電力が極めて低くなるよう最適化するため役立ちます。

ULP (超低消費電力) Advisor ULP Advisor™ソフトウェアは、MSPおよびMSP432マイクロコントローラ独自の超低消費電力機能を十分に活用できる、最も効率的なコードを開発者が作成できるよう手引きするツールです。ULP Advisorは、マイクロコントローラの熟練した開発者でも、新しい開発者でも使用でき、包括的なULPチェックリストと照らし合わせてコードのチェックを行い、アプリケーションの性能を最大限まで発揮できるようにします。ビルド時に、消費電力低減のためさらに最適化が可能なコードの部分を明らかにするため通知と注釈を出力します。

IEC60730ソフトウェア・パッケージ IEC60730 MSP430ソフトウェア・パッケージは、クラスBまでの製品について、お客様がIEC 60730-1:2010 (家庭および同様な用途に使用される自動電気制御 – 第1部: 一般的な要件)に準拠するため役立つよう開発されています。この分類には家電機器、アーク検出器、電力コンバータ、電動工具、電動アシスト自転車、その他多くの製品が含まれます。IEC60730 MSP430ソフトウェア・パッケージは、MSP430で実行するお客様のアプリケーションに組み込むことができるため、消費者向けデバイスがIEC 60730-1:2010クラスBの機能安全性に準拠していることの認定作業を簡素化できます。

MSP用の固定小数点算術ライブラリ MSP IQmathおよびQmathライブラリは、Cプログラマ向けの高度に最適化された高精度の算術関数のコレクションで、浮動小数点アルゴリズムをMSP430およびMSP432デバイスの固定小数点コードへシームレスに移行できます。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

MSP430用の浮動小数点算術ライブラリ 低消費電力かつ低コストのマイクロコントローラ分野で継続的な革新を行うため、TIはMSPMATHLIBを提供しています。このスカラー関数の浮動小数点数値演算ライブラリは、弊社デバイスのインテリジェントなペリフェラルを活用し、最高26倍の性能を実現します。Mathlibは、設計へ簡単に組み入れることができます。このライブラリは無償で、Code Composer Studio と IAR IDE の両方に組み込まれています。数値演算ライブラリと関連ベンチマークの詳細については、ユーザー・ガイドを参照してください。

開発ツール

Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境 Code Composer Studioは、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。Code Composer Studioは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。IDEは直感的で、アプリケーションの開発フローの各段階を、すべて同一のユーザー・インターフェイスで実行できます。使い慣れたユーティリティとインターフェイスにより、ユーザーは従来より迅速に作業を開始できます。Code Composer Studioは、Eclipseソフトウェア・フレームワークの利点と、TIの先進的な組み込みデバッグ機能の利点を組み合わせ、組み込み製品の開発者向けの魅力的な、豊富な機能を持つ開発環境を実現します。Code Composer Studio IDEをMSP MCUとともに使用すると、MSPマイクロコントローラを最大限に活用するための、ユニークで強力な一連のプラグインや組み込みソフトウェア・ユーティリティを利用できます。

コマンドライン・プログラマ MSP Flasher は、FETプログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェル・ベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txtまたは.hex) をMSPマイクロコントローラへ直接ダウンロードできます。

MSP MCUプログラマおよびデバッガ MSP-FETは強力なエミュレーション開発ツールで、多くの場合、デバッグ・プローブと呼ばれています。ユーザーはこのツールを使用して、MSP低消費電力マイクロコントローラ(MCU)のアプリケーション開発を迅速に開始できます。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。MSP-FETは、ホスト・コンピュータとターゲットMSPの間で、デバッグ通信経路を提供します。さらに、MSP-FETはコンピュータのUSBインターフェイスとMSP UARTの間で、バックチャネルUART接続も提供します。これにより、MSPプログラマは、コンピュータ上で動作している端末ソフトウェアとMSPとの間で、シリアル通信を簡単に実行できます。また、UARTやI²C通信プロトコルを経由するBSL (ブートローダー) を使用して、プログラム (多くの場合、ファームウェアと呼ばれます) をMSPターゲットにロードできます。

MSP-GANG量産プログラマ MSP Gang ProgrammerはMSP430またはMSP432用のデバイス・プログラマで、8つまでの同一のMSP430またはMSP432フラッシュまたはFRAMデバイスを同時にプログラムできます。MSP Gang Programmerは、標準のRS-232またはUSB接続を使用してホストPCに接続でき、柔軟なプログラミング・オプションにより、プロセスを完全にカスタマイズ可能です。MSP Gang Programmer には、Gang Splitter と呼ばれる拡張ボードが付属しており、MSP Gang Programmer と複数のターゲット・デバイスとの間で相互接続機能を実装します。拡張ボードと、8つのターゲット・デバイスとを接続するため、8本のケーブルが付属しています(JTAGまたはSpy-Bi-Wireコネクタ経由)。PCを使用してプログラムすることも、スタンドアロンのデバイスとしてプログラムすることもできます。PC側のグラフィカル・ユーザー・インターフェイスも用意されており、DLL ベースです。

7.4 ドキュメントのサポート

以下のドキュメントには、MSP430F532x MCUについて記載されています。これらのドキュメントのコピーは、www.ti.comで入手できます。

ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.comでお使いの製品のフォルダへ移動します(プロダクト・フォルダへのリンクについては、7.5を参照してください)。右上の隅にある「通知を受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

正誤表

『**MSP430F5342デバイス正誤表**』 このデバイスにおけるすべてのシリコンのリビジョンについて、機能仕様に関する既知の例外が記載されています。

『**MSP430F5341デバイス正誤表**』 このデバイスにおけるすべてのシリコンのリビジョンについて、機能仕様に関する既知の例外が記載されています。

『**MSP430F5340デバイス正誤表**』 このデバイスにおけるすべてのシリコンのリビジョンについて、機能仕様に関する既知の例外が記載されています。

ユーザー・ガイド

『**MSP430x5xxおよびMSP430x6xxファミリ・ユーザー・ガイド**』 このデバイス・ファミリで利用可能なモジュールとペリフェラルについての詳細情報です。

『**MSP430 フラッシュ・デバイス・ブートローダ(BSL)ユーザー・ガイド**』 MSP430ブートローダ(BSL)を使用すると、プロトタイプ作成フェーズ、最終的な量産、およびサービス中に、MSP430マイクロコントローラの組み込みメモリと通信を行うことができます。必要に応じて、プログラム可能メモリ(フラッシュ・メモリ)とデータ・メモリ(RAM)の両方を変更できます。このブートローダは、一部のデジタル・シグナル・プロセッサ(DSP)に見られる、外部メモリからDSPの内部メモリへプログラム・コード(およびデータ)を自動的にロードする、ブートストラップ・ローダ・プログラムとは異なることに注意してください。

『**JTAGインターフェイスによるMSP430のプログラミング**』 このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430デバイスで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してデバイスにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

『**MSP430ハードウェア・ツール ユーザー・ガイド**』 このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。このFETは、MSP430 超低消費電力マイクロコントローラ用のプログラム開発ツールです。利用可能なインターフェイスとして、パラレル・ポート・インターフェイスとUSBインターフェイスの両方について解説されています。

アプリケーション・レポート

『**MSP430 32kHz水晶発振器**』 適切な水晶、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器のために重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

『**MSP430 システム・レベルESDの考慮事項**』 シリコン・テクノロジーがますます低電圧化し、コスト効率の優れた非常に消費電力の低いコンポーネントを設計する必要性が高まってくにつれ、システム・レベルESDの要求はますます高くなりつつあります。このアプリケーション・レポートでは、基板の設計者およびOEMが強固なシステム・レベルの設計を理解して実行するため役立つよう、3つのESDトピックが扱われています。(1)部品レベルのESDテストとシステム・レベルのESDテスト、(2)システム・レベルのESD保護の一般的な設計ガイドライン、(3)システムの高効率ESD設計(SEED)の概要と、オンボードおよびオンチップESD保護のコードデザイン手法。現実世界でのシステム・レベルのESD保護を設計する例のいくつかと、その結果についても解説します。

7.5 関連リンク

表 7-2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 7-2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
MSP430F5342	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5341	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F5340	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Community

TI's *Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.7 商標

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7.8 静電気放電に関する注意事項



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7.10 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F5340IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5340	Samples
MSP430F5340IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5340	Samples
MSP430F5341IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5341	Samples
MSP430F5341IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5341	Samples
MSP430F5342IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5342	Samples
MSP430F5342IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5342	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5340IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430F5340IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430F5341IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430F5341IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430F5342IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430F5342IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5340IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430F5340IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5341IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430F5341IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5342IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430F5342IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

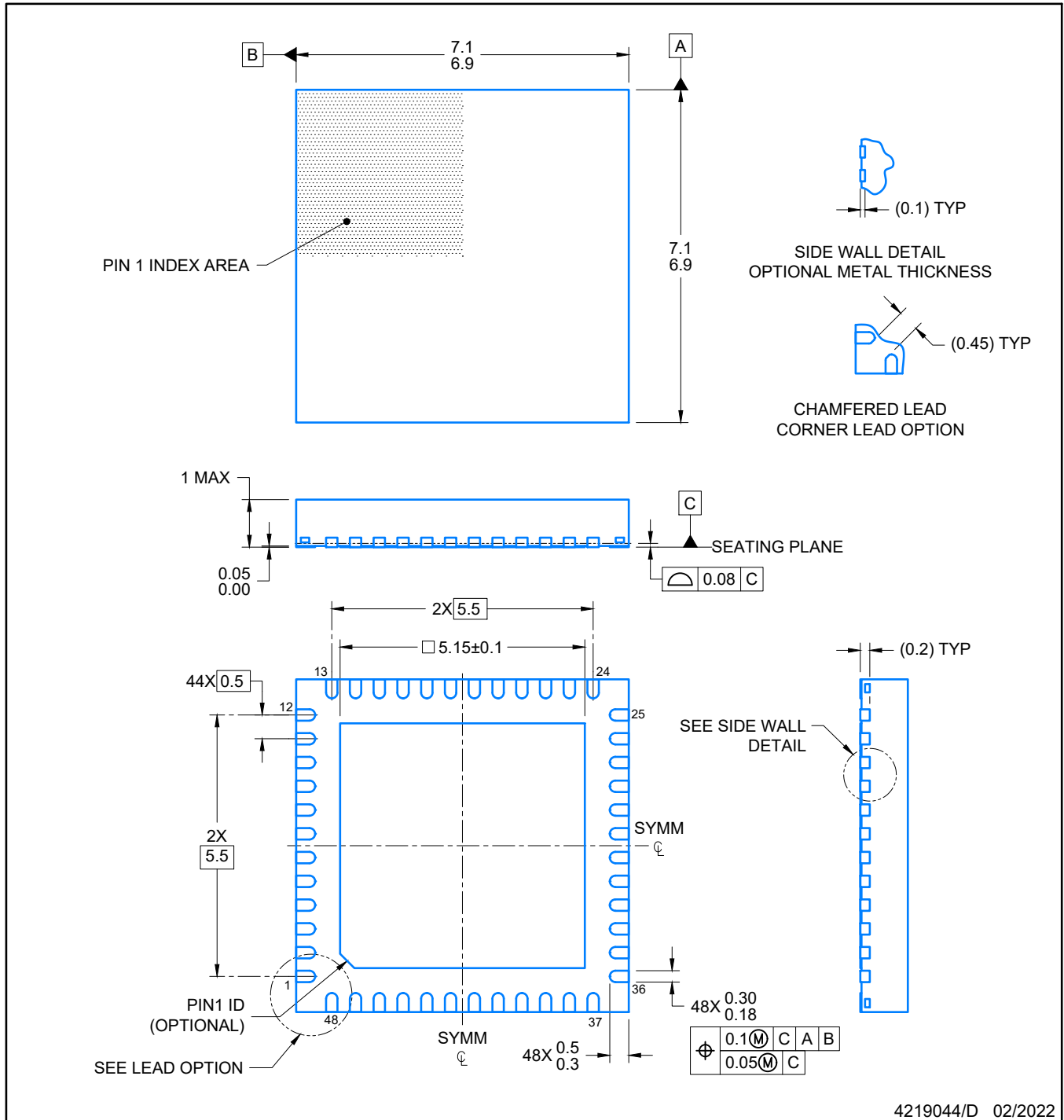
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



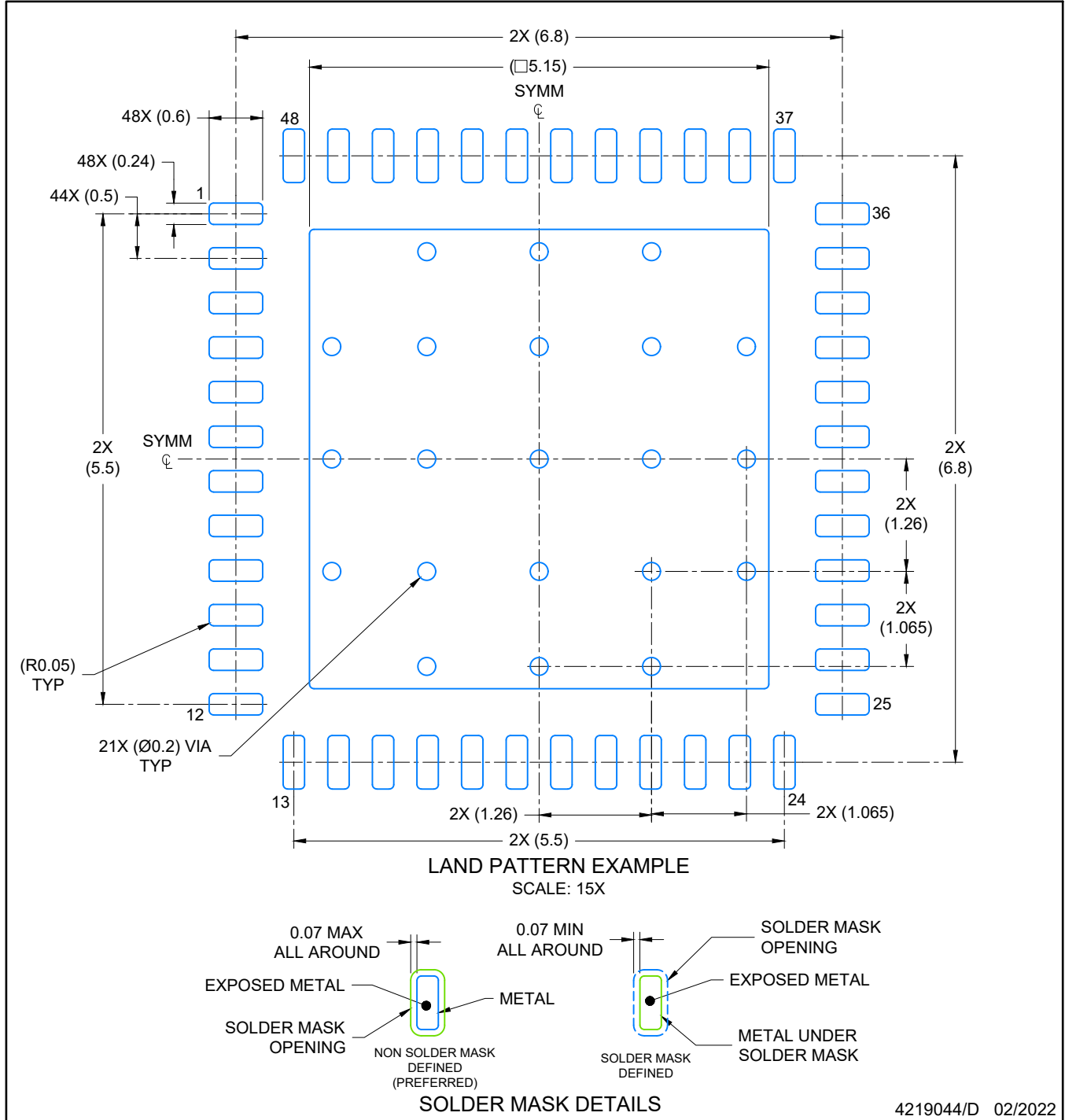
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048A

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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