

# MSPM0C110x-Q1 車載ミックスド・シグナル・マイクロコントローラ

## 1 特長

- 車載アプリケーション向けに **AEC-Q100** 認証済み
  - 温度グレード 1: -40°C ~ +125°C、T<sub>A</sub>
- コア
  - Arm® 32 ビット Cortex®-M0+ CPU、最高 24MHz の周波数
- 動作特性
  - 拡張動作温度範囲: -40°C ~ 125°C
  - 広い電源電圧範囲: 1.62V ~ 3.6V
- メモリ
  - 最大 16KB のフラッシュ
  - 1KB の SRAM
- 高性能アナログ ペリフェラル
  - 1 つの A/D コンバータ (ADC)、合計最大 10 本の外部チャネルを装備、VDD を電圧リファレンスとして使用して 1.7MSPS (10 ビット) または 1.5MSPS (12 ビット)
  - 1.4V または 2.5V の構成可能な内部共有電圧リファレンス (VREF)
  - 温度センサ内蔵
  - 統合型電源監視
- 最適化された低消費電力モード
  - RUN: 87µA/MHz
  - STOP: 4MHz で 609µA、32kHz で 311µA
  - STANDBY: 5µA (SRAM 保持)
  - SHUTDOWN: 200nA
- インテリジェント デジタル ペリフェラル
  - ADC 専用の 1 チャネル DMA コントローラ
  - 最大 14 の PWM チャネルをサポートする 3 つのタイマ
    - 1 つの 16 ビット高度タイマ、最大 8 個の PWM チャネルのデッドバンドをサポート
    - 1 つの 16 ビット汎用タイマ、4 つのキャプチャ / コンパレータを搭載
    - 1 つの 16 ビット汎用タイマ、2 つのキャプチャ / コンパレータを搭載
  - ウィンドウ付きウォッチドッグ タイマ
  - 外部ビープ音を駆動するための 1kHz、2kHz、4kHz、または 8kHz の方形波を生成する BEEPER
- 拡張通信インターフェイス
  - 1 つの UART インターフェイス: LIN、IrDA、DALI、スマートカード、マンチェスターをサポート、STANDBY モードで低消費電力動作
  - 1 つの I<sup>2</sup>C インターフェイス。FM+ (1Mbps)、SMBus、PMBus、STOP モードからのウェークアップをサポート

- 最大 12Mbps をサポートする 1 つの SPI
- クロック システム
  - -2% ~ +1.2% の精度 (SYSOSC) の 24MHz 発振器を内蔵
  - 32kHz の低周波数発振器 (LFOSC) を内蔵
- データの整合性
  - 巡回冗長検査 (CRC-16)
- 柔軟な I/O 機能
  - 最大 18 の GPIO
  - 2 つの 5V 許容オープンドレイン IO
- 開発サポート
  - 2 ピン シリアル ワイヤ デバッグ (SWD)
- パッケージ オプション
  - 20 ピン VSSOP (DGS)
  - 20 ピン WQFN (RUK)
  - 16 ピン SOT (DYY)
  - 8 ピン SOT (DDF)
  - 8 ピン WSON (DSG)
- ファミリの製品 ([「製品比較」](#)も参照)
  - MSPM0C1104: 16KB のフラッシュ、1KB の RAM
  - MSPM0C1103: 8KB のフラッシュ、1KB の RAM
- 開発キットとソフトウェア ([「ツールとソフトウェア」](#)も参照)
  - LP-MSPM0C1104 LaunchPad™ 開発キット
  - MSP ソフトウェア開発キット (SDK)

## 2 アプリケーション

- 車載用ボディ・エレクトロニクス / ライティング
- 車載用ゲートウェイ
- ステアリング・ホイール・システム
- 車載用モーター制御
- DC / AC インバータ
- 車内照明
- ドア・ハンドル・モジュール
- キック・ツル・オープン・モジュール
- 車両の乗員検出
- コンフォート・シート・モジュール



### 3 概要

MSPM0C110x マイクロコントローラ (MCU) は、最大 24MHz の周波数で動作する拡張 Arm® Cortex®-M0+ コア プラットフォームに基づく MSP 高集積超低消費電力 32 ビット MCU ファミリの一部です。コスト最適化されたこれらの MCU は高性能アナログ ペリフェラルを統合しており、-40°C ~ 125°C の拡張温度範囲をサポートしており、1.62V ~ 3.6V の電源電圧で動作します。

MSPM0C110x デバイスは最大 16KB の組み込みフラッシュ プログラム メモリと 1KB の SRAM を内蔵しています。これらの MCU は -2% ~ +1.2% の精度の高速オンチップ発振器を内蔵しているため、外部水晶振動子は不要です。追加機能には、1 チャンネル DMA、CRC-16 アクセラレータ、各種の高性能アナログ ペリフェラル (電圧リファレンスとして VDD を含む 12 ビット 1.5MSPS ADC、1 つのオンチップ温度センサなど) が含まれます。これらのデバイスは、1 つの 16 ビット高度タイマ、2 つの 16 ビット汎用タイマ、1 つのウィンドウ付きウォッチドッグ タイマ、各種通信ペリフェラル (1 つの UART、1 つの SPI、1 つの I<sup>2</sup>C など) などのインテリジェントなデジタル ペリフェラルも備えています。これらの通信ペリフェラルは LIN、IrDA、DALI、マンチェスター、スマート カード、SMBus、PMBus プロトコルをサポートしています。

テキサス・インスツルメンツの MSPM0 低消費電力 MCU ファミリーは、各種のアナログおよびデジタル集積度のデバイスで構成されているため、お客様はプロジェクトのニーズを満たす MCU を見つけることができます。そのアーキテクチャと豊富な低消費電力モードは、携帯型測定アプリケーションで長いバッテリー駆動時間を実現するように最適化されています。

MSPM0C110x MCU は、広範囲にわたるハードウェアおよびソフトウェアのエコシステムによってサポートされており、リファレンス デザインやコード サンプルを使って設計をすぐに開始できます。開発キットには、購入可能な LaunchPad™ キットとターゲット ソケット ボード用の設計ファイルが含まれています。また、テキサス・インスツルメンツは無償の MSP ソフトウェア開発キット (SDK) も提供しており、Code Composer Studio™ IDE デスクトップのコンポーネントとして利用できます。また、TI Resource Explorer ではクラウド バージョンを利用できます。MSPM0 MCU には、広範囲にわたるオンライン資料、MSP Academy によるトレーニング、TI E2E™ サポート フォーラムによるオンライン サポートも用意されています。

モジュールの詳細については、『MSPM0 C シリーズ 24MHz マイクロコントローラ テクニカル リファレンス マニュアル』を参照してください。

#### 注意

電氣的な過剰ストレスや、データやコード メモリの不安定化を防止するために、デバイス レベルの ESD 仕様に従って、システム レベルの ESD 保護を適用する必要があります。詳細については、『MSP430™ のシステム レベルの ESD に関する考慮事項』を参照してください (このアプリケーション ノートの原理は MSPM0 MCU にも当てはまるため)。

## 4 機能ブロック図

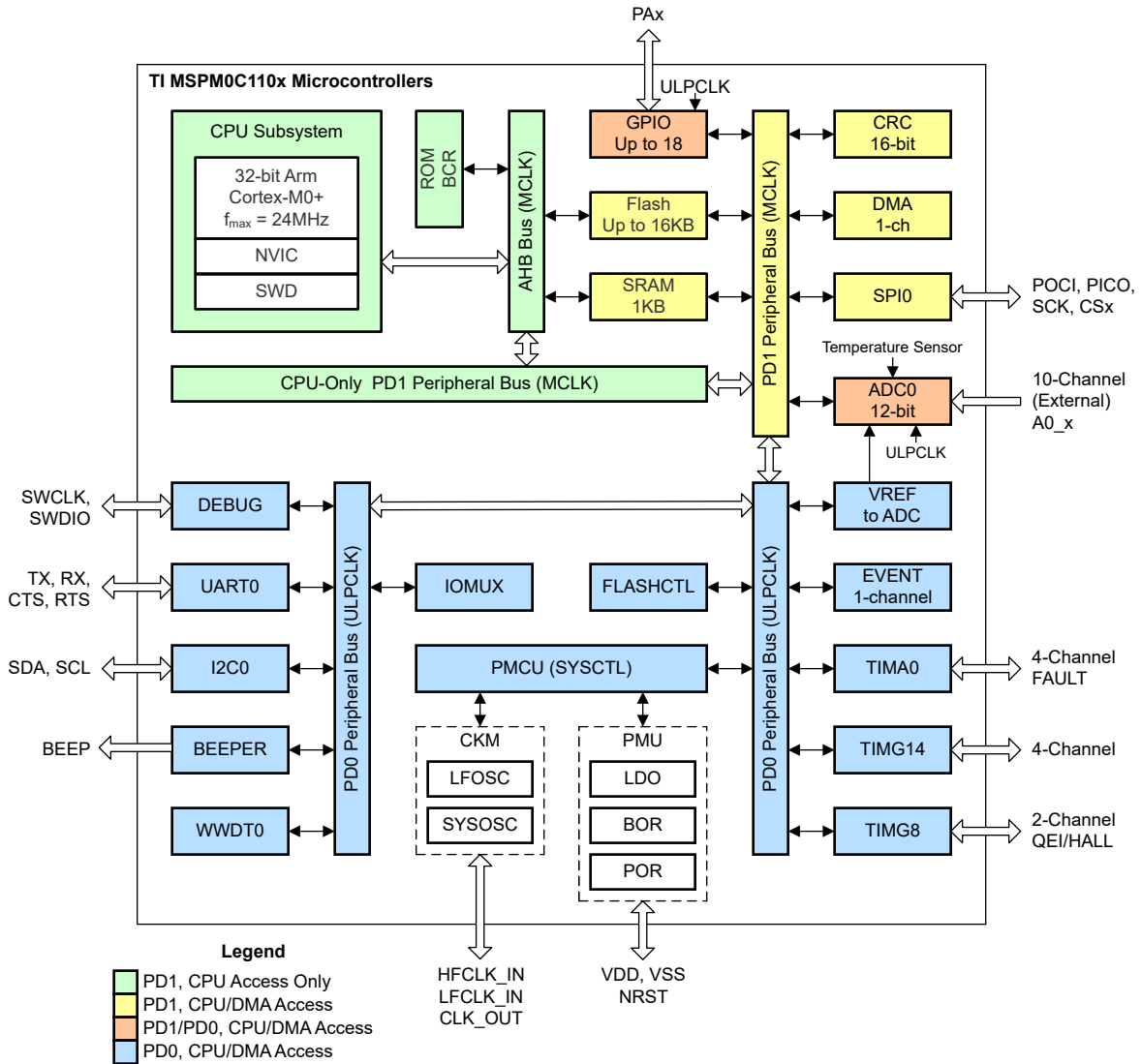


図 4-1. MSPM0C110x の機能ブロック図

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## 5 Device Comparison

表 5-1. Device Comparison

DEVICE NAME <sup>(1) (3)</sup>	FLASH / SRAM (KB)	ADC CH.	UART / I2C / SPI	TIMG	TIMA	GPIOs	5V TOL. IO	PACKAGE [PACKAGE SIZE] <sup>(2)</sup>
M0C1104QDGS20RQ1	16 / 1	10	1 / 1 / 1	2	1	18	2	20 VSSOP [5.1mm × 4.9mm]
M0C1103QDGS20RQ1	8 / 1							
M0C1104QRUKRQ1	16 / 1	10	1 / 1 / 1	2	1	18	2	20 WQFN [3mm × 3mm] <sup>(4)</sup>
M0C1103QRUKRQ1	8 / 1							
M0C1104QDYRQ1	16 / 1	8	1 / 1 / 1	2	1	14	2	16 SOT [4.2mm × 3.26mm]
M0C1103QDYRQ1	8 / 1							
M0C1104QDSGRQ1	16 / 1	3	1 / 1 / 1	2	1	6	2	8 WSON [2mm × 2mm] <sup>(4)</sup>
M0C1103QDSGRQ1	8 / 1							
M0C1104QDDFRQ1	16 / 1	3	1 / 1 / 1	2	1	6	2	8 SOT [2.9mm × 2.8mm]
M0C1103QDDFRQ1	8 / 1							

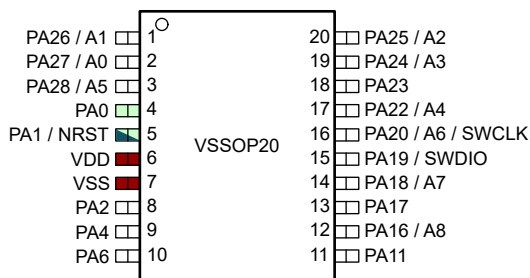
- (1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in [セクション 12](#), or see the [TI web site](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable. For package dimensions with tolerances, see the *Mechanical Data* in [セクション 12](#).
- (3) For more information about the device name, see [セクション 10.1](#).
- (4) The 8-pin WSON and 20-pin WQFN packages are available with wettable flanks.

## 6 Pin Configuration and Functions

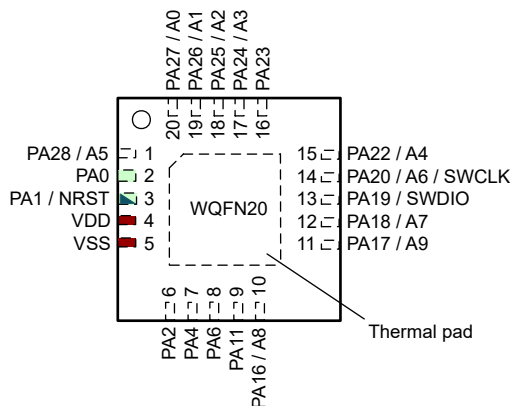
### 6.1 Pin Diagrams

- Power
- Reset
- 5-V Tolerant Open-Drain I/O (ODIO)

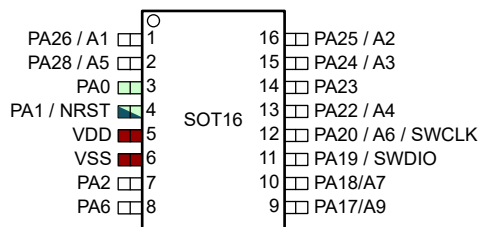
**6-1. Pin Diagram Color Coding**



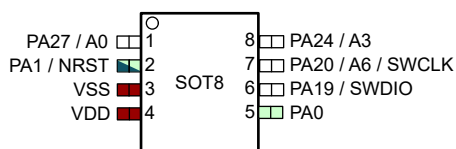
**6-2. 20-Pin DGS20 (VSSOP) (Top View)**



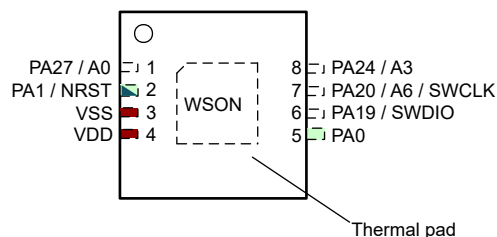
**6-3. 20-Pin RUK (WQFN) (Top View)**



**6-4. 16-Pin DYY (SOT) (Top View)**



**6-5. 8-Pin DDF (SOT) (Top View)**



**6-6. 8-Pin DSG (WSON) (Top View)**

## 6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

注

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

表 6-1. Pin Attributes

PINCMx	PIN FUNCTION			PIN NUMBER					I/O Structure
	PIN NAME	ANALOG	DIGITAL (1)	20 VSSOP	20 WQFN	16 SOT	8 SOT	8 WSON	
N/A			VDD	6	4	5	4	4	Power
N/A			VSS	7	5	6	3	3	Power
1	PA0		BEEP [2] / I2C0_SDA [3] / TIMG8_C0 [4] / SPI0_CS1 [5] / FCC_IN [6] / TIMA_FAL1 [7]	4	2	3	5	5	5V Tolerant Open-Drain
2	PA1		I2C0_SCL [2] / TIM8_C0 [3] / HFCLK_IN [4] / TIMA0_C1 [5]	5	3	4	2	2	5V Tolerant Open-Drain
N/A			NRST						Reset
3	PA2		TIMG8_C1[2] / SPI0_CS0[3] / TIMA0_C0[4] / TIMG8_IDX[5]	8	6	7	-	-	Standard
5	PA4		TIMA0_C0N[2] / SPI0_POCI[3] / LFCLK_IN[4] / HFCLK_IN[5] / TIMA0_C1N[6]	9	7	-	-	-	Standard
7	PA6		TIMG14_C1[2] / SPI0_SCK[3] / TIMA0_C1[4] / TIMG14_C2[5] / SPI0_CS0[6] / TIMA_FAL0[7]	10	8	8	-	-	Standard
12	PA11		SPI0_SCK[2] / I2C0_SCL[3] / TIMA_FAL0[4]	11	9	-	-	-	Standard
17	PA16	A8	TIMA0_C1N[2] / SPI0_POCI[3] / TIMG14_C0[4] / FCC_IN[5]	12	10	-	-	-	Standard
18	PA17	A9	UART0_TX[2] / TIMA0_C0N[3] / SPI0_SCK[4] / TIMA0_C2[5] / SPI0_CS1[6] / TIMA0_C3[7]	13	11	9	-	-	Standard
19	PA18	A7	UART0_RX[2] / SPI0_PICO[3] / TIMA0_C1N[4] / CLK_OUT[5] / TIMA0_C3[6] / TIMA0_C3N[7]	14	12	10	-	-	Standard
20	PA19		SWDIO[2] / SPI0_SCK[3] / SPI0_POCI[4] / TIMA0_C2[5] / TIMG14_C0[6] / UART0_CTS[7]	15	13	11	6	6	Standard
21	PA20	A6	SWCLK[2] / TIMA_FAL1[3] / SPI0_PICO[4] / TIMA0_C2N[5] / TIMA0_C0[6] / UART0_RTS[7]	16	14	12	7	7	Standard
23	PA22	A4	UART0_RX[2] / SPI0_POCI[3] / UART0_RTS[4] / CLK_OUT[5] / TIMA0_C1[6]	17	15	13	-	-	Standard
24	PA23		UART0_TX[2] / SPI0_CS3[3] / TIMG14_C0[4] / UART0_CTS[5] / TIMA0_C3[6] / TIMG14_C1[7]	18	16	14	-	-	Standard
25	PA24	A3	SPI0_CS2[2] / TIMG14_C1[3] / UART0_RTS[4] / TIMG14_C2[5] / TIMA0_C3N[6] / UART0_RX[7]	19	17	15	8	8	Standard
26	PA25	A2	TIMG14_C3[2] / UART0_TX[3] / SPI0_PICO[4] / TIMG14_C1[5] / TIMA_FAL2[6]	20	18	16	-	-	Standard
27	PA26	A1	TIMG8_C0[2] / UART0_RX[3] / SPI0_POCI[4] / BEEP[5] / TIMG14_C0[6] / TIMA_FAL0[7]	1	19	1	-	-	Standard
28	PA27	A0	TIMG8_C1[2] / SPI0_CS3[3] / TIMA0_C0N[4] / UART0_TX[5] / SPI0_POCI[6] / TIMA_FAL2[7]	2	20	-	1	1	Standard
29	PA28	A5	TIMA0_C0[2] / UART0_RX[3] / TIMG8_IDX[4]	3	1	2	-	-	Standard

(1) PINCM.PF and PINCM.PC in IOMUX must be set to 0 for analog functions like ADC inputs. Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

表 6-2. Digital IO Features by IO Type

IO Structure	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR
Standard-drive	Y			Y	Y
5V tolerant open-drain	Y		Y		Y

### 6.3 Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO. <sup>(1)</sup>					PIN TYPE <sup>(2)</sup>	DESCRIPTION
		20 VSSOP	20 WQFN	16 SOT	8 SOT	8 WSON		
ADC	A0	2	20	-	1	1	I	ADC0 analog input 0
	A1	1	19	1	-	-	I	ADC0 analog input 1
	A2	20	18	16	-	-	I	ADC0 analog input 2
	A3	19	17	15	8	8	I	ADC0 analog input 3
	A4	17	15	13	-	-	I	ADC0 analog input 4
	A5	3	1	2	-	-	I	ADC0 analog input 5
	A6	16	14	12	7	7	I	ADC0 analog input 6
	A7	14	12	10	-	-	I	ADC0 analog input 7
	A8	12	10	-	-	-	I	ADC0 analog input 8
	A9	13	11	9	-	-	I	ADC0 analog input 9
Clock	CLK_OUT	14, 17	12, 15	10, 13	-	-	O	Configurable clock output
Debug	SWDIO	15	14	11	6	6	I/O	Serial wire debug data input/output
	SWCLK	16	13	12	7	7	I	Serial wire debug input clock
GPIO	PA0	4	2	3	5	5	I/O	General-purpose digital I/O with open-drain capability
	PA1	5	3	4	2	2	I/O	General-purpose digital I/O with open-drain capability
	PA2	8	6	7	-	-	I/O	General-purpose digital I/O
	PA4	9	7	-	-	-	I/O	General-purpose digital I/O
	PA6	10	8	8	-	-	I/O	General-purpose digital I/O
	PA11	11	9	-	-	-	I/O	General-purpose digital I/O
	PA16	12	10	-	-	-	I/O	General-purpose digital I/O
	PA17	13	11	9	-	-	I/O	General-purpose digital I/O
	PA18	14	12	10	-	-	I/O	General-purpose digital I/O
	PA19	15	13	11	6	6	I/O	General-purpose digital I/O
	PA20	16	14	12	7	7	I/O	General-purpose digital I/O
	PA22	17	15	13	-	-	I/O	General-purpose digital I/O
	PA23	18	16	14	-	-	I/O	General-purpose digital I/O
	PA24	19	17	15	8	8	I/O	General-purpose digital I/O
	PA25	20	18	16	-	-	I/O	General-purpose digital I/O
	PA26	1	19	1	-	-	I/O	General-purpose digital I/O
	PA27	2	20	-	1	1	I/O	General-purpose digital I/O
PA28	3	1	2	-	-	I/O	General-purpose digital I/O	
I <sup>2</sup> C	I2C0_SCL	5, 11	3, 9	4	2	2	I/O	I2C0 serial clock
	I2C0_SDA	4	2	3	5	5	I/O	I2C0 serial data



FUNCTION	SIGNAL NAME	PIN NO. <sup>(1)</sup>					PIN TYPE <sup>(2)</sup>	DESCRIPTION
		20 VSSOP	20 WQFN	16 SOT	8 SOT	8 WSON		
Power	VSS	7	5	6	3	3	P	Ground supply
	VDD	6	4	5	4	4	P	Power supply
	QFN Pad	-	Pad	-	-	Pad	P	QFN package exposed thermal pad. TI recommends connection to V <sub>SS</sub> .
SPI	SPI0_CS0	8	6	7	-	-	I/O	SPI0 chip-select 0
	SPI0_CS1	4, 13	2, 11	3, 9	5	5	I/O	SPI0 chip-select 1
	SPI0_CS2	19	17	15	8	8	I/O	SPI0 chip-select 2
	SPI0_CS3	2, 18	16, 20	14	1	1	I/O	SPI0 chip-select 3
	SPI0_SCK	10, 11, 13, 15	8, 9, 11, 13	8, 9, 11	6	6	I/O	SPI0 clock signal input – SPI peripheral mode Clock signal output – SPI controller mode
	SPI0_POCI	1, 2, 9, 12, 15, 17	7, 10, 13, 15, 19, 20	1, 11, 13	1, 6	1, 6	I/O	SPI0 controller in/peripheral out
SPI0_PICO	14, 16, 20	12, 14, 18	10, 12, 16	7	7	I/O	SPI0 controller out/peripheral in	
System	NRST	5	3	4	2	2	I	Reset input active low

FUNCTION	SIGNAL NAME	PIN NO. <sup>(1)</sup>					PIN TYPE <sup>(2)</sup>	DESCRIPTION
		20 VSSOP	20 WQFN	16 SOT	8 SOT	8 WSON		
Timer	TIMA_FAL0	1, 10, 11	8, 9, 19	1, 8	-	-	I/O	Advanced control timer fault 0 handling input
	TIMA_FAL1	4, 16	2, 14	3, 12	5, 7	5, 7	I/O	Advanced control timer fault 1 handling input
	TIMA_FAL2	2, 20	18, 20	16	1	1	I/O	Advanced control timer fault 2 handling input
	TIMA0_C0	2, 3, 8, 9, 13, 16	1, 6, 7, 11, 14, 20	2, 7, 9, 12	1, 7	1, 7	I/O	Advanced control timer 0 CCR0 capture input/compare output
	TIMA0_C0N	2, 9, 13	7, 11, 20	9	1	1	I/O	Advanced control timer 0 CCR0 capture input/compare output (inverting)
	TIMA0_C1	5, 9, 10, 12, 14, 17	3, 7, 8, 10, 12, 15	4, 8, 10, 13	2	2	I/O	Advanced control timer 0 CCR1 capture input/compare output
	TIMA0_C1N	9, 12, 14	7, 10, 12	10	-	-	I/O	Advanced control timer 0 CCR1 capture input/compare output (inverting)
	TIMA0_C2	13, 15, 16	11, 13, 14	9, 11, 12	6, 7	6, 7	I/O	Advanced control timer 0 CCR2 capture input/compare output
	TIMA0_C2N	16	14	12	7	7	I/O	Advanced control timer 0 CCR2 capture input/compare output (inverting)
	TIMA0_C3	13, 14, 18, 19	11, 12, 16, 17	9, 10, 14, 15	8	8	I/O	Advanced control timer 0 CCR3 capture input/compare output
	TIMA0_C3N	14, 19	12, 17	10, 15	8	8	I/O	Advanced control timer 0 CCR3 capture input/compare output (inverting)
	TIMG14_C0	1, 12, 15, 18	10, 13, 16, 19	1, 11, 14	6	6	I/O	General purpose timer 0 CCR0 capture input/compare output
	TIMG14_C1	10, 18, 19, 20	8, 16, 17, 18	8, 14, 15, 16	8	8	I/O	General purpose timer 0 CCR1 capture input/compare output
	TIMG14_C2	10, 19	8, 17	8, 15	8	8	I/O	General purpose timer 0 CCR2 capture input/compare output
	TIMG14_C3	20	18	16	-	-	I/O	General purpose timer 0 CCR3 capture input/compare output
	TIMG8_C0	1, 4	2, 19	1, 3	5	5	I/O	General purpose timer 8 CCR0 capture input/compare output
	TIMG8_C1	2, 5, 8	3, 6, 20	4, 7	1, 2	1, 2	I/O	General purpose timer 8 CCR1 capture input/compare output
TIMG8_IDX	3, 8	1, 6	2, 7	-	-	I	General purpose timer 8 quadrature encoder index pulse input	
UART	UART0_TX	2, 13, 18, 20	11, 16, 18, 20	9, 14, 16	1	1	O	UART0 transmit data
	UART0_RX	1, 3, 14, 17, 19	1, 12, 15, 17, 19	1, 2, 10, 13, 15	8	8	I	UART0 receive data
	UART0_CTS	15, 18	13, 16	11, 14	6	6	I	UART0 "clear to send" flow control input
	UART0_RTS	16, 17, 19	14, 15, 17	12, 13, 15	7, 8	7, 8	O	UART0 "request to send" flow control output
Beeper	BEEP	1, 4	2, 19	1, 3	5	5	O	Beep output

FUNCTION	SIGNAL NAME	PIN NO. <sup>(1)</sup>					PIN TYPE <sup>(2)</sup>	DESCRIPTION
		20 VSSOP	20 WQFN	16 SOT	8 SOT	8 WSON		
FCC	FCC_IN	4, 12	2, 10	3	5	6	I	Frequency clock counter input

## 6.4 Connections for Unused Pins

表 6-3 lists the correct termination of unused pins.

**表 6-3. Connection of Unused Pins**

PIN <sup>(1)</sup>	POTENTIAL	COMMENT
PAX	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup or pulldown resistor.
NRST	VCC	NRST is an active-low reset signal. Pull high to VCC or the device cannot start. For more information, see <a href="#">セクション 9.1</a> .

(1) Any unused pin with a function that is shared with general-purpose I/O must follow the "PAX" unused pin connection guidelines.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	-0.3	4.1	V
V <sub>I</sub>	Input voltage	Applied to any 5-V tolerant open-drain pins	-0.3	5.5	V
V <sub>I</sub>	Input voltage	Applied to any common tolerance pins	-0.3	V <sub>DD</sub> + 0.3 (4.1 MAX)	V
I <sub>VDD</sub>	Current of VDD pin	Current into VDD pin (source), VDD ≥ 2.7V, -40 °C ≤ T <sub>a</sub> ≤ 85 °C		80	mA
I <sub>VSS</sub>	Current of VSS pin	Current out of VSS pin (sink), VDD ≥ 2.7V, -40 °C ≤ T <sub>a</sub> ≤ 85 °C		80	mA
I <sub>VDD</sub>	Current of VDD pin	Current into VDD pin (source), VDD ≥ 2.7V, -40 °C ≤ T <sub>a</sub> ≤ 125 °C		48	mA
I <sub>VSS</sub>	Current of VSS pin	Current out of VSS pin (sink), VDD ≥ 2.7V, -40 °C ≤ T <sub>a</sub> ≤ 125 °C		48	mA
I <sub>IO</sub>	Current for SDIO pin	Current sunk or sourced by SDIO pin, VDD ≥ 2.7V		6	mA
	Current for ODIO pin	Current sunk by ODIO pin		20	mA
I <sub>D</sub>	Supported diode current	Diode current at any device pin except PA0, PA1 and PA24		±2 <sup>(2)</sup>	mA
T <sub>stg</sub>		Storage temperature	-40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Open drain IOs PA0 and PA1 do not have the high side clamps, and PA24 has an internal connection for the testing purpose, there is no injection current allowed on these pins.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins <sup>(1)</sup>	±2000	V
V <sub>(ESD)</sub>	Electrostatic discharge	Charged device model (CDM), per pAEC Q100-011, all pins	±500	V
V <sub>(ESD)</sub>	Electrostatic discharge	Charged device model (CDM), per AEC-Q100-011, Corner pins	±750	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VDD	Supply voltage		1.62		3.6	V
C <sub>VDD</sub>	Capacitor placed between VDD and VSS <sup>(1)</sup>			10		uF
T <sub>A</sub>	Ambient temperature		-40		125	°C
T <sub>J</sub>	Max junction temperature				130	°C
f <sub>MCLK</sub>	MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states <sup>(2)</sup>				24	MHz

- (1) Connect C<sub>VDD</sub> between VDD/VSS, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C<sub>VDD</sub>.
- (2) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		PACKAGE	VALUE	UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	VSSOP-20 (DGS20)	91.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance		29.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance		48.3	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter		0.7	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter		47.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance		N/A	°C/W
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	WQFN-20 (RUK)	52.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance		55.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance		26.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter		2.1	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter		26.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance		12.0	°C/W
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	SOT-16 (DYY)	117.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance		54.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance		54.6	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter		3.0	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter		54.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance		N/A	°C/W
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	SOT-8 (DDF)	142.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance		65.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance		62.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter		3.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter		62.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance		N/A	°C/W
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	WSON-8 (DSG)	70.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance		85.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance		37.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter		2.7	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter		37.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance		12.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Supply Current Characteristics

### 7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER	MCLK	-40°C		25°C		85°C		125°C		UNIT	
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX		
<b>RUN Mode</b>											
IDDRUN	MCLK=SYSOSC, While(1), execute from flash	24MHz	2.06	2.20	2.08	2.35	2.09	2.40	2.21	2.45	mA
IDDRUN, per MHz	MCLK=SYSOSC, While(1), execute from flash	24MHz	86	92	87	98	87	100	92	102	uA/Mhz
<b>SLEEP Mode</b>											

### 7.5.1 RUN/SLEEP Modes (続き)

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDDSLEEP	MCLK=SYSOSC, CPU is halted	24MHz	1115	1256	1132	1268	1149	1380	1214	1680	uA

### 7.5.2 STOP/STANDBY Modes

VDD=3.3V unless otherwise noted. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
<b>STOP Mode</b>											
IDDSTOP0	SYSOSC=24MHz, DISABLESTOP=0	4MHz	598	640	609	646	622	710	662	733	uA
IDDSTOP2	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	305	343	311	346	324	359	364	430	
<b>STANDBY Mode</b>											
IDDSTBY0	STOPCLKSTBY=0, TIMG8, TIMG14 and TIMA0 enabled	32kHz	3.8	8.3	5.1	14	17.8	35.4	57.4	93	uA
IDDSTBY1	STOPCLKSTBY=1, TIMG8, TIMG14 and TIMA0 enabled		3.4	8.5	5.1	14	17.5	35.1	57	93	
	STOPCLKSTBY=1, GPIOA enabled		3.4	8.5	5.0	14	17.5	35.2	57	93	

### 7.5.3 SHUTDOWN Mode

All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDDSHDN	Supply current in SHUTDOWN mode	3.3V	140	320	200	350	428	932	1933	4680	nA

## 7.6 Power Supply Sequencing

### 7.6.1 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
		Falling (2)			0.01	
		Falling, STANDBY			0.1	V/ms
V <sub>POR+</sub>	Power-on reset voltage level	Rising (1)	0.92	1.284	1.59	V
V <sub>POR-</sub>		Falling (1)	0.87	1.236	1.54	V
V <sub>HYS, POR</sub>	POR hysteresis	(1)	16	47	80	mV
V <sub>BOR0+, COLD</sub>	Brown-out reset voltage level 0 (default level)	Cold start, rising (1)	1.45	1.54	1.615	V
V <sub>BOR0+</sub>		Rising (1) (2)	1.57	1.59	1.61	
V <sub>BOR0-</sub>		Falling (1) (2)	1.56	1.57	1.60	
V <sub>BOR0, STBY</sub>	Brown-out reset voltage level 0 (default level)	STANDBY mode (1)	1.52	1.57	1.60	V
V <sub>BOR1+</sub>	Brown-out-reset voltage level 1	Rising (1) (2)	2.15	2.17	2.23	V
V <sub>BOR1-</sub>		Falling (1) (2)	2.11	2.14	2.19	
V <sub>BOR1, STBY</sub>	Brown-out-reset voltage level 1	STANDBY mode (1)	2.07	2.14	2.19	V

### 7.6.1 POR and BOR (続き)

over operating free-air temperature range (unless otherwise noted)

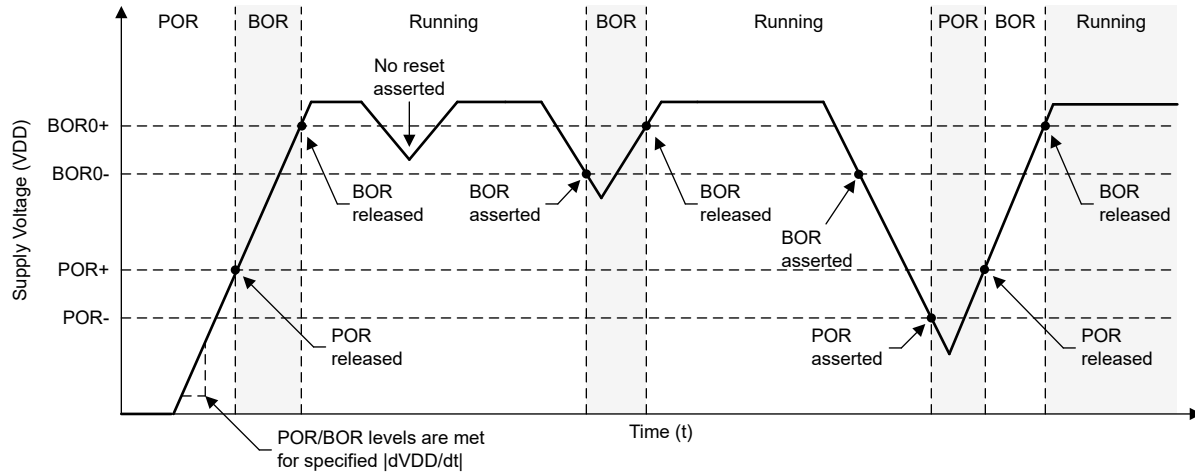
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>BOR2+</sub>	Brown-out-reset voltage level 2	Rising <sup>(1)</sup> <sup>(2)</sup>	2.74	2.77	2.83	V
V <sub>BOR2-</sub>		Falling <sup>(1)</sup> <sup>(2)</sup>	2.71	2.73	2.80	
V <sub>BOR2, STBY</sub>	Brown-out-reset voltage level 2	STANDBY mode <sup>(1)</sup>	2.67	2.73	2.80	V
V <sub>BOR3+</sub>	Brown-out-reset voltage level 3	Rising <sup>(1)</sup> <sup>(2)</sup>	2.88	2.96	3.04	V
V <sub>BOR3-</sub>		Falling <sup>(1)</sup> <sup>(2)</sup>	2.85	2.93	3.01	
V <sub>BOR3, STBY</sub>	Brown-out-reset voltage level 3	STANDBY mode <sup>(1)</sup>	2.83	2.92	3.00	V
V <sub>HYS,BOR</sub>	Brown-out reset hysteresis	Level 0 <sup>(1)</sup>		14	18	mV
		Levels 1-3 <sup>(1)</sup>		34	41	
T <sub>PD, BOR</sub>	BOR propagation delay	RUN/SLEEP/STOP mode			10	us
		STANDBY mode			100	us

(1) |dVDD/dt| ≤ 3V/s

(2) Device operating in RUN, SLEEP, or STOP mode.

### 7.6.2 Power Supply Ramp

☒ 7-1 gives the relationship of POR-, POR+, BOR0-, and BOR0+ during power-up and power-down.



☒ 7-1. Power Cycle POR/BOR Conditions

### 7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Supply</b>					
V <sub>DDPGM/ERASE</sub>	Program and erase supply voltage	1.62		3.6	V
I <sub>DDERASE</sub>	Supply current from VDD during erase operation		2		mA
I <sub>DDPGM</sub>	Supply current from VDD during program operation		2.5		mA
<b>Endurance</b>					
NWEC <sub>(LOWER)</sub>	Erase/program cycle endurance	100			k cycles
NE <sub>(MAX)</sub>	Total erase operations before failure <sup>(1)</sup>	802			k erase operations

## 7.7 Flash Memory Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NW <sub>(MAX)</sub>	Write operations per word line before sector erase <sup>(1)</sup>				83	write operations
<b>Retention</b>						
t <sub>RET_85</sub>	Flash memory data retention	-40°C ≤ T <sub>j</sub> ≤ 85°C	60			years
t <sub>RET_105</sub>	Flash memory data retention	-40°C ≤ T <sub>j</sub> ≤ 105°C	11.4			years
t <sub>RET_130</sub>	Flash memory data retention	-40°C ≤ T <sub>j</sub> ≤ 130°C	2.4			years
<b>Program and Erase Timing</b>						
t <sub>PROG (WORD, 64)</sub>	Program time for flash word <sup>(2)</sup>			40		μs
t <sub>PROG (SEC, 64)</sub>	Program time for 1kB sector			5.1		ms
t <sub>ERASE (SEC)</sub>	Sector erase time	<10k erase/program cycles		20	200	ms
t <sub>ERASE (BANK)</sub>	Bank erase time	<10k erase/program cycles		22	220	ms

- (1) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.
- (2) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.

## 7.8 Timing Characteristics

VDD=3.3V, T<sub>a</sub>=25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Wakeup Timing</b>						
t <sub>WAKE, SLEEP</sub>	Wakeup time from SLEEP to RUN			2		cycles
t <sub>WAKE, STOP</sub>	Wakeup time from STOP0 to RUN (SYSOSC enabled)			14		us
	Wakeup time from STOP2 to RUN (SYSOSC disabled)			15		us
t <sub>WAKE, STBY</sub>	Wakeup time from STANDBY to RUN			20		us
t <sub>WAKE, SHDN</sub>	Wakeup time from SHUTDOWN to RUN			112		us
<b>Asynchronous Fast Clock Request Timing</b>						
t <sub>DELAY</sub>	Delay time from edge of asynchronous request to first 24MHz MCLK edge	Mode is SLEEP2		1.2		us
		Mode is STOP2		1.2		us
		Mode is STANDBY1		5.0		us
<b>Startup Timing</b>						
t <sub>START, RESET</sub>	Device cold start-up time from reset/power-up <sup>(1)</sup>			210		us
<b>NRST Timing</b>						
t <sub>RST, BOOTRST</sub>	Pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz		2		us
		ULPCLK=32kHz		100		us
t <sub>RST, POR</sub>	Pulse length on NRST pin to generate POR			1		s

- (1) The start-up time is measured from the time that VDD crosses VBOR0+ (cold start-up) to the time that the first instruction of the user program is executed.



## 7.9 Clock Specifications

### 7.9.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{SYSOSC}}$	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		24		MHz
$f_{\text{SYSOSC}}$	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used <sup>(1)</sup>	SETUSEFCL=1, $T_a = 25\text{ }^\circ\text{C}$	-1.2		1.2	%
		SETUSEFCL=1, $0\text{ }^\circ\text{C} \leq T_a \leq 85\text{ }^\circ\text{C}$	-1.6		1.4	
		SETUSEFCL=1 $-40\text{ }^\circ\text{C} \leq T_a \leq 125\text{ }^\circ\text{C}$	-2		1.4	
$f_{\text{SYSOSC}}$	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 24MHz	SETUSEFCL=0, SYSOSCCFG.FREQ=00, $-40\text{ }^\circ\text{C} \leq T_a \leq 125\text{ }^\circ\text{C}$	-2.5		2.5	%
$t_{\text{settle, SYSOSC}}$	Settling time to target accuracy <sup>(2)</sup>	SETUSEFCL=1			30	us

- (1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.
- (2) When SYSOSC is enabled from a disabled state, the SYSOSC output will be released to the device within the time specified by  $t_{\text{start, SYSOSC}}$ . Once the output is released, the SYSOSC worst-case accuracy is specified by  $f_{\text{settle, SYSOSC}}$ . After the time specified by  $t_{\text{settle, SYSOSC}}$ , the SYSOSC will have settled to the target  $f_{\text{SYSOSC}}$  accuracy.

### 7.9.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{LFOSC}}$	LFOSC frequency			32768		Hz
$f_{\text{LFOSC}}$	LFOSC accuracy	$-40\text{ }^\circ\text{C} \leq T_a \leq 125\text{ }^\circ\text{C}$	-5		5	%
$f_{\text{LFOSC}}$	LFOSC accuracy	$-40\text{ }^\circ\text{C} \leq T_a \leq 85\text{ }^\circ\text{C}$	-3		3	%
$I_{\text{LFOSC}}$	LFOSC current consumption			300		nA
$t_{\text{start, LFOSC}}$	LFOSC start-up time			1.7		ms

## 7.10 Digital IO

### 7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{\text{IH}}$	High level input voltage	ODIO <sup>(1)</sup>	$V_{\text{DD}} \geq 1.62\text{V}$	$0.7 \cdot V_{\text{DD}}$		5.5	V
		ODIO <sup>(1)</sup>	$V_{\text{DD}} \geq 2.7\text{V}$	2		5.5	V
		All I/O except ODIO & Reset	$V_{\text{DD}} \geq 1.62\text{V}$	$0.7 \cdot V_{\text{DD}}$		$V_{\text{DD}} + 0.3$	V
$V_{\text{IL}}$	Low level input voltage	ODIO	$V_{\text{DD}} \geq 1.62\text{V}$	-0.3		$0.3 \cdot V_{\text{DD}}$	V
		ODIO	$V_{\text{DD}} \geq 2.7\text{V}$	-0.3		0.8	V
		All I/O except ODIO & Reset	$V_{\text{DD}} \geq 1.62\text{V}$	-0.3		$0.3 \cdot V_{\text{DD}}$	V
$V_{\text{HYS}}$	Hysteresis	ODIO		$0.05 \cdot V_{\text{DD}}$			V
		All I/O except ODIO		$0.1 \cdot V_{\text{DD}}$			V
$I_{\text{Ikg}}$	High-Z leakage current	SDIO <sup>(2) (3)</sup>	$V_{\text{DD}} = 3\text{V}$			50	nA
$R_{\text{PU}}$	Pull up resistance	All I/O except ODIO	$V_{\text{IN}} = V_{\text{SS}}$		40		k $\Omega$
$R_{\text{PD}}$	Pull down resistance		$V_{\text{IN}} = V_{\text{DD}}$		40		k $\Omega$
$C_{\text{I}}$	Input capacitance		$V_{\text{DD}} = 3.3\text{V}$		5		pF

### 7.10.1 Electrical Characteristics (続き)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High level output voltage	SDIO	VDD ≥ 2.7V,  I <sub>IO</sub>   <sub>max</sub> = 6mA	VDD-0.5			V
V <sub>OH</sub>	High level output voltage	SDIO	VDD ≥ 1.71V,  I <sub>IO</sub>   <sub>max</sub> = 2mA	VDD-0.4			V
V <sub>OL</sub>	Low level output voltage	SDIO	VDD ≥ 2.7V,  I <sub>IO</sub>   <sub>max</sub> = 6mA VDD ≥ 1.71V,  I <sub>IO</sub>   <sub>max</sub> = 2mA			0.4	V
V <sub>OL</sub>	Low level output voltage	ODIO	VDD ≥ 2.7V, I <sub>OL,max</sub> = 8mA VDD ≥ 1.71V, I <sub>OL,max</sub> = 4mA			0.5	V

- (1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed
- (2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
- (3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

### 7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f <sub>max</sub>	Port output frequency	SDIO (1)	VDD ≥ 1.71V, C <sub>L</sub> = 20pF			24	MHz
f <sub>max</sub>	Port output frequency	ODIO	VDD ≥ 1.71V, FM <sup>+</sup> , CL = 20pF - 100pF			1	MHz
t <sub>r</sub> , t <sub>f</sub>	Output rise/fall time	All output ports except ODIO	VDD ≥ 1.71V			0.3*f <sub>max</sub>	s
t <sub>f</sub>	Output fall time	ODIO	VDD ≥ 1.71V, FM <sup>+</sup> , CL = 20pF-100pF	20*VDD/5.5		120	ns

- (1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed , HDIO = High-Drive

## 7.11 ADC

### 7.11.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>IN(ADC)</sub>	Analog input voltage range <sup>(1)</sup>	Applies to all ADC analog input pins		0		VDD	V
V <sub>R+</sub>	Positive ADC reference voltage	V <sub>R+</sub> sourced from VDD			VDD		V
		V <sub>R+</sub> sourced from internal reference (VREF)			VREF		V
V <sub>R-</sub>	Negative ADC reference voltage				0		V
F <sub>S</sub>	ADC sampling frequency	RES = 0x0 (12-bit mode), VDD Reference				1.5	MSPS
		RES = 0x1 (10-bit mode), VDD Reference				1.7	
		RES = 0x2 (8-bit mode), VDD Reference				2	
F <sub>S</sub>	ADC sampling frequency	RES = 0x0 (12-bit mode), Internal Reference				0.866	MSPS
		RES = 0x1 (10-bit mode), Internal Reference				1	
		RES = 0x2 (8-bit mode), Internal Reference				1.2	
I <sub>(ADC)</sub>	Operating supply current into VDD terminal	F <sub>S</sub> = 1.5MSPS, V <sub>R+</sub> = VDD			200	220	μA
		F <sub>S</sub> = 0.856MSPS, V <sub>R+</sub> = VREF = 2.5V (VREF power consumption included)			220	250	
C <sub>S/H</sub>	ADC sample-and-hold capacitance				0.22		pF
R <sub>in</sub>	ADC switch resistance				25		kΩ
ENOB	Effective number of bits	VDD reference (2)		9.3	10.4		bit
		VDD reference with over sampling			12.2		
		Internal reference, V <sub>R+</sub> = VREF = 2.5V		9.4	9.8		
SNR	Signal-to-noise ratio	VDD reference (2)			64		dB
		VDD reference with over sampling			75		
		Internal reference, V <sub>R+</sub> = VREF = 2.5V			61		

### 7.11.1 Electrical Characteristics (続き)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR <sub>DC</sub>	Power supply rejection ratio, DC	VDD = VDD <sub>(min)</sub> to VDD <sub>(max)</sub> Internal reference, V <sub>R+</sub> = VREF = 2.5V		61		dB
T <sub>wakeup</sub>	ADC Wakeup Time	Assumes internal reference is active			5	us
V <sub>SupplyMon</sub>	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor <sup>(3)</sup>	-0.6		+2.5	%
I <sub>SupplyMon</sub>	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA

- (1) The analog input voltage range must be within the selected ADC reference voltage range V<sub>R+</sub> to V<sub>R-</sub> for valid conversion results.
- (2) VDD reference specifications are measured with V<sub>R+</sub> = VDD = 3.3V and V<sub>R-</sub> = VSS = 0V
- (3) Analog power supply monitor. Analog input on channel 15 is disconnected and is internally connected to the voltage divider which is VDD/3.

### 7.11.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>ADCCLK</sub>	ADC clock frequency		12		24	MHz
t <sub>ADC trigger</sub>	Software trigger minimum width		3			ADCCLK cycles
t <sub>Sample_step</sub>	Sampling time for step input	12-bit mode, R <sub>S</sub> = 50Ω, C <sub>pext</sub> = 10pF	0.166			μs
t <sub>Sample_VREF</sub>	Sample time with VREF	ADC CHANNEL=12, 12-bit mode, VDD as reference	4			μs
t <sub>Sample_SupplyMon</sub>	Sample time with Supply Monitor (VDD/3)		3			μs

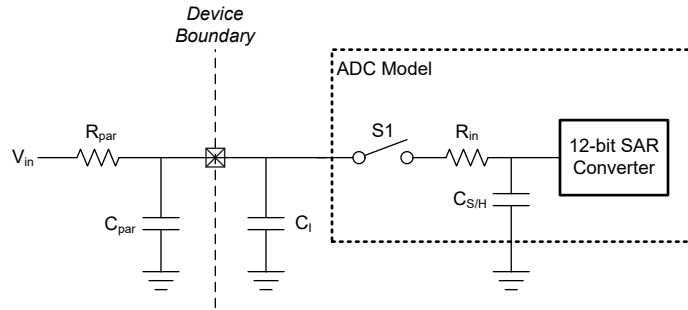
### 7.11.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E <sub>I</sub>	Integral linearity error (INL)	VDD reference, 10-bit <sup>(2)</sup>	-1.0		+1.0	LSB
		VDD reference, 12-bit <sup>(2)</sup>	-4.0		+4.0	LSB
E <sub>D</sub>	Differential linearity error (DNL)	VDD reference, 10-bit <sup>(2)</sup>	-1.0		+1.0	LSB
		VDD reference, 12-bit <sup>(2)</sup>	-1.0		+4.0	LSB
E <sub>O</sub>	Offset error	VDD reference, 10-bit <sup>(2) (3)</sup>	-3		3	mV
		VDD reference, 12-bit <sup>(2) (3)</sup>	-3		3	mV
E <sub>G</sub>	Gain error	VDD reference, 10-bit <sup>(2)</sup>	-5		5	LSB
		VDD reference, 12-bit <sup>(2)</sup>	-25		25	LSB

- (1) Total Unadjusted Error (TUE) can be calculated from E<sub>I</sub>, E<sub>O</sub>, and E<sub>G</sub> using the following formula: TUE = √(E<sub>I</sub><sup>2</sup> + |E<sub>O</sub>|<sup>2</sup> + E<sub>G</sub><sup>2</sup>)  
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate
- (2) VDD reference specifications are measured with V<sub>R+</sub> = VDD and V<sub>R-</sub> = VSS = 0V.
- (3) Offset error achieves +/-3mV after software calibration

### 7.11.4 Typical Connection Diagram



**図 7-2. ADC Input Network**

1. Refer to [ADC Electrical Characteristics](#) for the values of  $R_{in}$  and  $C_{S/H}$
2. Refer to [Digital IO Electrical Characteristics](#) for the value of  $C_i$
3.  $C_{par}$  and  $R_{par}$  represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1.  $\tau = (R_{par} + R_{in}) \times C_{S/H} + R_{par} \times (C_{par} + C_i)$
2.  $K = \ln(2^N / \text{Settling error}) - \ln((C_{par} + C_i) / C_{S/H})$
3.  $T \text{ (minimum sampling time)} = K \times \tau$

### 7.12 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{TRIM}$	Factory trim temperature <sup>(1)</sup>		27	30	33	°C
$TS_c$	Temperature coefficient		-1.9	-1.8	-1.7	mV/°C
$t_{SET, TS}$	Temperature sensor settling time <sup>(2)</sup>	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h (VREF=1.4V), ADC CHANNEL=11		2.5	10	us

- (1) Higher absolute accuracy may be achieved through user calibration.
- (2) This is the minimum required ADC sampling time when measuring the temperature sensor.

### 7.13 VREF

#### 7.13.1 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DDmin}$	Minimum supply voltage needed for VREF operation	BUFCONFIG = 1	1.62			V
		BUFCONFIG = 0	2.7			
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.378	1.4	1.421	V
		BUFCONFIG = 0	2.462	2.5	2.541	

#### 7.13.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{VREF}$	VREF operating supply current (this spec is an estimation and will be more reliable once the IP is further in the design phase)	BUFCONFIG = {0, 1}, No load	BUFCONFIG = {0, 1}, No load.		80	100	μA
$TC_{VREF}$	Temperature coefficient of VREF <sup>(1)</sup>	BUFCONFIG = {0, 1}	BUFCONFIG = {0, 1}			75	ppm/°C

### 7.13.2 Electrical Characteristics (続き)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$TC_{\text{drift}}$	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C			300	ppm
$T_{\text{startup}}$	VREF startup time	BUFCONFIG = {0, 1}, VDD = 2.7 V	BUFCONFIG = {0, 1}, VDD = 2.7 V			10	us

- (1) The temperature coefficient of the VREF output is the sum of  $TC_{V_{\text{RBUF}}}$  and the temperature coefficient of the internal bandgap reference.

## 7.14 I2C

### 7.14.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

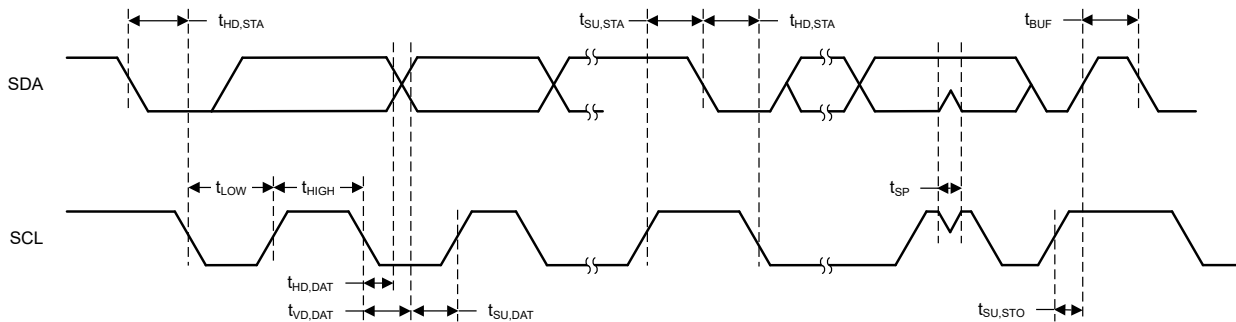
PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{I2C}}$	I2C input clock frequency	I2C in Power Domain0	24		24		24		MHz
$f_{\text{SCL}}$	SCL clock frequency		100		400		1000		kHz
$t_{\text{HD,STA}}$	Hold time (repeated) START		4		0.6		0.26		us
$t_{\text{LOW}}$	LOW period of the SCL clock		4.7		1.3		0.5		us
$t_{\text{HIGH}}$	High period of the SCL clock		4		0.6		0.26		us
$t_{\text{SU,STA}}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{\text{HD,DAT}}$	Data hold time		0		0		0		ns
$t_{\text{SU,DAT}}$	Data setup time		250		100		50		ns
$t_{\text{SU,STO}}$	Setup time for STOP		4		0.6		0.26		us
$t_{\text{BUF}}$	bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{\text{VD,DAT}}$	data valid time			3.45		0.9		0.45	us
$t_{\text{VD,ACK}}$	data valid acknowledge time			3.45		0.9		0.45	us

### 7.14.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{SP}}$	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		11	35	ns
$f_{\text{SP}}$	Pulse duration of spikes suppressed by input filter	AGFSELx = 1		14	35	ns
$f_{\text{SP}}$	Pulse duration of spikes suppressed by input filter	AGFSELx = 2		22	60	ns
$f_{\text{SP}}$	Pulse duration of spikes suppressed by input filter	AGFSELx = 3		35	90	ns

### 7.14.3 I<sup>2</sup>C Timing Diagram



7-3. I2C Timing Diagram

## 7.15 SPI

### 7.15.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SPI</b>						
$f_{SPI}$	SPI clock frequency	Clock max speed = 24MHz 1.62 < VDD < 3.6V Controller mode			12	MHz
$f_{SPI}$	SPI clock frequency	Clock max speed = 24MHz 1.62 < VDD < 3.6V Peripheral mode			12	MHz
$DC_{SCK}$	SCK Duty Cycle		40	50	60	%
<b>Controller</b>						
$t_{SCLK\_H/L}$	SCLK High or Low time		$(t_{SPI}/2) - 1$	$t_{SPI} / 2$	$(t_{SPI}/2) + 1$	ns
$t_{CS\_LEAD}$	CS lead-time, CS active to clock		1			ns
$t_{CS\_LAG}$	CS lag time, Last clock to CS inactive		11			ns
$t_{CS\_ACC}$	CS access time, CS active to PICO data out				93	ns
$t_{CS\_DIS}$	CS disable time, CS inactive to PICO high impedance				10	ns
$t_{SU,CI}$	POCI input data setup time <sup>(1)</sup>	2.7 < VDD < 3.6V, delayed sampling enabled	1			ns
		1.62 < VDD < 2.7V, delayed sampling enabled	1			
$t_{SU,CI}$	POCI input data setup time <sup>(1)</sup>	2.7 < VDD < 3.6V, no delayed sampling	27			ns
		1.62 < VDD < 2.7V, no delayed sampling	35			
$t_{HD,CI}$	POCI input data hold time		9			ns
$t_{VALID,CO}$	PICO output data valid time <sup>(2)</sup>				10	ns
$t_{HD,CO}$	PICO output data hold time <sup>(3)</sup>		1			ns
<b>Peripheral</b>						
$t_{CS\_LEAD}$	CS lead-time, CS active to clock		8			ns
$t_{CS\_LAG}$	CS lag time, Last clock to CS inactive		0			ns
$t_{CS\_ACC}$	CS access time, CS active to POCI data out				50	ns

### 7.15.1 SPI (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CS,DIS}$	CS disable time, CS inactive to POCI high impedance				50	ns
$t_{SU,PI}$	PICO input data setup time		2			ns
$t_{HD,PI}$	PICO input data hold time		1			ns
$t_{VALID,PO}$	POCI output data valid time <sup>(2)</sup>	$2.7 < VDD < 3.6V$			34	ns
$t_{VALID,PO}$	POCI output data valid time <sup>(2)</sup>	$1.62 < VDD < 2.7V$			41	ns
$t_{HD,PO}$	POCI output data hold time <sup>(3)</sup>		5			ns

- (1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
- (2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
- (3) Specifies how long data on the output is valid after the output changing SCLK clock edge

### 7.15.2 SPI Timing Diagrams

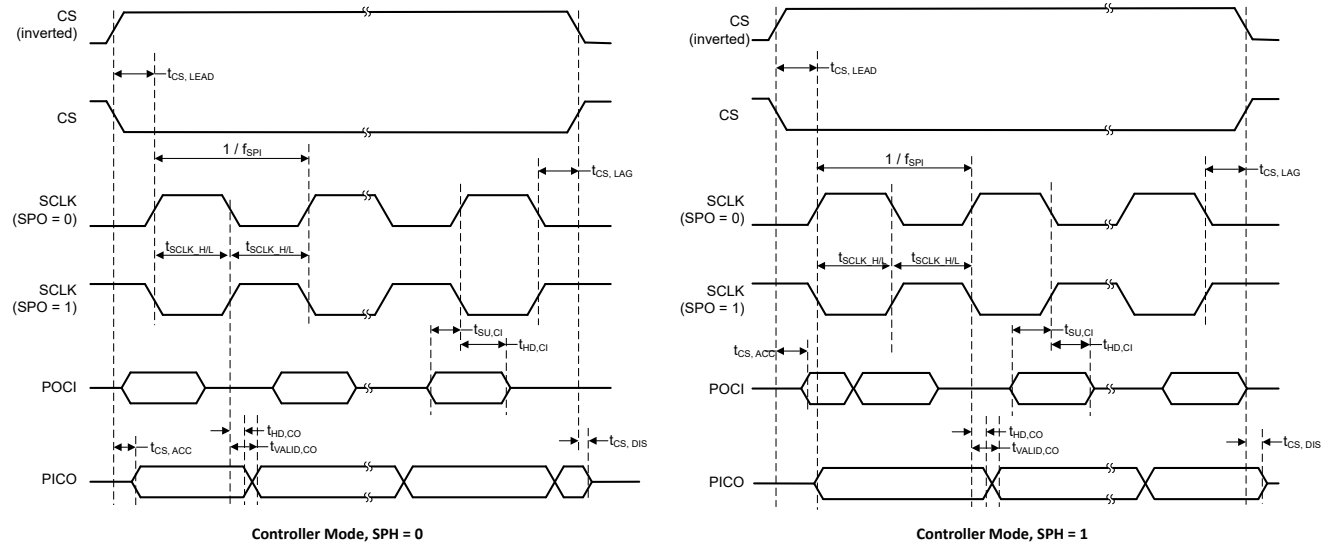


図 7-4. SPI Timing Diagram - Controller Mode

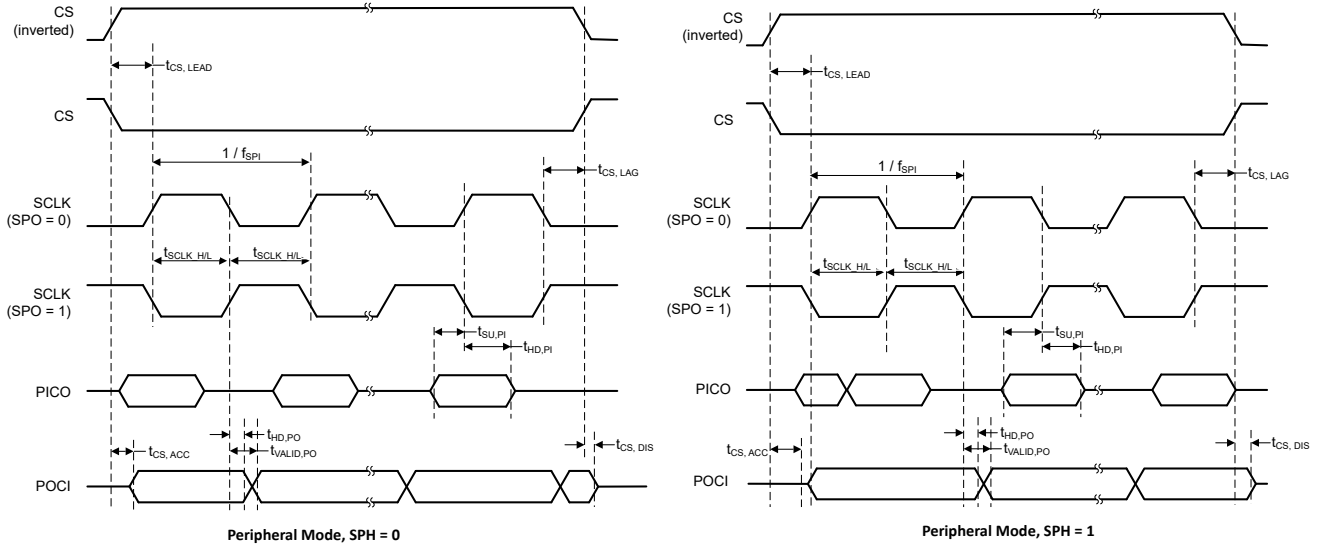


图 7-5. SPI Timing Diagram - Peripheral Mode

### 7.16 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{UART}}$	UART input clock frequency				24	MHz
$f_{\text{BITCLK}}$	BITCLK clock frequency (equals baud rate in MBaud)				3	MHz
$t_{\text{SP}}$	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		11	35	ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

### 7.17 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{res}}$	Timer resolution time	$f_{\text{TIMxCLK}} = 24\text{MHz}$	41.67			ns
			1			$t_{\text{TIMxCLK}}$
$t_{\text{res}}$	Timer resolution time	TIMx with 16bit counter			16	bit

### 7.18 Windowed Watchdog Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\text{WWDT}_{\text{FREQ}}$	WWDT operating frequency			32.768		kHz
$\text{WWDT}_{\text{Tstart}}$	WWDT counter start time	Write to WWDTCTL0 until WWDT counter starts ( $\text{WWDT}_{\text{FREQ}} = 32.768\text{kHz}$ )			30.5	$\mu\text{s}$
$\text{WWDT}_{\text{Trestart}}$	WWDT counter restart time	Write to WWDCNTRST until WWDT counter restarts ( $\text{WWDT}_{\text{FREQ}} = 32.768\text{kHz}$ )			30.5	$\mu\text{s}$



## 7.19 Emulation and Debug

### 7.19.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>SWD</sub>	SWD frequency				10	MHz

## 8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

### 8.1 CPU

The CPU subsystem (MCPUSS) implements an Arm Cortex-M0+ CPU, a system timer, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized 32-bit CPU that delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- Arm Cortex-M0+ CPU supports clock frequencies from 32kHz to 24MHz
  - ARMv6-M Thumb instruction set (little endian) with 32-cycle 32x32 slow multiply instruction
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail chaining

### 8.2 Operating Modes

MSPM0C MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST or SWD. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (for example, RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0C devices implement two power domains: **PD1** (for the CPU, memories, and high performance peripherals), and **PD0** (for low speed, low power peripherals).

- **PD1** is always powered in RUN and SLEEP modes, but is disabled in all other modes.
- **PD0** is always powered in RUN, SLEEP, STOP, and STANDBY modes.
- PD1 and PD0 are both disabled in SHUTDOWN mode.

#### 8.2.1 Functionality by Operating Mode (MSPM0C110x)

表 8-1 lists the supported functionality in each operating mode.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but use of the function is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained.

表 8-1. Supported Functionality by Operating Mode

Operating Mode		RUN			SLEEP			STOP		STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1	
Oscillators	SYSOSC	EN	EN	DIS	EN	EN	DIS	OPT <sup>(1)</sup>	DIS	DIS	DIS	OFF
	LFOSC	EN										OFF

表 8-1. Supported Functionality by Operating Mode (続き)

Operating Mode		RUN			SLEEP			STOP		STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1	
Clocks	CPUCLK	24M	32k	32k	DIS							OFF
	MCLK to PD1	24M	32k	32k	24M	32k	32k	DIS				OFF
	ULPCLK to PD0	24M	32k	32k	24M	32k	32k	4M <sup>(1)</sup>	32k	DIS	OFF	
	ULPCLK to TIMG14, TIMG8	24M	32k	32k	24M	32k	32k	4M <sup>(1)</sup>	32k		OFF	
	MFCLK	OPT	DIS		OPT	DIS		OPT	DIS			OFF
	LFCLK	32k							DIS		OFF	
	LFCLK to TIMG14, TIMG8	32k							DIS			OFF
	MCLK Monitor	OPT							DIS		OFF	
PMU	POR Monitor	EN										
	BOR Monitor	EN										
	Core Regulator	Full drive							Low drive		OFF	
Core Functions	CPU	EN			DIS					OFF		
	DMA	OPT					NS (triggers supported)				OFF	
	Flash	EN					OPT	DIS			OFF	
	SRAM	EN					OPT	DIS			OFF	
PD1 Peripherals	SPI0	OPT					DIS				OFF	
	CRC	OPT					DIS				OFF	
PD0 Peripherals	TIMA0	OPT					DIS					OFF
	TIMG8	OPT					DIS					OFF
	TIMG14	OPT					DIS					OFF
	UART0	OPT					DIS				OPT <sup>(2)</sup>	OFF
	I2C0	OPT					DIS				OPT <sup>(2)</sup>	OFF
	GPIOA	OPT					DIS				OPT <sup>(2)</sup>	OFF
	WWDT0	OPT					DIS				DIS	OFF
Analog	ADC0	OPT					NS (triggers supported)				OFF	
	VREF	OPT					NS				OFF	
	Temperature Sensor	OPT					NS				OFF	
IOMUX and IO Wakeup	EN										DIS	
Wake Sources	N/A			ANY IRQ			PD0 IRQ				NRST, SWD	

- (1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as it was in RUN1, and ULPCLK remains at 32kHz as it was in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as it was in RUN2, and ULPCLK remains at 32kHz as it was in RUN2.
- (2) When using the STANDBY1 policy for STANDBY, only TIMG8, TIMG14 and TIMA0 are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.

### 8.3 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor

- Brown-out reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

## 8.4 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32kHz)
- **SYSOSC**: Internal high-frequency oscillator (24MHz)
- **LFCKIN**: low-frequency digital clock input (32KHz)
- **HFCKIN**: high-frequency digital clock input (4 to 24MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC or LFCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **CLK\_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes

For more details, see the CKM chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

## 8.5 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA in these devices support the following key features:

- 1 DMA transfer channel
- Direct peripheral to DMA trigger is supported only from ADC.
- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection

表 8-2 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

**表 8-2. DMA Trigger Mapping**

TRIGGER 0:6	SOURCE
0	Software
1	Generic Subscriber 0 (FSUB_0)
2	Generic Subscriber 1 (FSUB_1)
3	ADC0 Publisher 2

## 8.6 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) that are interconnected through an event fabric containing a combination of static and programmable routes.

Events that are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: GPIO interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: ADC trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
  - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

For more details, see the Event chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

**表 8-3. Generic Event Channels**

A generic route is a point-to-point (1:1) route in which the peripheral publishing the event is configured to use the available generic route channel to publish the event to another entity. An entity can be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1

## 8.7 Memory

### 8.7.1 Memory Organization

表 8-4 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* section in the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

**表 8-4. Memory Organization**

Memory Region	Subregion	MSPM0C1103, MSPS003F3	MSPM0C1104, MSPS003F4
Code (Flash)	Flash	8KB <sup>(1)</sup> 0x0000.0000 to 0x0000.1FFF	16KB <sup>(1)</sup> 0x0000.0000 to 0x0000.3FFF
SRAM (SRAM)	SRAM	1KB 0x2000.0000 to 0x2000.03FF	1KB 0x2000.0000 to 0x2000.03FF
Peripheral	Peripherals	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF
	Flash	0x0040.0000 to 0x0040.1FFF	0x0040.0000 to 0x0040.3FFF
	Configuration NVM	512 bytes 0x41C0.0000 to 0x41C0.0200	512 bytes 0x41C0.0000 to 0x41C0.0200
	FACTORY	0x41C4.0000 to 0x41C4.0080	0x41C4.0000 to 0x41C4.0080
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

(1) Up to 100000 program and erase cycles.

### 8.7.2 Peripheral File Map

表 8-5 lists the available peripherals and the register base address for each.

**表 8-5. Peripherals Summary**

PERIPHERAL NAME	BASE ADDRESS	SIZE
VREF	0x40030000	0x2000
WWDT0	0x40080000	0x2000
TIMG14	0x40084000	0x2000
TIMG8	0x40090000	0x2000
GPIO0	0x400A0000	0x2000
SYSCTL	0x400AF000	0x3000
DEBUGSS	0x400C7000	0x2000
EVENT	0x400C9000	0x3000
NVMNW	0x400CD000	0x2000
I2C0	0x400F0000	0x2000
UART0	0x40108000	0x2000
MCPUSS	0x40400000	0x2000
WUC	0x40424000	0x1000
IOMUX	0x40428000	0x2000
DMA	0x4042A000	0x2000
CRC	0x40440000	0x2000
SPI0	0x40468000	0x2000
ADC0	0x40004000	0x2000
TIMA0	0x40860000	0x2000
ADC0 <sup>(1)</sup>	0x4055A000	0x2000

(1) Aliased region of ADC0 memory-mapped registers

### 8.7.3 Peripheral Interrupt Vector

表 8-6 shows the IRQ number and the interrupt group number for each peripherals. There is only one group GROUP0 in this device.

**表 8-6. Interrupt Vector Number**

PERIPHERAL NAME	NVIC IRQ	GROUP0 IIDX
WWDT0	0	0
DEBUGSS	0	2
NVMNW	0	3
SYSCTL	0	6
GPIO0	1	-
TIMG8	2	-
ADC	4	-
SPI0	9	-
UART0	15	-
TIMG14	16	-
TIMA0	18	-
I2C0	24	-
DMA	31	-

## 8.8 Flash Memory

A single bank of nonvolatile flash memory is provided for storing executable program code and application data.

Key features of the flash include:

- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1KB sector sizes (minimum erase resolution of 1KB)
- Up to 100000 program and erase cycles

For a complete description of the flash memory, see the NVM chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

## 8.9 SRAM

MSPM0Cxx MCUs include a low-power high-performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in RUN, SLEEP, STOP, and STANDBY operating modes and is lost in SHUTDOWN mode. A write protection mechanism is provided to allow the application to dynamically write protect the SRAM memory with 1KB resolution. Write protection is useful when placing executable code into SRAM to provide a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

## 8.10 GPIO

The general purpose input/output (GPIO) peripheral lets the application write data out and read data in through the device pins. Through the use of the Port A GPIO peripheral, these devices support up to 18 GPIO pins.

The key features of the GPIO module include:

- 0 wait state MMR access from CPU
- Set, clear, or toggle multiple bits without the need of a read-modify-write construct in software
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

## 8.11 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO pad configuration registers allow for programmable drive strength, speed, pullup or pulldown, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#) ..

## 8.12 ADC

The 12-bit analog-to-digital converter (ADC) module in these devices support fast 12-bit conversions with single-ended inputs.

ADC features include:

- 12-bit output resolution at up to 1.5-Msps with greater than 10-bit ENOB
- Up to 10 external input channels
- Internal channels for temperature sensing, supply monitoring, and analog signal chain
- Software selectable reference:
  - Configurable internal dedicated ADC reference voltage of 1.4V and 2.5V (VREF)
  - MCU supply voltage (VDD)
- Operates in RUN, SLEEP, and STOP modes and supports triggers from STANDBY mode

**表 8-7. ADC0 Channel Mapping**

CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME
0	A0	8	A8
1	A1	9	A9
2	A2	10	-
3	A3	11	<i>Temperature Sensor</i>
4	A4	12	<i>VREF</i>
5	A5	13	-
6	A6	14	-
7	A7	15	<i>Supply/Battery Monitor</i>

*Italicized* signal names are internal to the SoC. These signals are used for internal peripheral interconnections.

For more details, see the ADC chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#) .

## 8.13 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 1.4V internal VREF at the factory trim temperature ( $TS_{TRIM}$ ). This calibration value can be used with the temperature sensor temperature coefficient ( $TS_C$ ) to estimate the device temperature. See the temperature sensor section of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#) for guidance on estimating the device temperature with the factory trim value.



## 8.14 VREF

The voltage reference module (VREF) in these devices contains a configurable voltage reference buffer dedicated for the on-board ADC.

VREF features include:

- 1.4V and 2.5V user-selectable internal references
- Internal reference supports ADC operation up to 1Msps at 10-bit mode

For more details, see the VREF chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

## 8.15 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for bit reversal

For more details, see the CRC chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

## 8.16 UART

The UART peripherals provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Glitch filter on the input signals
  - Programmable baud rate generation with oversampling by 16, 8, or 3
  - Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs
- Support transmit and receive loopback mode operation
- See [表 8-8](#) for detail information on supported protocols

**表 8-8. UART Features**

UART FEATURES	UART0 (Extend)
Active in stop and standby modes	Yes
Separate transmit and receive FIFOs	Yes
Support hardware flow control	Yes
Support 9-bit configuration	Yes
Support LIN mode	Yes
Support DALI	Yes
Support IrDA	Yes
Support ISO7816 Smart Card	Yes
Support Manchester coding	Yes

For more details, see the UART chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

## 8.17 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPCLK/2 bit rate and up to 12 Mb/s in both controller and peripheral modes
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode)
- Programmable data frame size from 7 bits to 16 bits (peripheral mode)
- Separated transmit and receive FIFOs
- Supports TI mode, Motorola mode, and National Microwire format

For more details, see the SPI chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

## 8.18 I2C

The inter-integrated circuit interface (I<sup>2</sup>C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
- Separated transmit and receive FIFOs
- Support SMBus 3.0 with PEC, ARP, timeout detection, and host support
- Wakeup from low-power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression

For more details, see the I2C chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

## 8.19 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

## 8.20 Timers (TIMx)

The timer peripherals in these devices support the following key features. For specific configuration, see [表 8-9](#).

Specific features for the **general-purpose timer (TIMGx)** include:

- 16-bit down, up/down, or up counter with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent channels for

- Output compare
- Input capture
- PWM output
- One-shot mode
- Support quadrature encoder interface (QEI) for positioning and movement sensing
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt trigger generation and cross peripherals (such as ADC) trigger capability
- Cross-trigger event logic for Hall sensor inputs

Specific features for the **advanced timer (TIMAx)** include:

- 16-bit down or up-down counter, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- Up to four independent channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow register for load and CC register available
- Complementary output PWM
- Asymmetric PWM with programmable dead band insertion
- Fault handling mechanism to keep the output signals in a safe user-defined state when a fault condition is encountered
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

**表 8-9. TIMx Configurations**

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEAD-BAND	FAULT	QEI
TIMG14	PD0	16 bit	8 bit	–	4	–	–	–	–	–	–
TIMG8	PD0	16 bit	8 bit	–	2	–	–	–	–	–	Yes
TIMA0	PD1	16 bit	8 bit	8-bit	4	Yes	Yes	Yes	Yes	Yes	–

For more details, see the timer chapters of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

## 8.21 Device Analog Connections

図 8-1 shows the internal analog connection of the device.

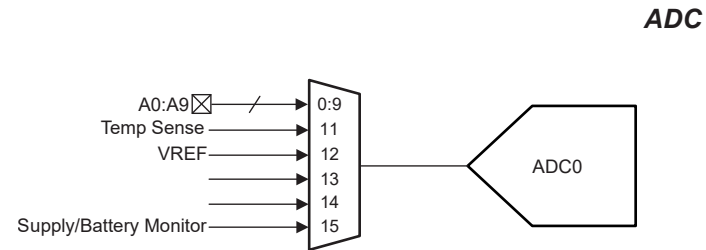


図 8-1. Analog Connections

## 8.22 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO and provides the controls for the output driver and input path. For more information, see the IOMUX section of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in [Figure 8-2](#). Not all pins have analog functions, drive strength control, and pullup or pulldown resistors available.

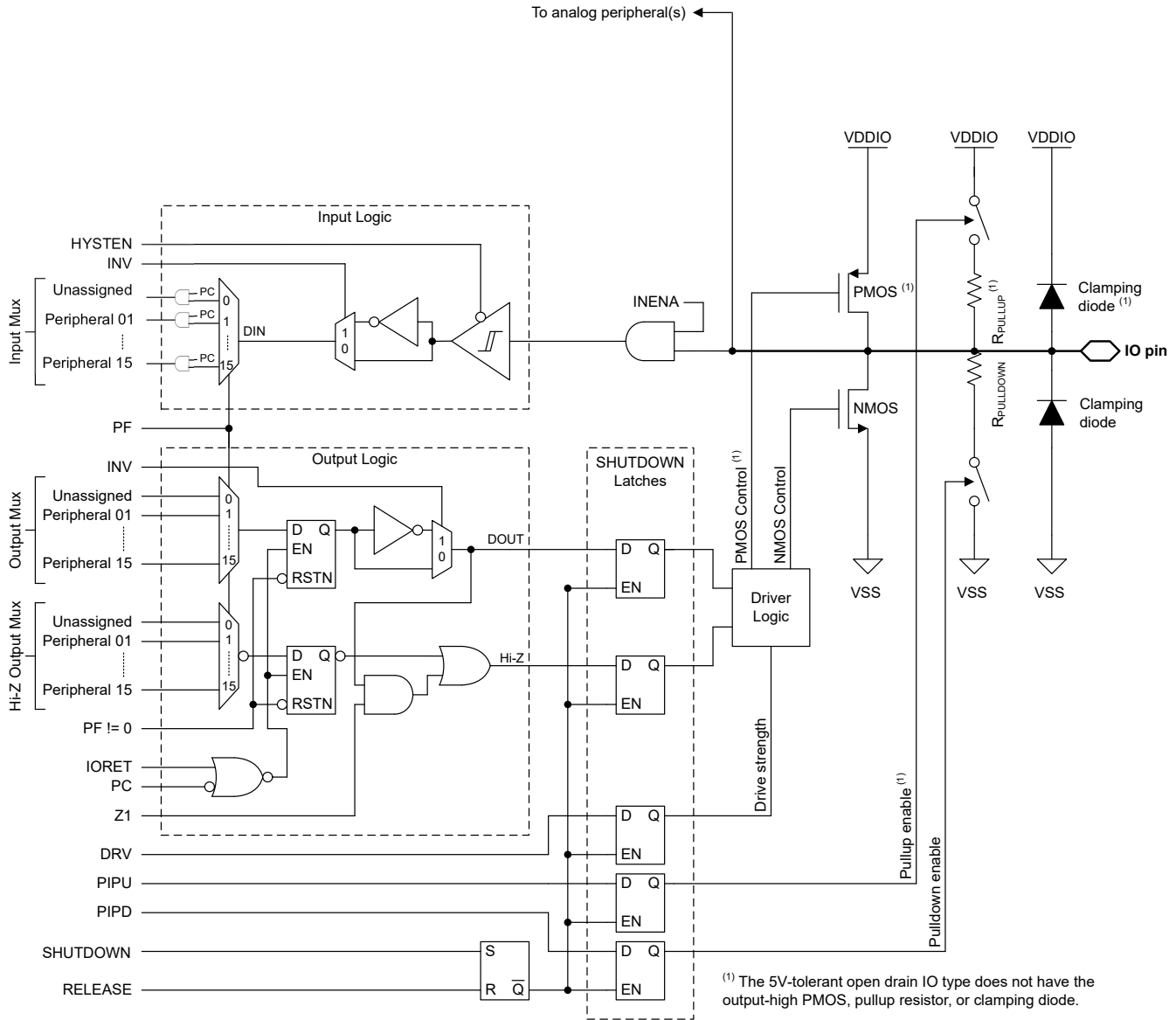


Figure 8-2. Superset Input/Output Diagram

## 8.23 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality offered on MSPM0 devices, see the debug chapter of the technical reference manual.

**表 8-10. Serial Wire Debug Pin Requirements and Functions**

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

## 8.24 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. See the *Factory Constants* section of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

**表 8-11. DEVICEID**

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	DEVICEID.PARTNUM	DEVICEID.MANUFACTURER
MSPM0C1103-Q1	0xBBA1	0x17
MSPM0C1104-Q1	0xBBA1	0x17

**表 8-12. USERID**

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	PART	VARIANT	Device	PART	VARIANT
M0C1104QDGS20RQ1	A608	10	M0C1103QDGS20RQ1	8A2B	15
M0C1104QRUKRQ1	A608	11	M0C1103QRUKRQ1	8A2B	16
M0C1104QDYRQ1	A608	12	M0C1103QDYRQ1	8A2B	17
M0C1104QDDFRQ1	A608	13	M0C1103QDDFRQ1	8A2B	18
M0C1104QDSDGRQ1	A608	14	M0C1103QDSDGRQ1	8A2B	19

## 8.25 Identification

### Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region (see the Device Factory Constants section) which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. For more information, see the *Factory Constants* chapter of the [MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual](#).

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata describes these markings.

## 9 Applications, Implementation, and Layout

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Typical Application

#### 9.1.1 Schematic

TI recommends connecting a combination of a 10- $\mu\text{F}$  and a 0.1- $\mu\text{F}$  low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors can be used but can affect the supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins (within a few millimeters).

PA1 and NRST are double bonded for some variants. If it's used as a NRST, it must connect an external 47-k $\Omega$  pullup resistor with a 10-nF pulldown capacitor.

For 5V-tolerant open drain (ODIO), a pullup resistor is required to output high for I2C and UART functions if the ODIO are used.

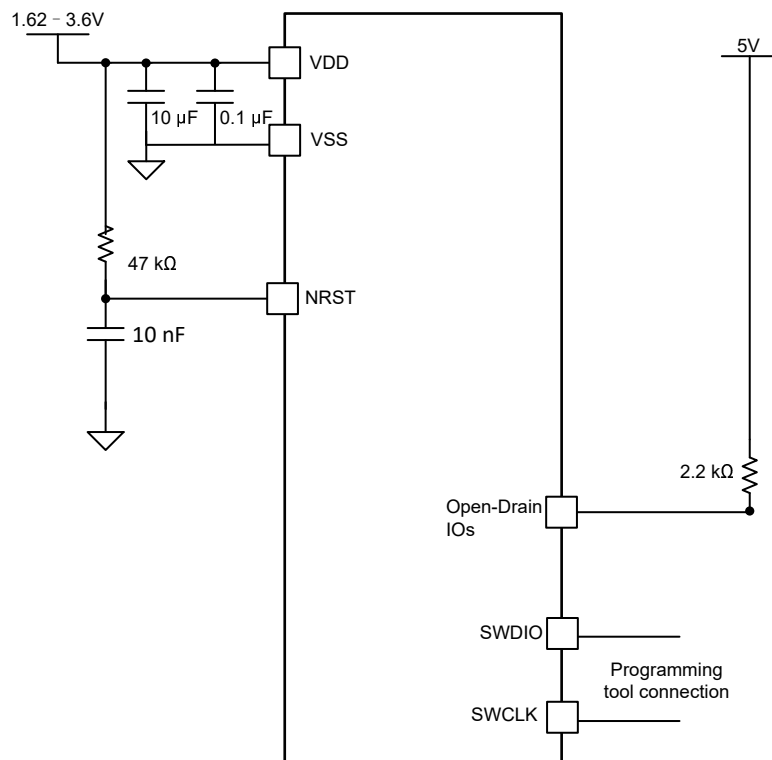


図 9-1. Typical Application Schematic

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

**X** – Experimental device that is not necessarily representative of the final device's electrical specifications

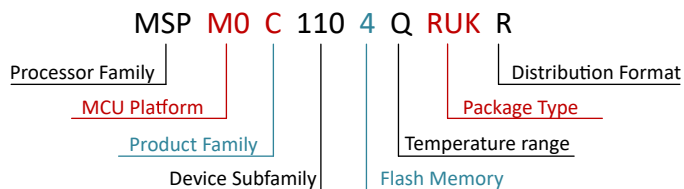
**MSP** – Fully qualified production device

**X** devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [Figure 10-1](#) provides a legend for reading the complete device name.

**Figure 10-1. Device Nomenclature**



**Table 10-1. Device Nomenclature**

<b>Processor Family</b>	MSP = Mixed-signal processor X= Experimental silicon
<b>MCU Platform</b>	M0 = Arm-based 32-bit M0+
<b>Product Family</b>	C = 24MHz frequency
<b>Device Subfamily</b>	110 = ADC
<b>Flash Memory</b>	3 = 8KB 4 = 16KB
<b>Temperature Range</b>	Q = -40°C to 125°C, AEC-Q100 qualified
<b>Package Type</b>	See <a href="#">Table 5-1</a> and <a href="http://www.ti.com/packaging">www.ti.com/packaging</a>
<b>Distribution Format</b>	R = Large reel

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, [ti.com](http://ti.com), or contact your TI sales representative.



## 10.2 Tools and Software

### Design Kits and Evaluation Modules

[MSPM0 LaunchPad \(LP\)](#)  
[Boards: LP-MSPM0C1104](#)

Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming, debugging, and EnergyTrace™ technology.

The LP ecosystem includes dozens of [BoosterPack™](#) stackable plug-in modules to extend functionality.

### Embedded Software

[MSPM0 Software Development Kit \(SDK\)](#)

Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

### Software Development Tools

[TI Cloud Tools](#)

Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.

[TI Resource Explorer](#)

Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.

[SysConfig](#)

Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE or in TI Cloud Tools. ([offline version](#))

[MSP Academy](#)

Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.

[GUI Composer](#)

GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

### IDE and compiler tool chains

[Code Composer Studio™ \(CCS\)](#)

Includes [TI Arm-Clang](#) compiler. Supports all TI Arm Cortex MCUs and boasts competitive code size performance advantages, fast compile time, code coverage support, safety certification support, and completely free to use.

[IAR Embedded Workbench® IDE](#)

[Keil® MDK IDE](#)

[GNU Arm Embedded Tool Chain](#)

## 10.3 サポート・リソース

[テキサス・インスツルメンツ E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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## 10.4 Trademarks

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## 10.5 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

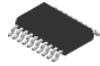
### Changes from Revision \* (October 2023) to Revision A (August 2024)

Page

- このデータシートのステータスを「量産データ」に変更、ドキュメント全体を通して最終的な特性を更新..... 1

## 12 Mechanical, Packaging, and Orderable Information

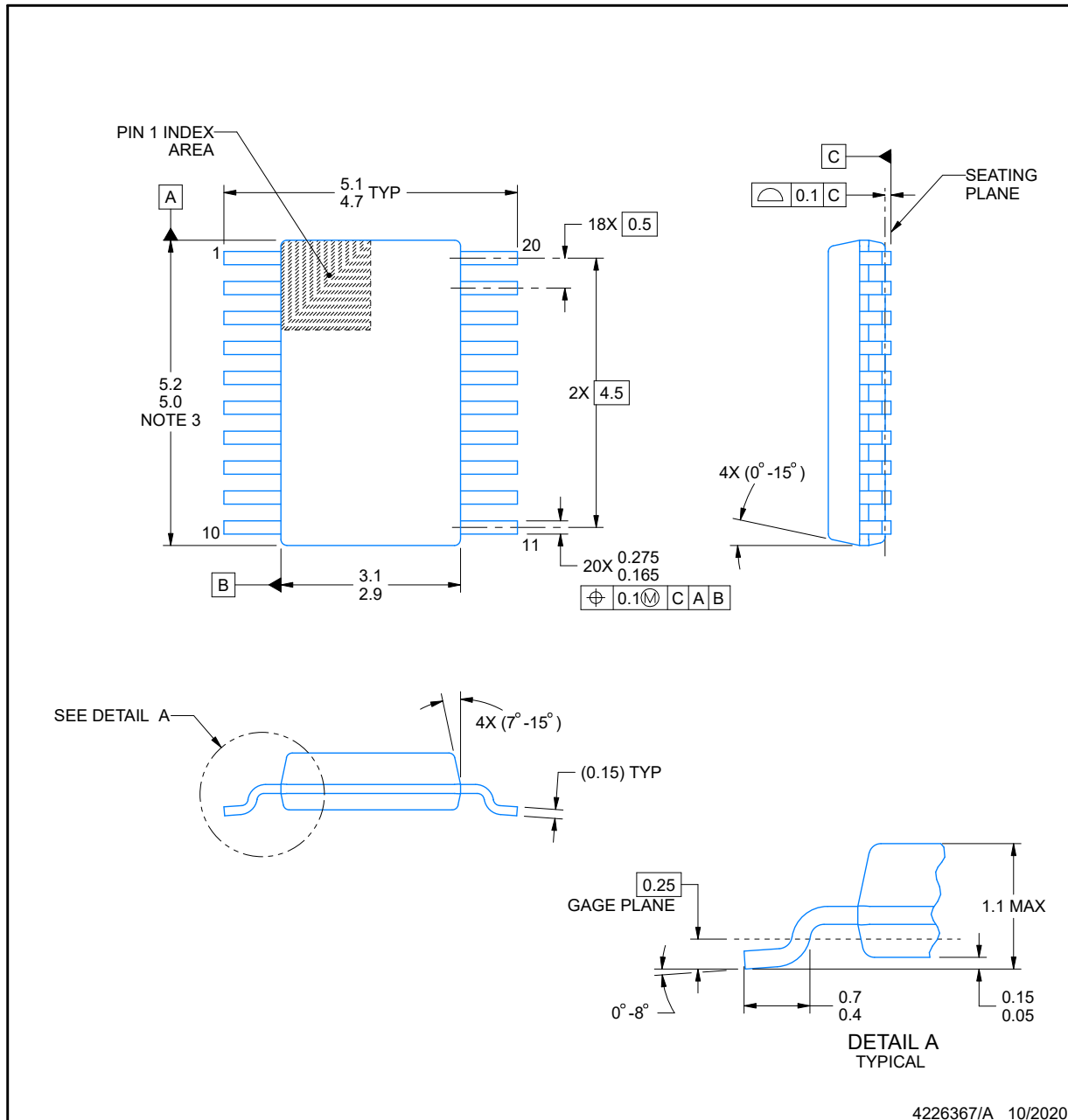
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



# DGS0020A

# PACKAGE OUTLINE VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

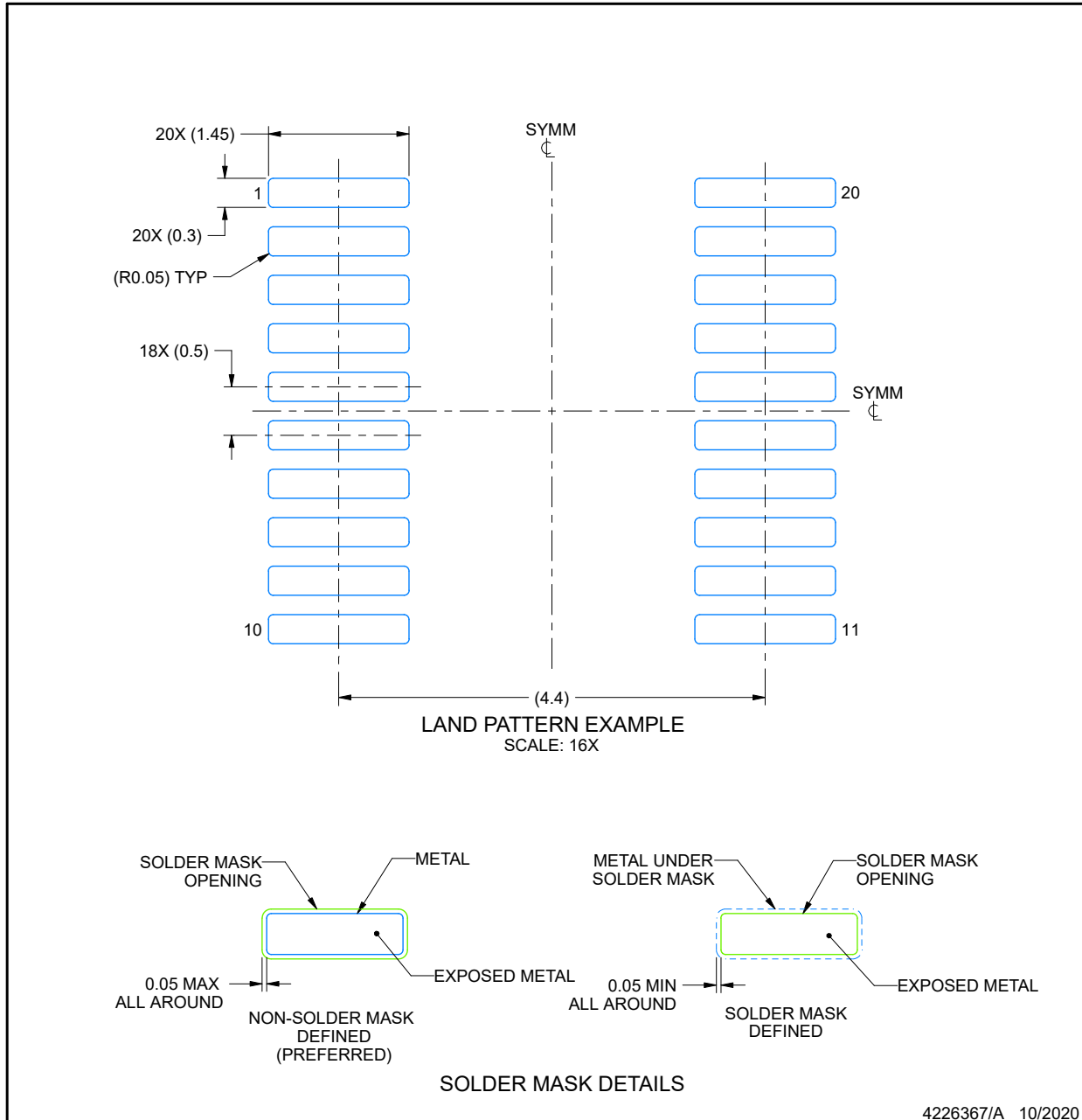
PowerPAD is a trademark of Texas Instruments.

## EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

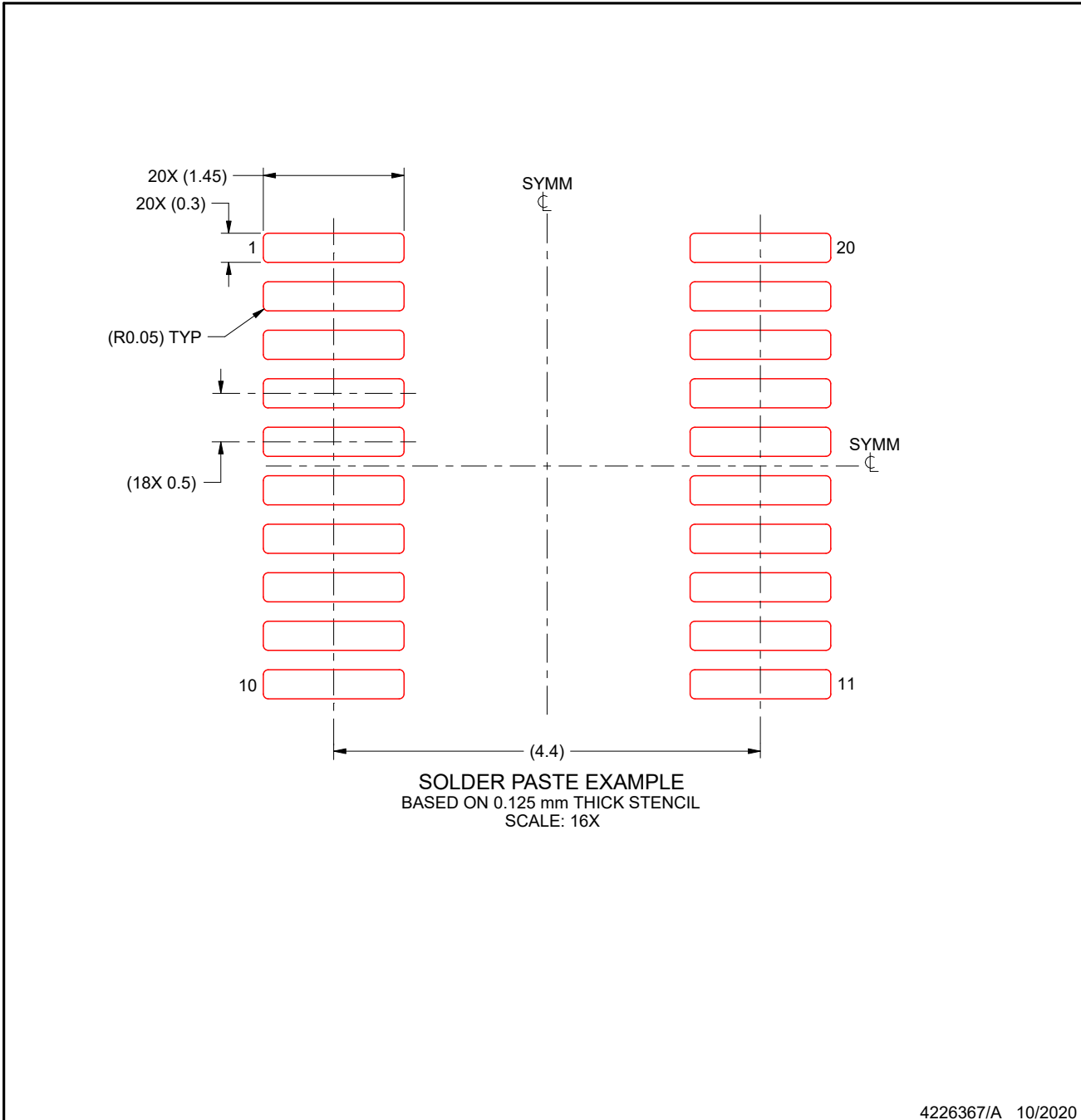
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

### DGS0020A

### VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

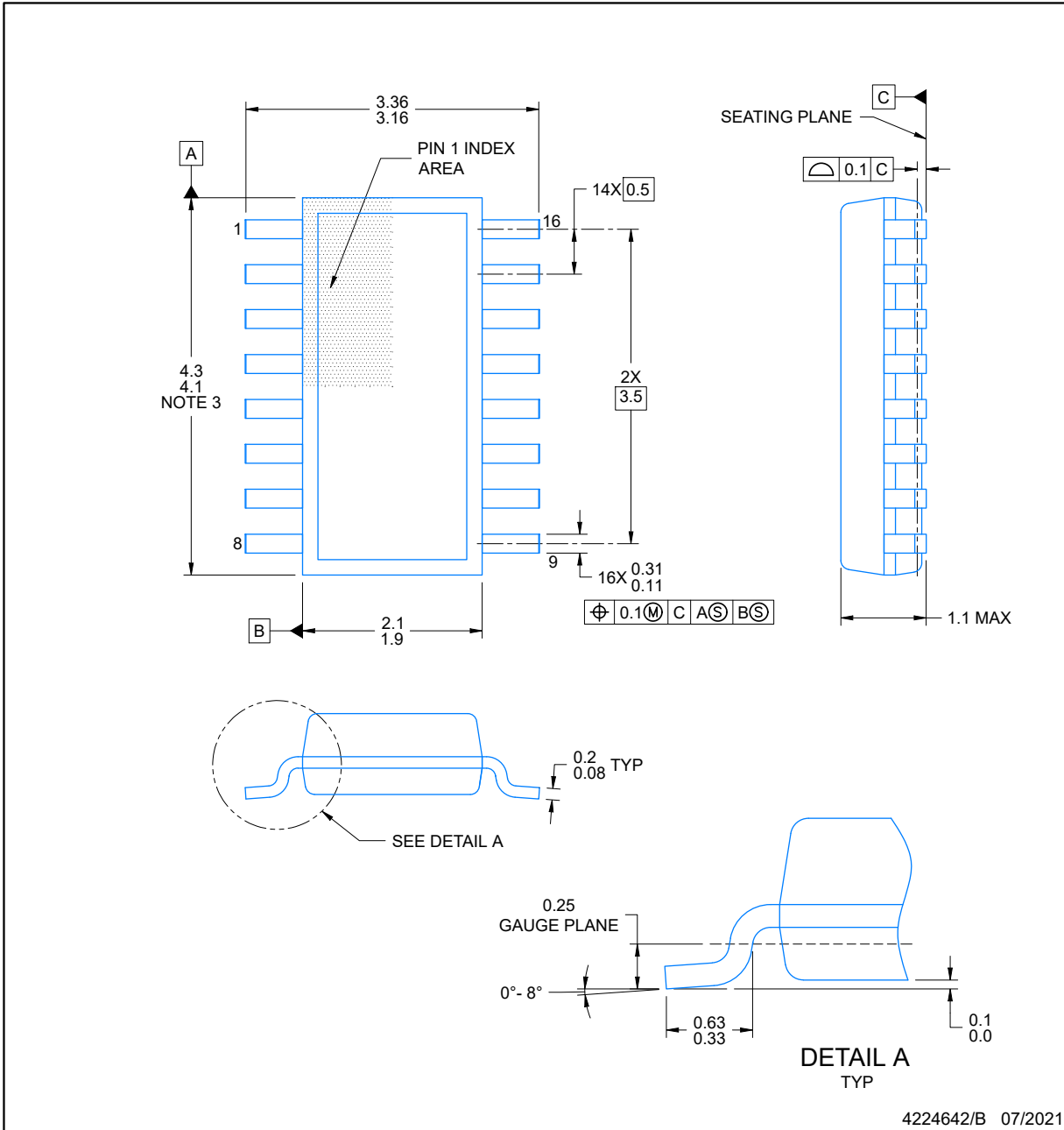
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## PACKAGE OUTLINE

**DYY0016A**

**SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



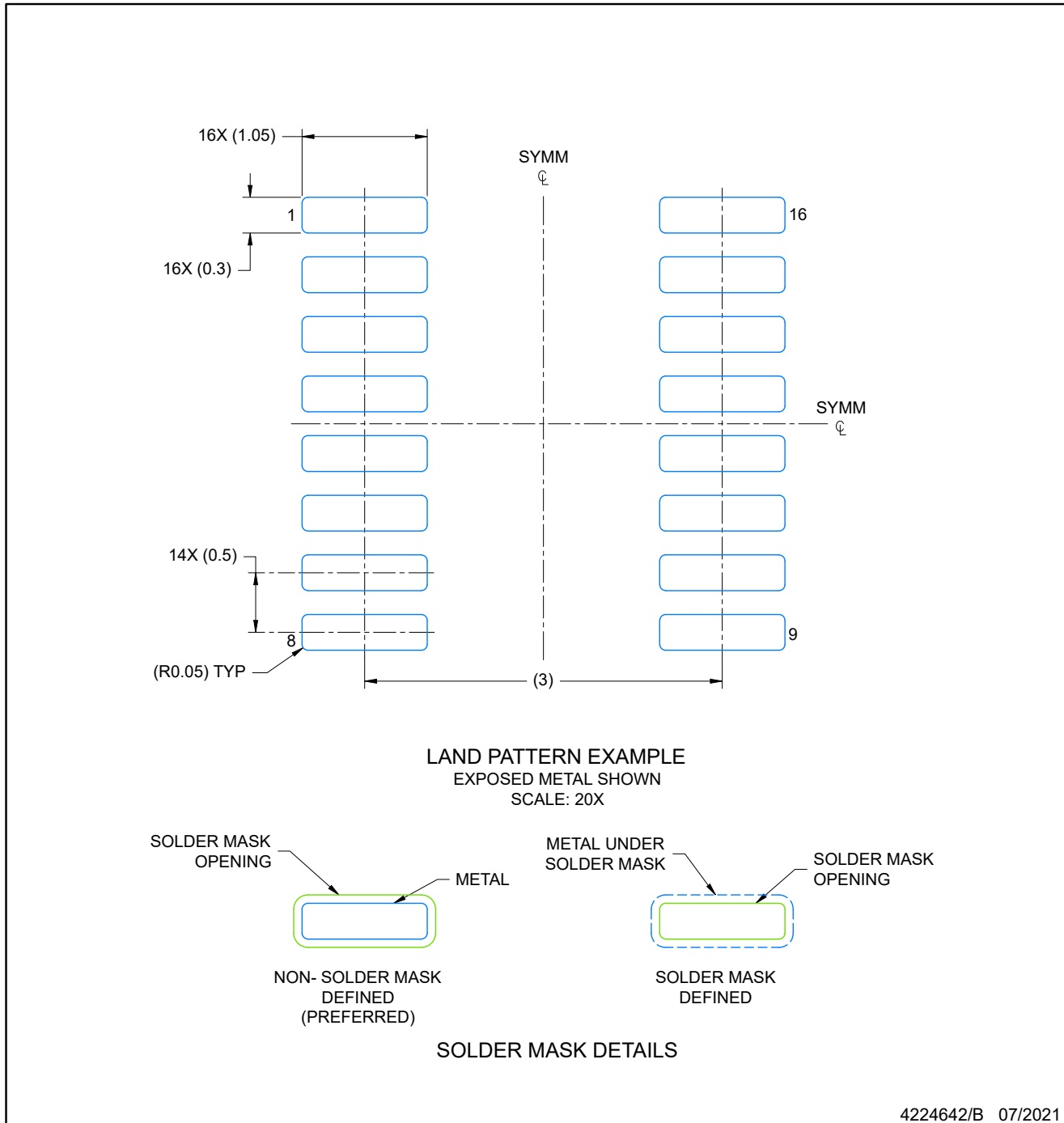
**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA

# DYY0016A

## EXAMPLE BOARD LAYOUT SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

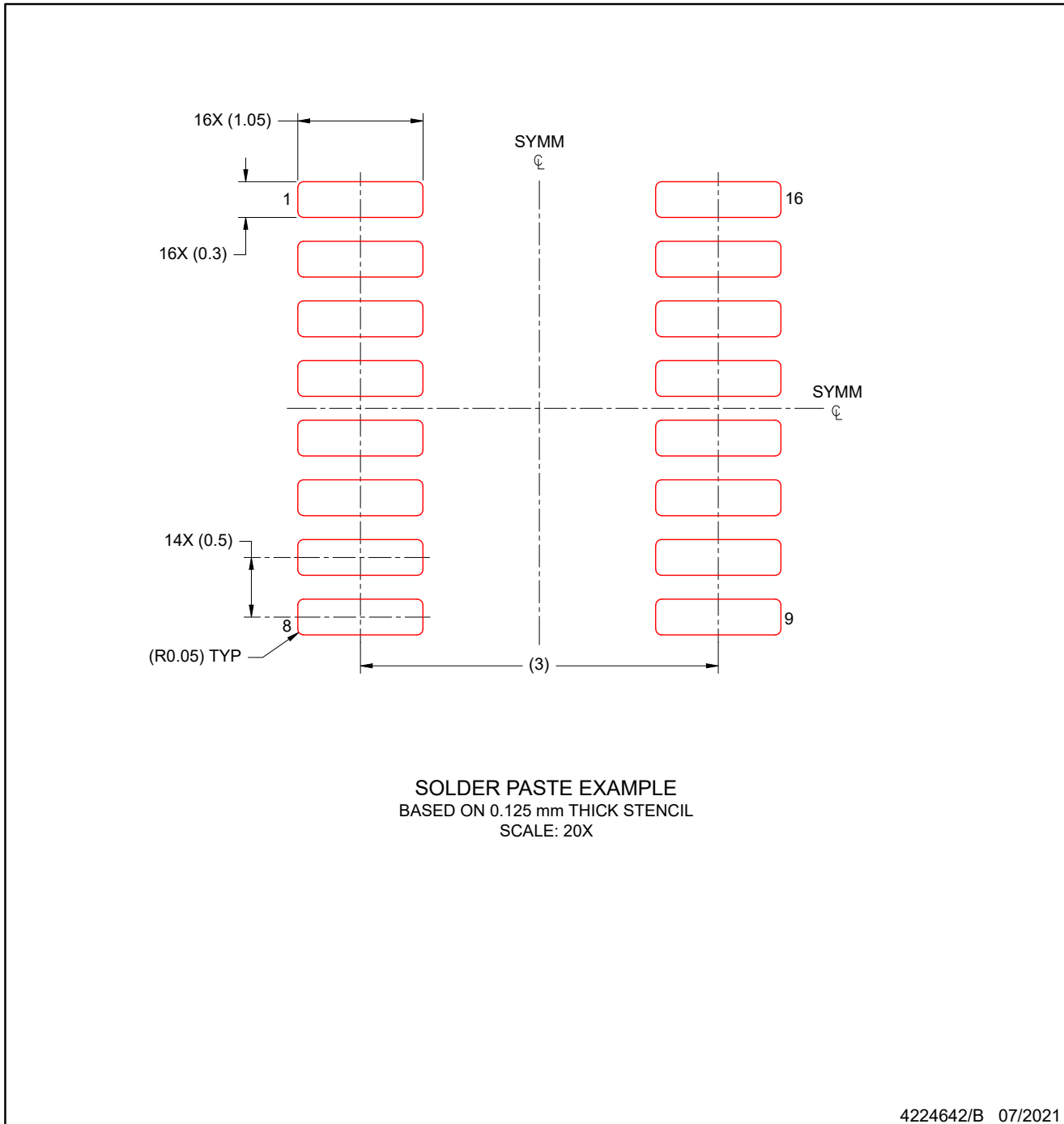


## EXAMPLE STENCIL DESIGN

### SOT-23-THIN - 1.1 mm max height

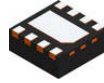
**DYY0016A**

PLASTIC SMALL OUTLINE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

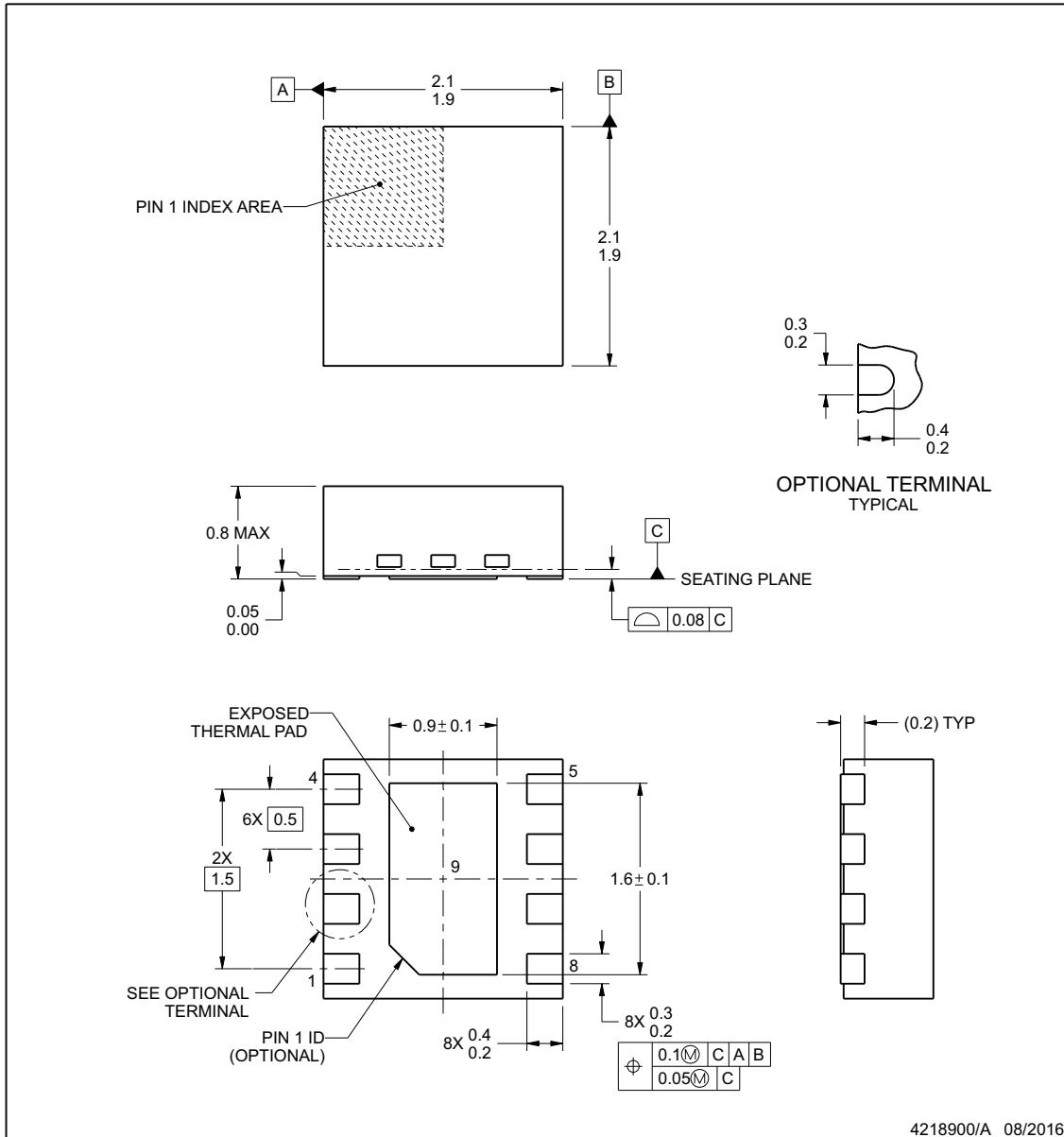


# DSG0008A

# PACKAGE OUTLINE

## WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

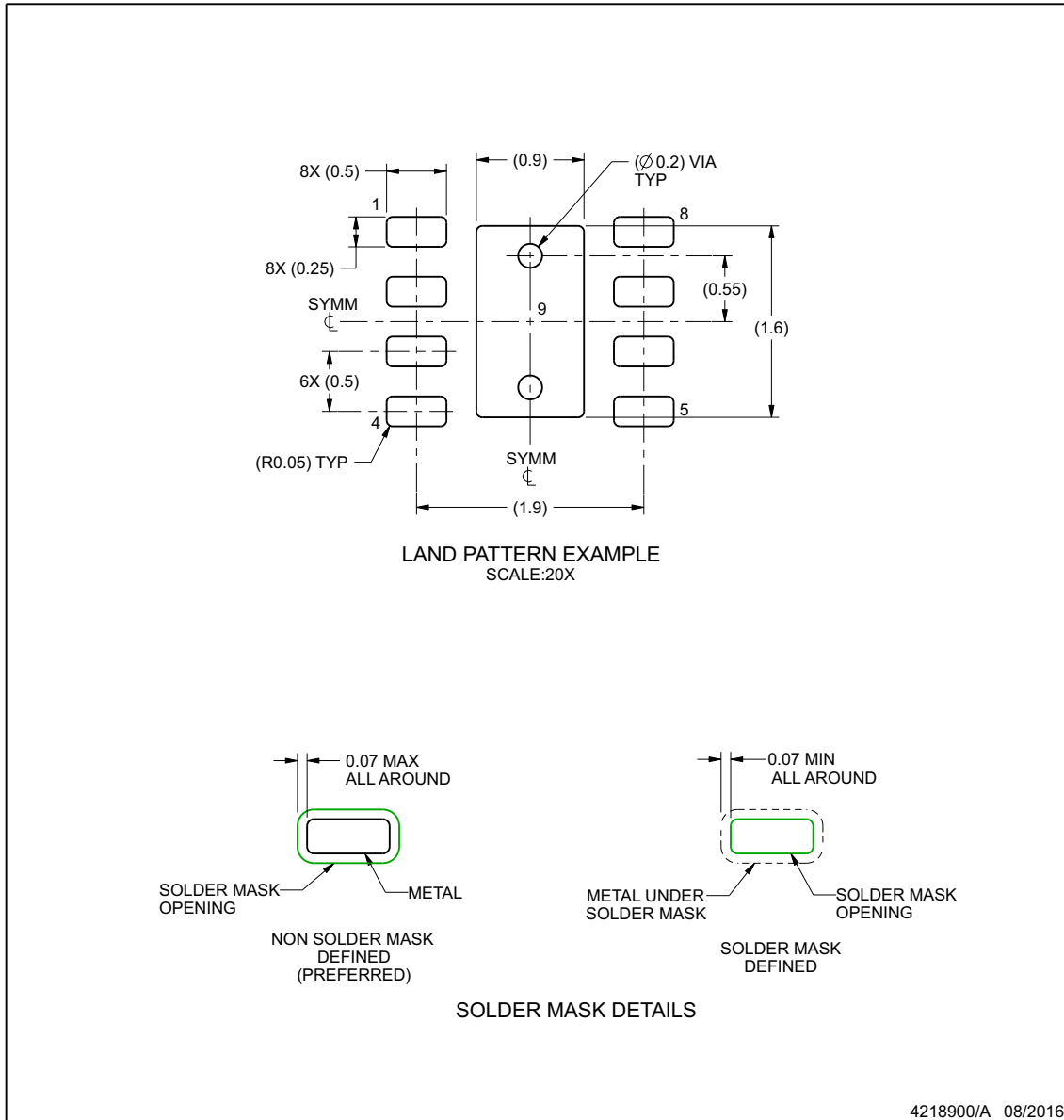
www.ti.com

## EXAMPLE BOARD LAYOUT

**DSG0008A**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

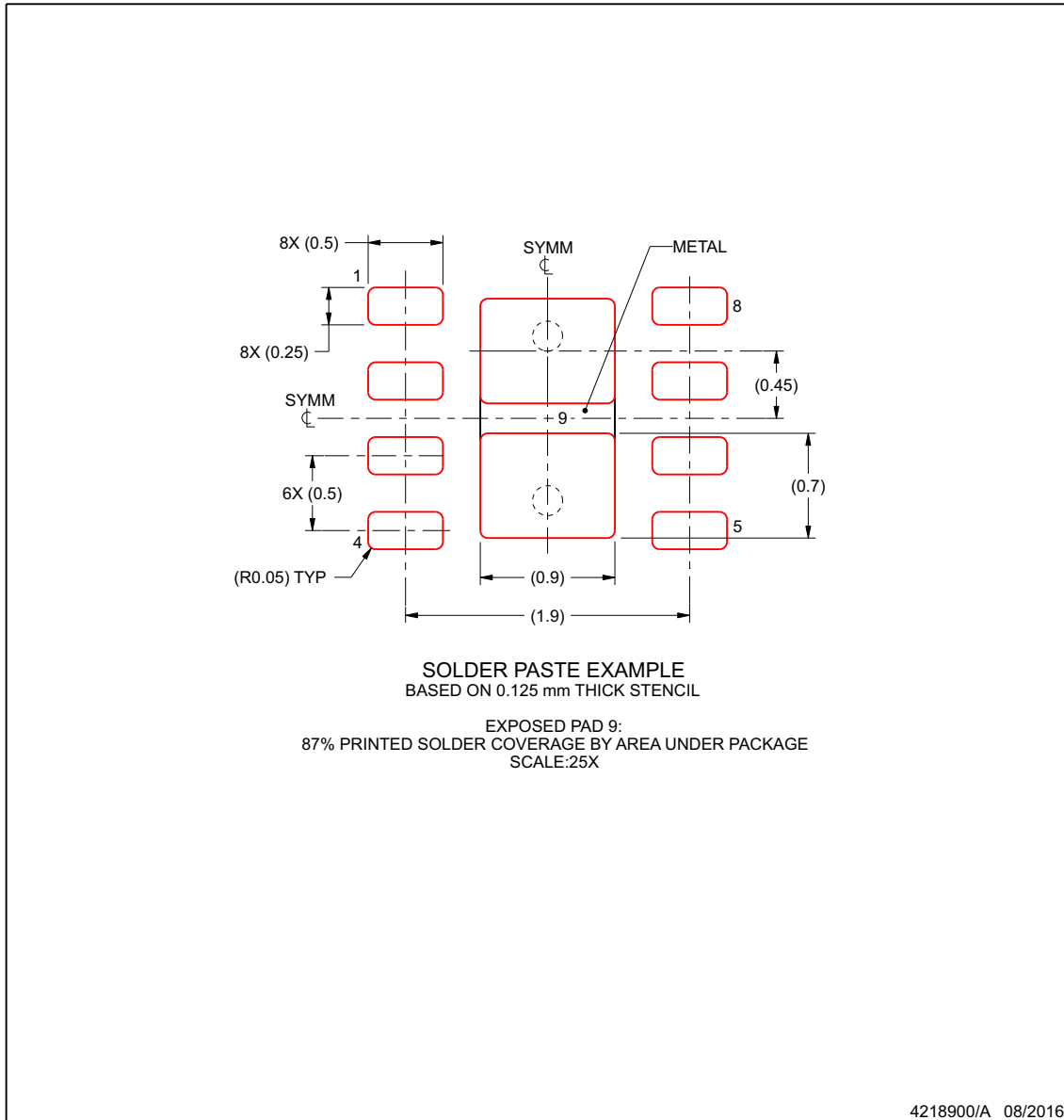
[www.ti.com](http://www.ti.com)

## EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

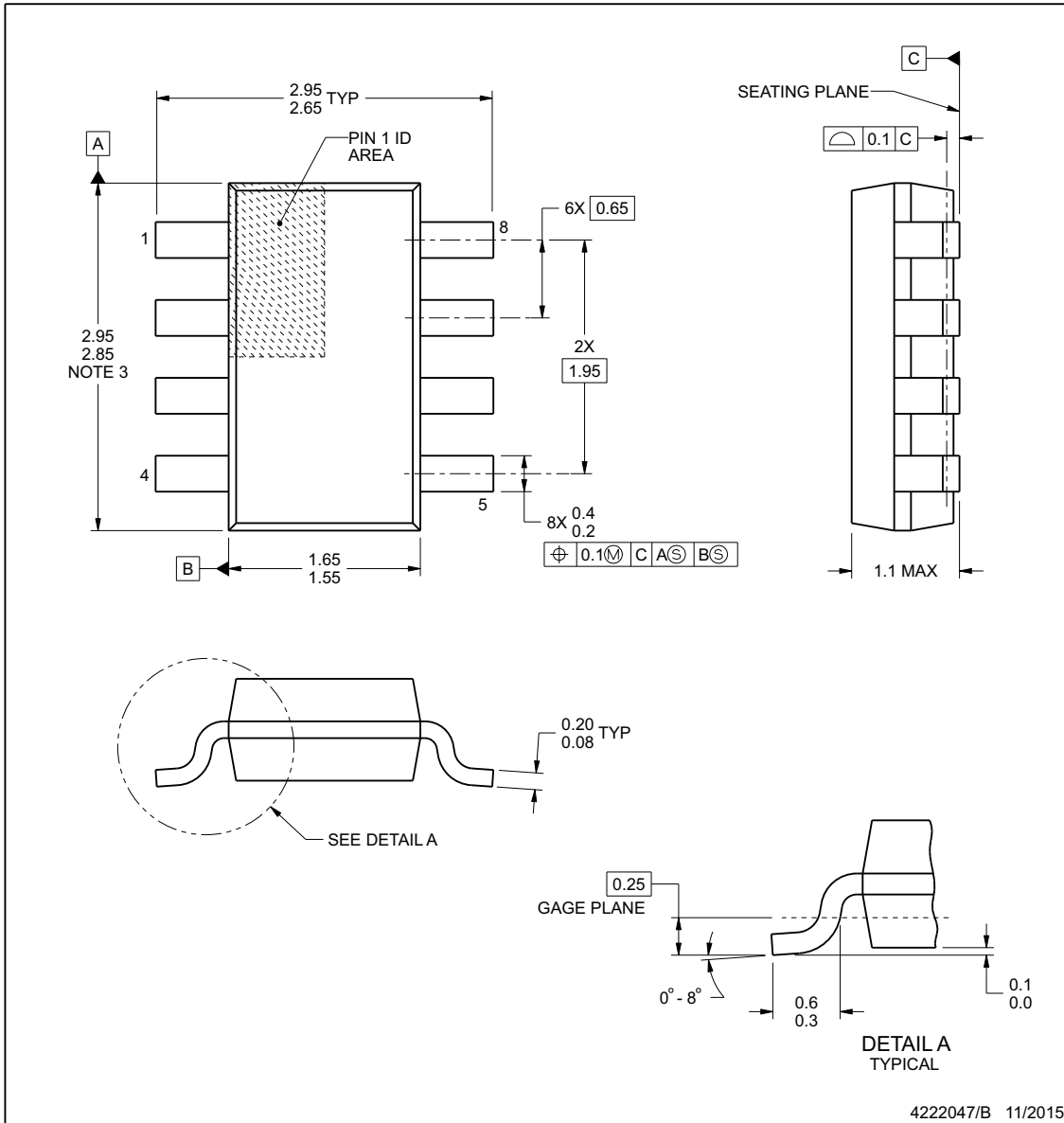
www.ti.com



**DDF0008A**

**PACKAGE OUTLINE**  
**SOT-23 - 1.1 mm max height**

PLASTIC SMALL OUTLINE



NOTES:

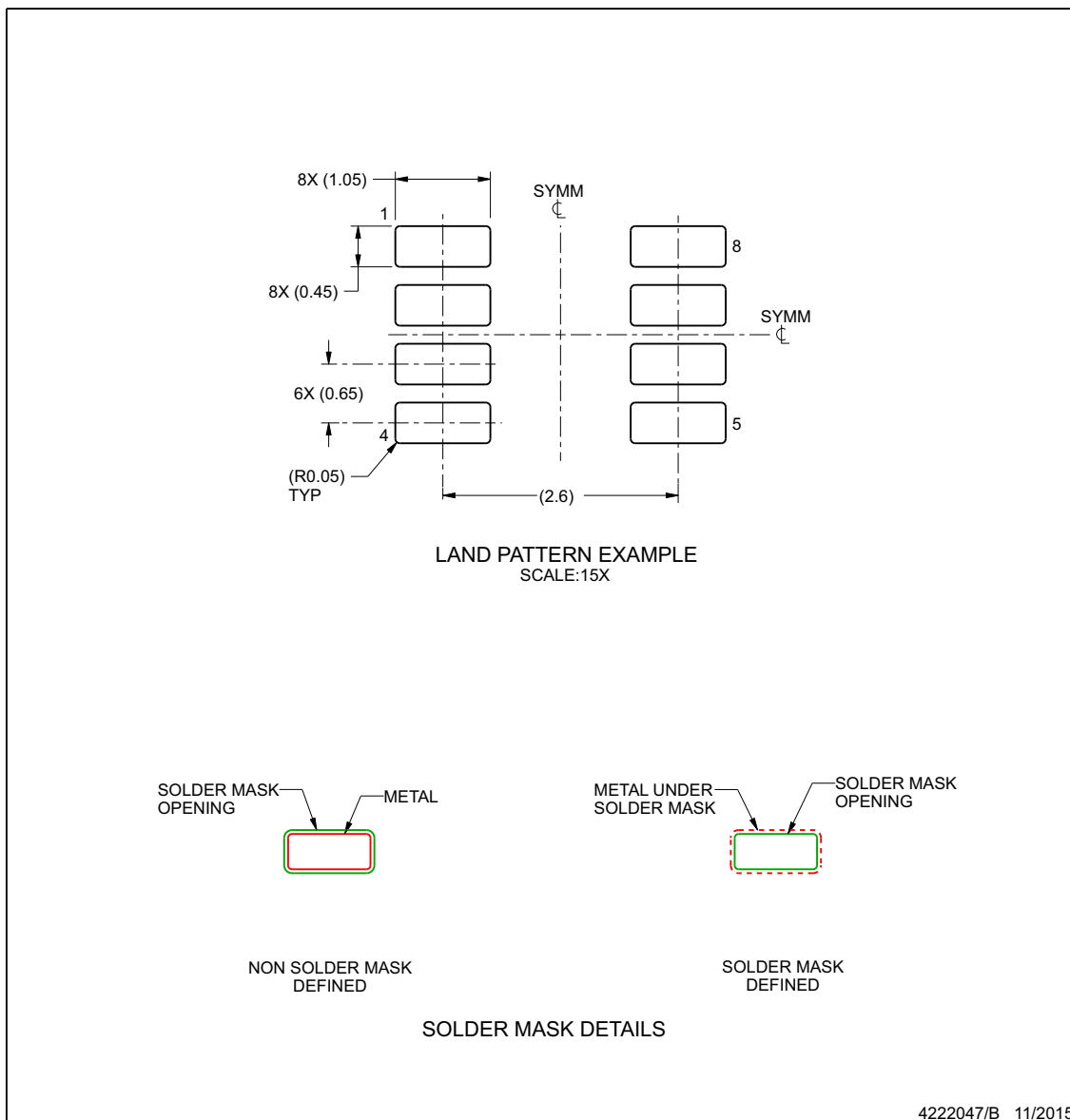
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

## EXAMPLE BOARD LAYOUT

**DDF0008A**

**SOT-23 - 1.1 mm max height**

PLASTIC SMALL OUTLINE



NOTES: (continued)

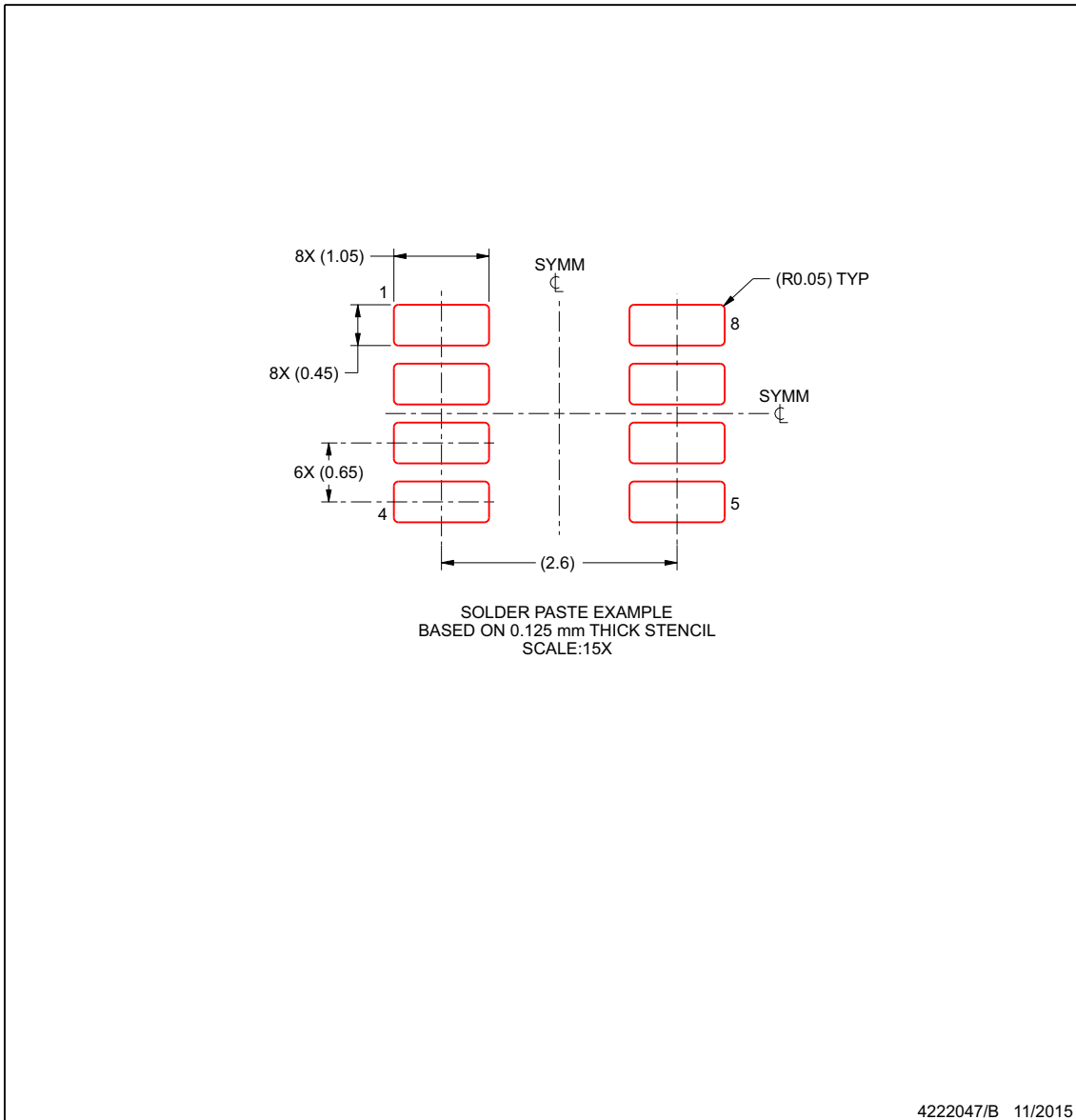
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**DDF0008A**

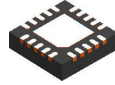
**SOT-23 - 1.1 mm max height**

PLASTIC SMALL OUTLINE



NOTES: (continued)

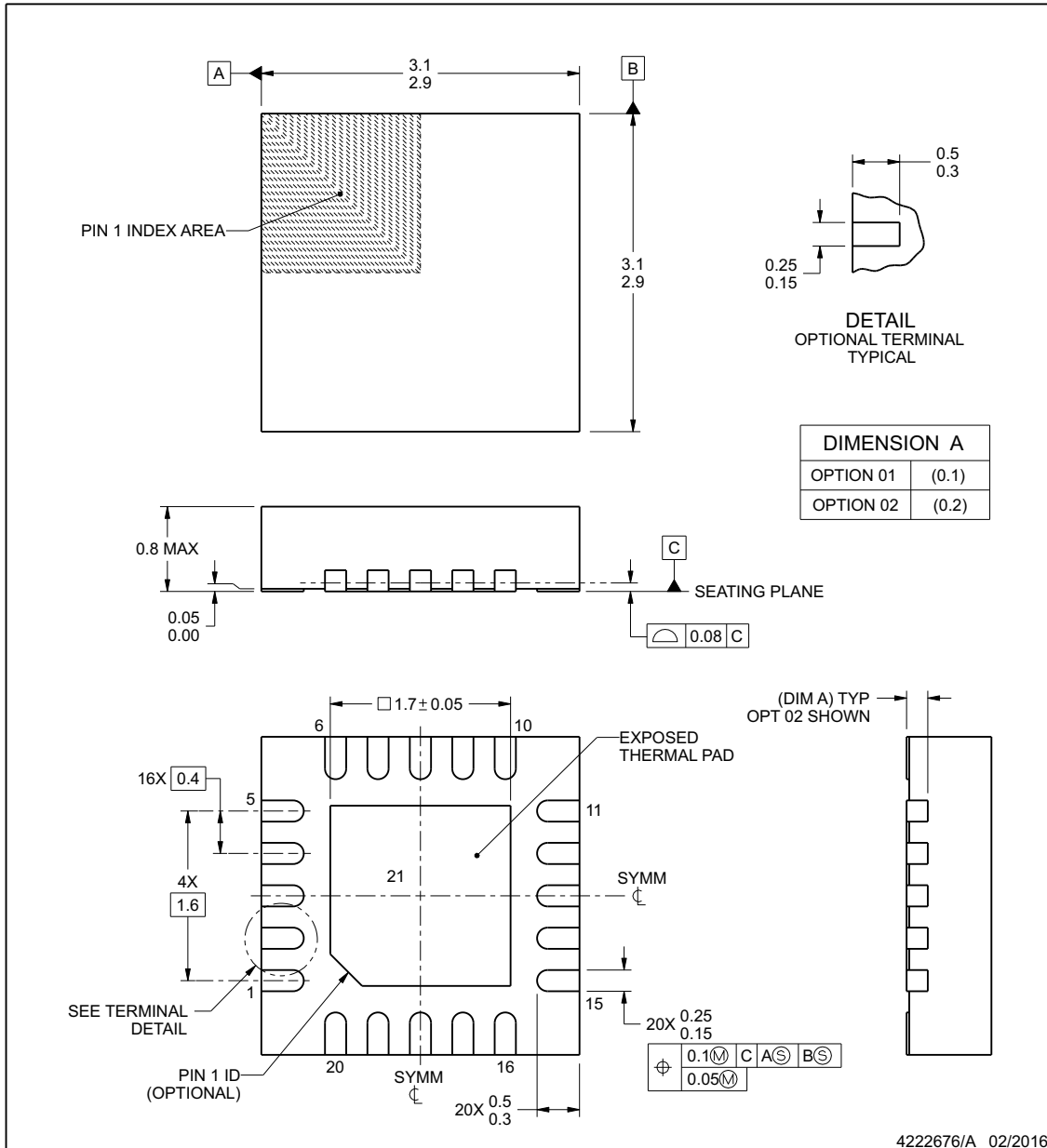
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



**RUK0020B**

**PACKAGE OUTLINE**  
**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

www.ti.com

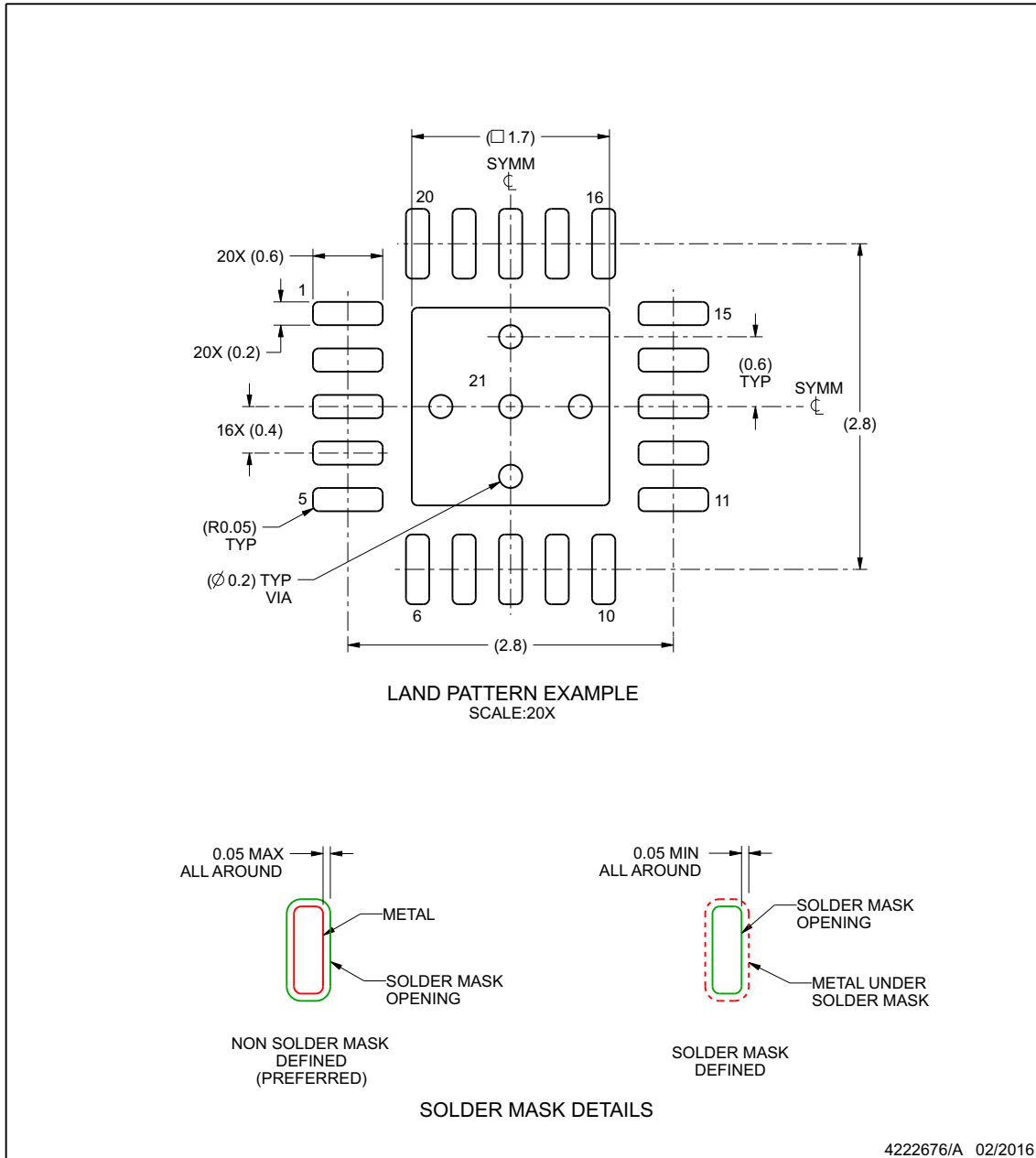


## EXAMPLE BOARD LAYOUT

**RUK0020B**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

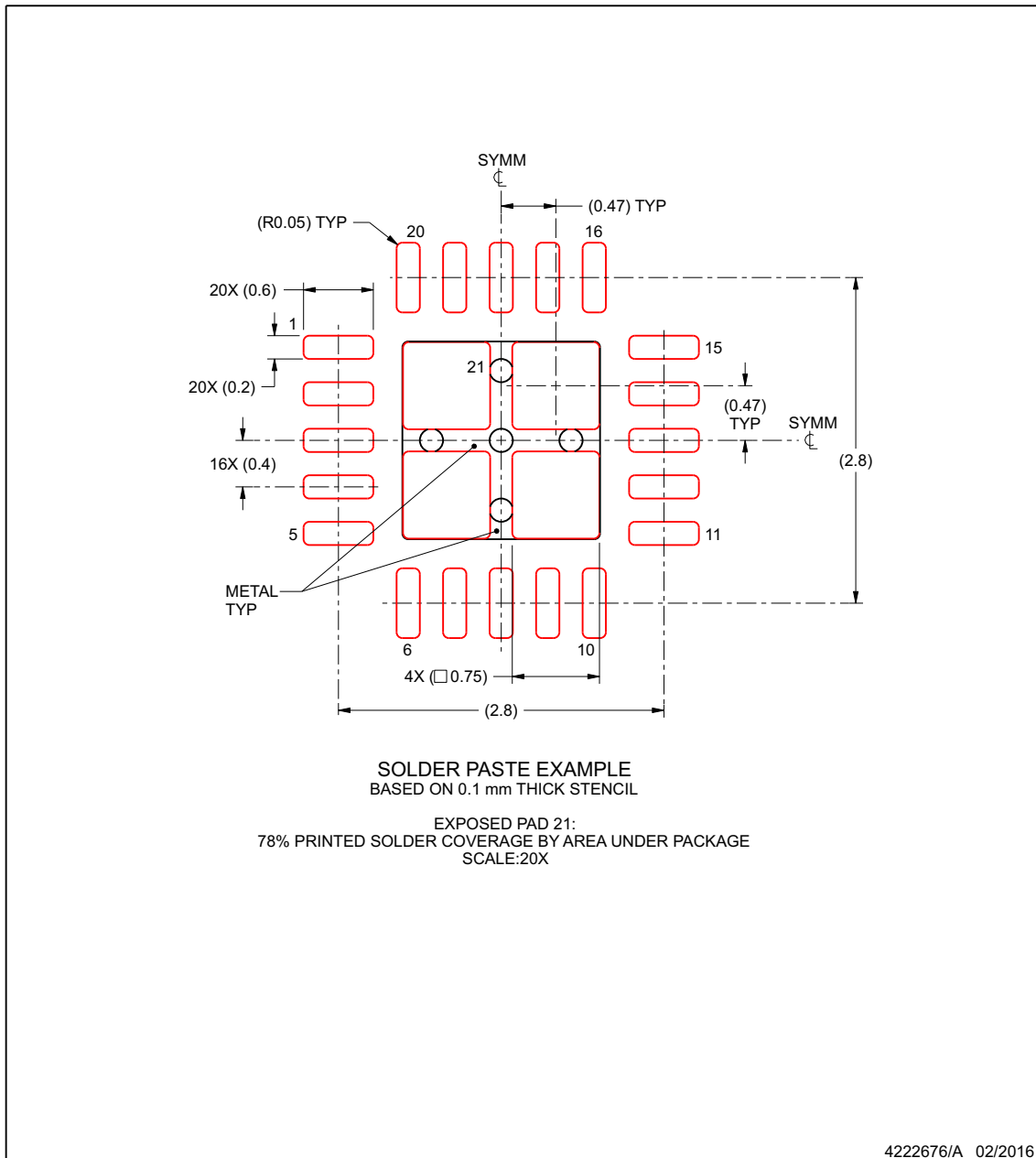
[www.ti.com](http://www.ti.com)

## EXAMPLE STENCIL DESIGN

**RUK0020B**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

[www.ti.com](http://www.ti.com)

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上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

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郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M0C1103QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C04Q	<a href="#">Samples</a>
M0C1103QDGS20RQ1	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1103Q	<a href="#">Samples</a>
M0C1103QDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	C03Q	<a href="#">Samples</a>
M0C1103QDYRQ1	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1103Q	<a href="#">Samples</a>
M0C1103QRUKRQ1	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	C1103Q	<a href="#">Samples</a>
M0C1104QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C04Q	<a href="#">Samples</a>
M0C1104QDGS20RQ1	ACTIVE	VSSOP	DGS	20	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1104Q	<a href="#">Samples</a>
M0C1104QDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	C04Q	<a href="#">Samples</a>
M0C1104QDYRQ1	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1104Q	<a href="#">Samples</a>
M0C1104QRUKRQ1	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	C1104Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF MSPM0C1103-Q1, MSPM0C1104-Q1 :**

- Catalog : [MSPM0C1103](#), [MSPM0C1104](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

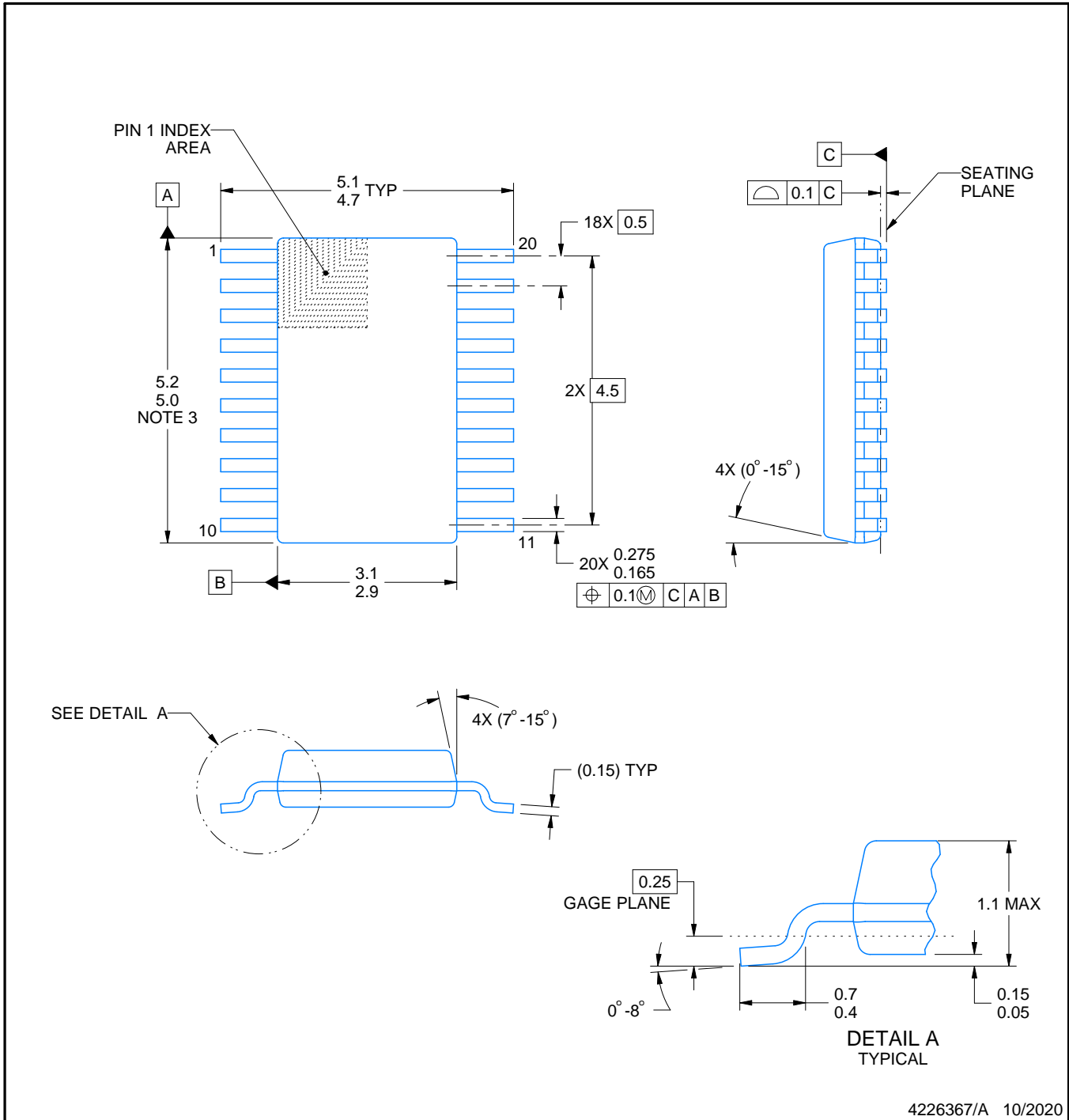
# DGS0020A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

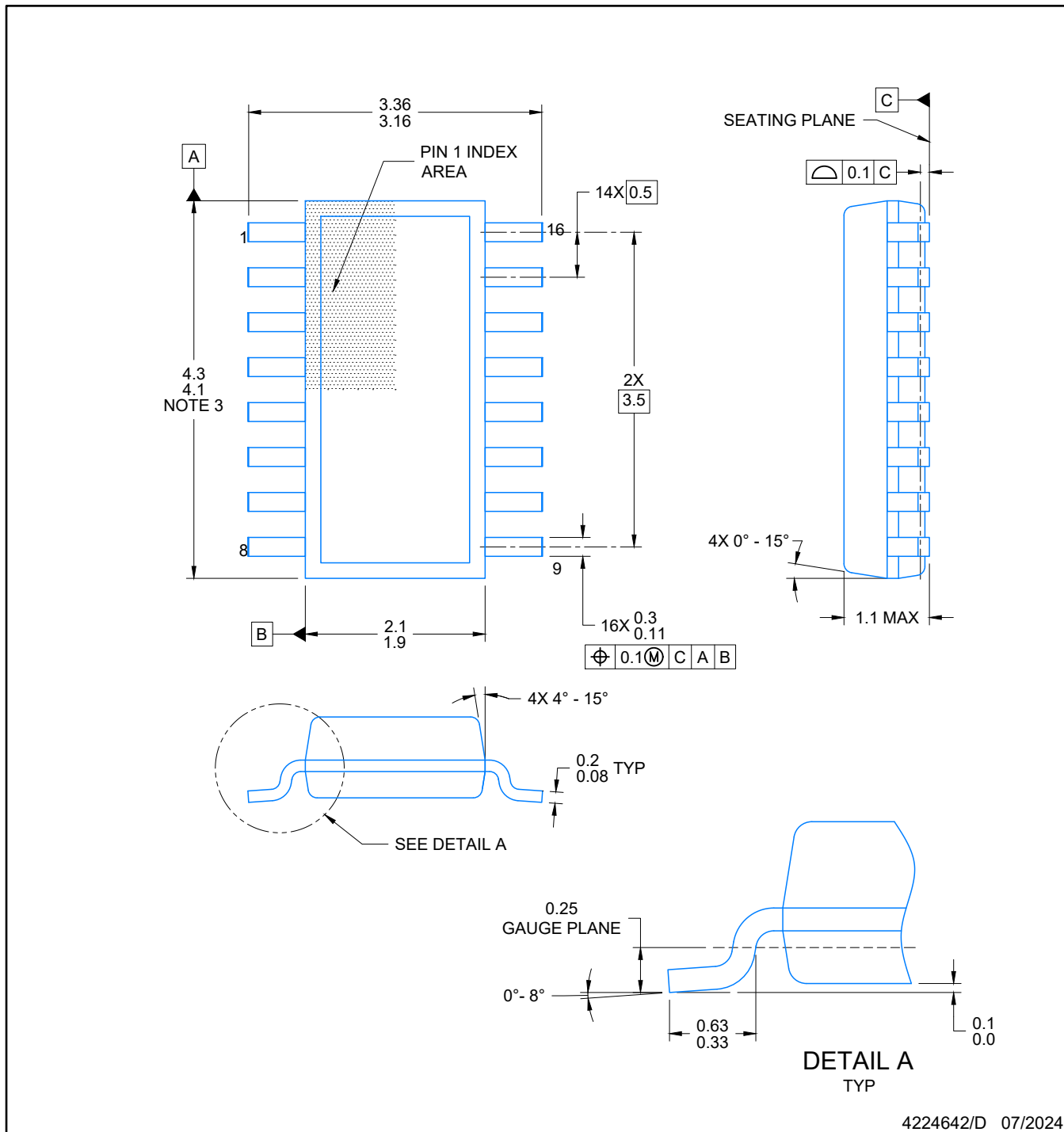
SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

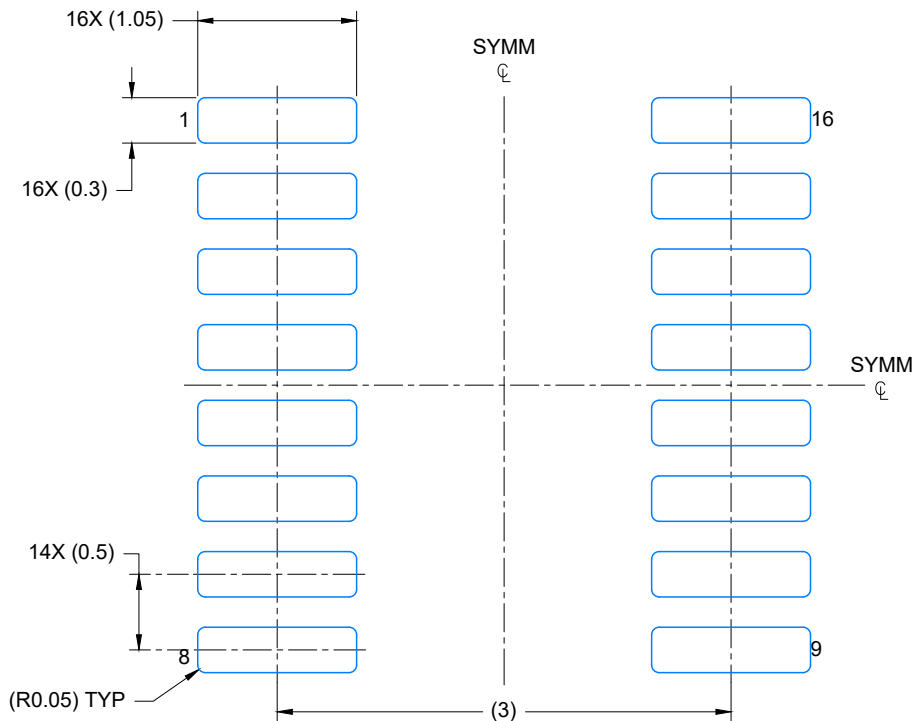




4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



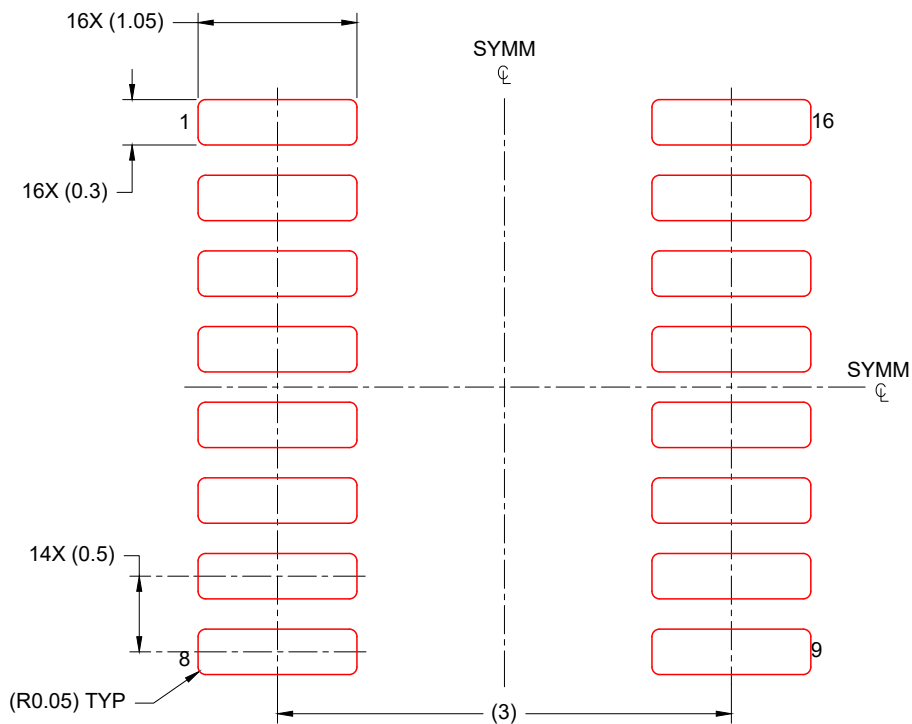
LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

# DDF0008A



# PACKAGE OUTLINE

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

### NOTES:

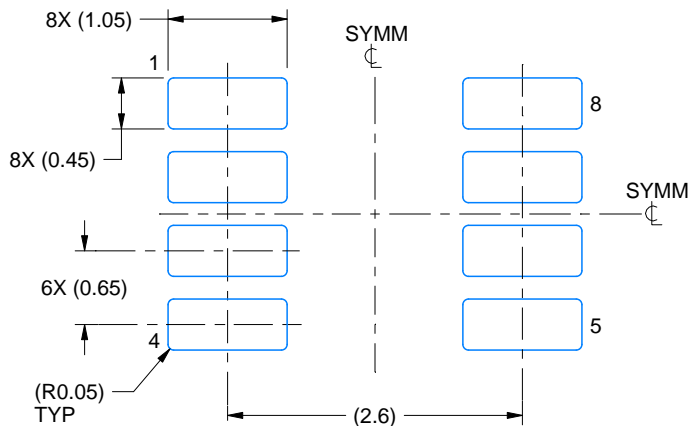
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

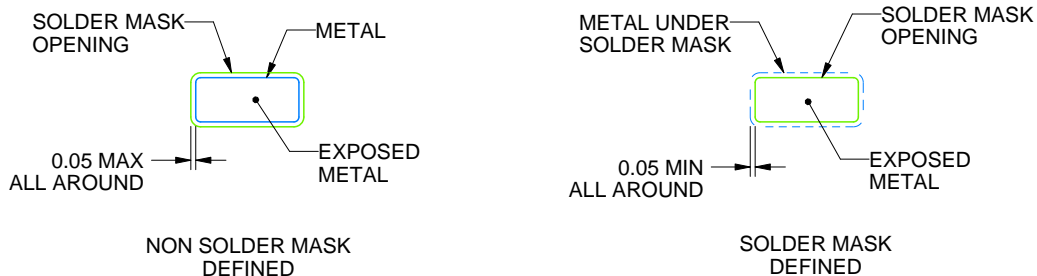
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

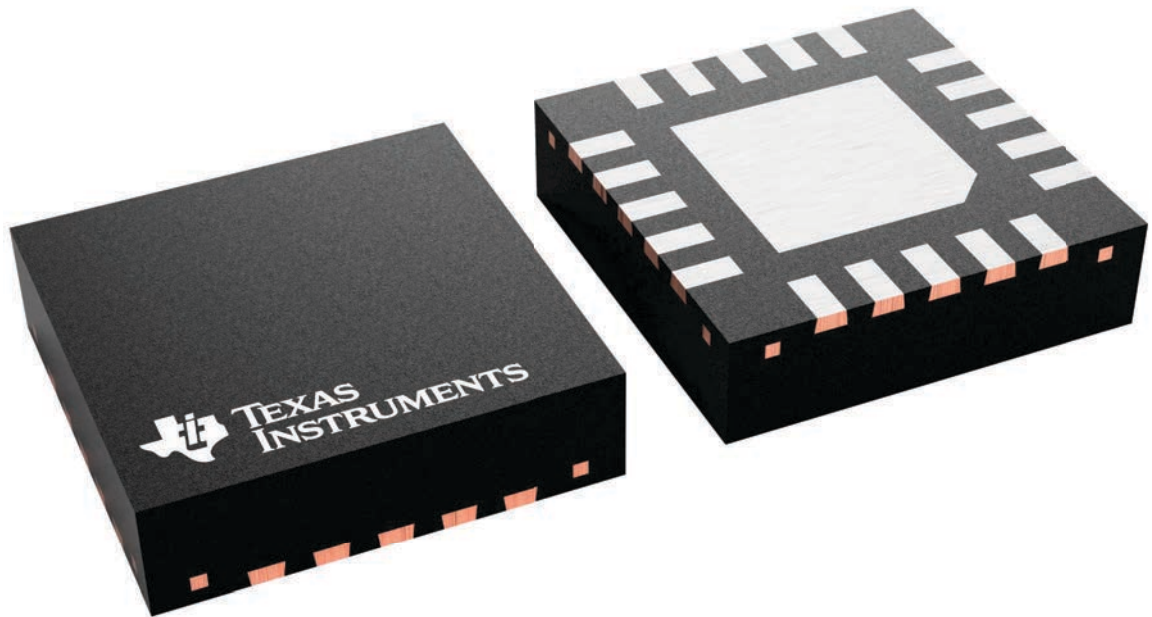
**RUK 20**

**WQFN - 0.8 mm max height**

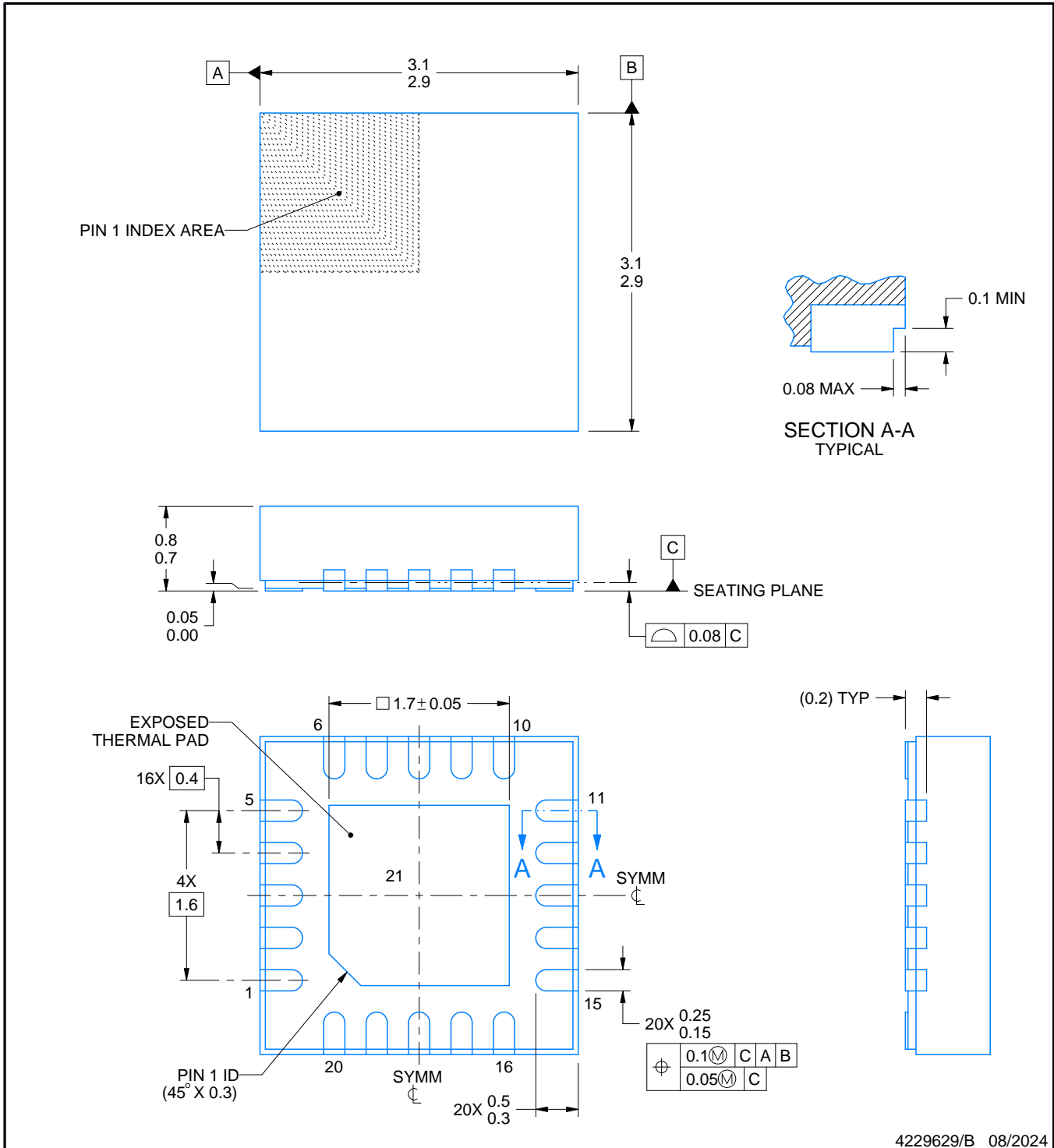
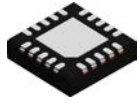
3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229651/A



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

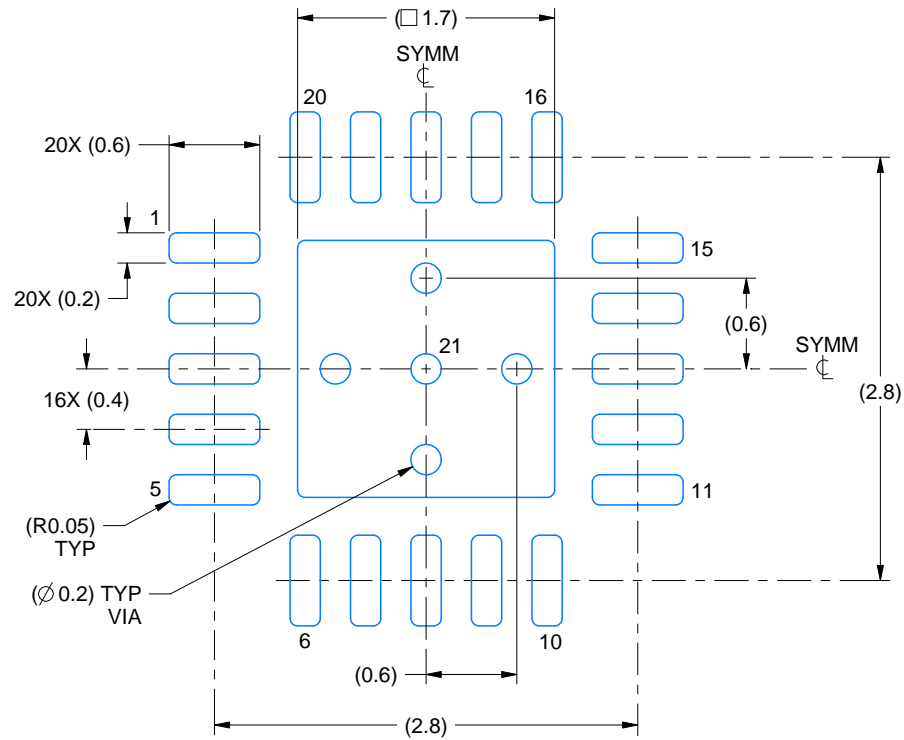


# EXAMPLE BOARD LAYOUT

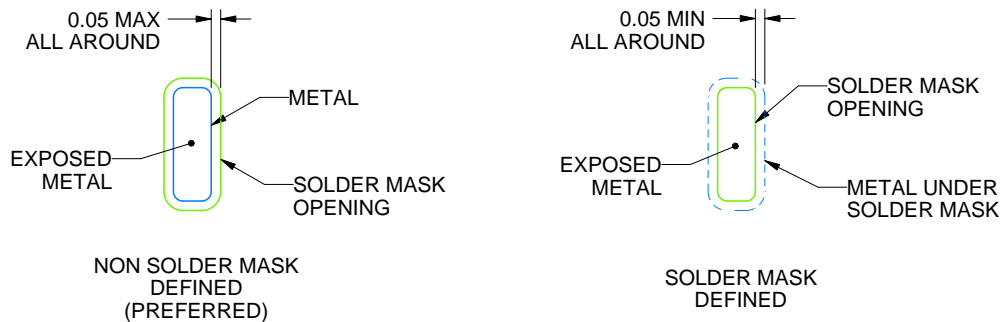
RUK0020C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:20X



**SOLDER MASK DETAILS**

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NOTES: (continued)

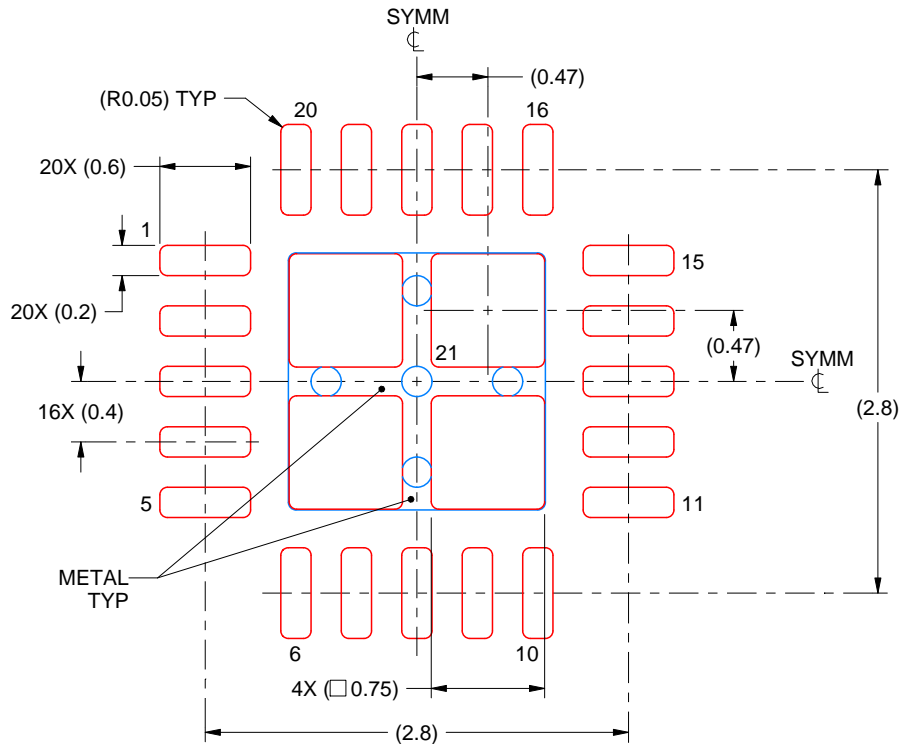
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RUK0020C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

**DSG 8**

**WSON - 0.8 mm max height**

2 x 2, 0.5 mm pitch

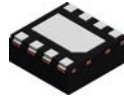
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A

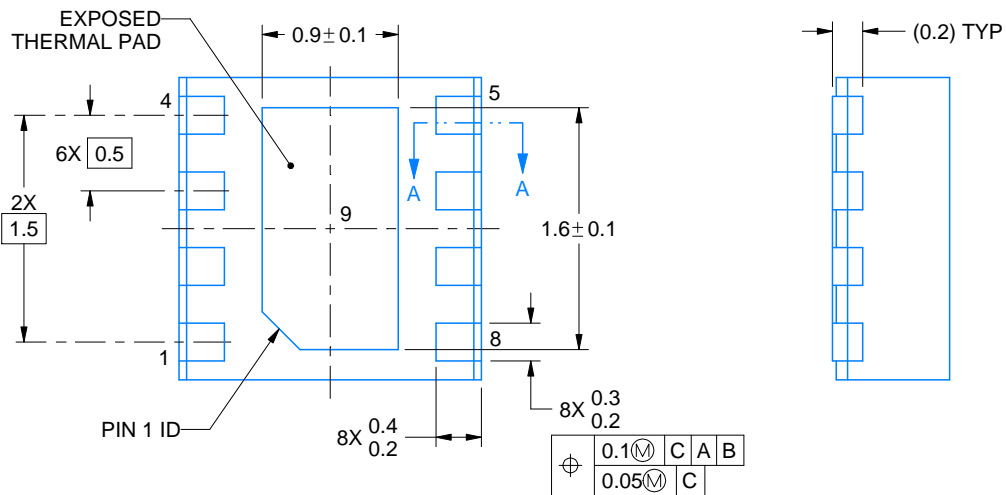
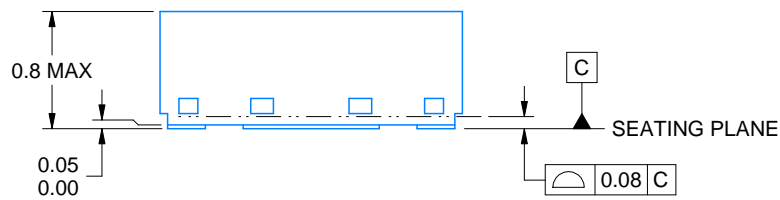
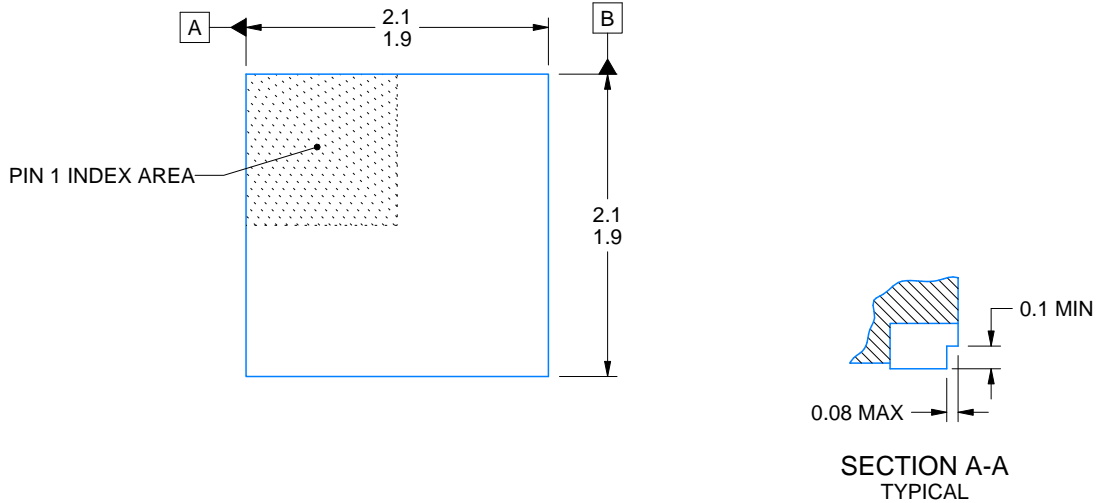
# DSG0008D



# PACKAGE OUTLINE

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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### NOTES:

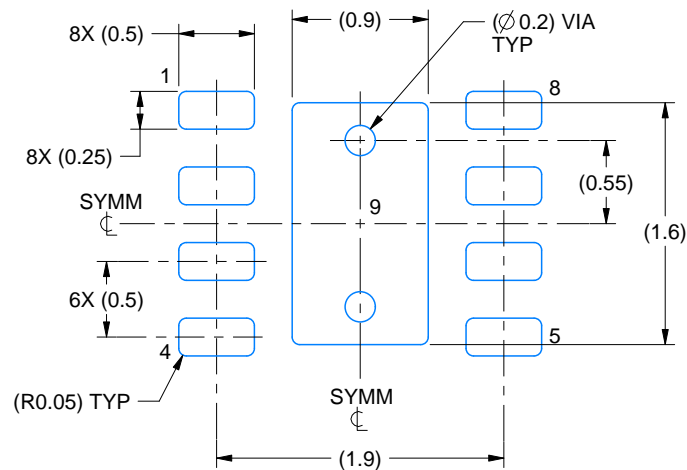
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

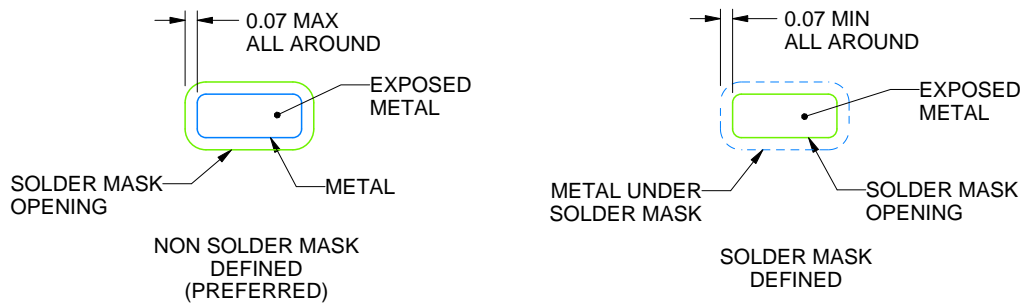
DSG0008D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

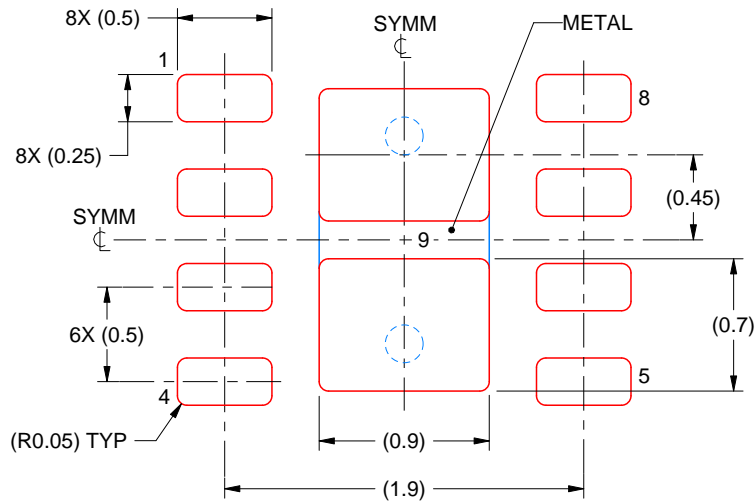
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DSG0008D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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