OPAx325
高精度、10MHz、低ノイズ、低消費電力、RRIO の CMOS オペアンプ

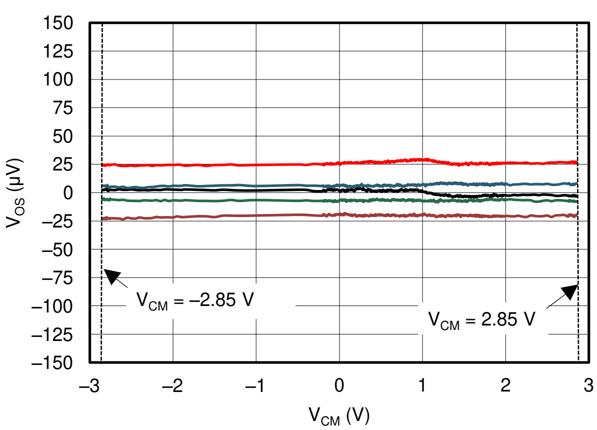
1 特長

- **ゼロ・クロスオーバー歪みで高精度**
  - 低いオフセット電圧：150µV (最大値)
  - 高いCMRR: 114dB
  - レール・ツー・レール I/O
- **広い帯域幅**：10MHz
- **静止電流**：650µA/ch
- **単一電源電圧範囲**：2.2～5.5V
- **低い入力バイアス電流**：0.2pA
- **低ノイズ**：9nV/√Hz (10kHz 時)
- **スルーレート**：5V/µs
- **ユニティ・ゲイン安定**

2 アプリケーション

- 高インピーダンス・センサの信号コンディショニング
- トランスインピーダンス・アンプ
- 試験および計測機器
- プログラマブル・ロジック・コントローラ (PLC)
- モータ制御ループ
- 通信
- ADC と DAC の入力/出力バッファ
- アクティブ・フィルタ

オフセット電圧 対 入力同相電圧



3 概要

OPA325、OPA2325、OPA4325 (OPAx325) は、超低ノイズで広い帯域幅を提供し、わずか 650µA の低い静止電流で動作するように最適化された高精度、低電圧の CMOS (相補型金属酸化膜半導体) オペアンプです。

OPAx325 はゼロ・クロスオーバー歪みのリニア入力段を特長とし、入力範囲全体で 114dB (標準値) という優れた同相除去比 (CMRR) を実現しています。入力同相範囲は、負および正の電源レールよりも100mV拡張されています。出力電圧のスイングは通常、レールから10mVの範囲内です。

ゼロ・クロスオーバー歪み、広い帯域幅 (10MHz)、高いスルーレート (5V/µs)、低ノイズ (9nV/√Hz) を特長とする OPAx325 は、逐次比較型 (SAR) A/D コンバータ (ADC) の入力ドライバ・アンプとして非常に優れています。また OPA325 は、2.2V～5.5V の広い電源電圧範囲を持ち、電源電圧範囲全体にわたって電源除去比 (PSRR) が優れているため、レギュレーションなしで直接バッテリ動作する高精度、低消費電力アプリケーションに適しています。

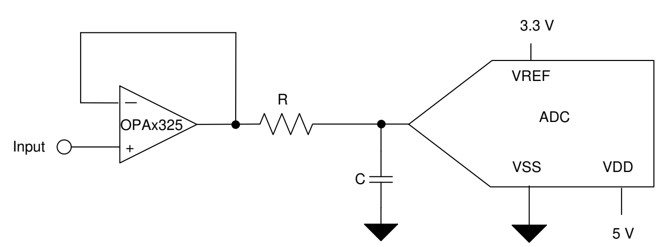
OPA325 (シングル・チャネル・バージョン) は SOT23-5 パッケージで供給されます。OPA2325 (デュアル・チャネル・バージョン)はSO-8およびMSOP-8パッケージで供給されます。OPA4325 (クワッド・チャネル・バージョン)は TSSOP-14パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA325	SOT-23 (5)	2.90mm×1.60mm
OPA2325	SOIC (8)	4.90mm×3.91mm
	VSSOP (8)	3.00mm×3.00mm
OPA4325	TSSOP (14)	5.00mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

OPAx325 を ADC ドライバ・アンプとして使用する例



English Data Sheet: SBOS637

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (May 2019) から Revision D に変更	**Page**
• OPA325 と関連情報をデータシートに 追加	1

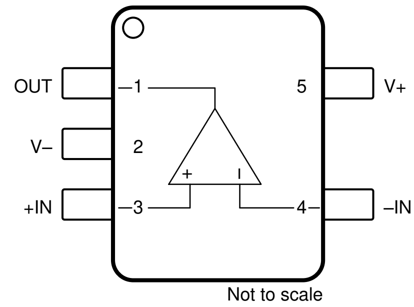
Revision B (February 2019) から Revision C に変更	**Page**
• OPA4325 のステータスをプレビューから量産データ (アクティブ) に 変更	1

Revision A (July 2017) から Revision B に変更	**Page**
• OPA4325 事前情報デバイスをデータシートに 追加	1
• Added operating temperature to *Absolute Maximum Ratings* table	5
• Deleted specified temperature from *Absolute Maximum Ratings* table; specified temperature already listed in *Recommended Operating Conditions* table	5

2016年10月発行のものから更新	**Page**
• デュアル・チャネル・デバイス用の新しい VSSOP パッケージ・オプションを 追加	1
• TI リファレンス・デザインのナビゲータ・アイコンを上端に 追加	1

5 Pin Configuration and Functions

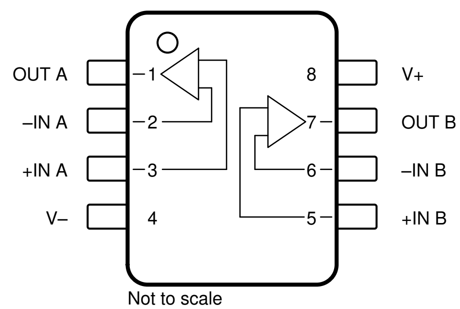
OPA325: DBV Package
5-Pin SOT-23
Top View



Pin Functions: OPA325

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
V–	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply

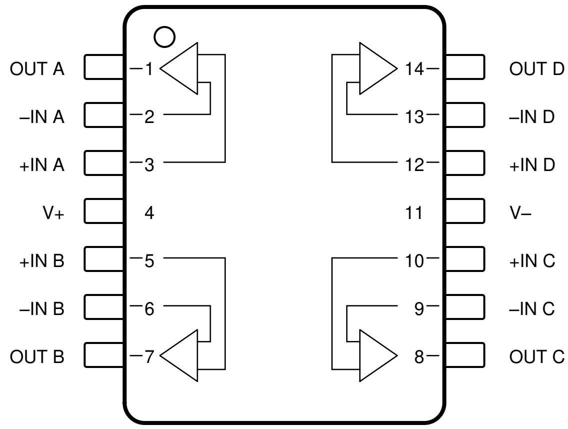
OPA2325: D and DGK Packages
8-Pin SOIC, 8-Pin VSSOP
Top View



Pin Functions: OPA2325

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
V–	4	—	Negative supply
V+	8	—	Positive supply

OPA4325: PW Package
14-Pin TSSOP
Top View



Not to scale

Pin Functions: OPA4325

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input channel A
+IN A	3	I	Noninverting input channel A
–IN B	6	I	Inverting input channel B
+IN B	5	I	Noninverting input channel B
–IN C	9	I	Inverting input channel C
+IN C	10	I	Noninverting input channel C
–IN D	13	I	Inverting input channel D
+IN D	12	I	Noninverting input channel D
OUT A	1	O	Output channel A
OUT B	7	O	Output channel B
OUT C	8	O	Output channel C
OUT D	14	O	Output channel D
V–	11	—	Negative supply
V+	4	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)		6	V
Signal input pins	Voltage(2)	(V–) – 0.5	(V+) + 0.5	V
	Current(2)	–10	10	mA
Output short-circuit(3)		Continuous		mA
Temperature	Operating, T_A	–40	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single supply	2.2		5.5	V
		Dual supply	±1.1		±2.75	
T_A	Specified temperature		–40		125	°C

6.4 Thermal Information: OPA325

THERMAL METRIC[(1)]		OPA325 DBV (SOT) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	200	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	113	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	38.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	104.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2325

THERMAL METRIC[(1)]		OPA2325		UNIT
		D (SOIC) 8 PINS	DGK (VSSOP) 8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119	143	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60	47	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61	64	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	15.0	5.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	60.4	62.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4325

THERMAL METRIC[(1)]		OPA4325 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics: V_S = 2.2 V to 5.5 V or ±1.1 V to ±2.75 V

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			40	150	µV
dV_{OS}/dT	Input offset voltage drift	V_S = 5.5 V, T_A = –40°C to +125°C		2	7.5	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.2 V to +5.5 V		6	20	µV/V
		V_S = 2.2 V to 5.5 V, T_A = –40°C to +125°C		15		
	Channel separation	At 1 kHz		130		dB
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	100	114		dB
		T_A = –40°C to +125°C	95			
INPUT BIAS CURRENT						
I_B	Input bias current			±0.2	±10	pA
		T_A = –40°C to +85°C			±500	
		T_A = –40°C to +125°C			±10	nA
I_{OS}	Input offset current			±0.2	±10	pA
		T_A = –40°C to +85°C			±500	
		T_A = –40°C to +125°C			±10	nA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		2.8		$µV_{PP}$
e_n	Input voltage noise density	f = 1 kHz		10		nV/√Hz
		f = 10 kHz		9		
i_n	Input current noise density	f = 1 kHz		1.3		fA/√Hz
INPUT CAPACITANCE						
	Differential			5		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ	105	130		dB
		0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ, T_A = –40°C to +125°C	95	128		
		0.2 V < V_O < (V+) – 0.2 V, R_L = 2 kΩ	100	110		
PM	Phase margin	G = 1 V/V, V_S = 5 V, C_L = 15 pF		67		Degrees
FREQUENCY RESPONSE (V_S = 5.0 V, C_L = 50 pF)						
GBP	Gain bandwidth product	Unity gain		10		MHz
SR	Slew rate	G = +1		5		V/µs
t_S	Settling time	To 0.1%, 2-V step, G = +1		0.6		µs
		To 0.01%, 2-V step, G = +1		1		
	Overload recovery time	V_{IN} × G > V_S		200		ns
THD+N	Total harmonic distortion + noise (1)	V_O = 4 V_{PP}, G = +1, f = 10 kHz, R_L = 10 kΩ		0.0005%		
		V_O = 2 V_{PP}, G = +1, f = 10 kHz, R_L = 600 Ω		0.005%		

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics: V_S = 2.2 V to 5.5 V or ±1.1 V to ±2.75 V (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from both rails	R_L = 10 kΩ		10	20	mV
		R_L = 10 kΩ, T_A = –40°C to +125°C			30	
		R_L = 2 kΩ		25	45	
		R_L = 2 kΩ, T_A = –40°C to +125°C			55	
I_{SC}	Short-circuit current	V_S = 5.5 V	See the *Typical Characteristics*			mA
C_L	Capacitive load drive		See the *Typical Characteristics*			
R_O	Open-loop output resistance	I_O = 0 mA, f = 1 MHz		180		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5 V		0.65	0.75	mA
		I_O = 0 mA, V_S = 5.5 V, T_A = –40°C to +125°C			0.8	
	Power-on time	V+ = 0 V to 5 V, to 90% I_Q level		28		µs

6.8 Typical Characteristics

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

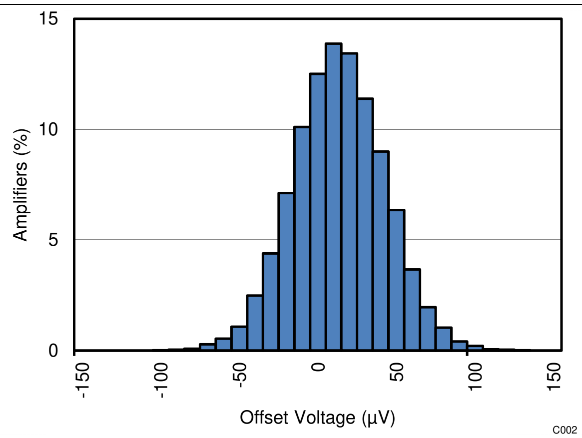


図 1. Offset Voltage Production Distribution Histogram

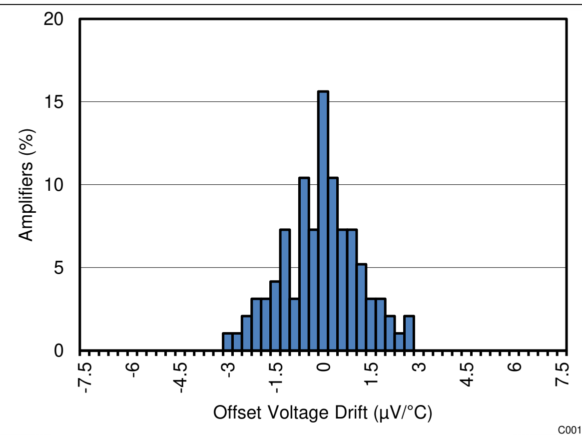


図 2. Offset Voltage Drift Distribution Histogram

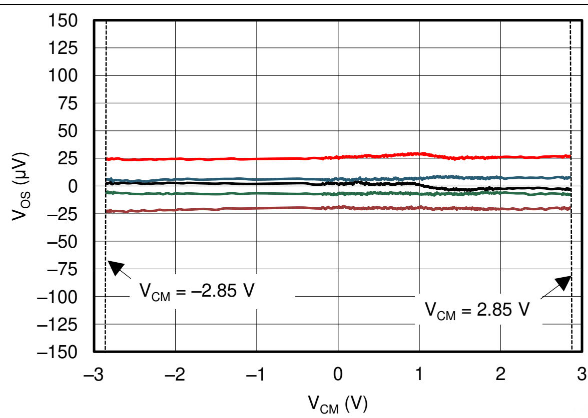


図 3. Offset Voltage vs Common-Mode Voltage

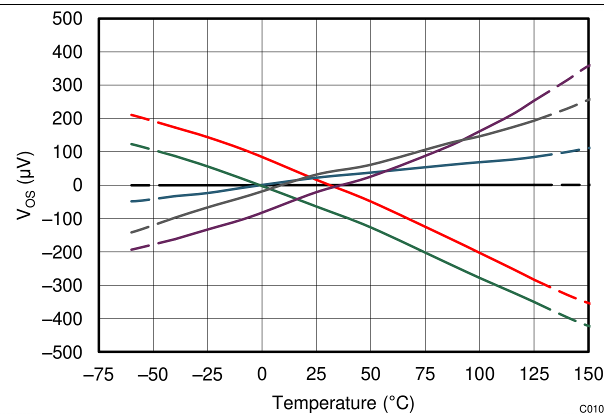


図 4. Offset Voltage vs Temperature

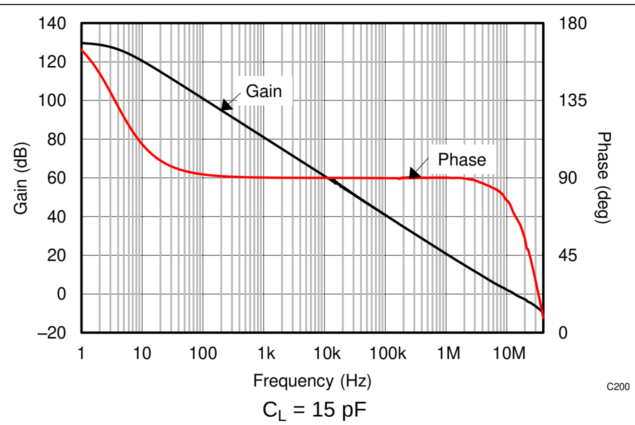


図 5. Open-Loop Gain and Phase vs Frequency

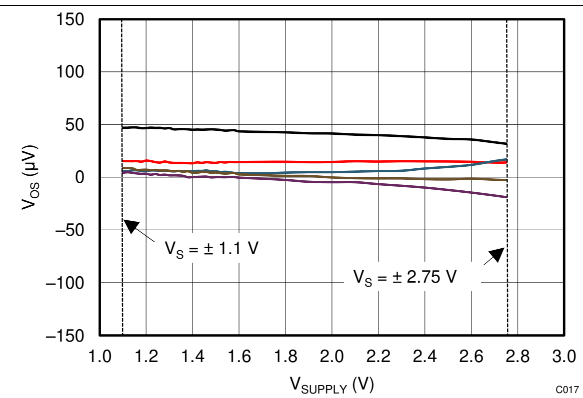


図 6. Offset Voltage vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

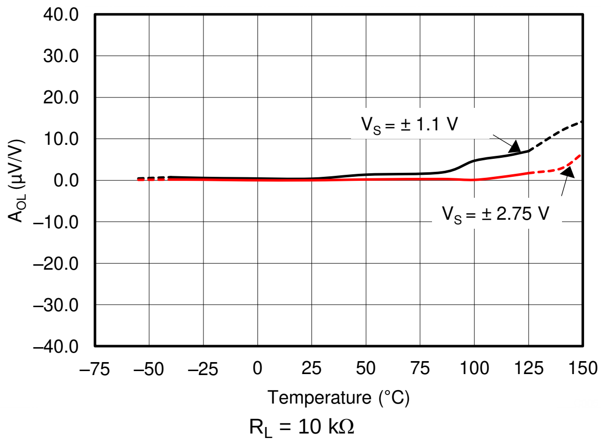


図 7. Open-Loop Gain vs Temperature

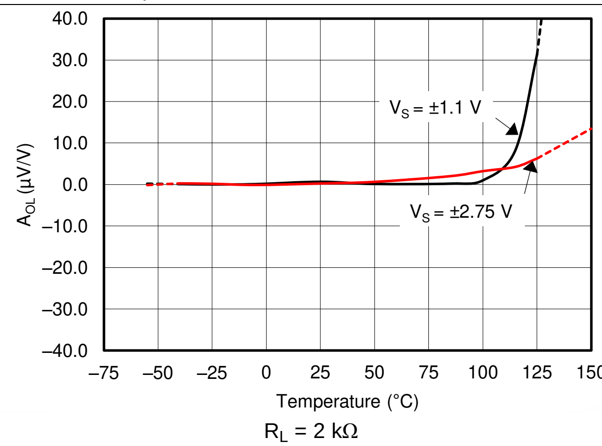


図 8. Open-Loop Gain vs Temperature

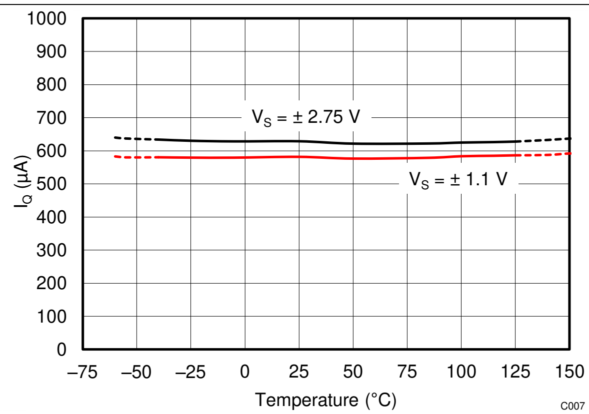


図 9. Quiescent Current vs Temperature

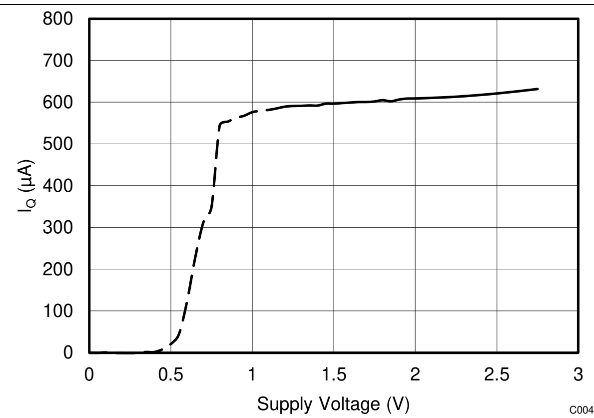


図 10. Quiescent Current vs Supply Voltage

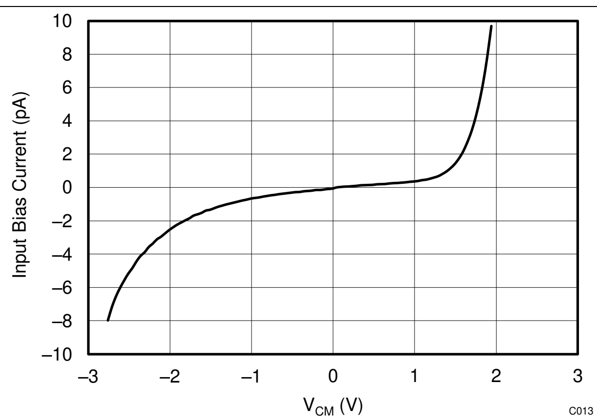


図 11. Input Bias Current vs Common-Mode Voltage

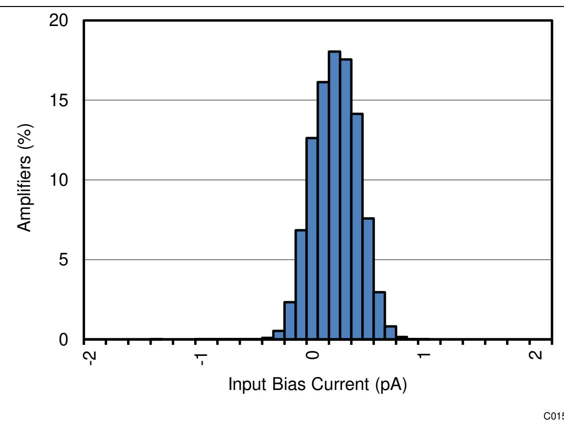


図 12. Input Bias Current Distribution Histogram

Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

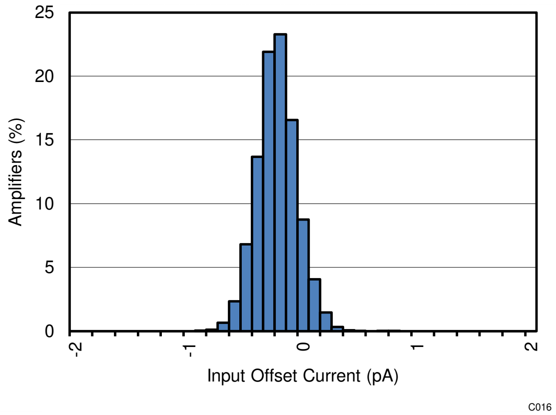


図 13. Input Offset Current Distribution Histogram

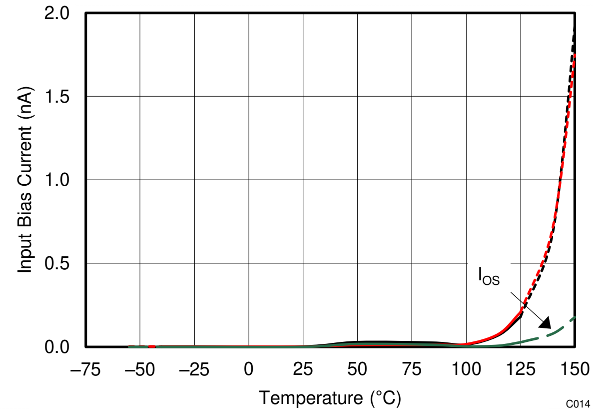


図 14. Input Bias Current vs Temperature

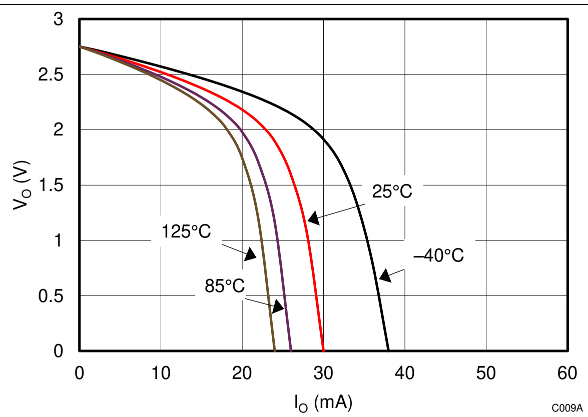


図 15. Output Voltage Swing (Positive) vs Output Current

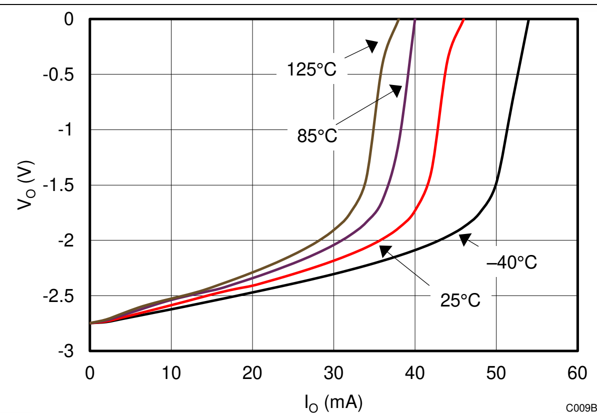


図 16. Output Voltage Swing (Negative) vs Output Current

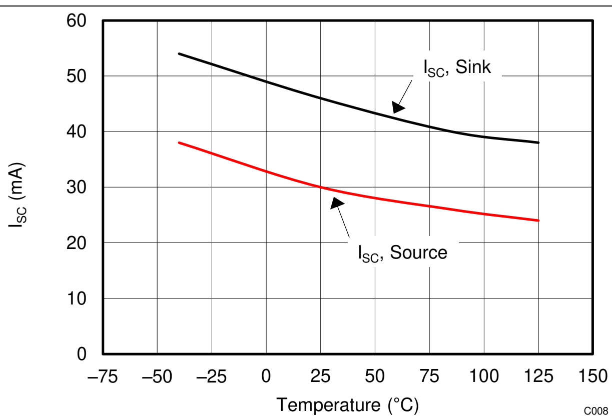


図 17. Short-Circuit Current vs Temperature

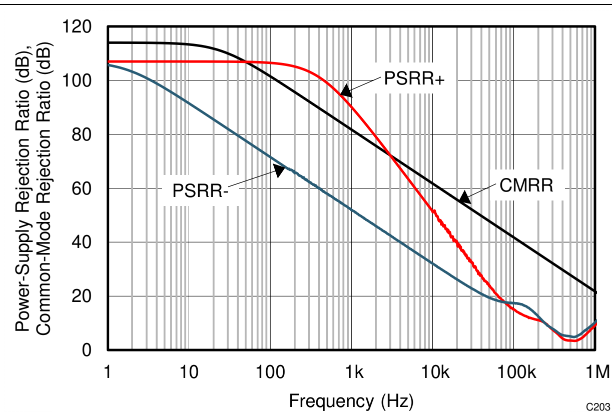


図 18. CMRR and PSRR vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

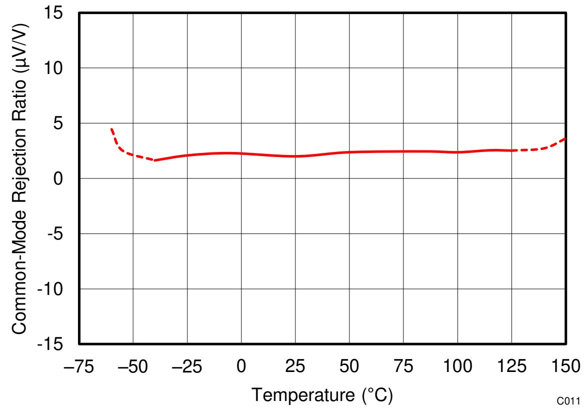


図 19. CMRR vs Temperature

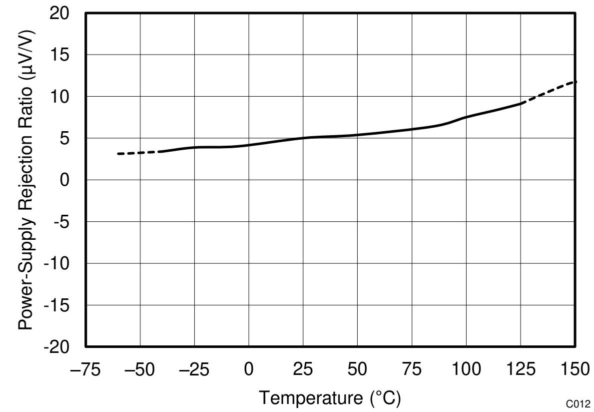


図 20. PSRR vs Temperature

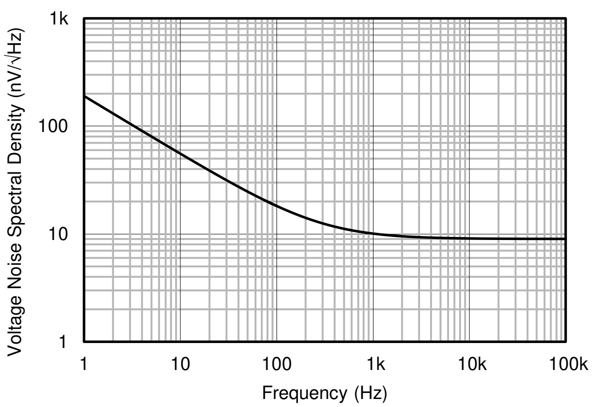


図 21. Input Voltage Noise Spectral Density vs Frequency

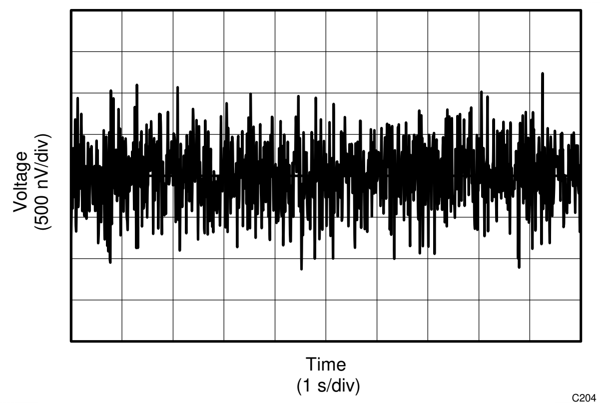
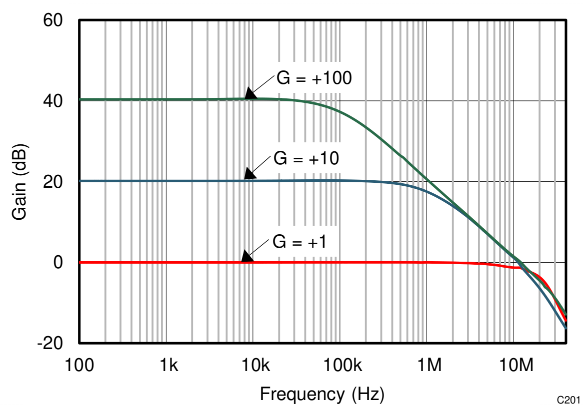
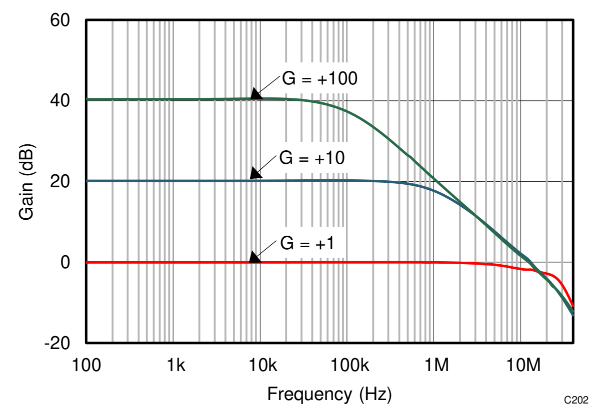


図 22. 0.1-Hz to 10-Hz Input Voltage Noise



V_S = 1.8 V, R_L = 10 kΩ, C_L = 15 pF

図 23. Closed-Loop Gain vs Frequency



V_S = 5.5 V, R_L = 10 kΩ, C_L = 15 pF

図 24. Closed-Loop Gain vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

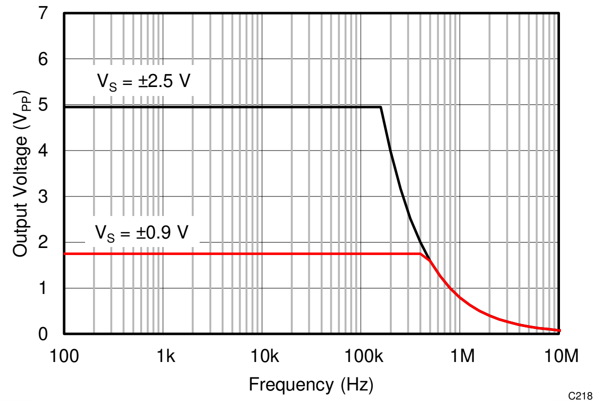


図 25. Maximum Output Voltage vs Frequency

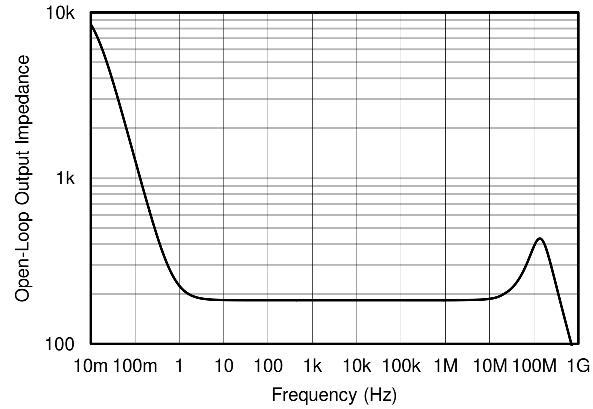


図 26. Open-Loop Output Impedance vs Frequency

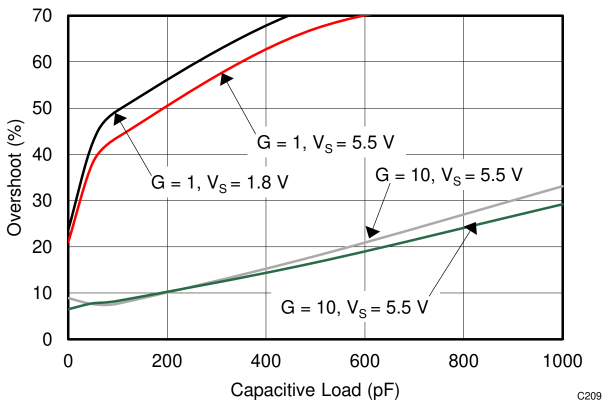
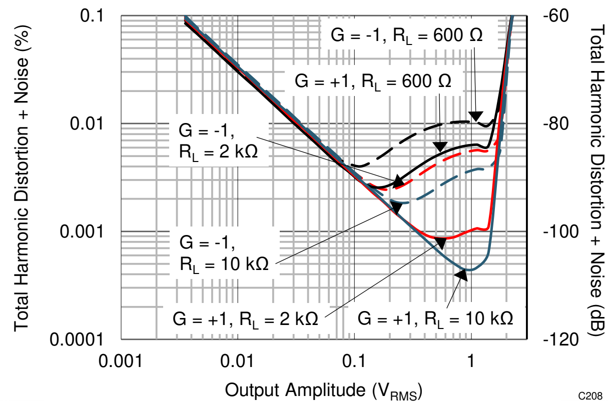
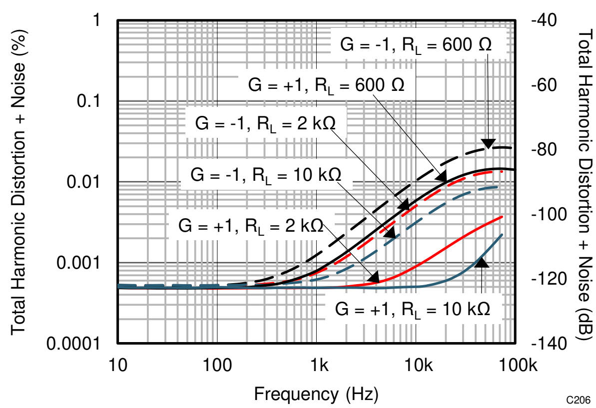


図 27. Small-Signal Overshoot vs Load Capacitance



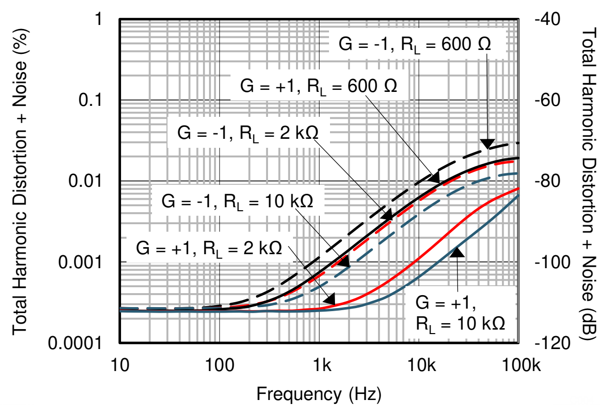
f = 10 kHz, V_S = ±2.5 V, filter bandwidth = 500 kHz

図 28. THD+N vs Amplitude



V_{IN} = 2 V_{PP}, V_S = ±2.5 V, filter bandwidth = 500 kHz

図 29. THD+N vs Frequency



V_{IN} = 4 V_{PP}, V_S = ±2.5 V, filter bandwidth = 500 kHz

図 30. THD+N vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

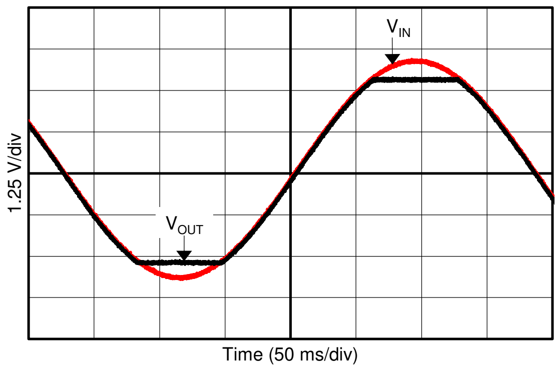


図 31. No Phase Reversal

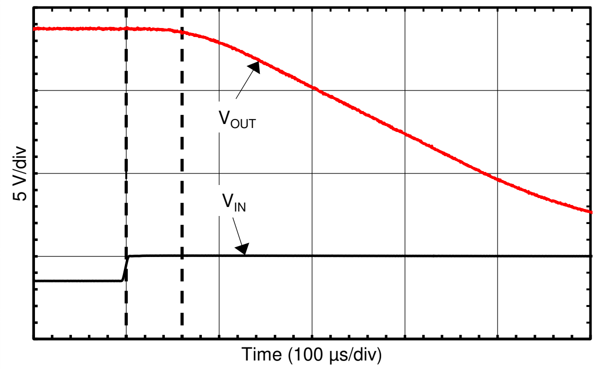


図 32. Positive Overload Recovery

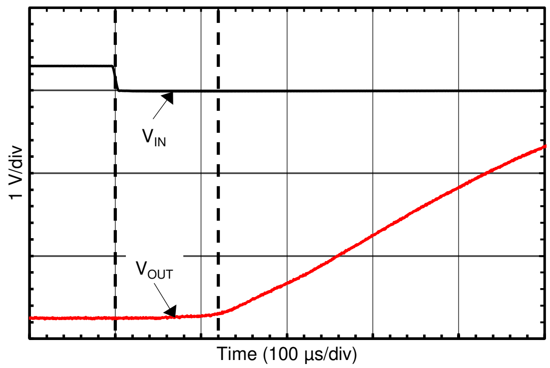
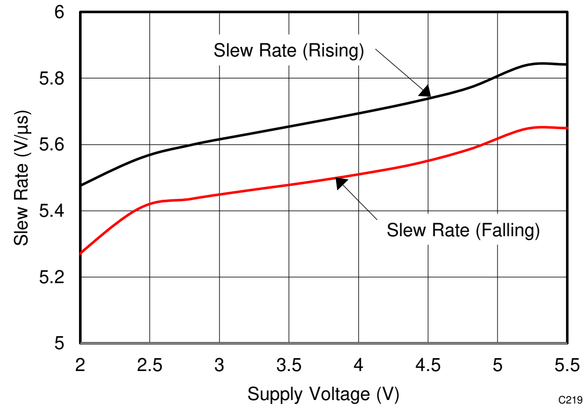
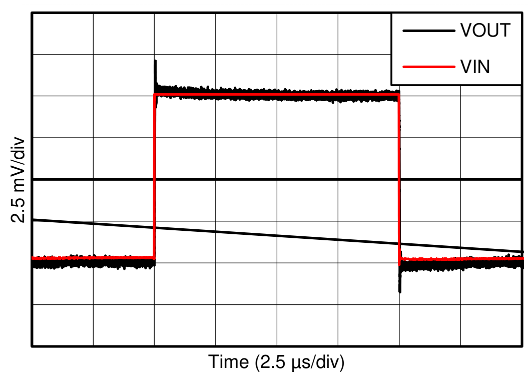


図 33. Negative Overload Recovery



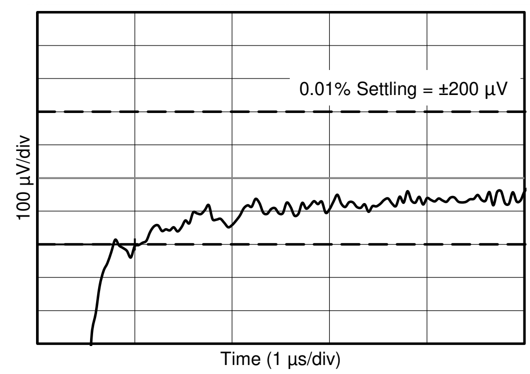
C_L = 15 pF

図 34. Slew Rate vs Supply Voltage



V_{IN} = 10 mV_{PP}, G = +1, C_L = 15 pF

図 35. Small-Signal Step Response

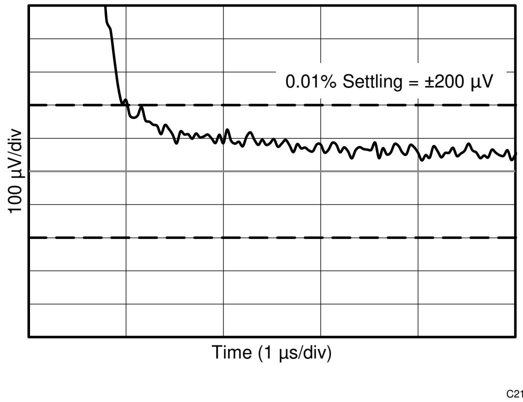


V_{IN} = 2-V step

図 36. 0.01% Positive Settling Time

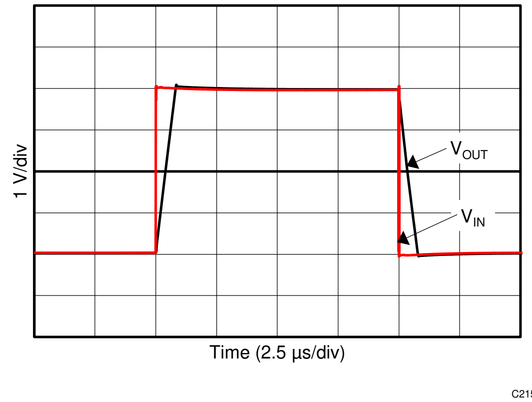
Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)



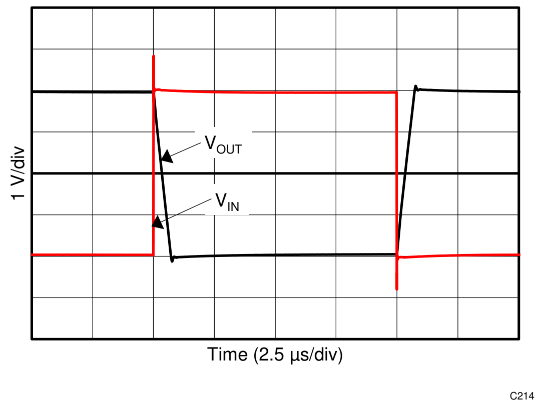
V_{IN} = 2-V step

図 37. 0.01% Negative Settling Time



V_{IN} = 4 V_{PP}, G = +1, C_L = 15 pF

図 38. Large-Signal Step Response



V_{IN} = 4 V_{PP}, G = –1, C_L = 15 pF

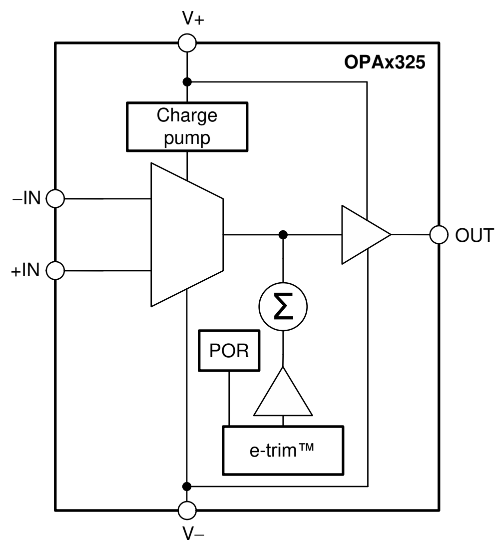
図 39. Large-Signal Step Response

7 Detailed Description

7.1 Overview

The OPA325, OPA2325, and OPA4325 (OPAx325) belong to a new generation of low-noise, e-trim™ operational amplifiers that provide outstanding dc precision. The OPAx325 also have a highly linear input stage with zero-crossover distortion that delivers excellent CMRR and distortion performance across the full rail-to-rail input range. In addition, this device has a wide supply range with excellent PSRR. This feature, combined with low quiescent current, makes the OPAx325 an excellent choice for applications that are battery-powered without regulation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Zero-Crossover Input Stage

Traditional complementary metal-oxide semiconductor (CMOS) rail-to-rail input amplifiers use a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. This configuration results in sudden change in offset voltage when the input stage transitions from the p-channel metal-oxide-semiconductor field effect transistor (PMOS) to the n-type field effect transistor (NMOS), or vice-versa, as shown in 図 40. This transition results in significant degradation of CMRR and PSRR performance of the amplifier.

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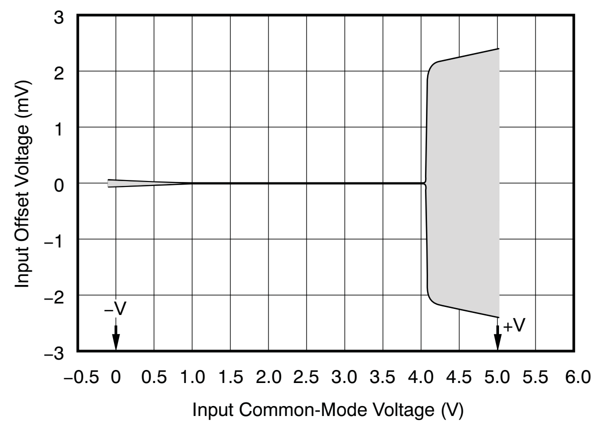

図 40. Input Common-Mode Voltage vs Input Offset Voltage (Traditional Rail-to-Rail Input CMOS Amplifiers)

The OPAx325 series of amplifiers includes an internal charge pump that powers the amplifier input stage with an internal supply rail that is higher than the external power supply. The internal supply rail allows a single differential pair to operate and to be linear across the entire input common-mode voltage range, thus eliminating crossover distortion. Rail-to-rail amplifiers that use this technique to eliminate crossover distortion are called *zero-crossover amplifiers*.

The single differential pair combined with the charge pump allows the OPAx325 to provide superior CMRR across the entire common-mode input range, which extends 100 mV beyond both power-supply rails. 図 41 shows the input offset voltage versus input common-mode voltage plot for the OPAx325. Note that unlike traditional rail-to-rail CMOS amplifiers, there is no transition region for the OPAx325.

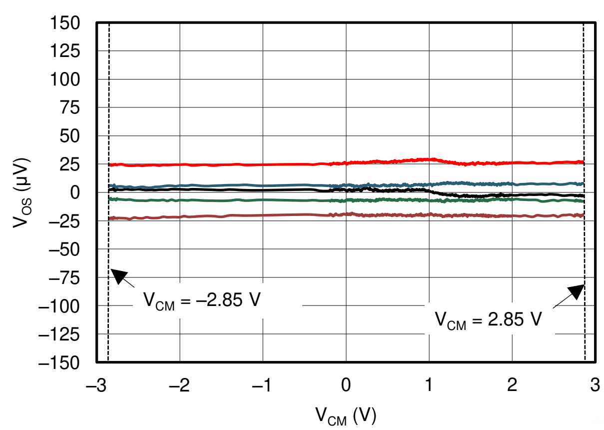

図 41. Offset Voltage vs Common-Mode Voltage (Zero-Crossover)

Feature Description (continued)

7.3.2 Low Input Offset Voltage

The OPAx325 are manufactured using TI's e-trim technology. Each amplifier is trimmed in production, thereby minimizing errors associated with input offset voltage. The e-trim technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing. This process allows the OPAx325 to have an excellent offset specification of 150 µV (maximum). 図 42 shows the offset voltage distribution for the OPAx325.

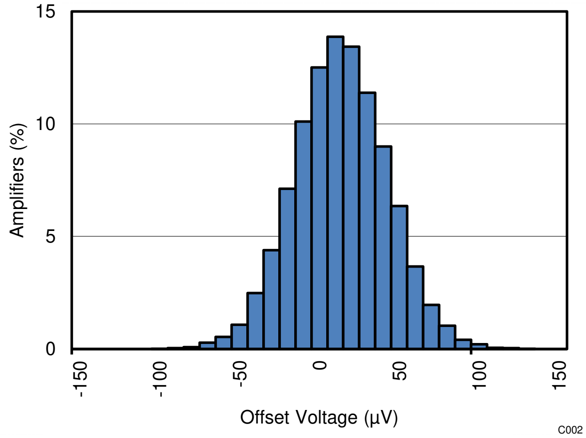

図 42. Offset Voltage Distribution

7.3.3 Input and ESD Protection

The OPAx325 incorporate internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. 図 43 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input; thus, keep the value to a minimum in noise-sensitive applications.

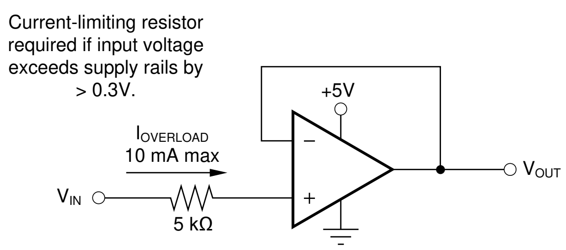

図 43. Input Current Protection

7.4 Device Functional Modes

The OPAx325 have a single functional mode and are operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power-supply voltage for the OPAx325 is 5.5 V (±2.75 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx325 series features e-trim, a proprietary technique in which the offset voltage is adjusted during the final steps of manufacturing. As a result, the OPAx325 deliver excellent offset voltage (40 µV, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A_{OL}. The OPAx325 also feature a linear input stage with zero-crossover distortion, resulting in excellent CMRR over the entire input range, which extends from 100 mV below the negative rail to 100 mV above the positive rail.

8.1.1 Operating Characteristics

The OPAx325 family of amplifiers has parameters that are fully specified from 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

8.1.2 Basic Amplifier Configurations

The OPAx325 are unity-gain stable. The devices do not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in 図 44. The OPAx325 are configured as a basic inverting amplifier with a gain of –10 V/V. This single-supply connection has an output centered on the common-mode voltage, V_{CM}. For the circuit shown, this voltage is 2.5 V, but can be any value within the common-mode input voltage range.

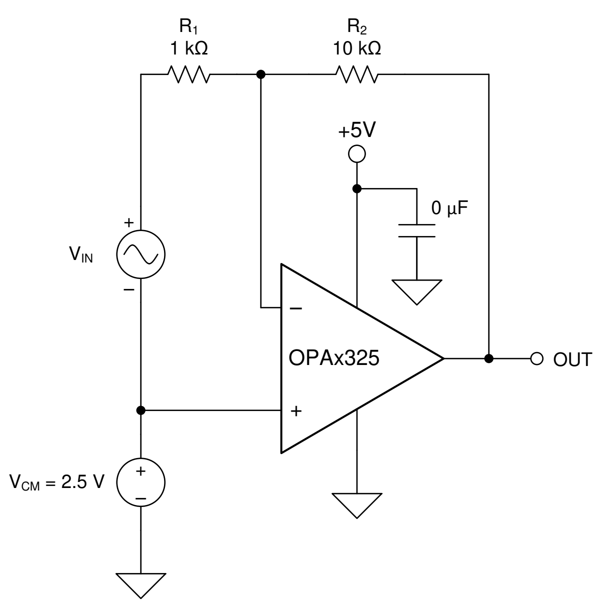

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図 44. Basic Single-Supply Connection

Application Information (continued)

8.1.3 Driving an Analog-to-Digital Converter

The low-noise and wide-gain bandwidth of the OPAx325, combined with rail-to-rail input/output and zero-crossover distortion, make these devices an excellent input driver for ADCs. 図 45 shows the OPAx325 driving an ADC. The amplifier is connected as a unity-gain, noninverting buffer.

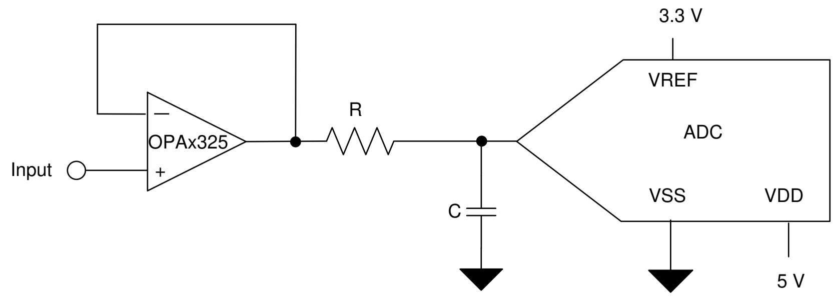

図 45. The OPAx325 as an Input Driver for ADCs

8.2 Typical Application

Operational amplifiers are commonly used as unity-gain buffers. 図 46 shows the schematic for an amplifier configured as a unity-gain buffer. If the input signal range to the amplifier is very close to the rails or includes the rails, a rail-to-rail amplifier must be used. However, regular rail-to-rail amplifiers introduce significant distortion to the signal. This design compares the distortion introduced by a typical CMOS input amplifier with that of the OPAx325 (a zero-crossover amplifier).

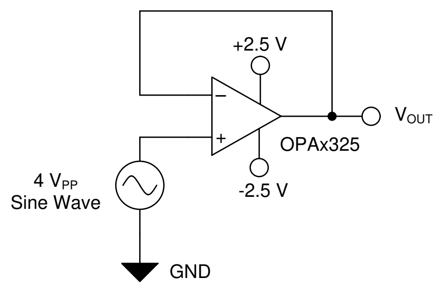

図 46. The OPAx325 Configured as a Unity-Gain Buffer Amplifier

8.2.1 Design Requirements

The following parameters are used for this design example:

- Gain = +1 V/V (inverting gain)
- V+ = 2.5 V, V– = –2.5 V
- Input signal = 4 V_{PP}, f = 1-kHz sine wave

Typical Application (continued)

8.2.2 Detailed Design Procedure

Traditional CMOS rail-to-rail input amplifiers use a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in 図 47.

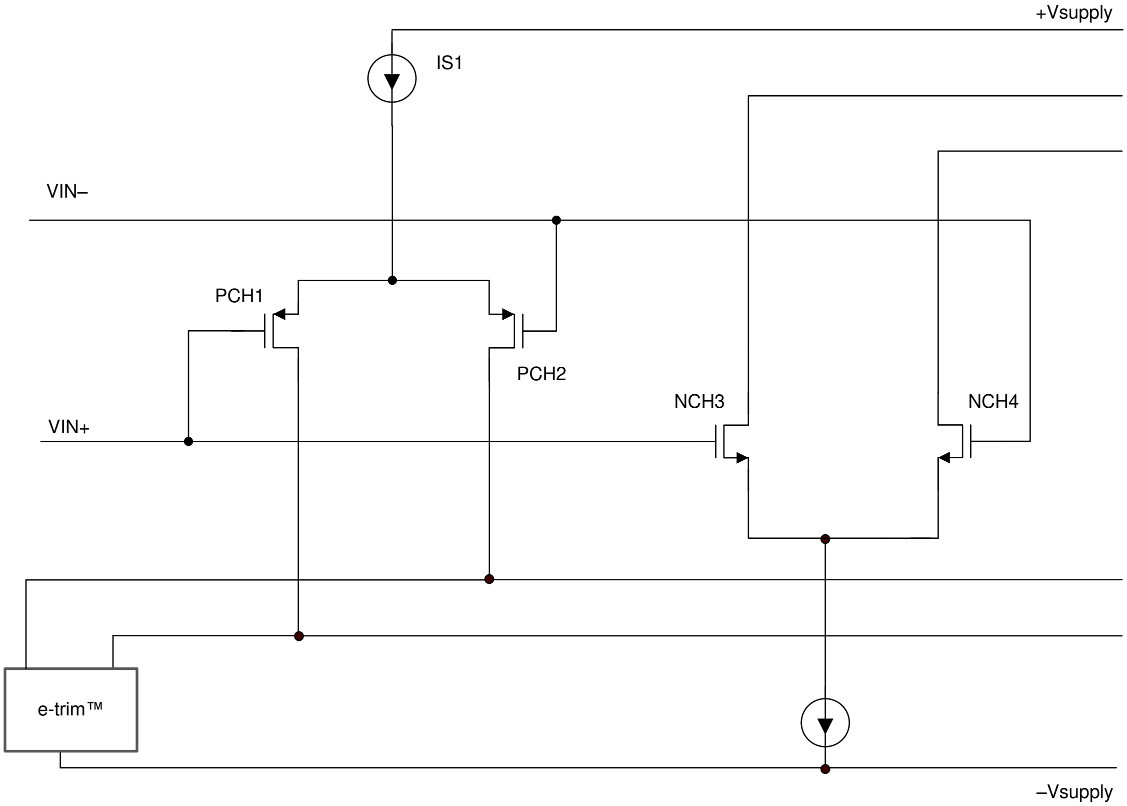

図 47. Complementary Input Stage (Traditional Rail-to-Rail Input CMOS Amplifiers)

Typical Application (continued)

The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 200 mV above the positive supply, and the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1 V. There is a small transition region, typically (V+) – 1.1 V to (V+) – 0.9 V, in which both pairs are on. This transition region is shown in 図 48 for a traditional rail-to-rail input CMOS amplifier. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded when compared to device operation outside of this region.

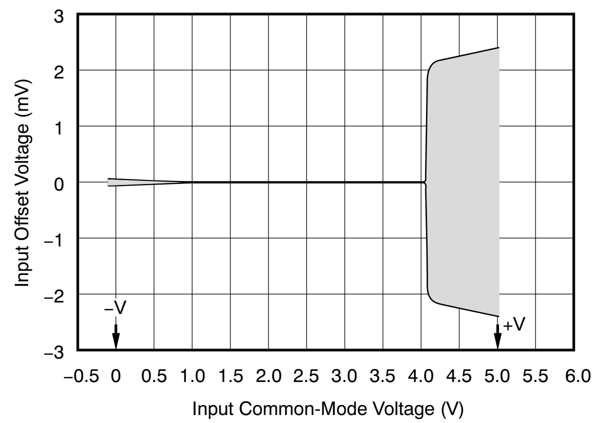

図 48. Input Offset Voltage vs Common-Mode Voltage (For Traditional Rail-to-Rail Input CMOS Amplifiers)

The OPAx325 amplifiers include an internal charge pump that powers the amplifier input stage with an internal supply rail that is higher than the external power supply. The internal supply rail allows a single differential pair to operate and to be linear across the entire input common-mode voltage range, as shown in 表 1.

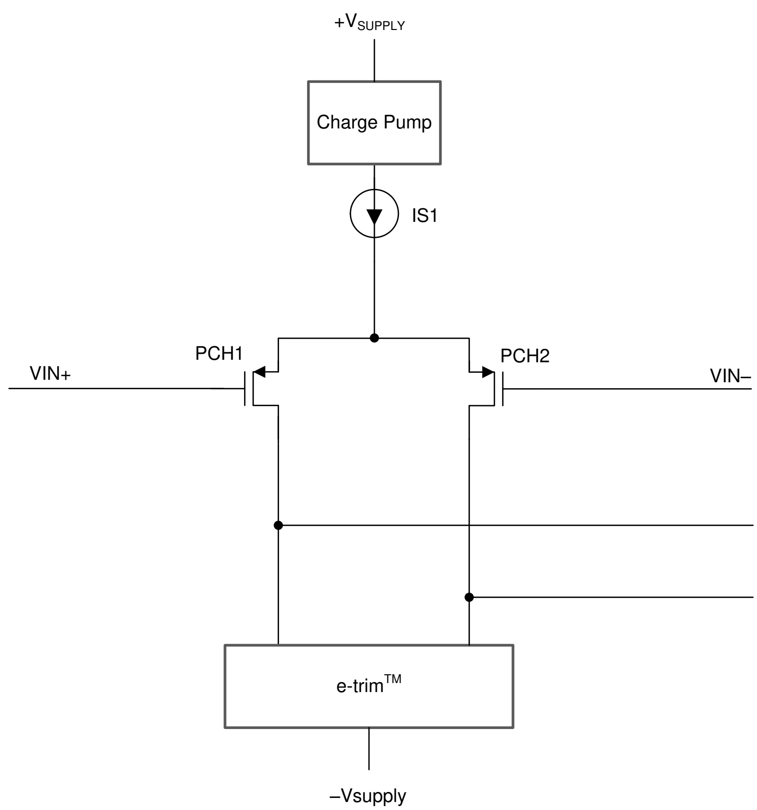

図 49. Single Differential Input Pair with a Charge Pump (Zero-Crossover)

Typical Application (continued)

The unique zero-crossover topology shown in 表 1 eliminates the input offset transition region, typical of most rail-to-rail input operational amplifiers. This topology allows the OPAx325 to provide superior CMRR across the entire common-mode input range that extends 100 mV beyond both power-supply rails. 図 50 shows the input offset voltage versus input common-mode voltage plot for the OPAx325.

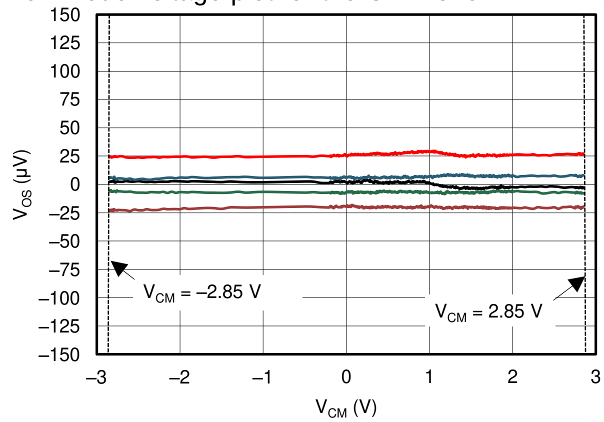

図 50. Offset Voltage vs Common-Mode Voltage (OPAx325, Zero-Crossover Amplifier)

The OPAx325 and a typical CMOS amplifier were used in identical circuits where these amplifiers were configured as a unity-gain buffer amplifier; see 図 51 and 図 52. A pure sine wave with an amplitude of 2 V (4 V_{PP}) was given as input to the two identical circuits of 図 51 and 図 52. The outputs of these circuits were captured on a spectrum analyzer. 図 53 and 図 54 illustrate the output voltage spectrum for the OPAx325 and a typical CMOS rail-to-rail amplifier, respectively. The output of the OPAx325 has very few spurs and harmonics when compared to the typical rail-to-rail CMOS amplifier, as illustrated in 図 55.

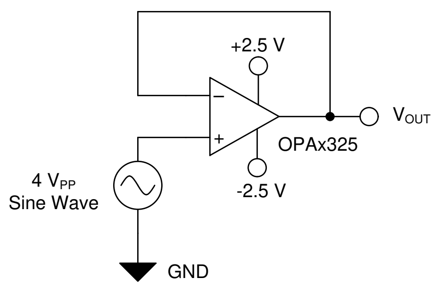

図 51. OPAx325 as a Unity-Gain Buffer

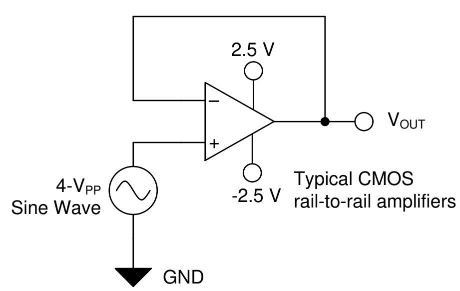

図 52. Typical CMOS Rail-to-Rail Amplifier as a Unity-Gain Buffer

Typical Application (continued)

8.2.3 Application Curves

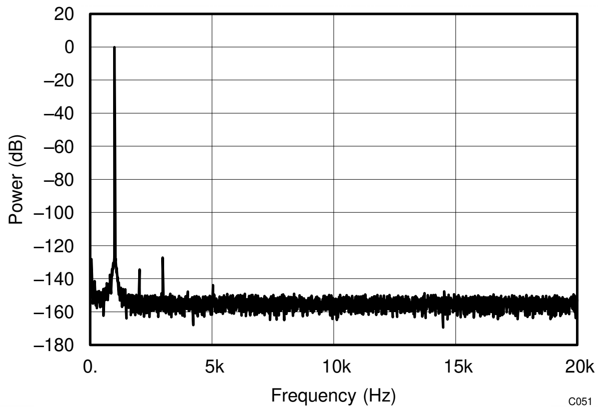

図 53. Output Voltage Spectrum (OPAx325)

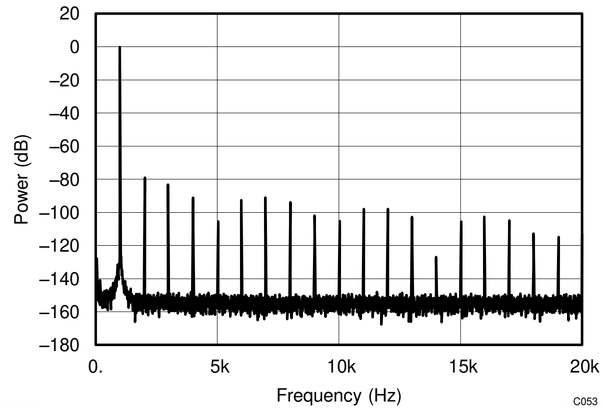

図 54. Output Voltage Spectrum (Typical CMOS Rail-to-Rail Amplifier)

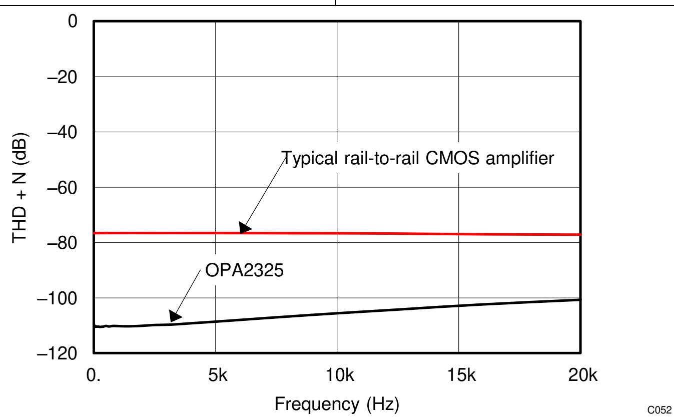

図 55. THD+N vs Frequency

9 Power Supply Recommendations

The OPAx325 are specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information refer to, see *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in 図 57, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

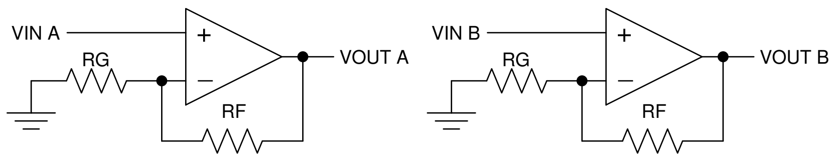

図 56. Schematic Representation for 図 57

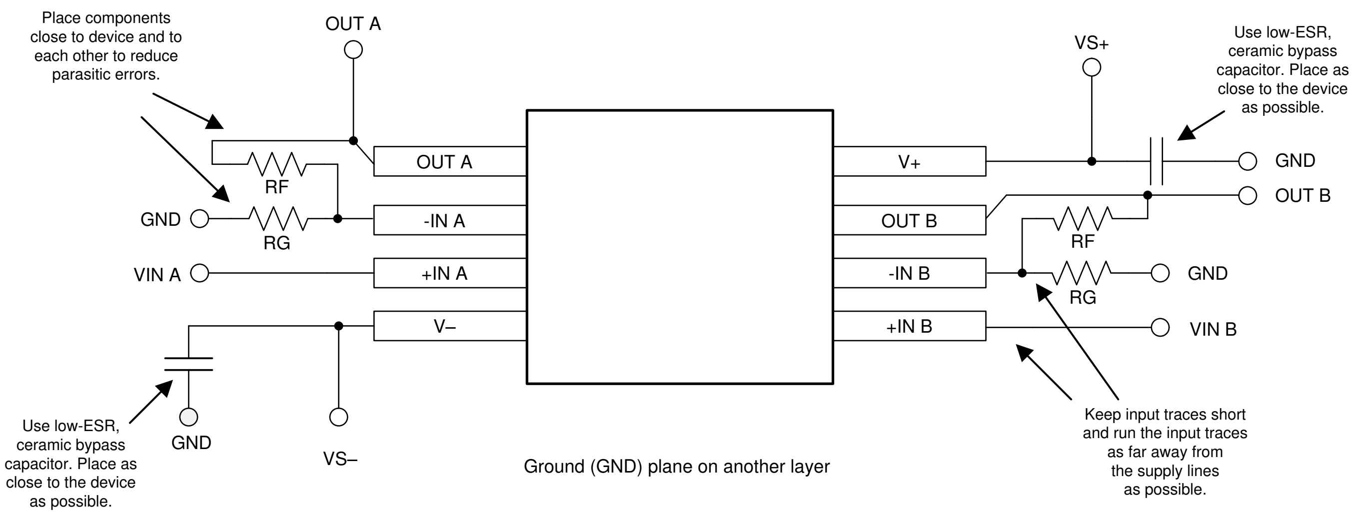

図 57. Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

テキサス・インスツルメンツ、『*Circuit Board Layout Techniques*』アプリケーション・レポート (英語)

11.2 関連リンク

表 1 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA325	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2325	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4325	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商標

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11.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2325ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2325
OPA2325ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2325
OPA2325IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	18L6
OPA2325IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18L6
OPA2325IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	18L6
OPA2325IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18L6
OPA2325IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2325
OPA2325IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2325
OPA2325IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2325
OPA2325IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2325
OPA325IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1UEV
OPA325IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1UEV
OPA325IDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1UEV
OPA325IDBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1UEV
OPA325IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1UEV
OPA325IDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1UEV
OPA4325IPW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4325
OPA4325IPW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4325
OPA4325IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4325
OPA4325IPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4325

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[(4)] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[(5)] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[(6)] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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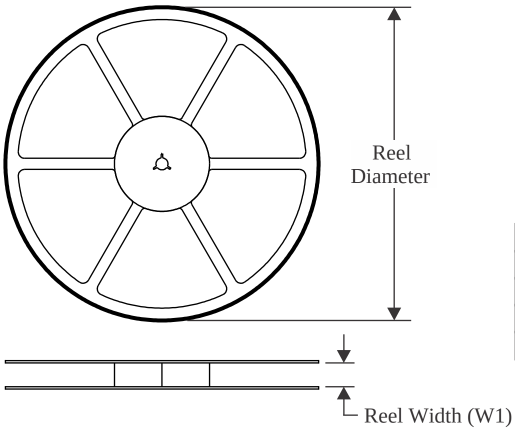
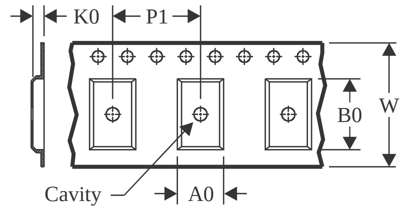
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

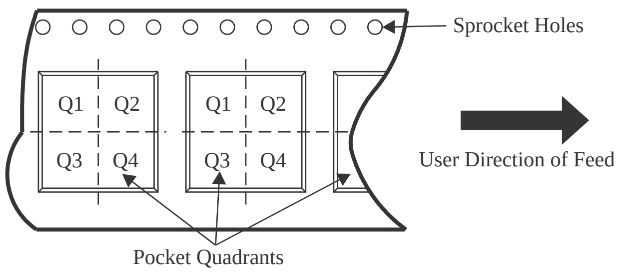


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

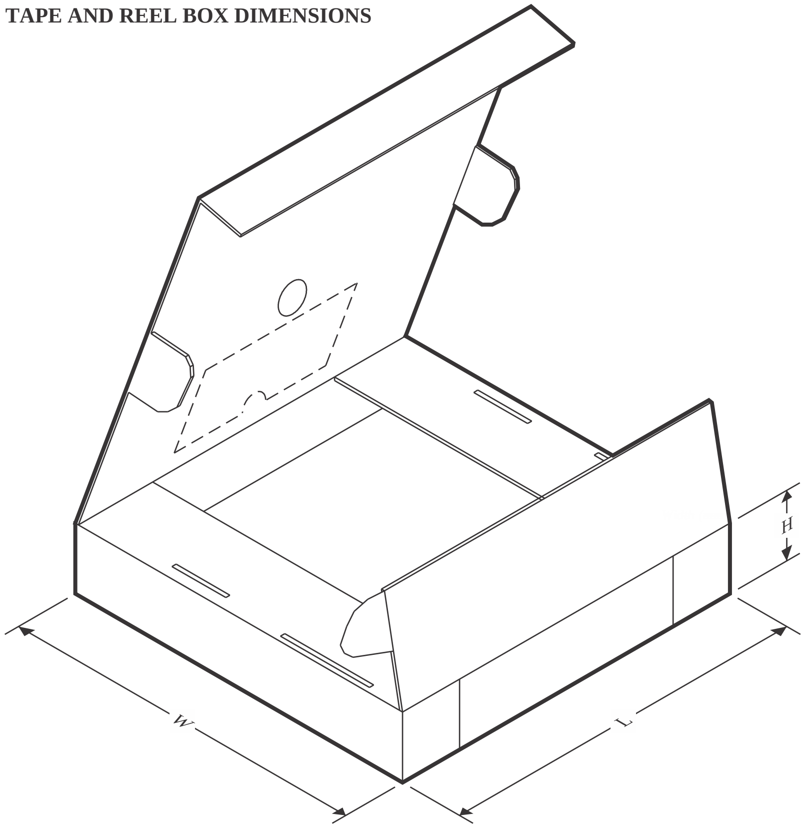
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2325IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2325IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2325IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2325IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2325IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA325IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA325IDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA325IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA4325IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

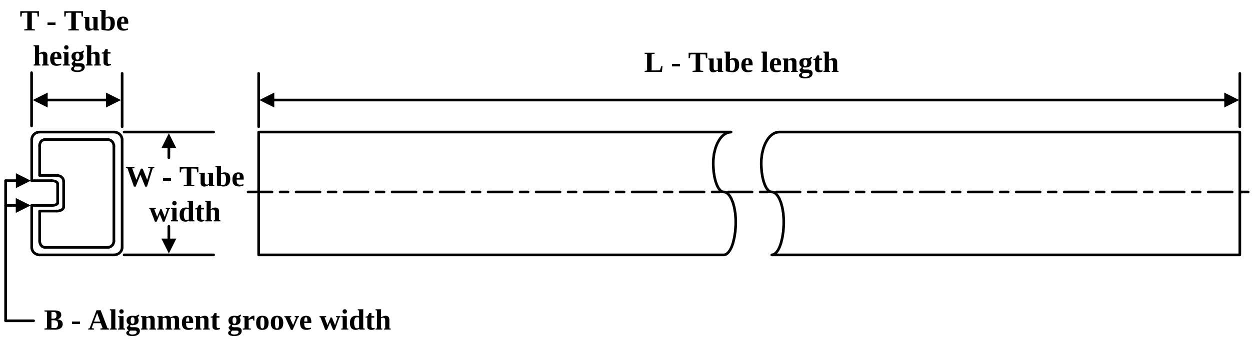
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

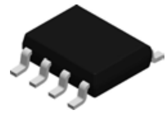
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2325IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2325IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2325IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2325IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2325IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA325IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA325IDBVRG4	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA325IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA4325IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

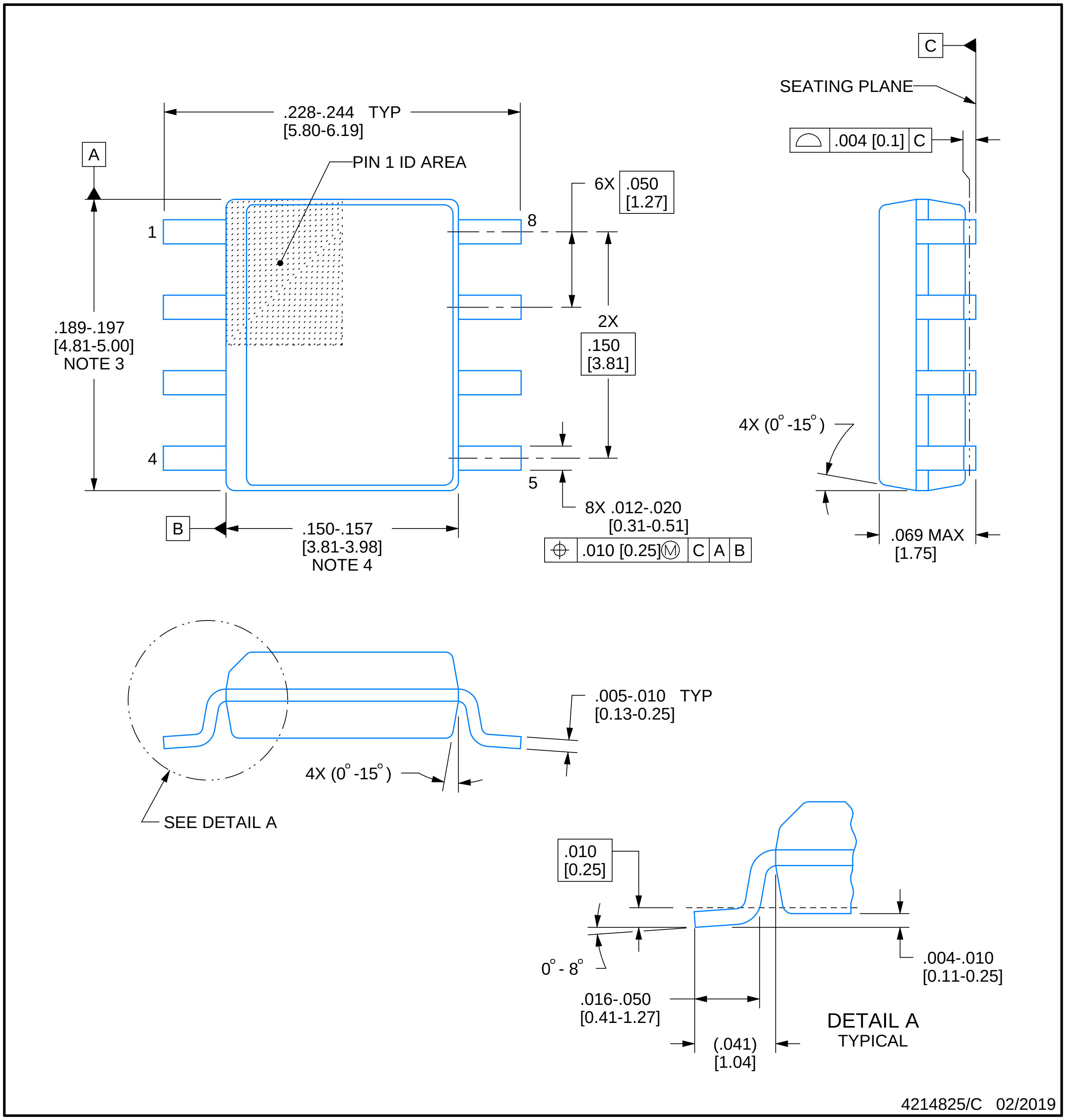
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2325ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2325ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA4325IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
OPA4325IPW.B	PW	TSSOP	14	90	530	10.2	3600	3.5



D0008A

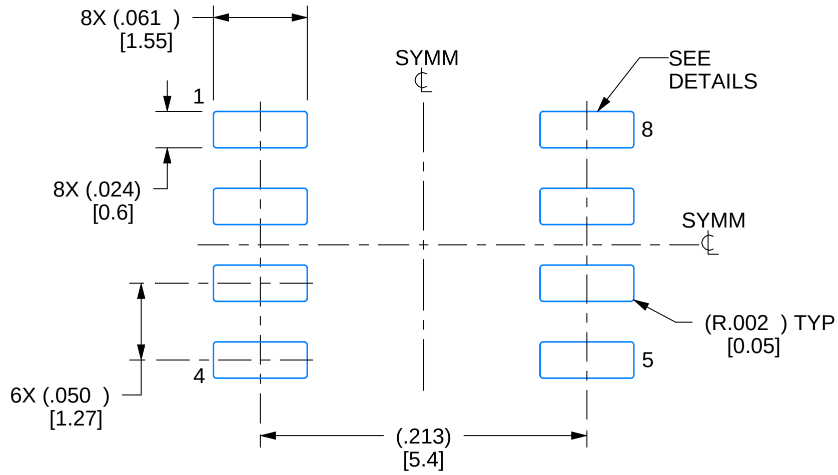
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

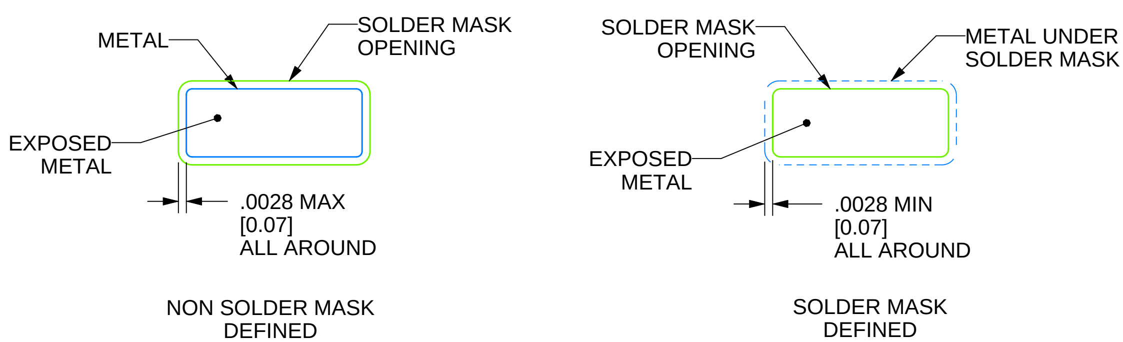


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

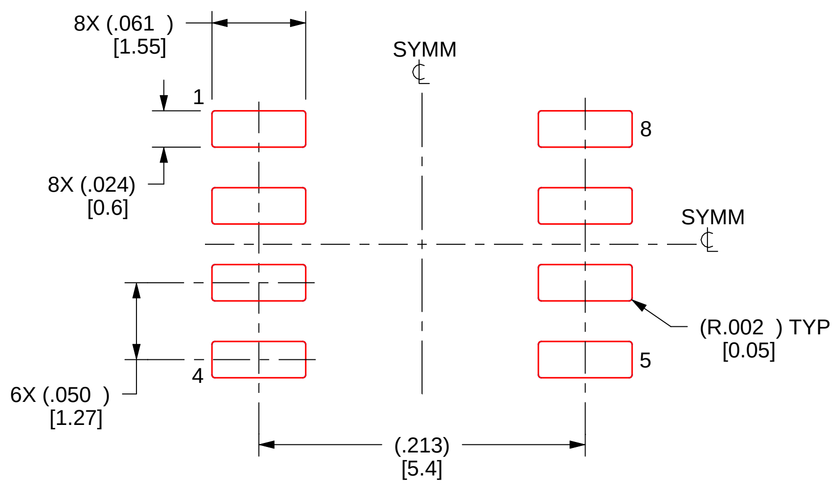


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

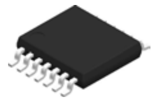


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

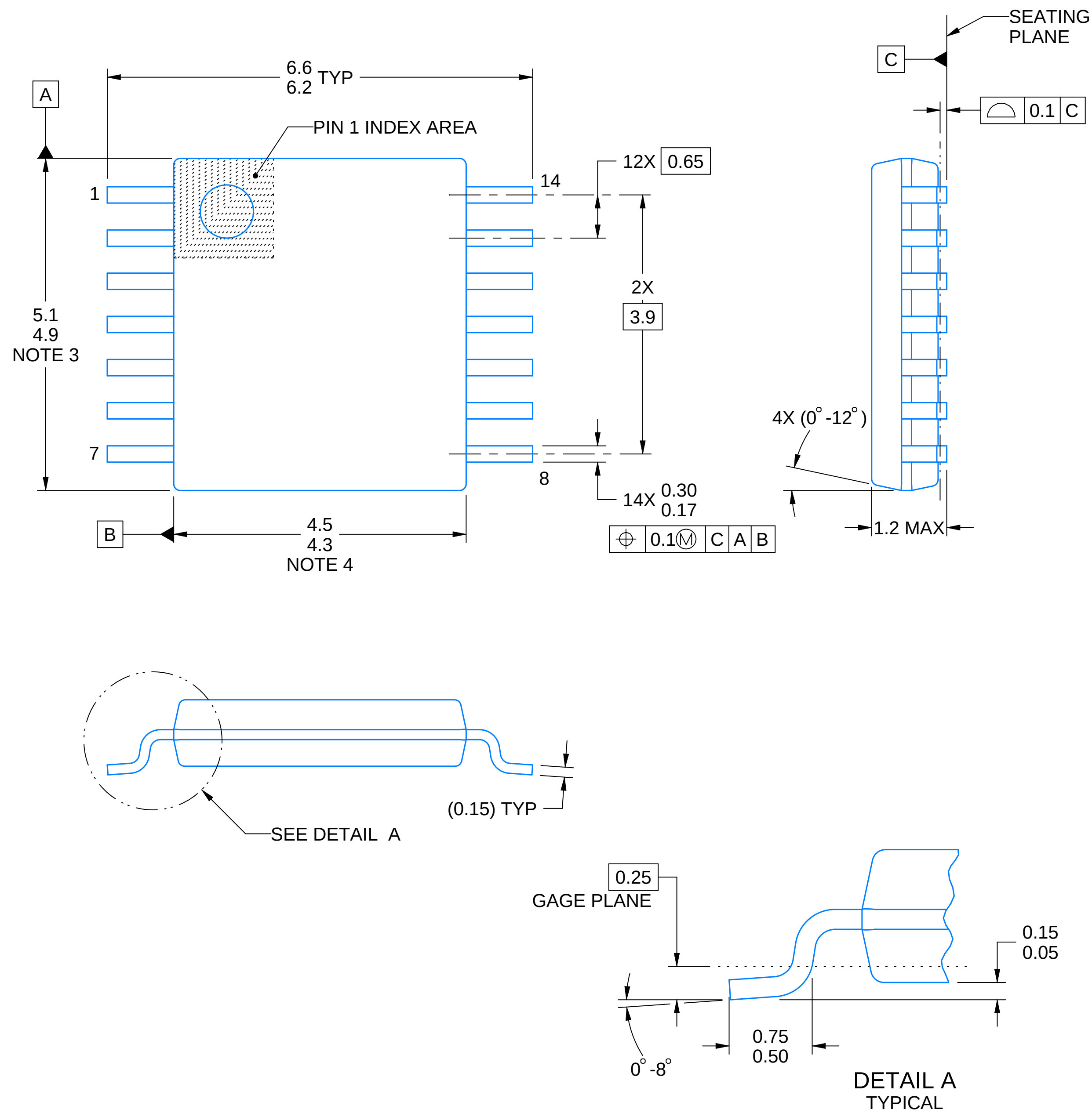
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

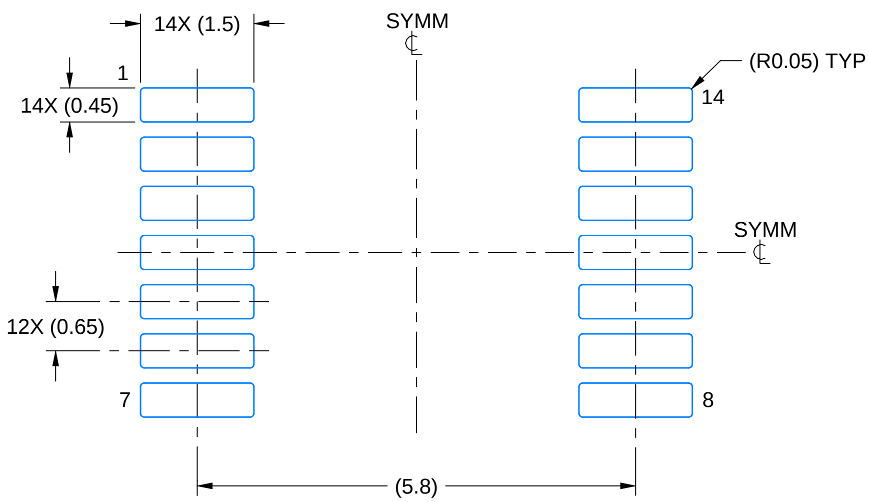
SMALL OUTLINE PACKAGE



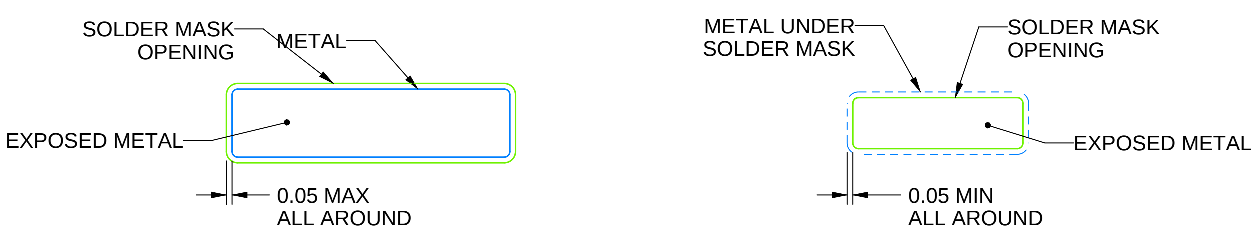
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

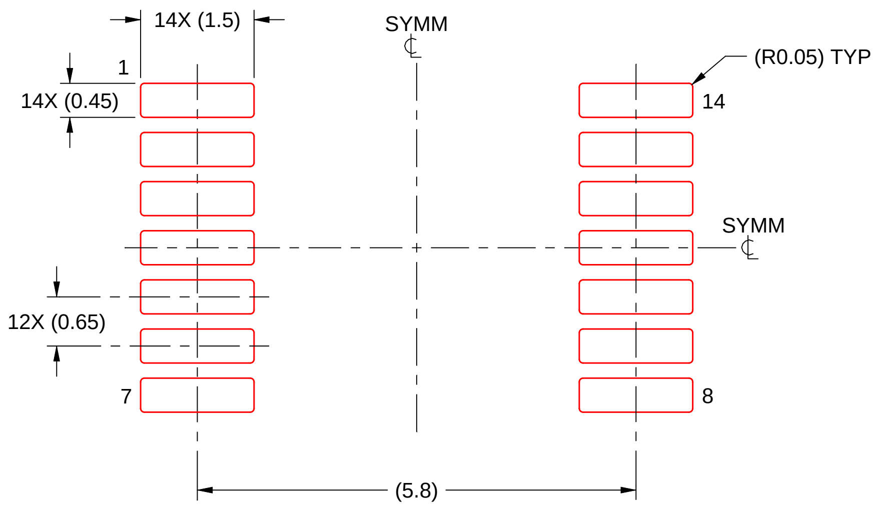
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

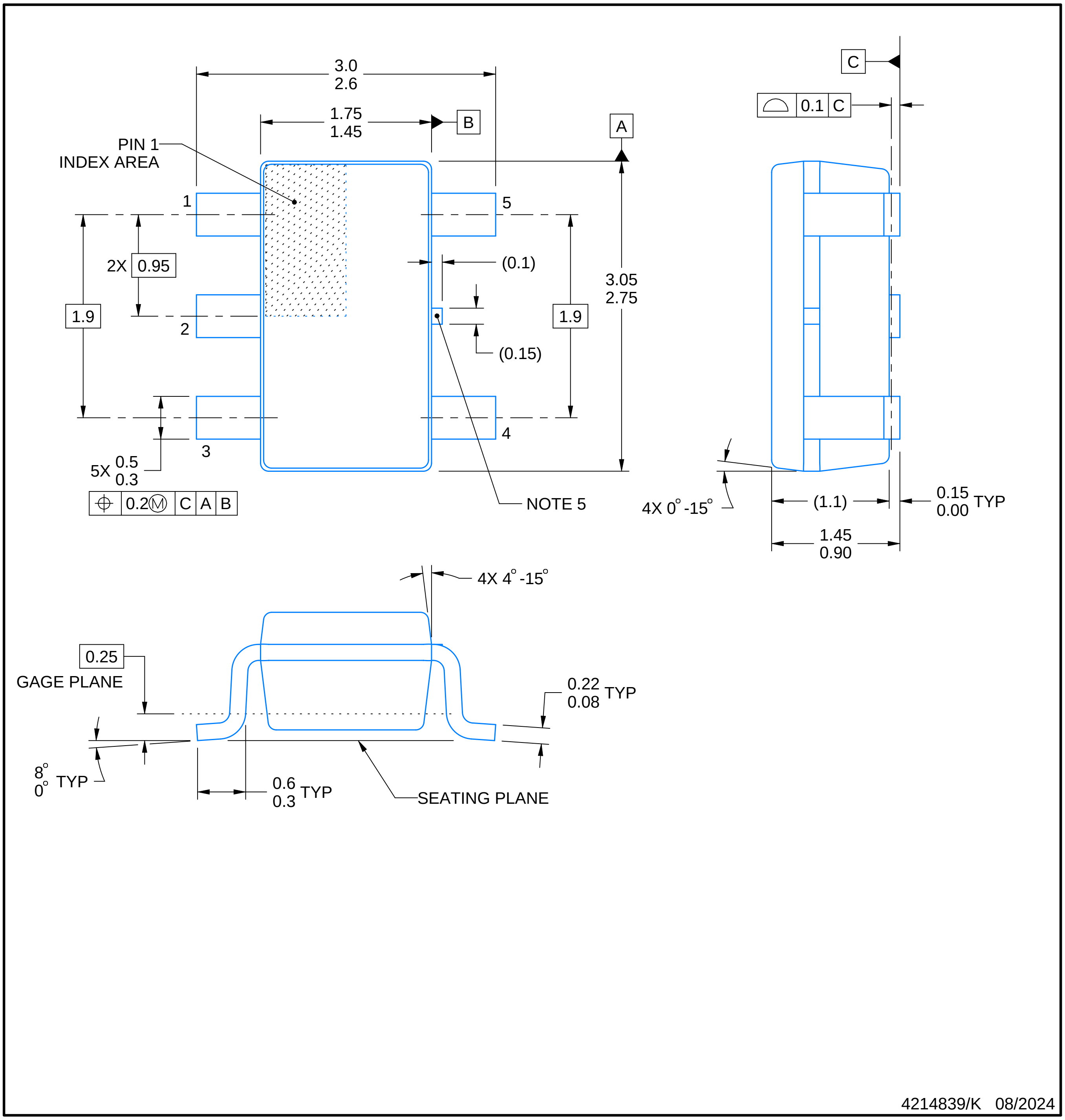


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

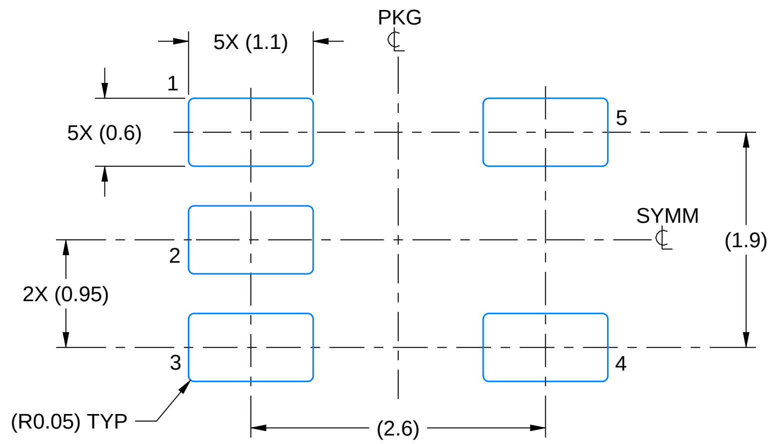
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

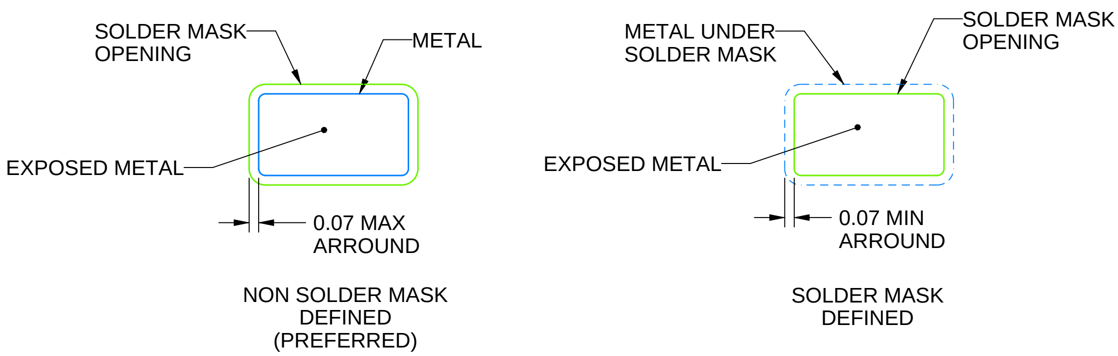


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

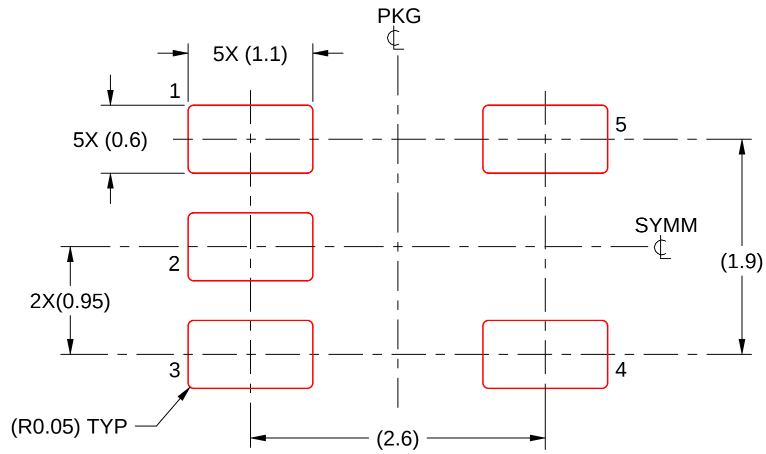


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

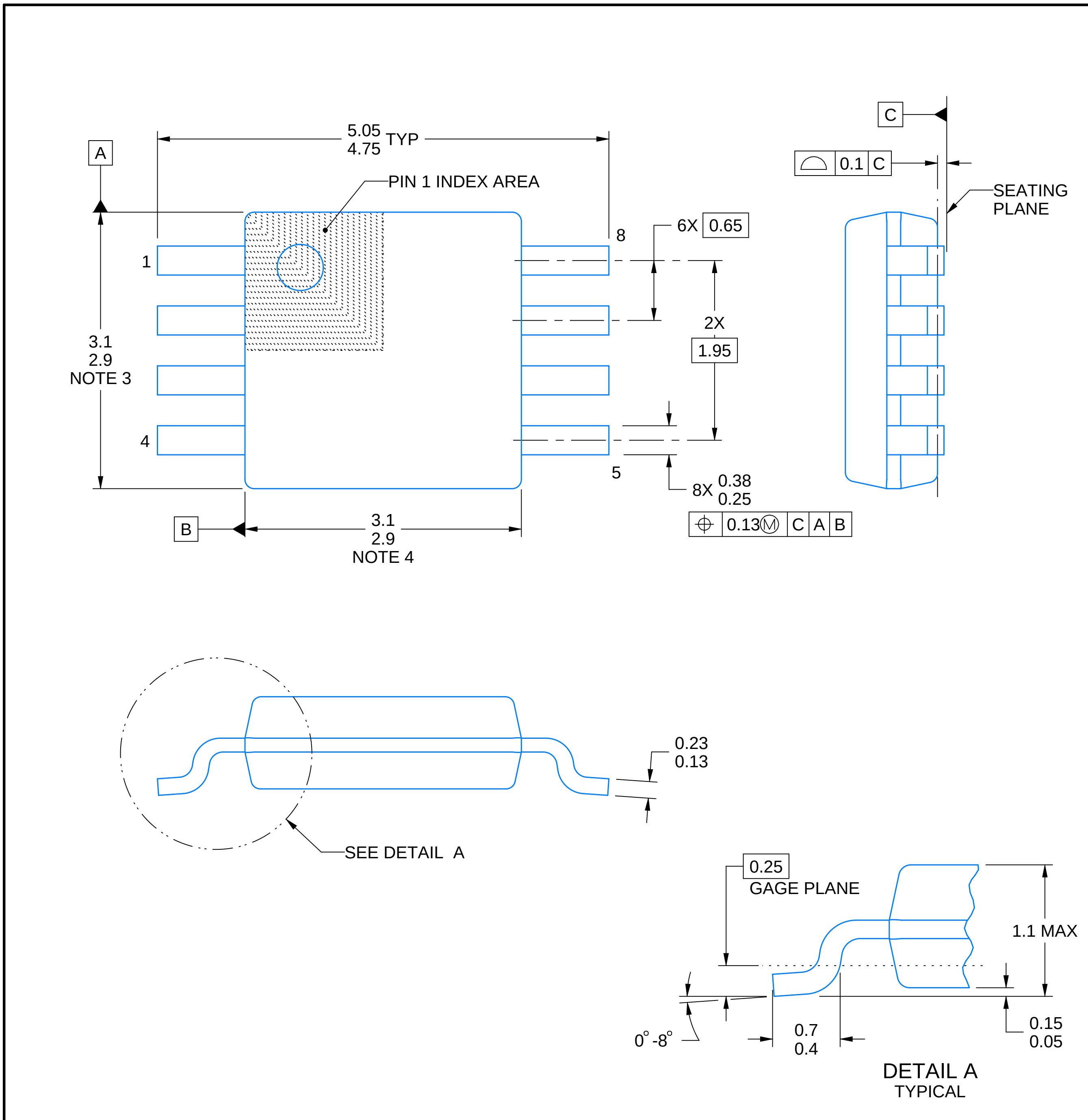


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

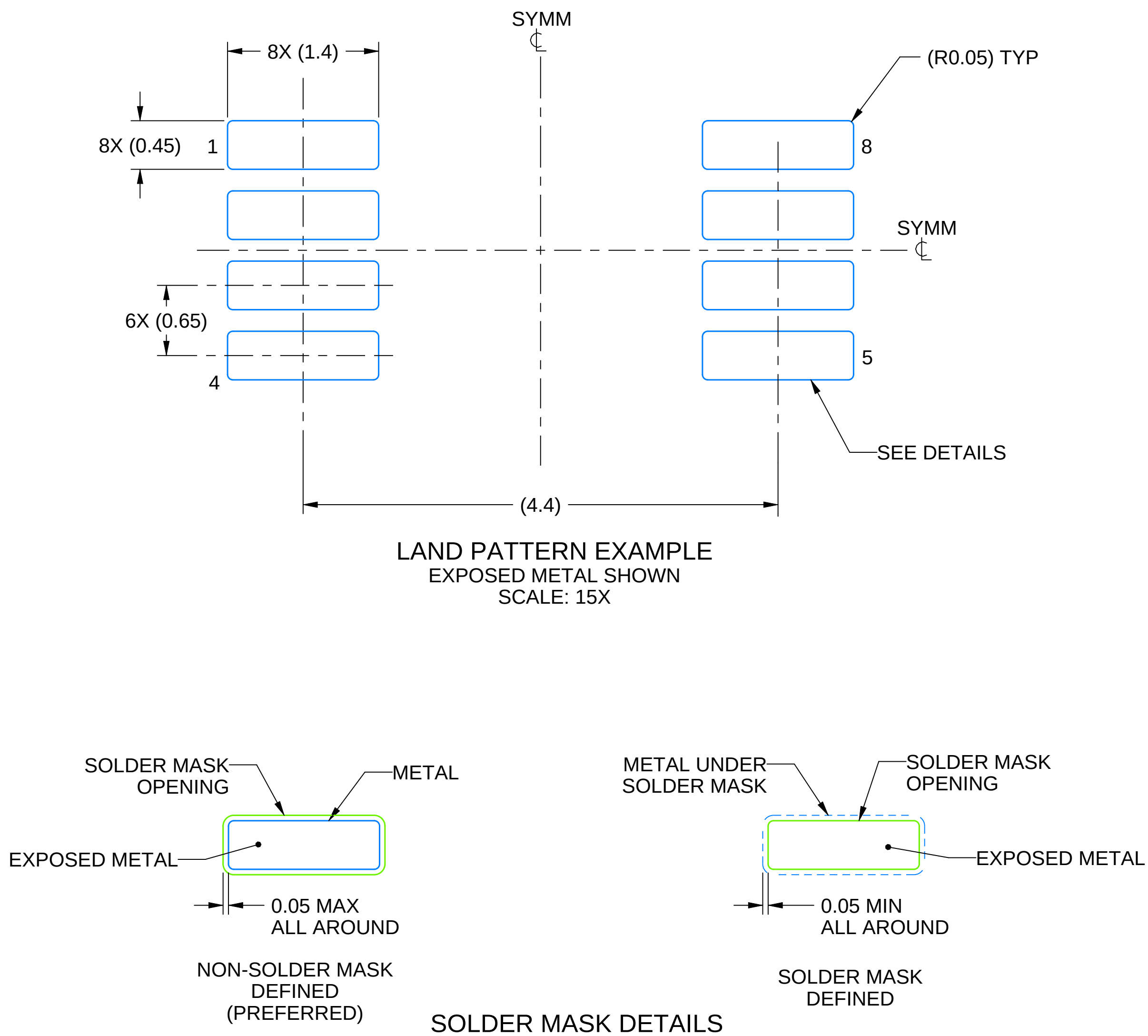
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214862/A 04/2023

NOTES:

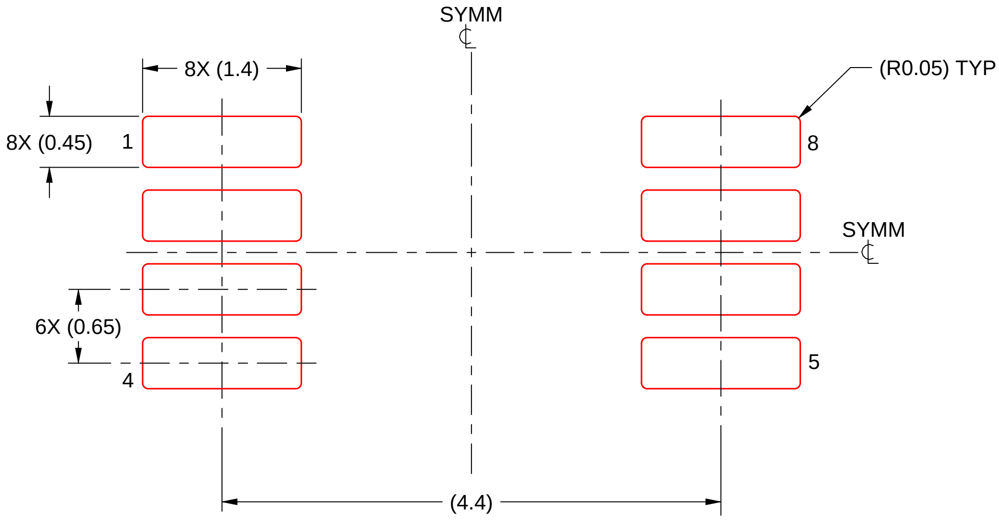
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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