OPA830 低消費電力、単電源、広帯域オペアンプ

1 特長

- 広い帯域幅:
  - 250MHz (ゲイン = +1)
  - 110MHz (ゲイン = +2)
- 低い消費電流: 3.9mA (V_S = 5V)
- フレキシブルな電源電圧範囲:
  - デュアル電源:±1.4V～±5.5V
  - シングル電源:2.8V～11V
- シングル電源の場合、入力範囲はグランドにも対応
- 出力スイング:5V 電源で 4.88V
- 高いスルーレート:550V/µs
- 小さい入力電圧ノイズ:9.2nV/√Hz
- パッケージ:鉛フリー SOT23

2 アプリケーション

- 単一電源 A/D コンバータ (ADC) の入力バッファ
- 単一電源 ビデオ ライン ドライバ
- CCD イメージング チャネル
- 低消費電力超音波
- PLL 積分器
- 携帯型消費者向け電子機器

3 概要

OPA830 は、低消費電力、単一電源、広帯域、電圧帰還型アンプであり、3V または 5V の単一電源で動作するよう設計されています。このデバイスは、±5V または +10V 電源での動作もサポートしています。入力範囲は、負の電源よりも下から始まり、正の電源の 1.7V 内側までとなっています。相補的共通エミッタ出力を使用することにより、150Ω を駆動して、どちらの電源からも 25mV 以内の出力スイングが得られます。また、大きい出力駆動電流 (±80mA) と、小さい差動ゲインおよび位相誤差により、このデバイスは単一電源の消費者向けビデオ製品に最適です。

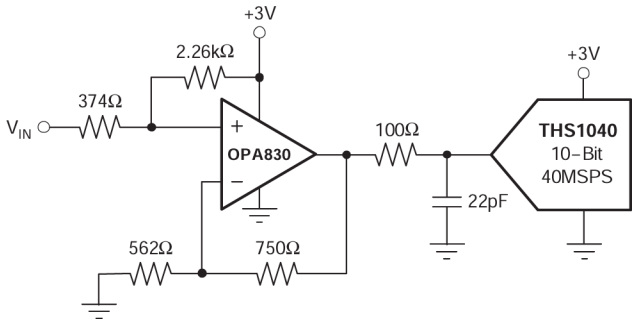
大きいゲイン帯域幅積 (110MHz) とスルーレート (550V/µs) により低歪み動作を実現しているため、OPA830 は 3V および 5V CMOS ADC への優れた入力バッファ段となります。他の低消費電力、単電源のアンプとは異なり、信号振幅が小さくなるにつれて歪み性能は向上します。入力電圧ノイズが 9.2nV/√Hz と低いため、広いダイナミック レンジでの動作に対応できます。

OPA830 は、業界標準の SO-8 パッケージおよび超小型の SOT23-5 パッケージで供給されます。固定ゲイン ライン ドライバ アプリケーションについては、OPA832 をご検討ください。

パッケージ情報

部品番号 (1)	パッケージ (2)	パッケージ サイズ(3)
OPA830	D (SOIC、8)	4.9mm × 6mm
	DBV (SOT-23、5)	2.9mm × 2.8mm

(1) セクション 4 を参照してください。
(2) 詳細については、セクション 11 を参照してください。
(3) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



DC 結合、3V ADC ドライバ

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4 Device Comparison Table

DESCRIPTION	SINGLES	DUALS	TRIPLES	QUADS
Rail-to-rail	—	OPA2830	—	OPA4830
Rail-to-rail fixed gain	OPA832	OPA2832	OPA3832	—
General-purpose (1800V/µs slew rate)	OPA690	OPA2690	OPA3690	—
Low-noise, high dc precision	OPA820	OPA2822	—	OPA4820

5 Pin Configurations

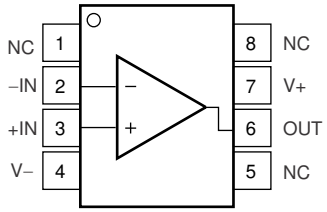


図 5-1. D Package, 8-Pin SO-8 (Top View)

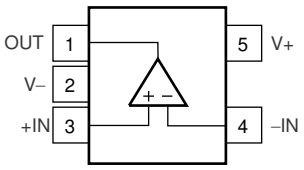


図 5-2. DBV Package, 5-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SO-8)	DBV (SOT-23)		
–IN	2	4	Input	Inverting input
+IN	3	3	Input	Noninverting input
NC	1, 5, 8	—	—	No internal connection (float this pin)
OUT	6	1	Output	Output
V–	4	2	—	Negative (lowest) supply
V+	7	5	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply	For DBV package		±6.5	V_{DC}
	For D package		12	
Internal power dissipation		See *Thermal Information*		
Differential input voltage			±2.5	V
Input voltage			$V_{S–}$ – 0.5V to V_{S+} + 0.3V	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	3	10	11	V
T_A	Operating temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA830		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125	186.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	N/A	84.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	53.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	N/A	21.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	N/A	52.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics for D Package V_S = ±5V

at T_A = 25°C[1], G = +2, R_F = 750Ω, R_L = 150Ω to ground, and R_{SRC} = 375Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE					
Small-signal bandwidth	G = +1, V_O ≤ 0.2V_{PP}		310		MHz
Small-signal bandwidth[2]	G = +2, V_O ≤ 0.2V_{PP}	70	120		
	G = +2, V_O ≤ 0.2V_{PP}, T_A = 0°C to 70°C	68			
	G = +2, V_O ≤ 0.2V_{PP}, T_A = –40°C to +85°C	65			
	G = +5, V_O ≤ 0.2V_{PP}	18	25		
	G = +5, V_O ≤ 0.2V_{PP}, T_A = 0°C to 70°C	16			
	G = +5, V_O ≤ 0.2V_{PP}, T_A = –40°C to +85°C	15			
	G = +10, V_O ≤ 0.2V_{PP}	8	11		
	G = +10, V_O ≤ 0.2V_{PP}, T_A = 0°C to 70°C	7			
	G = +10, V_O ≤ 0.2V_{PP}, T_A = –40°C to +85°C	6			
Gain bandwidth product[2]	G ≥ +10	85	110		MHz
	G ≥ +10, T_A = 0°C to 70°C	82			
	G ≥ +10, T_A = –40°C to +85°C	80			
Peaking at a gain of +1	V_O ≤ 0.2V_{PP}		6		dB
Slew rate[2]	G = +2, 2V step	280	600		V/µs
	G = +2, 2V step, T_A = 0°C to 70°C	270			
	G = +2, 2V step, T_A = –40°C to +85°C	260			
Rise time[2]	0.5V step		3.3	5.8	ns
	0.5V step, T_A = 0°C to 70°C			5.85	
	0.5V step, T_A = –40°C to +85°C			5.9	
Fall time[2]	0.5V step		3.5	5.9	ns
	0.5V step, T_A = 0°C to 70°C			5.95	
	0.5V step, T_A = –40°C to +85°C			6.0	
Settling time[2]	G = +2, 1V step, to 0.1%		42	63	ns
	G = +2, 1V step, to 0.1%, T_A = 0°C to 70°C			65	
	G = +2, 1V step, to 0.1%, T_A = –40°C to +85°C			66	

6.5 Electrical Characteristics for D Package V_S = ±5V (続き)

at T_A = 25°C(1), G = +2, R_F = 750Ω, R_L = 150Ω to ground, and R_{SRC} = 375Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Harmonic distortion(2)	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω		–67	–59	dBc
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω, T_A = 0°C to 70°C			–57	
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω, T_A = –40°C to +85°C			–56	
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω		–71	–62	
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω, T_A = 0°C to 70°C			–61	
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω, T_A = –40°C to +85°C			–60	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω		–60	–50	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω, T_A = 0°C to 70°C			–49	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω, T_A = –40°C to +85°C			–48	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω		–77	–65	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω, T_A = 0°C to 70°C			–62	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω, T_A = –40°C to +85°C			–59	
Input voltage noise(2)	f > 1MHz		9.5	10.5	nV/√Hz
	f > 1MHz, T_A = 0°C to 70°C			11.0	
	f > 1MHz, T_A = –40°C to +85°C			11.5	
Input current noise(2)	f > 1MHz		3.7	4.7	pA/√Hz
	f > 1MHz, T_A = 0°C to 70°C			5.2	
	f > 1MHz, T_A = –40°C to +85°C			5.7	
NTSC differential gain			0.07		%
NTSC differential phase			0.17		°
DC PERFORMANCE					
Open-loop voltage gain	V_O = ±1V	66	74		dB
	V_O = ±1V, T_A = 0°C to 70°C	65			
	V_O = ±1V, T_A = –40°C to +85°C	64			
Input offset voltage			±1.5	±7	mV
	T_A = 0°C to 70°C			±8.1	
	T_A = –40°C to +85°C			±8.6	
Average offset voltage drift(2)	T_A = –40°C to +85°C			±25	µV/°C
Input bias current	V_{CM} = 0V		+5	+10	µA
	V_{CM} = 0V, T_A = 0°C to 70°C			+12	
	V_{CM} = 0V, T_A = –40°C to +85°C			+13	
Input bias current drift(2)	V_{CM} = 0V, T_A = –40°C to +85°C			±12	nA/°C
Input offset current	V_{CM} = 0V		±0.1	±1	µA
	V_{CM} = 0V, T_A = 0°C to 70°C			±1.2	
	V_{CM} = 0V, T_A = –40°C to +85°C			±1.4	
Input offset current drift(2)	V_{CM} = 0V, T_A = –40°C to +85°C			±5	nA/°C

6.5 Electrical Characteristics for D Package V_S = ±5V (続き)

at T_A = 25°C(1), G = +2, R_F = 750Ω, R_L = 150Ω to ground, and R_{SRC} = 375Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Negative input voltage(3)			–5.5	–5.4	V
	T_A = 0°C to 70°C			–5.3	
	T_A = –40°C to +85°C			–5.2	
Positive input voltage(3)		3.1	3.2		V
	T_A = 0°C to 70°C	3.0			
	T_A = –40°C to +85°C	2.9			
Common-mode rejection ratio, CMRR	Input-referred	76	80		dB
	Input-referred, T_A = 0°C to 70°C	74			
	Input-referred, T_A = –40°C to +85°C	72			
Input impedance	Differential		10 || 2.1		kΩ || pF
	Common-mode		400 || 1.2		
OUTPUT					
Output voltage swing	R_L = 1kΩ to ground	±4.86	±4.88		V
	R_L = 1kΩ to ground, T_A = 0°C to 70°C	±4.85			
	R_L = 1kΩ to ground, T_A = –40°C to +85°C	±4.84			
	R_L = 150Ω to ground	±4.60	±4.64		
	R_L = 150Ω to ground, T_A = 0°C to 70°C	±4.58			
	R_L = 150Ω to ground, T_A = –40°C to +85°C	±4.56			
Current output, sinking and sourcing	Output shorted to ground	±65	±85		mA
	Output shorted to ground, T_A = 0°C to 70°C	±60			
	Output shorted to ground, T_A = –40°C to +85°C	±55			
Short-circuit current	Output shorted to ground		150		mA
Closed-loop output impedance	G = +2, f ≤ 100kHz		0.06		Ω
POWER SUPPLY					
Quiescent current		4	4.25	4.7	mA
	T_A = 0°C to 70°C	3.6		5.3	
	T_A = –40°C to +85°C	3.3		5.9	
Power-supply rejection ratio, +PSRR	Input-referred	61	66		dB
	Input-referred, T_A = 0°C to 70°C	60			
	Input-referred, T_A = –40°C to +85°C	59			

(1) Junction temperature = ambient for 25°C specifications.
(2) Limits set by characterization and simulation.
(3) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

6.6 Electrical Characteristics for D Package V_S = 5V

at T_A = 25°C[1], G = +2, R_F = 750Ω, and R_L = 150Ω to ground (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE					
Small-signal bandwidth	G = +1, V_O ≤ 0.2V_{PP}		250		MHz
Small-signal bandwidth[2]	G = +2, V_O ≤ 0.2V_{PP}	72	110		
	G = +2, V_O ≤ 0.2V_{PP}, T_A = 0°C to 70°C	70			
	G = +2, V_O ≤ 0.2V_{PP}, T_A = –40°C to +85°C	68			
	G = +5, V_O ≤ 0.2V_{PP}	17	24		
	G = +5, V_O ≤ 0.2V_{PP}, T_A = 0°C to 70°C	16			
	G = +5, V_O ≤ 0.2V_{PP}, T_A = –40°C to +85°C	15			
	G = +10, V_O ≤ 0.2V_{PP}	8	11		
	G = +10, V_O ≤ 0.2V_{PP}, T_A = 0°C to 70°C	7			
	G = +10, V_O ≤ 0.2V_{PP}, T_A = –40°C to +85°C	6			
Gain bandwidth product[2]	G ≥ +10	84	110		MHz
	G ≥ +10, T_A = 0°C to 70°C	80			
	G ≥ +10, T_A = –40°C to +85°C	79			
Peaking at a gain of +1	V_O ≤ 0.2V_{PP}		5		dB
Slew rate[2]	G = +2, 2V step	280	550		V/µs
	G = +2, 2V step, T_A = 0°C to 70°C	270			
	G = +2, 2V step, T_A = –40°C to +85°C	260			
Rise time[2]	0.5V step		3.3	5.7	ns
	0.5V step, T_A = 0°C to 70°C			5.8	
	0.5V step, T_A = –40°C to +85°C			5.9	
Fall time[2]	0.5V step		3.3	5.7	ns
	0.5V step, T_A = 0°C to 70°C			5.8	
	0.5V step, T_A = –40°C to +85°C			5.9	
Settling time[2]	G = +2, 1V step, to 0.1%		43	64	ns
	G = +2, 1V step, to 0.1%, T_A = 0°C to 70°C			66	
	G = +2, 1V step, to 0.1%, T_A = –40°C to +85°C			67	

6.6 Electrical Characteristics for D Package V_S = 5V (続き)

at T_A = 25°C[1], G = +2, R_F = 750Ω, and R_L = 150Ω to ground (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Harmonic distortion[2]	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω		–62	–55	dBc
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω, T_A = 0°C to 70°C			–54	
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω, T_A = –40°C to +85°C			–53	
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω		–64	–58	
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω, T_A = 0°C to 70°C			–57	
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω, T_A = –40°C to +85°C			–56	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω		–58	–50	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω, T_A = 0°C to 70°C			–49	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω, T_A = –40°C to +85°C			–48	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω		–84	–66	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω, T_A = 0°C to 70°C			–63	
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω, T_A = –40°C to +85°C			–60	
Input voltage noise[2]	f > 1MHz		9.2	10.2	nV/√Hz
	f > 1MHz, T_A = 0°C to 70°C			10.7	
	f > 1MHz, T_A = –40°C to +85°C			11.2	
Input current noise[2]	f > 1MHz		3.5	4.5	pA/√Hz
	f > 1MHz, T_A = 0°C to +70°C			5.0	
	f > 1MHz, T_A = –40°C to +85°C			5.5	
NTSC differential gain[2]			0.08		%
NTSC differential phase[2]			0.09		°
DC PERFORMANCE					
Open-loop voltage gain	V_O = ±1V	66	72		dB
	V_O = ±1V, T_A = 0°C to 70°C	65			
	V_O = ±1V, T_A = –40°C to +85°C	64			
Input offset voltage			±0.5	±5.0	mV
	T_A = 0°C to 70°C			±6.0	
	T_A = –40°C to +85°C			±6.5	
Average offset voltage drift[2]	T_A = –40°C to +85°C			±20	µV/°C
Input bias current	V_{CM} = 2.5V		+5	+10	µA
	V_{CM} = 2.5V, T_A = 0°C to 70°C			+12	
	V_{CM} = 2.5V, T_A = –40°C to +85°C			+13	
Input bias current drift[2]	V_{CM} = 2.5V, T_A = –40°C to +85°C			±12	nA/°C
Input offset current	V_{CM} = 2.5V		±0.1	±0.8	µA
	V_{CM} = 2.5V, T_A = 0°C to 70°C			±1.2	
	V_{CM} = 2.5V, T_A = –40°C to +85°C			±1.2	
Input offset current drift[2]	V_{CM} = 2.5V, T_A = –40°C to +85°C			±5	nA/°C

6.6 Electrical Characteristics for D Package V_S = 5V (続き)

at T_A = 25°C(1), G = +2, R_F = 750Ω, and R_L = 150Ω to ground (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Negative input voltage(3)			–0.5	–0.4	V
	T_A = 0°C to 70°C			–0.3	
	T_A = –40°C to +85°C			–0.2	
Positive input voltage(3)		3.1	3.2		V
	T_A = 0°C to 70°C	3.0			
	T_A = –40°C to +85°C	2.9			
Common-mode rejection ratio, CMRR	Input-referred	76	80		dB
	Input-referred, T_A = 0°C to 70°C	74			
	Input-referred, T_A = –40°C to +85°C	72			
Input impedance	Differential		10 || 2.1		kΩ || pF
	Common-mode		400 || 1.2		
OUTPUT					
Output voltage swing low	G = +5, R_L = 1kΩ to 2.5V		0.09	0.11	V
	G = +5, R_L = 1kΩ to 2.5V, T_A = 0°C to 70°C			0.12	
	G = +5, R_L = 1kΩ to 2.5V, T_A = –40°C to +85°C			0.13	
	G = +5, R_L = 150Ω to 2.5V		0.21	0.24	
	G = +5, R_L = 150Ω to 2.5V, T_A = 0°C to 70°C			0.25	
	G = +5, R_L = 150Ω to 2.5V, T_A = –40°C to +85°C			0.26	
Output voltage swing high	G = +5, R_L = 1kΩ to 2.5V	4.89	4.91		V
	G = +5, R_L = 1kΩ to 2.5V, T_A = 0°C to 70°C	4.87			
	G = +5, R_L = 1kΩ to 2.5V, T_A = –40°C to +85°C	4.87			
	G = +5, R_L = 150Ω to 2.5V	4.75	4.78		
	G = +5, R_L = 150Ω to 2.5V, T_A = 0°C to 70°C	4.73			
	G = +5, R_L = 150Ω to 2.5V, T_A = –40°C to +85°C	4.72			
Current output, sinking and sourcing		±60	±80		mA
	T_A = 0°C to 70°C	±55			
	T_A = –40°C to +85°C	±52			
Short-circuit output current	Output shorted to either supply		140		mA
Closed-loop output impedance	G = +2, f ≤ 100kHz		0.06		Ω
POWER SUPPLY					
Quiescent current		3.7	3.9	4.1	mA
	T_A = 0°C to 70°C	3.1		4.8	
	T_A = –40°C to +85°C	3.1		5.5	
Power-supply rejection ratio, PSRR	Input-referred	61	66		dB
	Input-referred, T_A = 0°C to 70°C	60			
	Input-referred, T_A = –40°C to +85°C	59			

(1) Junction temperature = ambient for 25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +18°C at high temperature limit for over temperature specifications.
(3) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

6.7 Electrical Characteristics for D Package V_S = 3V

at T_A = 25°C[1], G = +2, R_F = 750Ω, and R_L = 150Ω to V_S/3, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE					
Small-signal bandwidth[2]	G = +2, V_O ≤ 0.2V_{PP}	72	100		MHz
	G = +2, V_O ≤ 0.2V_{PP}, T_A = 0°C to 70°C	68			
	G = +5, V_O ≤ 0.2V_{PP}	17	22		
	G = +5, V_O ≤ 0.2V_{PP}, T_A = 0°C to 70°C	16			
	G = +10, V_O ≤ 0.2V_{PP}	8	10		
	G = +10, V_O ≤ 0.2V_{PP}, T_A = 0°C to 70°C	7			
Gain bandwidth product[2]	G ≥ +10	80	100		MHz
	G ≥ +10, T_A = 0°C to 70°C	76			
Slew rate[2]	1V step	140	225		V/µs
	1V step, T_A = 0°C to 70°C	110			
Rise time[2]	0.5V step		3.3	5.5	ns
	0.5V step, T_A = 0°C to 70°C			5.6	
Fall time[2]	0.5V step		3.3	5.5	ns
	0.5V step, T_A = 0°C to 70°C			5.6	
Settling time[2]	1V step, to 0.1%		45	72	ns
	1V step, to 0.1%, T_A = 0°C to 70°C			87	
Harmonic distortion[2]	2nd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L = 150Ω		–67	–61	dBc
	2nd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L = 150Ω, T_A = 0°C to +70°C			–59	
	2nd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L ≥ 500Ω		–67	–61	
	2nd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L ≥ 500Ω, T_A = 0°C to +70°C			–59	
	3rd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L = 150Ω		–66	–59	
	3rd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L = 150Ω, T_A = 0°C to +70°C			–58	
	3rd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L ≥ 500Ω		–77	–59	
	3rd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L ≥ 500Ω, T_A = 0°C to +70°C			–58	
Input voltage noise[2]	f > 1MHz		9.2	10.2	nV/√Hz
	f > 1MHz, T_A = 0°C to 70°C			10.7	
Input current noise[2]	f > 1MHz		3.5	4.5	pA/√Hz
	f > 1MHz, T_A = 0°C to 70°C			5.0	
DC PERFORMANCE					
Open-loop voltage gain	V_O = ±0.5V	66	72		dB
	V_O = ±0.5V, T_A = 0°C to 70°C	65			
Input offset voltage			±1.5	±7	mV
	T_A = 0°C to 70°C			±8.1	
Average offset voltage drift[2]	T_A = 0°C to 70°C			±25	µV/°C
Input bias current	V_{CM} = 1V		+5	+10	µA
	V_{CM} = 1V, T_A = 0°C to 70°C			+12	
Input bias current drift[2]	T_A = 0°C to 70°C			±12	nA/°C
Input offset current	V_{CM} = 1V		±0.1	±1	µA
	V_{CM} = 1V, T_A = 0°C to 70°C			±1.2	
Input offset current drift[2]	T_A = 0°C to 70°C			±5	nA/°C

6.7 Electrical Characteristics for D Package V_S = 3V (続き)

at T_A = 25°C(1), G = +2, R_F = 750Ω, and R_L = 150Ω to V_S/3, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Negative input voltage(3)			–0.45	–0.4	V
	T_A = 0°C to 70°C			–0.27	
Positive input voltage(3)		1.1	1.2		
	T_A = 0°C to 70°C	1.0			
Common-mode rejection ratio, CMRR	Input-referred	75	80		dB
	Input-referred, T_A = 0°C to 70°C	73			
Input impedance	Differential		10 || 2.1		kΩ || pF
	Common-mode		400 || 1.2		
OUTPUT					
Output voltage swing low	G = +5, R_L = 1kΩ to 1.5V		0.08	0.11	V
	G = +5, R_L = 1kΩ to 1.5V, T_A = 0°C to 70°C			0.125	
	G = +5, R_L = 150Ω to 1.5V		0.17	0.39	
	G = +5, R_L = 150Ω to 1.5V, T_A = 0°C to 70°C			0.40	
Output voltage swing high	G = +5, R_L = 1kΩ to 1.5V	2.88	2.91		V
	G = +5, R_L = 1kΩ to 1.5V, T_A = 0°C to 70°C	2.85			
	G = +5, R_L = 150Ω to 1.5V	2.74	2.82		
	G = +5, R_L = 150Ω to 1.5V, T_A = 0°C to 70°C	2.70			
Current output, sinking and sourcing		±20	±30		mA
	T_A = 0°C to 70°C	±18			
Short-circuit output current	Output shorted to either supply		45		
Closed-loop output impedance	G = +2, f ≤ 100kHz		0.06		Ω
POWER SUPPLY					
Quiescent current		3.3	3.7	4	mA
	T_A = 0°C to 70°C	3.1		4.7	
Power-supply rejection ratio, PSRR	Input-referred, 0.3V step	60	64		dB
	Input-referred, T_A = 0°C to 70°C	58			

(1) Junction temperature = ambient for 25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +18°C at high temperature limit for over temperature specifications.
(3) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

6.8 Electrical Characteristics for DBV Package V_S = ±5V

at T_A = 25°C[1], G = +2, R_F = 750Ω, R_L = 150Ω to ground, and R_{SRC} = 375Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE					
Small-signal bandwidth	G = +1, V_O ≤ 0.2V_{PP}		310		MHz
	G = +2, V_O ≤ 0.2V_{PP}		100		
	G = +5, V_O ≤ 0.2V_{PP}		30		
	G = +10, V_O ≤ 0.2V_{PP}		13		
Gain bandwidth product	G ≥ +10		110		MHz
Peaking at a gain of +1	V_O ≤ 0.2V_{PP}		1		dB
Slew rate	2V step, 20% to 80%		640		V/µs
Rise time	0.5V step, 10% to 90%		3.3	5.8	ns
Fall time	0.5V step, 10% to 90%		3.5	5.9	ns
Settling time	1V step, to 0.1%		42	63	ns
Harmonic distortion	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω		–77		dBc
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω		–78		
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω		–78		
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω		–77		
Input voltage noise	f > 1MHz		5.6	10.5	nV/√Hz
	f > 1MHz, T_A = –40°C to +85°C			11.5	
Input current noise	f > 1MHz		4	5.4	pA/√Hz
	f > 1MHz, T_A = –40°C to +85°C			6.4	
DC PERFORMANCE					
Open-loop voltage gain	V_O = ±1V	66	74		dB
	V_O = ±1V, T_A = –40°C to +85°C	64			
Input offset voltage			±1.5	±7	mV
	T_A = –40°C to +85°C			±8.6	
Average offset voltage drift	T_A = –40°C to +85°C			±25	µV/°C
Input bias current	V_{CM} = 0V		5	18	µA
	V_{CM} = 0V, T_A = –40°C to +85°C			19	
Input bias current drift	V_{CM} = 0V, T_A = –40°C to +85°C			±12	nA/°C
Input offset current	V_{CM} = 0V		±0.1	±1	µA
	V_{CM} = 0V, T_A = –40°C to +85°C			±1.4	
Input offset current drift	V_{CM} = 0V, T_A = –40°C to +85°C			±5	nA/°C
INPUT					
Negative input voltage[2]			–5.5	–5.4	V
	T_A = –40°C to +85°C			–5.2	
Positive input voltage[2]		3.1	3.2		V
	T_A = –40°C to +85°C	2.9			
Common-mode rejection ratio, CMRR	Input-referred	76	80		dB
	Input-referred, T_A = –40°C to +85°C	72			
Input impedance	Differential		10 || 2.1		kΩ || pF
	Common-mode		400 || 1.2		

6.8 Electrical Characteristics for DBV Package V_S = ±5V (続き)

at T_A = 25°C(1), G = +2, R_F = 750Ω, R_L = 150Ω to ground, and R_{SRC} = 375Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT					
Output voltage swing	R_L = 1kΩ to ground	±4.86	±4.88		V
	R_L = 1kΩ to ground, T_A = –40°C to +85°C	±4.84			
	R_L = 150Ω to ground	±4.60	±4.64		
	R_L = 150Ω to ground, T_A = –40°C to +85°C	±4.56			
Current output, sinking and sourcing	V_O = ±2.75V, V_{OS} = 20mV	±65	±85		mA
	V_O = ±2.75V, V_{OS} = 20mV, T_A = –40°C to +85°C	±55			
Short-circuit current	Output shorted to ground		120		mA
Closed-loop output impedance	G = +2, f ≤ 100kHz		0.03		Ω
POWER SUPPLY					
Quiescent current			4.5		mA
	T_A = –40°C to +85°C	3.1		6.1	
Power-supply rejection ratio, PSRR	Input-referred	61	66		dB
	Input-referred , T_A = –40°C to +85°C	59			

(1) Junction temperature = ambient for 25°C specifications.
(2) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

6.9 Electrical Characteristics for DBV Package V_S = 5V

at T_A = 25°C[1], G = +2, R_F = 750Ω, and R_L = 150Ω to ground (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE					
Small-signal bandwidth	G = +1, V_O ≤ 0.2V_{PP}		250		MHz
	G = +2, V_O ≤ 0.2V_{PP}		100		
	G = +5, V_O ≤ 0.2V_{PP}		30		
	G = +10, V_O ≤ 0.2V_{PP}		13		
Gain bandwidth product	G ≥ +10		130		MHz
Peaking at a gain of +1	V_O ≤ 0.2V_{PP}		2		dB
Slew rate	2V step, 20% to 80%		550		V/µs
Rise time	0.5V step, 10% to 90%		3.3	5.7	ns
Fall time	0.5V step, 10% to 90%		3.3	5.7	ns
Settling time	G = +2, 1V step, to 0.1%		43	64	ns
Harmonic distortion	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω		–69		dBc
	2nd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω		–71		
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L = 150Ω		–69		
	3rd-harmonic, V_O = 2V_{PP}, f = 5MHz, R_L ≥ 500Ω		–78		
Input voltage noise	f > 1MHz		5.8	10.2	nV/√Hz
	f > 1MHz, T_A = –40°C to +85°C			11.2	
Input current noise	f > 1MHz		4	5.4	pA/√Hz
	f > 1MHz, T_A = –40°C to +85°C			6.4	
DC PERFORMANCE					
Open-loop voltage gain	V_O = ±1V	66	72		dB
	V_O = ±1V, T_A = –40°C to +85°C	64			
Input offset voltage			±0.5	±5.0	mV
	T_A = –40°C to +85°C			±6.5	
Average offset voltage drift	T_A = –40°C to +85°C			±20	µV/°C
Input bias current	V_{CM} = 0V		+15	+18	µA
	V_{CM} = 0V, T_A = –40°C to +85°C			+19	
Input bias current drift	V_{CM} = 0V, T_A = –40°C to +85°C			±12	nA/°C
Input offset current	V_{CM} = 0V		±0.1	±0.8	µA
	V_{CM} = 0V, T_A = –40°C to +85°C			±1.2	
Input offset current drift	V_{CM} = 0V, T_A = –40°C to +85°C			±5	nA/°C
INPUT					
Negative input voltage[2]			–0.5	–0.4	V
	T_A = –40°C to +85°C			–0.2	
Positive input voltage[2]		3.1	3.2		V
	T_A = –40°C to +85°C	2.9			
Common-mode rejection ratio, CMRR	Input-referred	76	80		dB
	Input-referred, T_A = –40°C to +85°C	72			
Input impedance	Differential		10 || 2.1		kΩ || pF
	Common-mode		400 || 1.2		

6.9 Electrical Characteristics for DBV Package V_S = 5V (続き)

at T_A = 25°C(1), G = +2, R_F = 750Ω, and R_L = 150Ω to ground (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT					
Output voltage swing low	G = +5, R_L = 1kΩ to 2.5V		0.09	0.11	V
	G = +5, R_L = 1kΩ to 2.5V, T_A = –40°C to +85°C			0.13	
	G = +5, R_L = 150Ω to 2.5V		0.21	0.24	
	G = +5, R_L = 150Ω to 2.5V, T_A = –40°C to +85°C			0.26	
Output voltage swing high	G = +5, R_L = 1kΩ to 2.5V	4.89	4.91		V
	G = +5, R_L = 1kΩ to 2.5V, T_A = –40°C to +85°C	4.87			
	G = +5, R_L = 150Ω to 2.5V	4.75	4.78		
	G = +5, R_L = 150Ω to 2.5V, T_A = –40°C to +85°C	4.72			
Current output, sinking and sourcing	V_O = ±0.88V, V_{OS} = 20mV	±60	±80		mA
	V_O = ±0.88V, V_{OS} = 20mV, T_A = –40°C to +85°C	±52			
Short-circuit output current	Output shorted to either supply		140		mA
Closed-loop output impedance	G = +2, f ≤ 100kHz		0.06		Ω
POWER SUPPLY					
Quiescent current		3.7	4.4	5	mA
	T_A = –40°C to +85°C	3.1		5.7	
Power-supply rejection ratio, PSRR	Input-referred	61	66		dB
	Input-referred, T_A = –40°C to +85°C	59			

(1) Junction temperature = ambient for 25°C specifications.
(2) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

6.10 Electrical Characteristics for DBV Package V_S = 3V

at T_A = 25°C[1], G = +2, R_F = 750Ω, and R_L = 150Ω to V_S/3, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE					
Small-signal bandwidth	G = +2, V_O ≤ 0.2V_{PP}		100		MHz
	G = +5, V_O ≤ 0.2V_{PP}		30		
	G = +10, V_O ≤ 0.2V_{PP}		13		
Gain bandwidth product	G ≥ +10		130		MHz
Slew rate	1V step, 20% to 80%		225		V/µs
Rise time	0.5V step, 10% to 90%		3.3	5.5	ns
Fall time	0.5V step, 10% to 90%		3.3	5.5	
Settling time	G = +2, 1V step, to 0.1%		45	72	
Harmonic distortion	2nd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L = 150Ω		–67		dBc
	2nd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L ≥ 500Ω		–67		
	3rd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L = 150Ω		–66		
	3rd-harmonic, V_O = 1V_{PP}, f = 5MHz, R_L ≥ 500Ω		–77		
Input voltage noise	f > 1MHz		5.8	10.2	nV/√Hz
	f > 1MHz, T_A = 0°C to 70°C			10.7	
Input current noise	f > 1MHz		4	5.2	pA/√Hz
	f > 1MHz, T_A = 0°C to 70°C			6	
DC PERFORMANCE					
Open-loop voltage gain	V_O = ±0.5V	66	72		dB
	V_O = ±0.5V, T_A = 0°C to 70°C	65			
Input offset voltage			±1.5	±7	mV
	T_A = 0°C to 70°C			±8.1	
Average offset voltage drift	T_A = 0°C to 70°C			±25	µV/°C
Input bias current	V_{CM} = 0V		14	18	µA
	V_{CM} = 0V, T_A = 0°C to 70°C			19	
Input bias current drift	V_{CM} = 0V, T_A = 0°C to 70°C			±12	nA/°C
Input offset current	V_{CM} = 0V		±0.1	±1	µA
	V_{CM} = 0V, T_A = 0°C to 70°C			±1.2	
Input offset current drift	V_{CM} = 0V, T_A = 0°C to 70°C			±5	nA/°C
INPUT					
Negative input voltage[2]			–0.45	–0.4	V
	T_A = 0°C to 70°C, 0.4V step			–0.27	
Positive input voltage[2]		1.1	1.2		
	T_A = 0°C to 70°C, 0.4V step	1.0			
Common-mode rejection ratio, CMRR	Input-referred	75	80		dB
	Input-referred, T_A = 0°C to 70°C	73			
Input impedance	Differential		10 || 2.1		kΩ || pF
	Common-mode		400 || 1.2		

6.10 Electrical Characteristics for DBV Package V_S = 3V (続き)

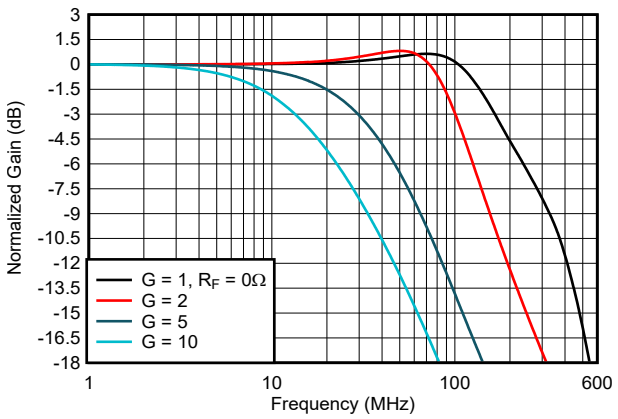
at T_A = 25°C(1), G = +2, R_F = 750Ω, and R_L = 150Ω to V_S/3, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT					
Output voltage swing low	G = +5, R_L = 1kΩ to 1.5V		0.08	0.11	V
	G = +5, R_L = 1kΩ to 1.5V, T_A = 0°C to 70°C			0.125	
	G = +5, R_L = 150Ω to 1.5V		0.17	0.39	
	G = +5, R_L = 150Ω to 1.5V, T_A = 0°C to 70°C			0.40	
Output voltage swing high	G = +5, R_L = 1kΩ to 1.5V	2.88	2.91		V
	G = +5, R_L = 1kΩ to 1.5V, T_A = 0°C to 70°C	2.85			
	G = +5, R_L = 150Ω to 1.5V	2.74	2.82		
	G = +5, R_L = 150Ω to 1.5V, T_A = 0°C to 70°C	2.70			
Current output, sinking and sourcing	V_O = ±0.125V, V_{OS} = 20mV	±20	±30		mA
	V_O = ±0.125V, V_{OS} = 20mV, T_A = 0°C to 70°C	±18			
Short-circuit output current	Output shorted to either supply		45		
Closed-loop output impedance	G = +2, f ≤ 100kHz		0.03		Ω
POWER SUPPLY					
Quiescent current		3.3	4.3	4.9	mA
	T_A = 0°C to 70°C	3.1		5.5	
Power-supply rejection ratio, PSRR	Input-referred	60	64		dB
	Input-referred, T_A = 0°C to 70°C	58			

(1) Junction temperature = ambient for 25°C specifications.
(2) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

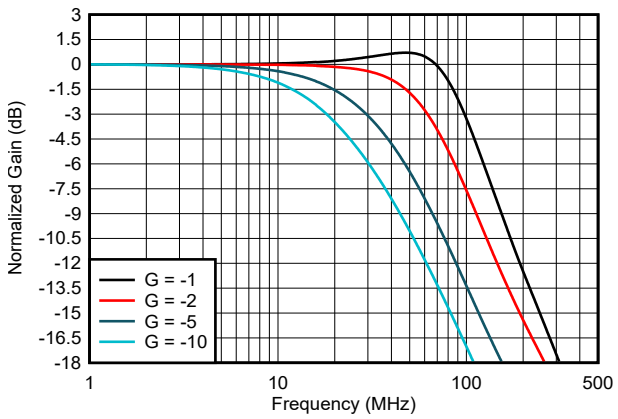
6.11 Typical Characteristics: V_S = ±5V

at T_A = 25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to GND (unless otherwise noted); see also 図 8-3



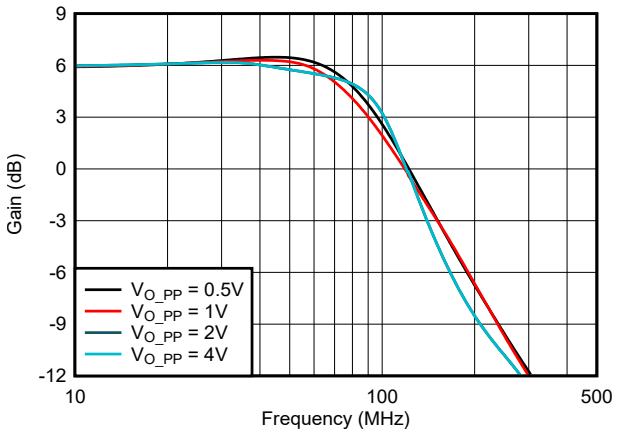
R_L = 150Ω V_O = 0.2V_{PP}

図 6-1. Noninverting Small-Signal Frequency Response



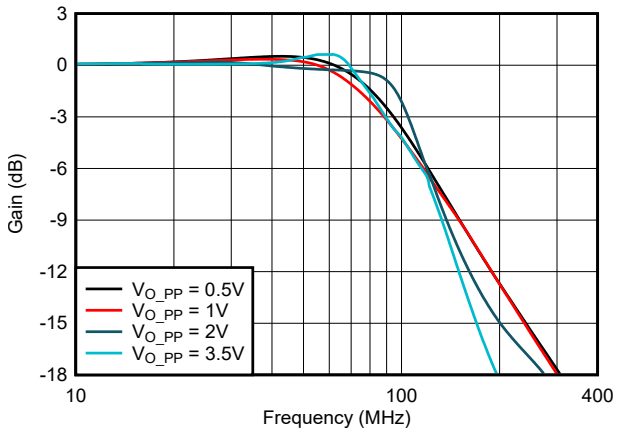
R_L = 150Ω V_O = 0.2V_{PP}

図 6-2. Inverting Small-Signal Frequency Response



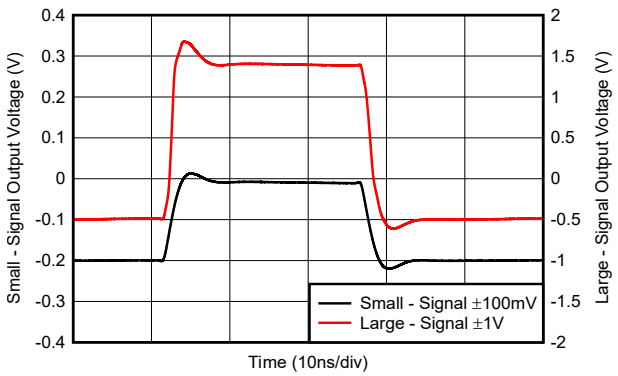
R_L = 150Ω G = +2V/V

図 6-3. Noninverting Large-Signal Frequency Response



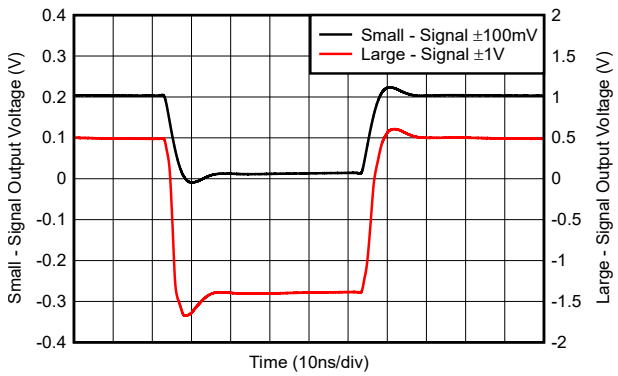
R_L = 150Ω G = -1V/V

図 6-4. Inverting Large-Signal Frequency Response



G = +2V/V

図 6-5. Noninverting Pulse Response

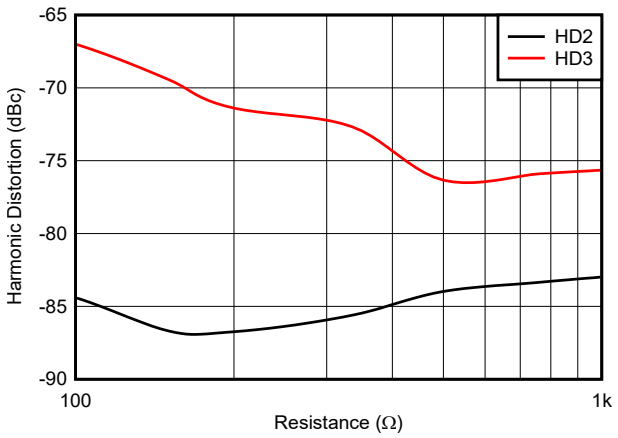


G = -1V/V

図 6-6. Inverting Pulse Response

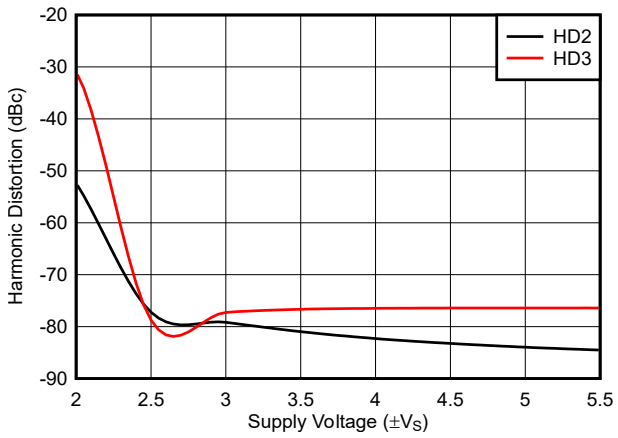
6.11 Typical Characteristics: V_S = ±5V (continued)

at T_A = 25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to GND (unless otherwise noted); see also 図 8-3



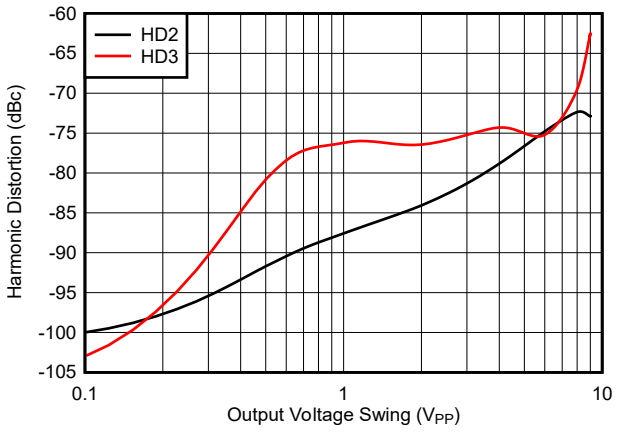
f = 5MHz V_O = 2V_{PP} G = +2V/V

図 6-7. Harmonic Distortion vs Load Resistance



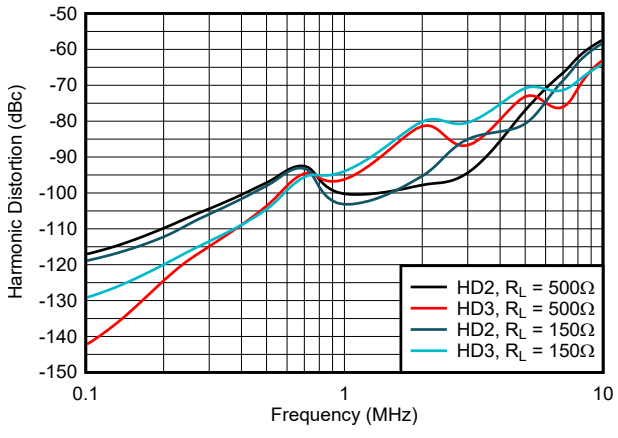
R_L = 500Ω V_O = 2V_{PP} G = +2V/V

図 6-8. 5MHz Harmonic Distortion vs Supply Voltage



f = 5MHz R_L = 500Ω G = +2V/V

図 6-9. Harmonic Distortion vs Output Voltage



V_O = 2V_{PP} G = +2V/V

図 6-10. Harmonic Distortion vs Frequency

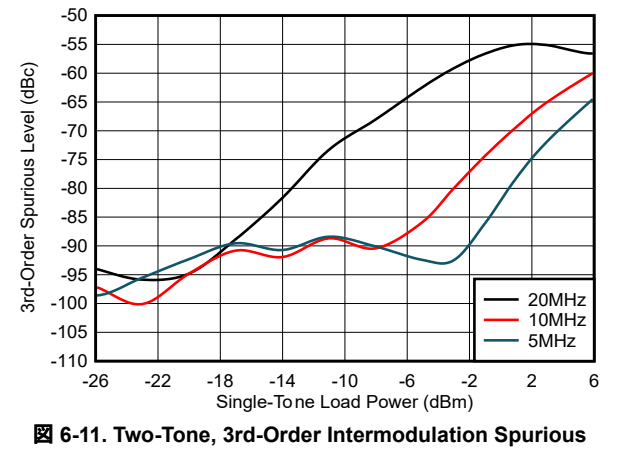


図 6-11. Two-Tone, 3rd-Order Intermodulation Spurious

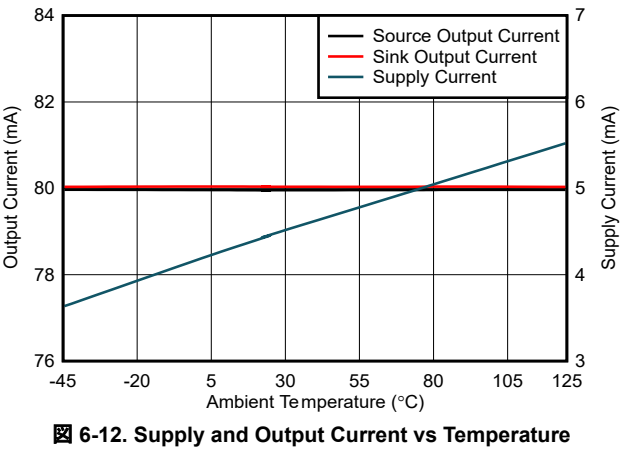


図 6-12. Supply and Output Current vs Temperature

6.11 Typical Characteristics: V_S = ±5V (continued)

at T_A = 25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to GND (unless otherwise noted); see also 図 8-3

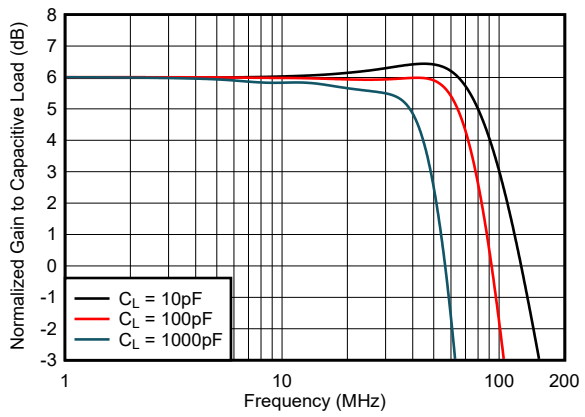


図 6-13. Frequency Response vs Capacitive Load

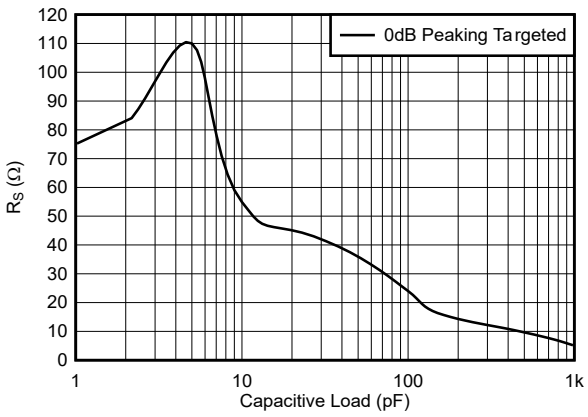


図 6-14. Recommended R_S vs Capacitive Load

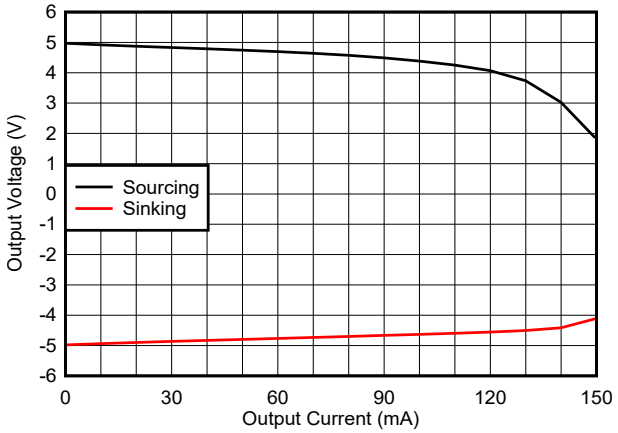


図 6-15. Output Voltage Swing vs Output Current

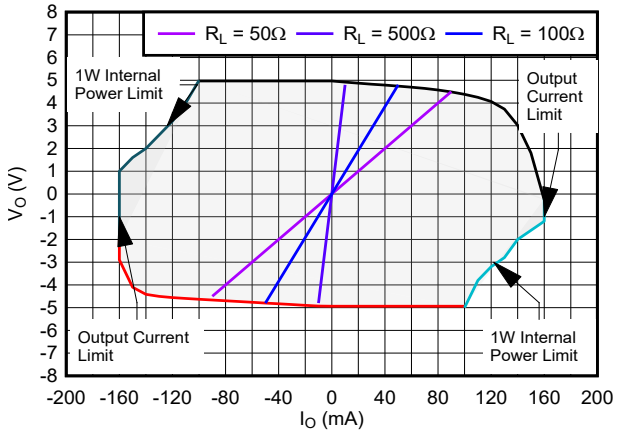


図 6-16. Output Voltage and Current Limitations

6.12 Typical Characteristics: V_S = ±5V, Differential Configuration

at T_A = 25°C, G_D = +2, R_F = 604Ω, and R_L = 500Ω (unless otherwise noted). Refer to 図 7-1

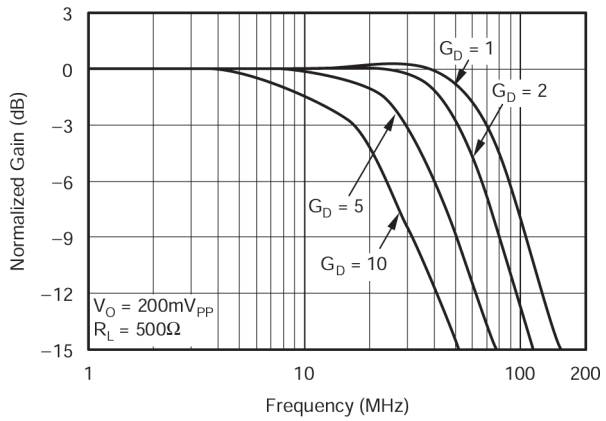


図 6-17. Differential Small-Signal Frequency Response

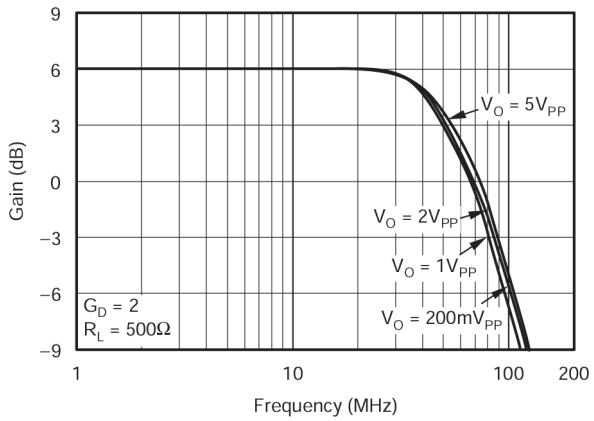


図 6-18. Differential Large-Signal Frequency Response

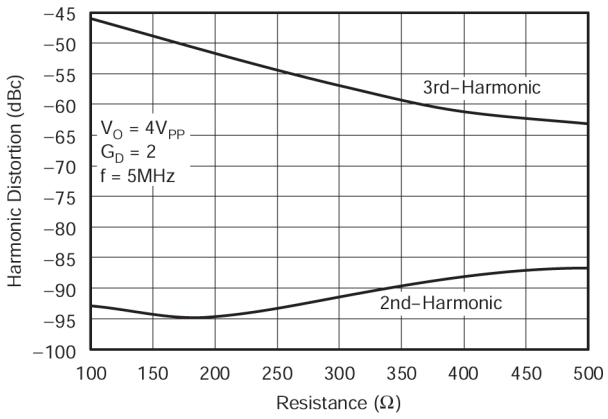


図 6-19. Differential Distortion vs Load Resistance

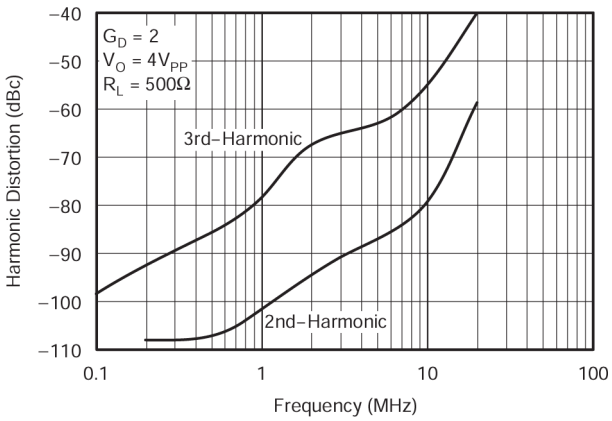


図 6-20. Differential Distortion vs Frequency

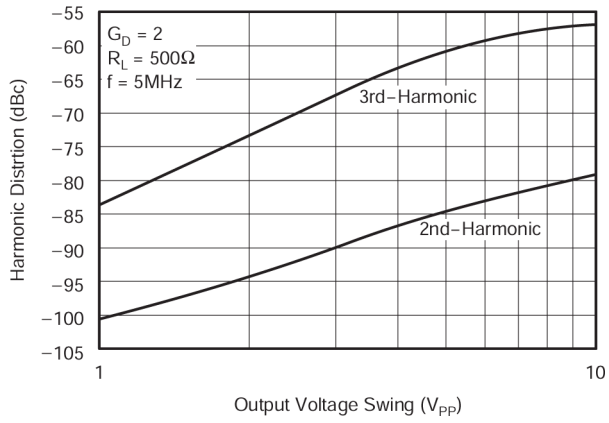
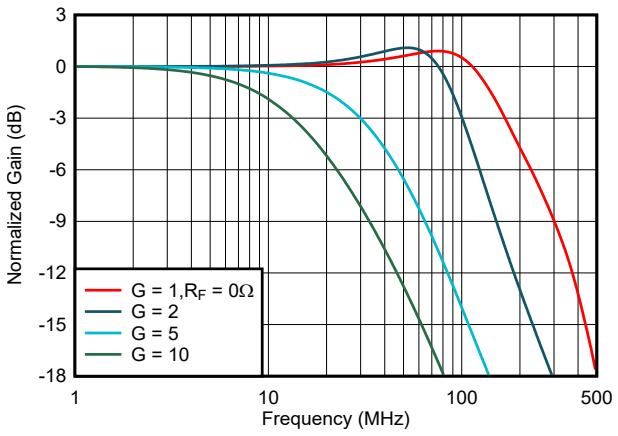


図 6-21. Differential Distortion vs Output Voltage

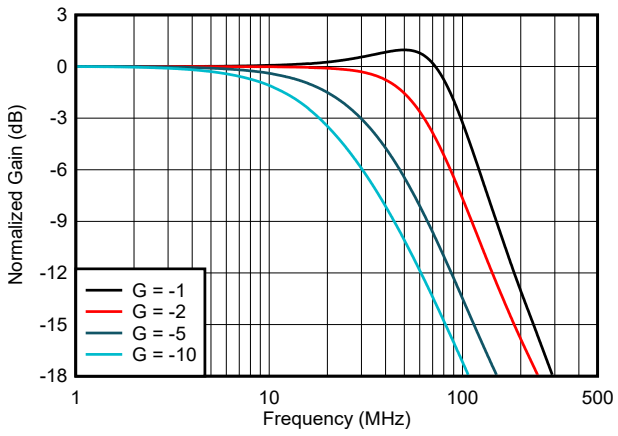
6.13 Typical Characteristics: V_S = 5V

at T_A = 25°C, G = +2, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V (unless otherwise noted); see also 図 8-1



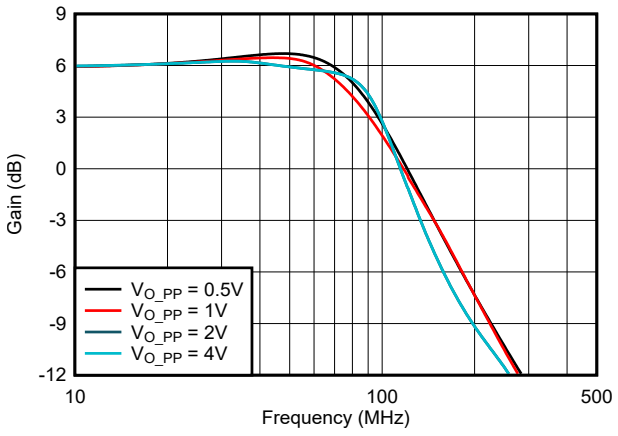
R_L = 150Ω V_O = 0.2V_{PP}

図 6-22. Noninverting Small-Signal Frequency Response



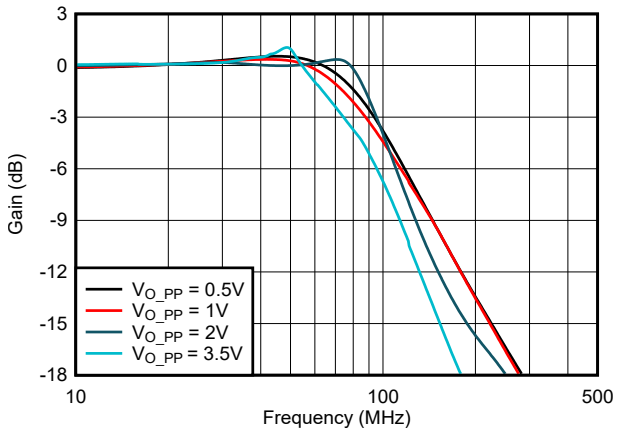
R_L = 150Ω V_O = 0.2V_{PP}

図 6-23. Inverting Small-Signal Frequency Response



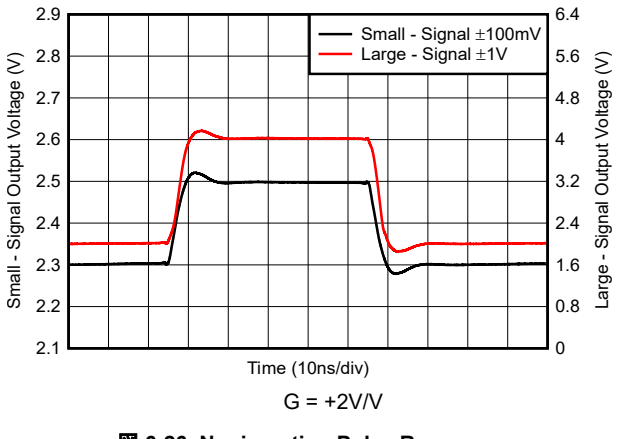
R_L = 150Ω G = +2V/V

図 6-24. Noninverting Large-Signal Frequency Response



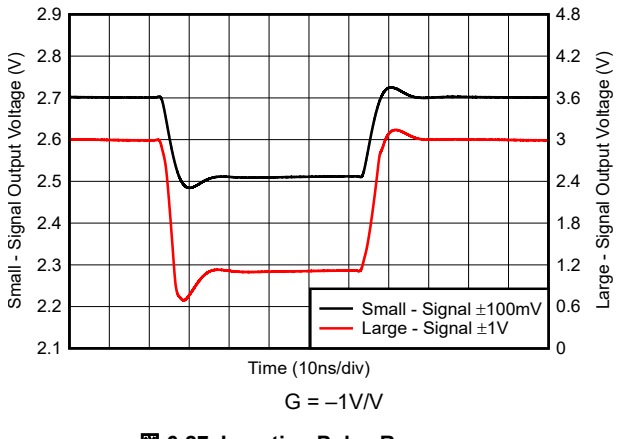
R_L = 150Ω G = –1V/V

図 6-25. Inverting Large-Signal Frequency Response



G = +2V/V

図 6-26. Noninverting Pulse Response

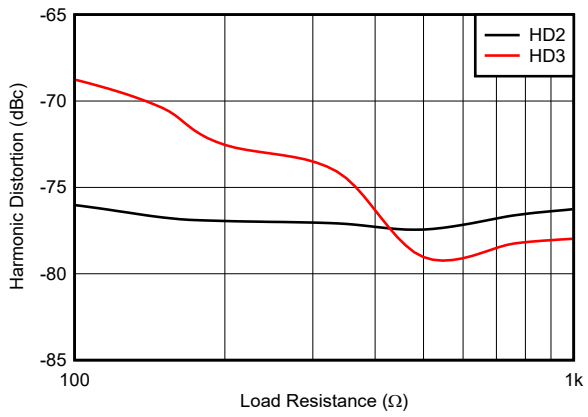


G = –1V/V

図 6-27. Inverting Pulse Response

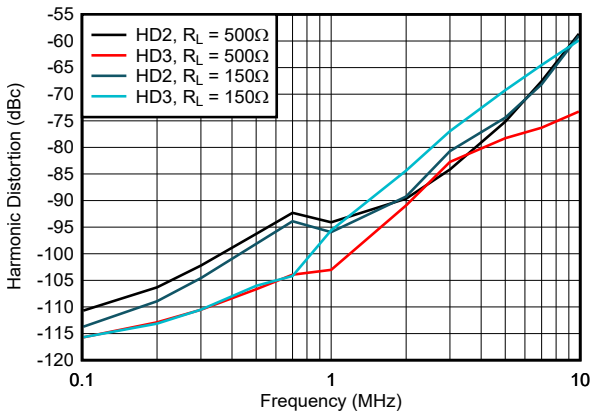
6.13 Typical Characteristics: V_S = 5V (continued)

at T_A = 25°C, G = +2, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V (unless otherwise noted); see also 図 8-1



f = 5MHz V_O = 2V_{PP} G = +2V/V

図 6-28. Harmonic Distortion vs Load Resistance



V_O = 2V_{PP} G = +2V/V

図 6-29. Harmonic Distortion vs Frequency

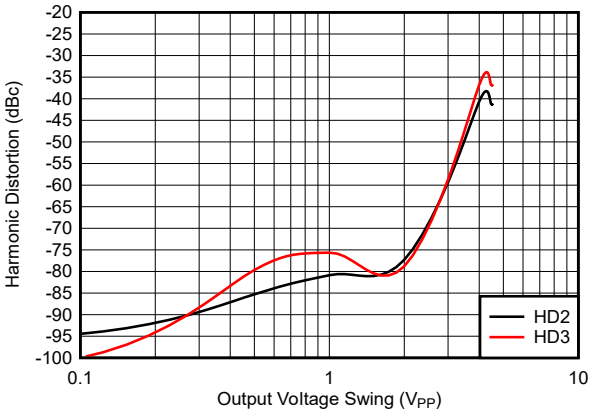
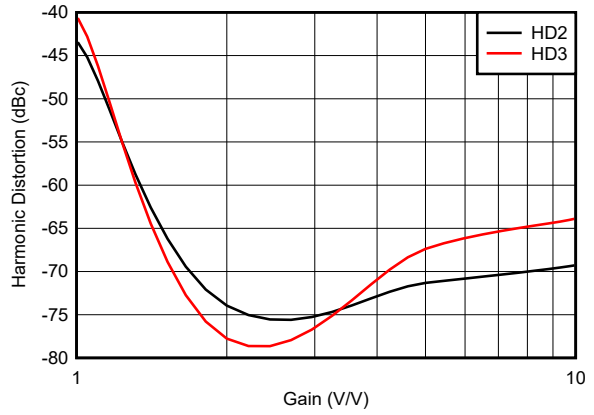
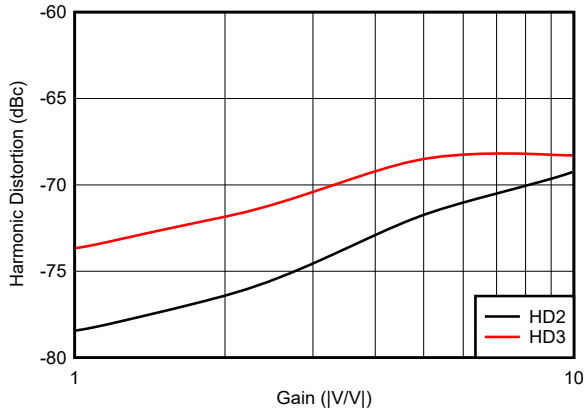


図 6-30. Harmonic Distortion vs Output Voltage



f = 5MHz R_L = 500Ω V_O = 2V_{PP}

図 6-31. Harmonic Distortion vs Non inverting Gain



f = 5MHz R_L = 500Ω V_O = 2V_{PP}

図 6-32. Harmonic Distortion vs Inverting Gain

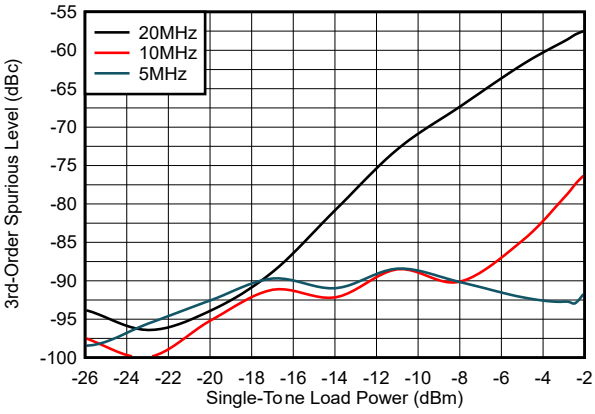


図 6-33. Two-Tone, 3rd-Order Intermodulation Spurious

6.13 Typical Characteristics: V_S = 5V (continued)

at T_A = 25°C, G = +2, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V (unless otherwise noted); see also 図 8-1

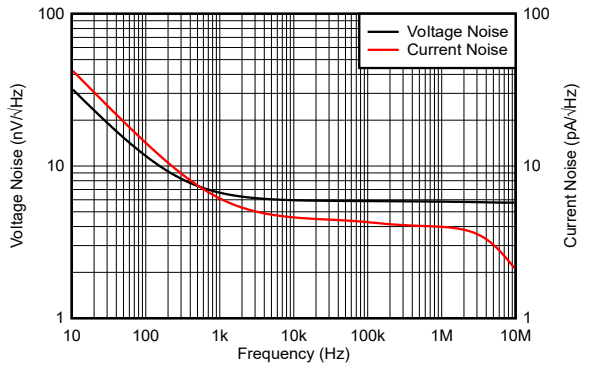


図 6-34. Input Voltage and Current Noise Density

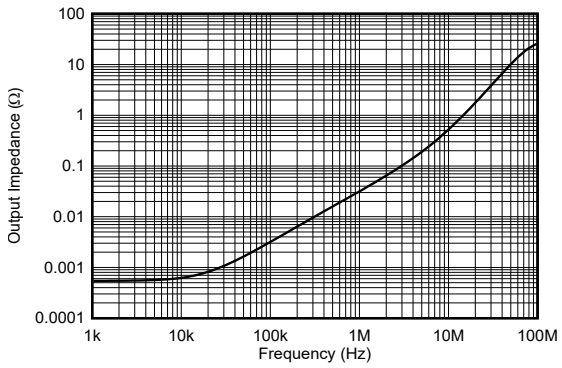


図 6-35. Closed-Loop Output Impedance vs Frequency

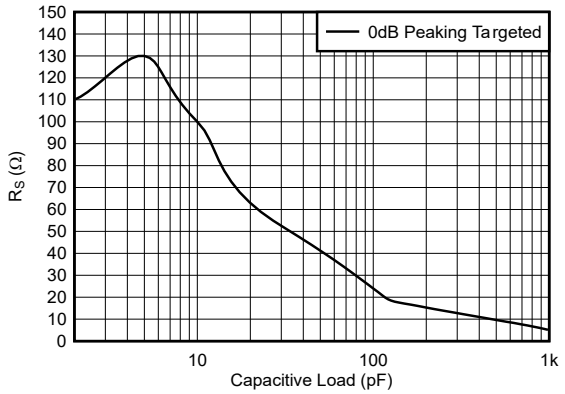


図 6-36. Recommended R_S vs Capacitive Load

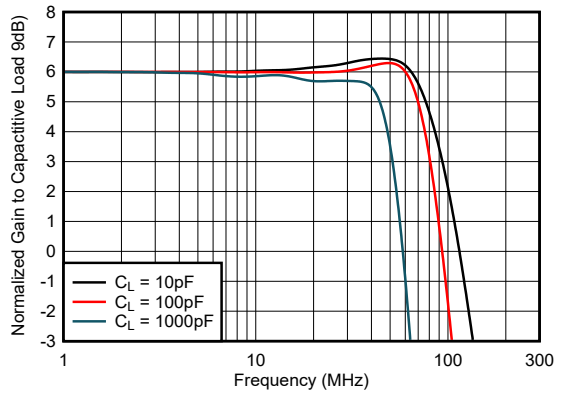


図 6-37. Frequency Response vs Capacitive Load

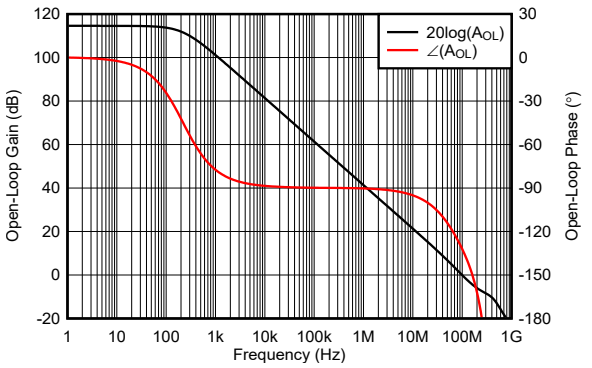


図 6-38. Open-Loop Gain and Phase

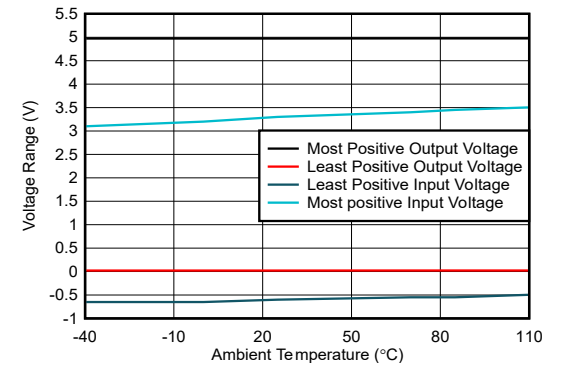


図 6-39. Voltage Ranges vs Temperature

6.13 Typical Characteristics: V_S = 5V (continued)

at T_A = 25°C, G = +2, R_F = 750Ω, R_L = 150Ω to V_S/2, and input V_{CM} = 2.5V (unless otherwise noted); see also 図 8-1

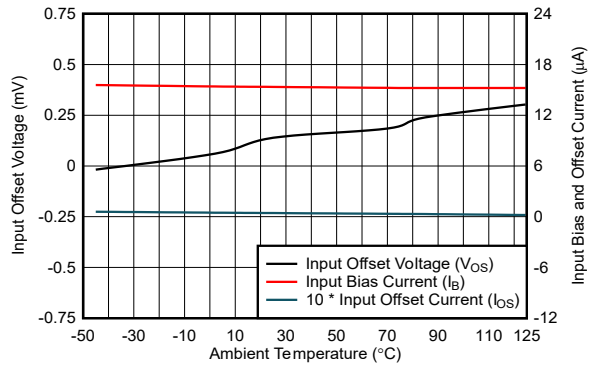


図 6-40. Typical DC Drift Over Temperature

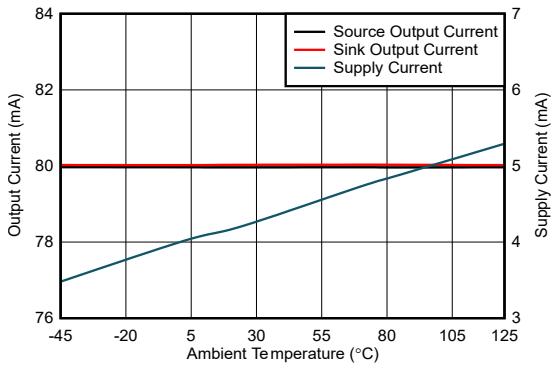


図 6-41. Supply and Output Current vs Temperature

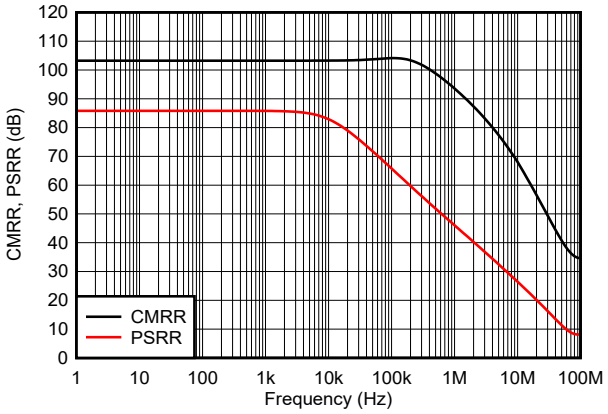


図 6-42. CMRR and PSRR vs Frequency

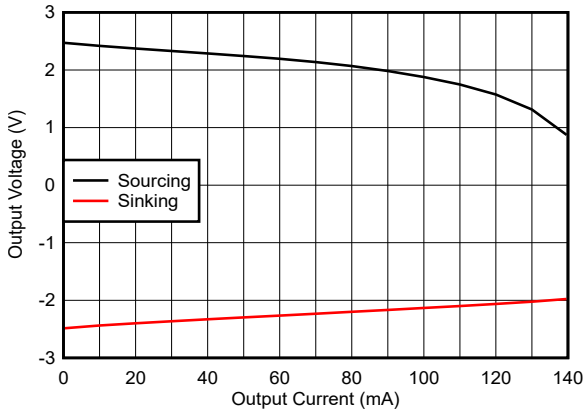


図 6-43. Output Voltage Swing vs Output Current

6.14 Typical Characteristics: V_S = 5V, Differential Configuration

at T_A = 25°C, G = +2, R_F = 604Ω, and R_L = 500Ω differential (unless otherwise noted). Refer to 図 7-2

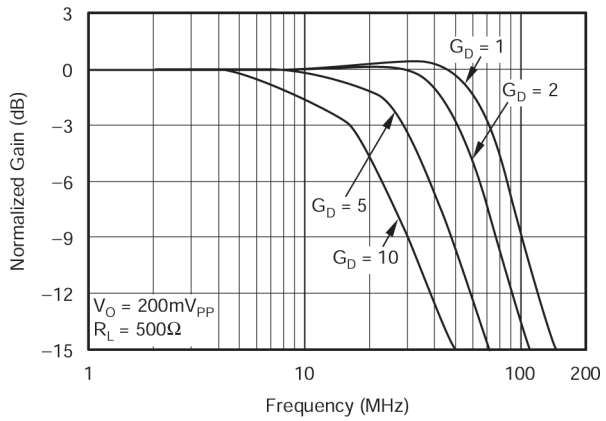


図 6-44. Differential Small-Signal Frequency Response

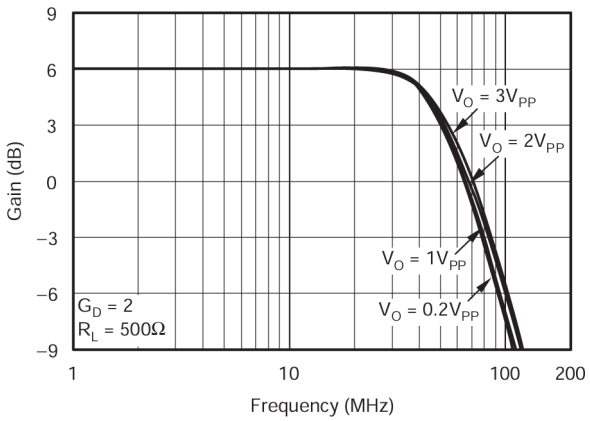


図 6-45. Differential Large-Signal Frequency Response

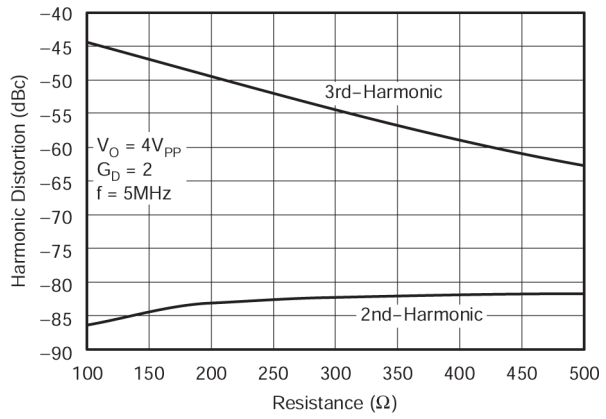


図 6-46. Differential Distortion vs Load Resistance

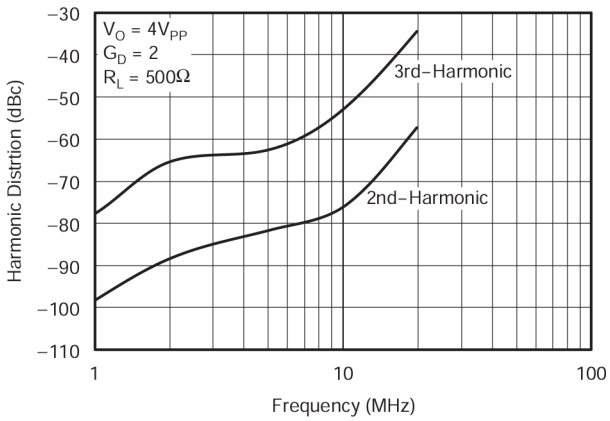


図 6-47. Differential Distortion vs Frequency

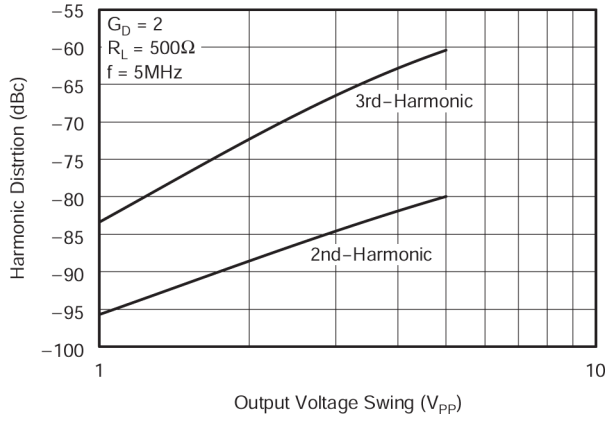
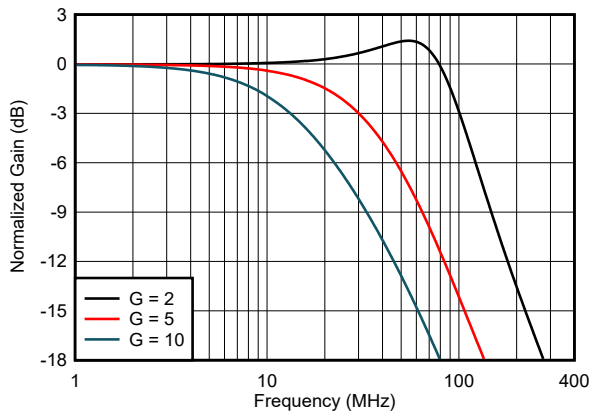


図 6-48. Differential Distortion vs Output Voltage

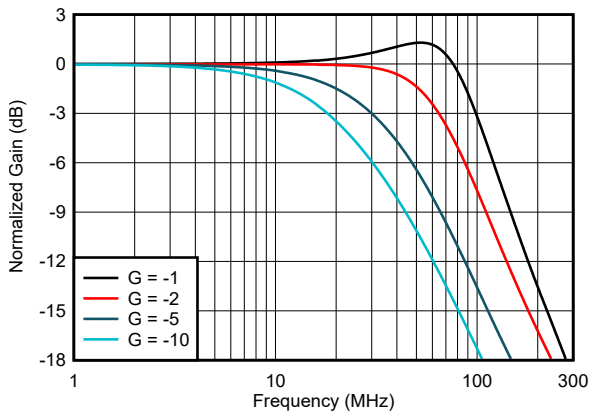
6.15 Typical Characteristics: V_S = 3V

at T_A = 25°C, G = +2, and R_L = 150Ω to V_S/3 (unless otherwise noted); see also 図 8-2



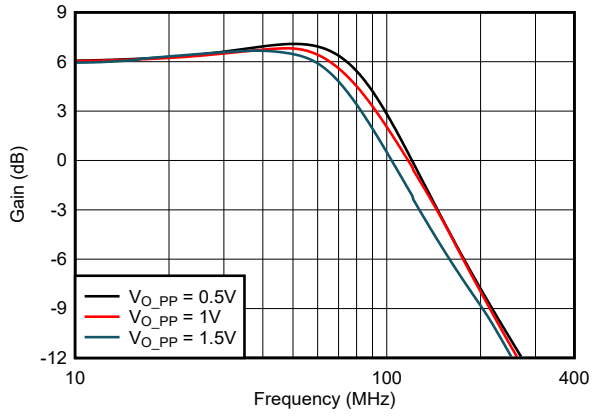
R_L = 150Ω V_O = 0.2V_{PP}

図 6-49. Noninverting Small-Signal Frequency Response



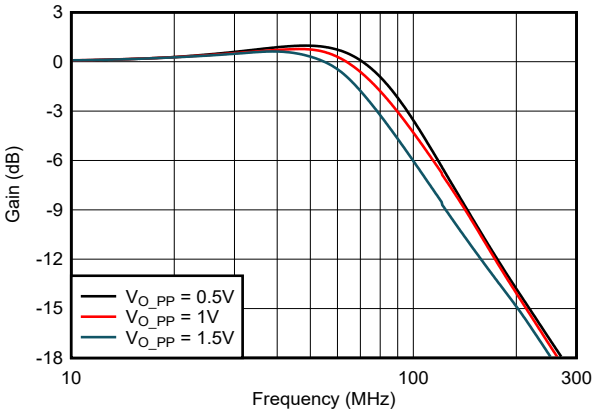
R_L = 150Ω V_O = 0.2V_{PP}

図 6-50. Inverting Small-Signal Frequency Response



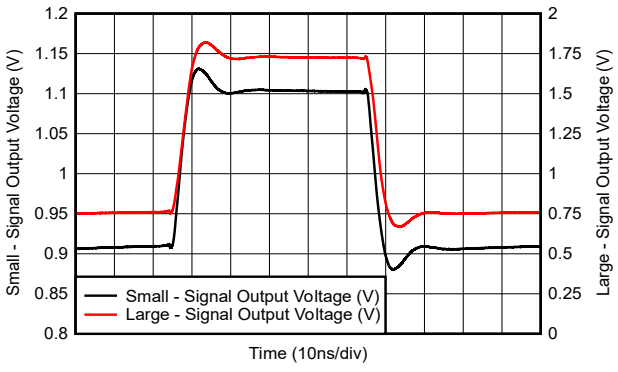
R_L = 150Ω G = +2V/V

図 6-51. Noninverting Large-Signal Frequency Response



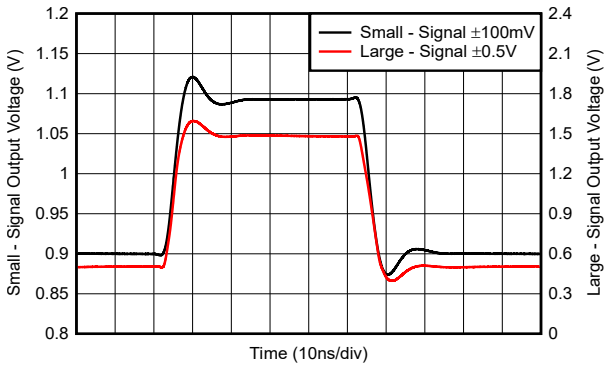
R_L = 150Ω G = –1V/V

図 6-52. Inverting Large-Signal Frequency Response



G = +2V/V

図 6-53. Noninverting Pulse Response

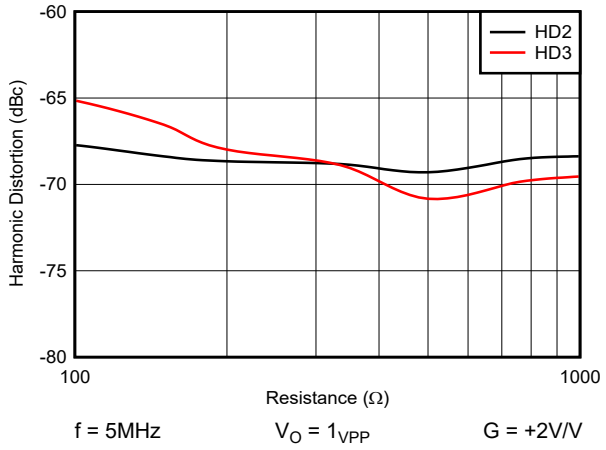


G = –1V/V

図 6-54. Inverting Pulse Response

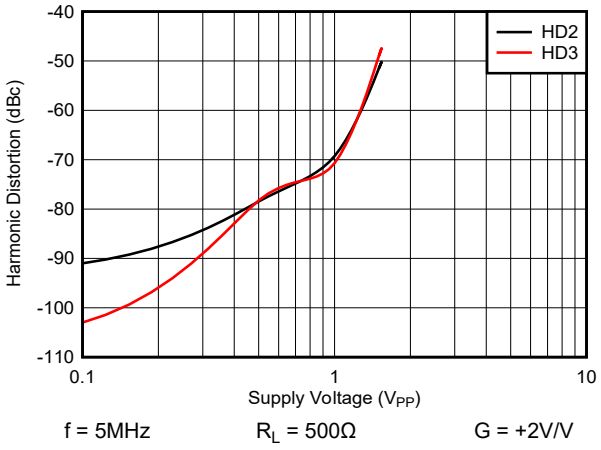
6.15 Typical Characteristics: V_S = 3V (continued)

at T_A = 25°C, G = +2, and R_L = 150Ω to V_S/3 (unless otherwise noted); see also 図 8-2



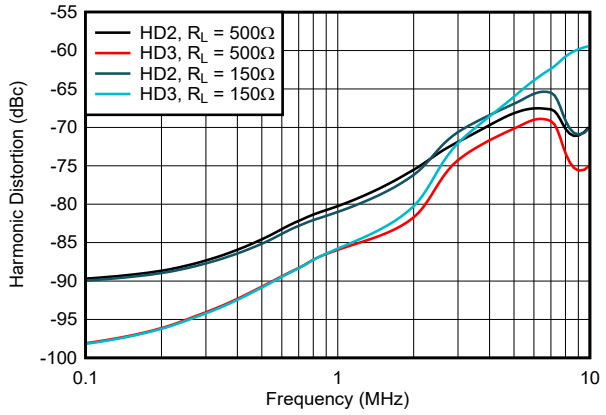
f = 5MHz $V_O = 1_{VPP}$ G = +2V/V

図 6-55. Harmonic Distortion vs Load Resistance



f = 5MHz R_L = 500Ω G = +2V/V

図 6-56. Harmonic Distortion vs Output Voltage



$V_O = 1V_{pp}$ G = +2V/V

図 6-57. Harmonic Distortion vs Frequency

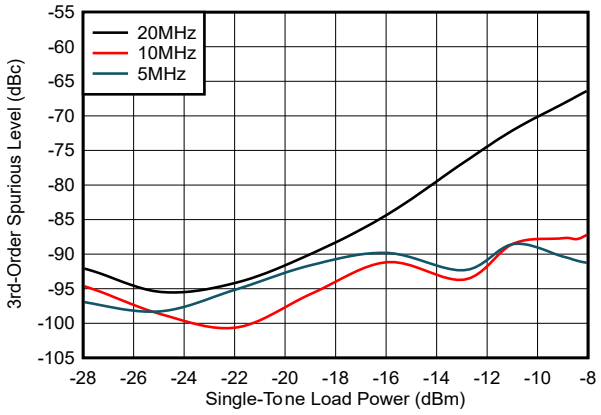


図 6-58. Two-Tone, 3rd-Order Intermodulation Spurious

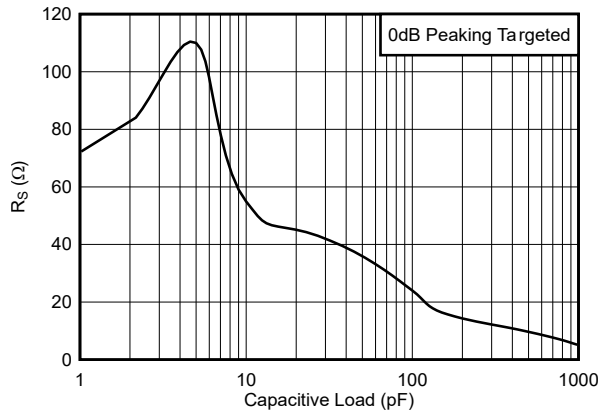


図 6-59. Recommended R_S vs Capacitive Load

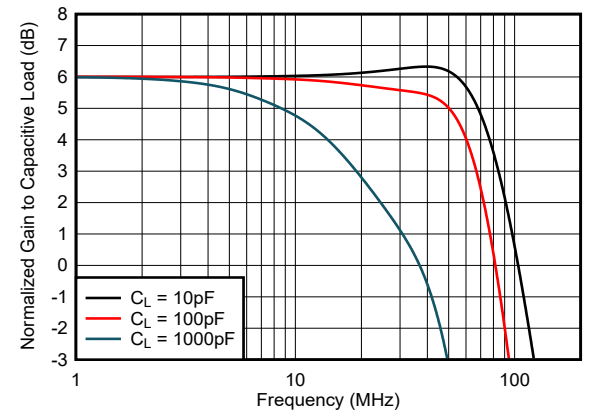


図 6-60. Frequency Response vs Capacitive Load

6.15 Typical Characteristics: V_S = 3V (continued)

at T_A = 25°C, G = +2, and R_L = 150Ω to V_S/3 (unless otherwise noted); see also 図 8-2

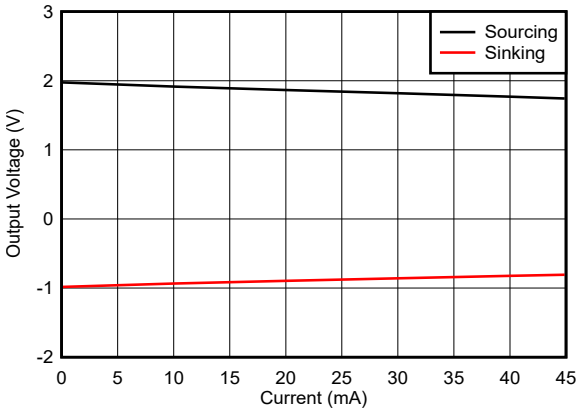


図 6-61. Output Swing vs Load Resistance

6.16 Typical Characteristics: V_S = 3V, Differential Configuration

at T_A = 25°C, G = +2, R_F = 604Ω, and R_L = 500Ω differential (unless otherwise noted). Refer to 図 7-3

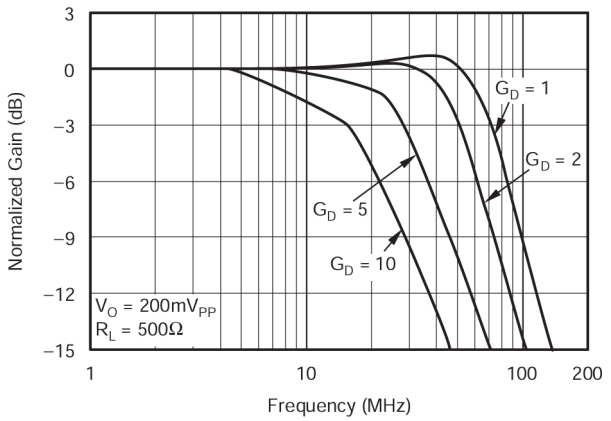


図 6-62. Differential Small−Signal Frequency Response

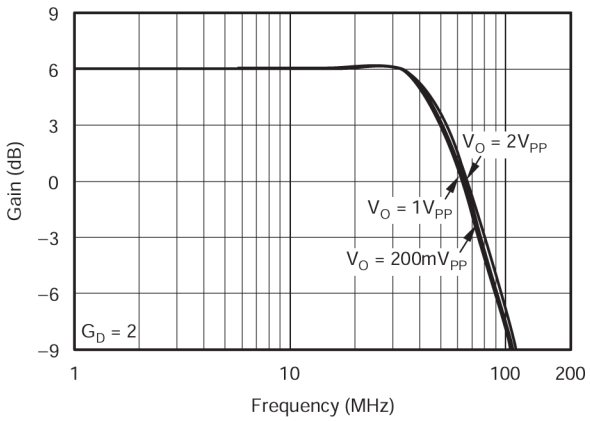


図 6-63. Differential Large−Signal Frequency Response

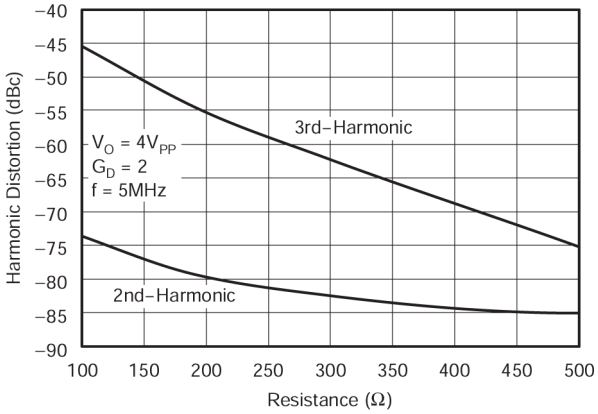


図 6-64. Differential Distortion vs Load Resistance

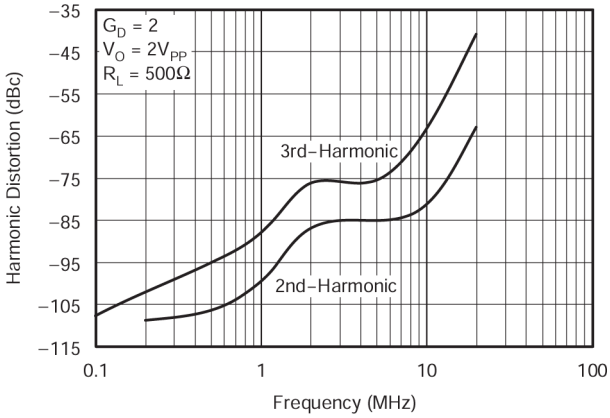


図 6-65. Differential Distortion vs Frequency

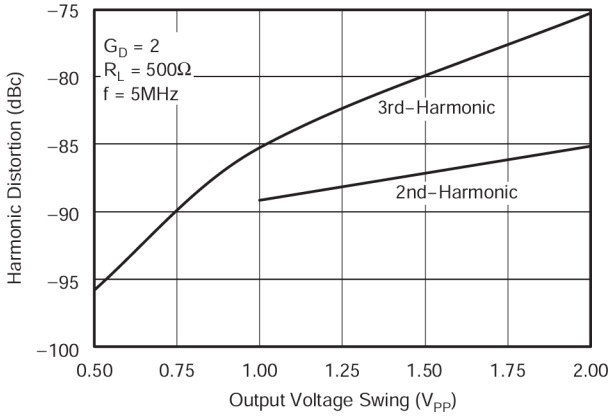


図 6-66. Differential Distortion vs Output Voltage

7 Parameter Measurement Information

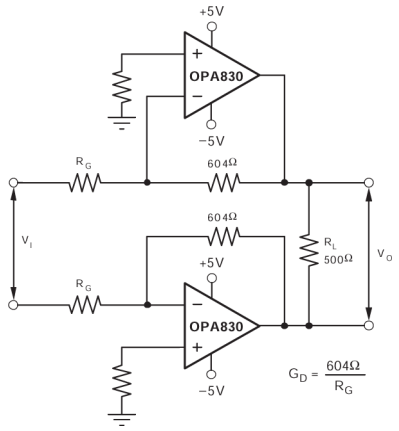


図 7-1. 10V Differential Configuration Test Circuit

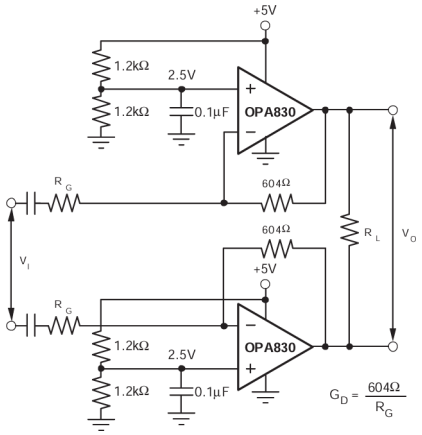


図 7-2. 5V Differential Configuration Test Circuit

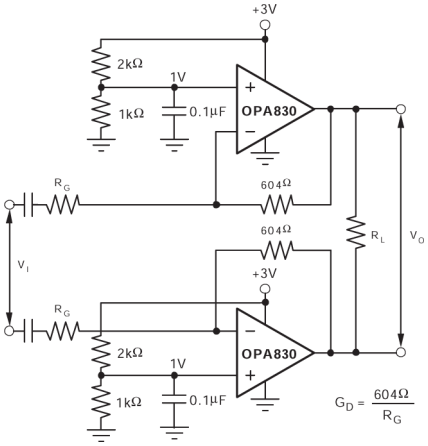


図 7-3. 3V Differential Configuration Test Circuit

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Wideband Voltage-Feedback Operation

The OPA830 is a unity-gain stable, very high-speed voltage-feedback op amp designed for single-supply operation (+3V to +10V). The input stage supports input voltages below ground and to within 1.7V of the positive supply. The complementary common-emitter output stage provides an output swing to within 25mV of ground and the positive supply. The OPA830 is compensated to provide stable operation with a wide range of resistive loads.

図 8-1 shows the AC-coupled, gain of +2 configuration used for the +5V Specifications and Typical Characteristic Curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of 図 8-1, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The 1.5kΩ resistors at the noninverting input provide the common-mode bias voltage. The parallel combination equals the DC resistance at the inverting input (R_F), reducing the DC output offset due to input bias current.

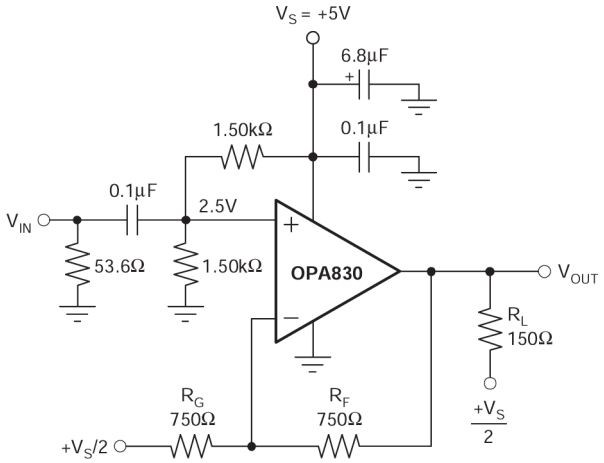


図 8-1. AC-Coupled, G = +2, +5V Single-Supply Specification and Test Circuit

図 8-2 shows the ac-coupled, gain of +2 configuration used for the 3V *Electrical Characteristics* and *Typical Characteristics*. For test purposes, the input impedance is set to 50Ω with a resistor to ground. Voltage swings reported in the *Electrical Characteristics* are taken directly at the input and output pins. For the circuit of 図 8-2, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The 1.13kΩ and 2.26kΩ resistors at the noninverting input provide the common-mode bias voltage. The parallel combination equals the dc resistance at the inverting input (R_F), reducing the dc output offset due to input bias current.

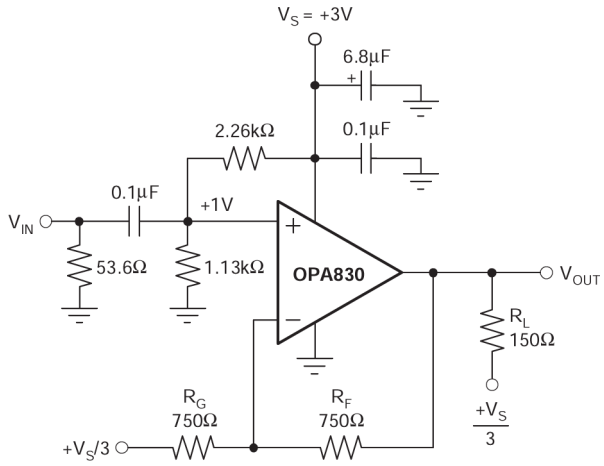


図 8-2. AC-Coupled, G = +2, +3V Single-Supply Specification and Test Circuit

図 8-3 shows the dc-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V *Electrical Characteristics* and *Typical Characteristics*. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 150Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of 図 8-3, the total effective load is 150Ω || 1.5kΩ. Two optional components are included in 図 8-3. An additional resistor (348Ω) is included in series with the noninverting input. Combined with the 25Ω dc source resistance looking back towards the signal generator, this configuration gives an input bias current canceling resistance that matches the 375Ω source resistance seen at the inverting input (see also セクション 8.1.10). In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical printed circuit board (PCB) layouts, this optional capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB.

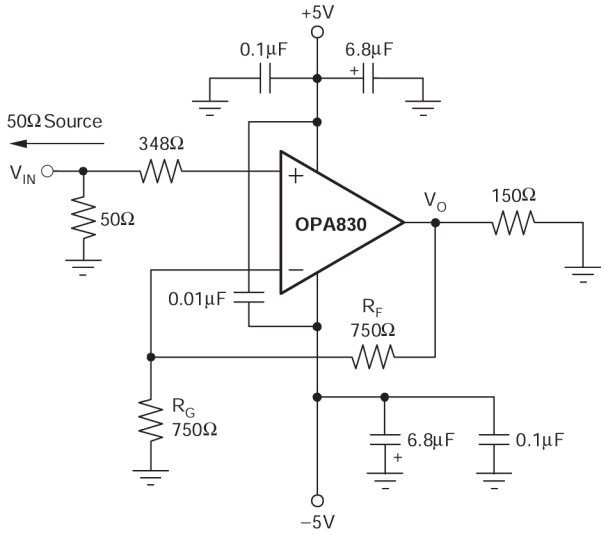


図 8-3. DC-Coupled, G = +2, Bipolar-Supply Specification and Test Circuit

8.1.2 DC Level-Shifting

図 8-4 shows a dc-coupled non inverting amplifier that level-shifts the input up to accommodate the desired output voltage range. Given the desired signal gain (G), and the amount V_{OUT} needs to be shifted up (ΔV_{OUT}) when V_{IN} is at the center of the range, the following equations give the resistor values that produce the desired performance. Assume that R_4 is between 200Ω and 1.5kΩ.

$NG = G + V_{OUT} / V_S$

$R_1 = R_4 / G$

$R_2 = R_4 / (NG – G)$

$R_3 = R_4 / (NG – 1)$

where:

$NG = 1 + R_4 / R_3$

$V_{OUT} = (G)V_{IN} + (NG – G)V_S$

Make sure that V_{IN} and V_{OUT} stay within the specified input and output voltage ranges.

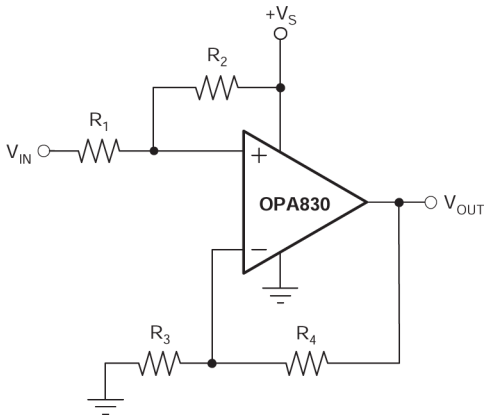


図 8-4. DC Level-Shifting

The circuit on the front page is a good example of this type of application. The circuit is designed to take V_{IN} between 0V and 0.5V and produce V_{OUT} between 1V and 2V when using a 3V supply. This configuration means G = 2.00, and ΔV_{OUT} = 1.50V – G × 0.25V = 1.00V. Plugging these values into the previous equations (with R_4 = 750Ω) gives: NG = 2.33, R_1 = 375Ω, R_2 = 2.25kΩ, and R_3 = 563Ω. The resistors changed to the nearest standard values for the front-page circuit.

8.1.3 Optimizing Resistor Values

The OPA830 is a unity-gain stable, voltage-feedback op amp; therefore, a wide range of resistor values can be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting, unity-gain follower application, make the feedback connection with a direct short.

At less than 200Ω, the feedback network presents additional output loading that can degrade the harmonic distortion performance of the OPA830. At greater than 1kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor can cause unintentional band limiting in the amplifier response.

A good practice is to target the parallel combination of R_F and R_G (see also 図 8-3) to be less than approximately 400Ω. The combined impedance of R_F || R_G interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding R_F || R_G < 400Ω keeps this pole greater than 200MHz. Independently, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This increase is acceptable if the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, be aware of an additional design consideration: R_G becomes the input resistor, and therefore, the load impedance to the driving source. If impedance matching is desired, R_G can be set equal to the required termination value. However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50Ω input matching resistor (= R_G) requires a 100Ω feedback resistor, which contributes to output loading in parallel with the external load. In such a case, increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground (see 図 8-5). The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

8.1.4 Bandwidth Versus Gain: Noninverting Operation

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the gain bandwidth product (GBP) shown in the specifications. Ideally, dividing GBP by the noninverting signal gain (also called the noise gain, or NG) predicts the closed-loop bandwidth. In practice, this prediction only holds true when the phase margin approaches 90°, as in high-gain configurations. At low gains (increased feedback factors), most amplifiers exhibit a more complex response with lower phase margin. The OPA830 is compensated to give a slightly peaked response in a noninverting gain of 2 (see 図 8-3). This compensation results in a typical gain of +2 bandwidth of 110MHz, far exceeding the result predicted by dividing the 110MHz GBP by 2. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 11MHz bandwidth shown in the *Electrical Characteristics* agrees with the result predicted using the simple formula and the typical GBP of 110MHz.

Frequency response in a gain of +2 can be modified to achieve exceptional flatness simply by increasing the noise gain to 3. One method, without affecting the +2 signal gain, is to add a 2.55kΩ resistor across the two inputs (see also 図 8-9). A similar technique can be used to reduce peaking in unity-gain (voltage follower) applications. For example, by using a 750Ω feedback resistor along with a 750Ω resistor across the two op amp inputs, the voltage follower response is similar to the gain of +2 response of 図 8-2. Further reducing the value of the resistor across the op amp inputs further dampens the frequency response due to increased noise gain. The OPA830 exhibits minimal bandwidth reduction going to single-supply (5V) operation as compared with ±5V. This minimal reduction is because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins changes.

8.1.5 Inverting Amplifier Operation

All of the familiar op amp application circuits are available with the OPA830 to the designer. See 図 8-5 for a typical inverting configuration where the I/O impedances and signal gain from 図 8-1 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. Inverting operation also allows the input to be biased at $V_S/2$ without any headroom issues. The output voltage can be independently moved to within the output voltage range with coupling capacitors or bias adjustment resistors.

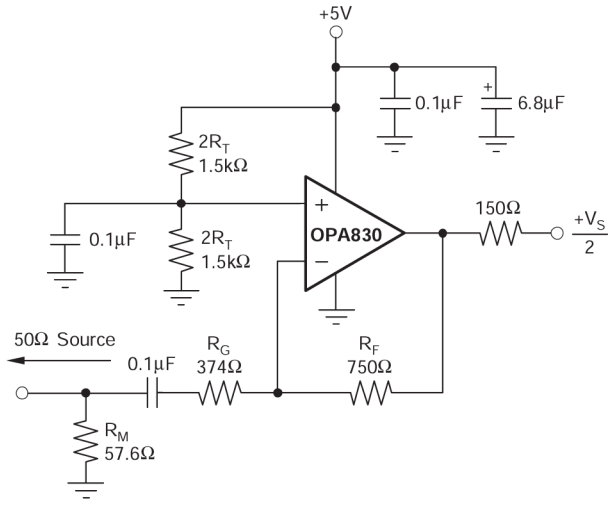


図 8-5. AC-Coupled, G = –2 Example Circuit

In the inverting configuration, be aware of three key design considerations. The first consideration is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PCB trace, or other transmission line conductor), R_G can be set equal to the required termination value and R_F adjusted to give the desired gain. This approach is the simplest and results in optimized bandwidth and noise performance.

However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 100Ω feedback resistor. This configuration has the interesting advantage of the noise gain becoming equal to 2 for a 50Ω source impedance—the same as the noninverting circuits considered previously. The amplifier output now has the 100Ω feedback resistor in parallel with the external load. In general, limit the feedback resistor to the 200Ω to 1.5kΩ range. In this case, increase both the R_F and R_G values (see also 図 8-5), and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

The second major consideration, mentioned briefly in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation, and thus influences the bandwidth. For the example in 図 8-5, the R_M value combines in parallel with the external 50Ω source impedance (at high frequencies), yielding an effective driving impedance of 50Ω || 57.6Ω = 26.8Ω. This impedance is added in series with R_G for calculating the noise gain. The resulting noise gain is 2.87 for 図 8-5, as opposed to only 2 if R_M is eliminated as discussed previously. Therefore, the bandwidth is lower for the gain of −2 circuit of 図 8-5 (NG = +2.87) than for the gain of +2 circuit of 図 8-1.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistors on the noninverting input (a parallel combination of R_T = 750Ω). If this resistor is set equal to the total dc resistance coming out of the inverting node, the output dc error, as a result of the input bias currents, is reduced to (input offset current) times R_F. With the dc blocking capacitor in series with R_G, the dc source impedance coming out of

the inverting mode is simply R_F = 750Ω for 図 8-5. To reduce the additional high-frequency noise introduced by this resistor and power-supply feed-through, bypass R_T with a capacitor.

8.1.6 Output Current and Voltages

The OPA830 provides outstanding output voltage capability. For the 5V supply, under no-load conditions at +25°C, the output voltage typically swings closer than 90mV to either supply rail.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold start-up does the output current and voltage decrease to the numbers shown in the specified tables. As the output transistors deliver power, the junction temperatures increase, decreasing the V_{BE}s (increasing the available output voltage swing) and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current is always greater than that shown in the over temperature specifications because the output-stage junction temperatures are greater than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This configuration is not normally a problem because most applications include a series matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (8-pin packages) in most cases destroys the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. This resistor reduces the available output voltage swing under heavy output loads.

8.1.7 Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that can be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA830 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the primary considerations are frequency response flatness, pulse response fidelity, or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load.

The typical characteristic curves show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA830. Long PCB traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the output pin (see also the *Layout Guidelines* section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain also reduces the peaking (see 図 8-9).

8.1.8 Distortion Performance

The OPA830 provides good distortion performance into a 150Ω load. Relative to alternative solutions, the OPA830 provides exceptional performance into lighter loads, and operating on a single 3V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see 図 8-3) this result is the sum of R_F + R_G, while in the inverting configuration, only R_F must be included in parallel with the actual load. Running differential suppresses the 2nd-harmonic (see also the differential typical characteristic curves).

8.1.9 Noise Performance

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve a slew rate at the expense of a higher input noise voltage. The 9.2nV/√Hz input voltage noise for the OPA830, however, is much lower than comparable amplifiers. The input-referred voltage noise and the two input-referred current noise terms (2.8pA/√Hz) combine to give low output noise under a wide variety of operating conditions. 図 8-6 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

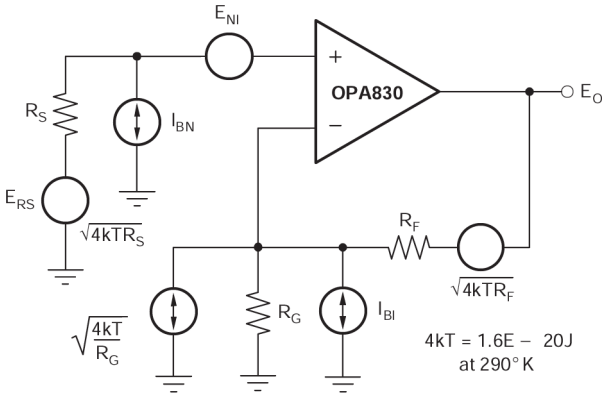


図 8-6. Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. 図 8-4 shows the general form for the output noise voltage using the terms shown in 図 8-6:

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (4)$$

Dividing this expression by the noise gain (NG = (1 + R_F / R_G)) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in 図 8-7:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (5)$$

Evaluating these two equations for the circuit and component values shown in 図 8-1 gives a total output spot noise voltage of 19.3nV/√Hz and a total equivalent input spot noise voltage of 9.65nV/√Hz. This result includes the noise added by the resistors. This total input-referred spot noise voltage is not much greater than the 9.2nV/√Hz specification for the op amp voltage noise alone.

8.1.10 DC Accuracy and Offset Control

The balanced input stage of a wideband voltage-feedback op amp allows good output dc accuracy in a wide variety of applications. The power-supply current trim for the OPA830 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically 5µA out of each input terminal), the close matching between the pins can be used to reduce the output dc error caused by this current. This reduction is done by matching the dc source resistances appearing at the two inputs. Evaluating the configuration of 図 8-3 (which has matched dc input resistances), using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

(NG = noninverting signal gain at DC)

$\pm(NG \times V_{OS(MAX)}) + (R_F \times I_{OS(MAX)})$

$= \pm(2 \times 7mV) \times (375\Omega \times 1\mu A)$

$= \pm 14.38mV$

A fine-scale output offset null, or dc operating point adjustment, is often required. Numerous techniques are available for introducing dc offset control into an op amp circuit. Most of these techniques are based on adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input can be considered. Bring the dc offsetting current into the inverting input node through resistor values that are much larger than the signal path resistors. This adjustment circuit configuration has minimal effect on the loop gain, and hence, the frequency response.

8.1.11 Thermal Analysis

The maximum desired junction temperature sets the maximum allowed internal power dissipation. Do not allow the maximum junction temperature to exceed 150°C.

The operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; although, for resistive loads connected to mid-supply (V_S / 2), P_{DL} is at a maximum when the output is fixed at a voltage equal to V_S / 4 or $3V_S$ / 4. Under this condition, $P_{DL} = V_S{}^2$ / c × (16 × R_L), where R_L includes feedback network loading.

The power in the output stage, and not into the load, determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA830 (SOT-23-5 package) in the circuit of 図 8-1 operating at the maximum specified ambient temperature of 85°C and driving a 150Ω load at mid-supply.

P_D = 10V × 3.9mA + 52 / (16 × (150Ω || 750Ω)) = 51.5mW

Maximum T_J = 85°C + (0.051W × 186.3°C/W) = 94.5°C.

Although this result is still much less than the specified maximum junction temperature, system reliability considerations can require lower specified junction temperatures. The highest possible internal dissipation occurs if the load requires current to be forced into the output at high output voltages, or sourced from the output at low output voltages. This configuration puts a high current through a large internal voltage drop in the output transistors.

8.2 Typical Applications

8.2.1 Single-Supply ADC Interface

The ADC interface on the front page shows a dc-coupled, single-supply ADC driver circuit. Many systems are now requiring 3V supply capability of both the ADC and driver. The OPA830 provides excellent performance in this demanding application. The large input and output voltage ranges and low distortion support converters such as the THS1040 shown in the figure on page 1. The input level-shifting circuitry was designed so that V_{IN} can be between 0V and 0.5V, while delivering an output voltage of 1V to 2V for the THS1040.

8.2.2 AC-Coupled Output Video Line Driver

Low-power and low-cost video line drivers often buffer digital-to-analog converter (DAC) outputs with a gain of 2 into a doubly-terminated line. Those interfaces typically require a dc blocking capacitor. For a simple design, that interface often has used a very large value blocking capacitor (220µF) to limit tilt, or SAG, across the frames. One approach to creating a very low high-pass pole location using much lower capacitor values is shown in 図 8-7. This circuit gives a voltage gain of 2 at the output pin with a high-pass pole at 8Hz. Given the 150Ω load, a simple blocking capacitor approach requires a 133µF value. The two much lower valued capacitors give this same low-pass pole using this simple *SAG correction* circuit of 図 8-7.

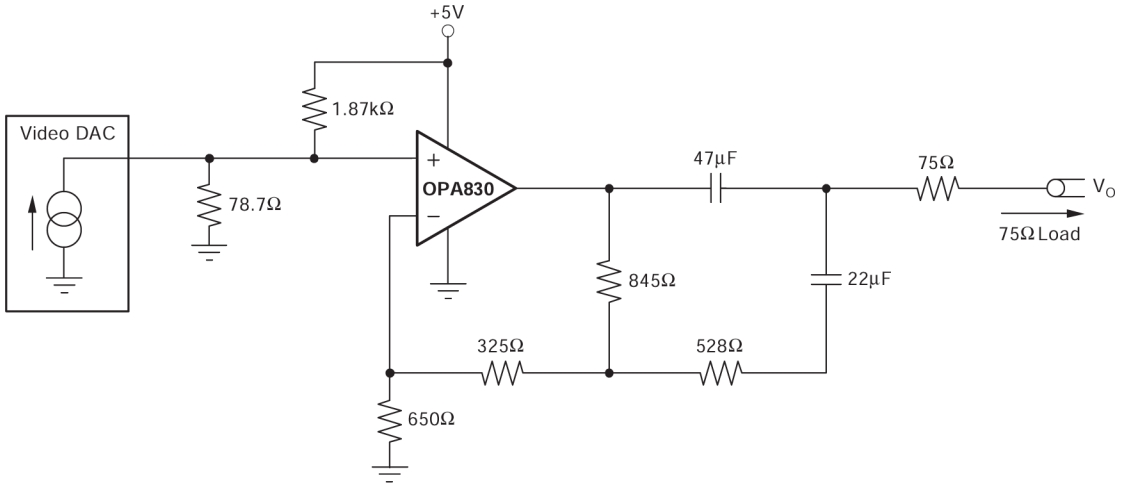


図 8-7. Video Line Driver With SAG Correction

The input is shifted slightly positive in 図 8-7 using the voltage divider from the positive supply. This shift gives about a 200mV input dc offset that shows up at the output pin as a 400mV dc offset when the DAC output is at zero current during the sync tip portion of the video signal. This offset acts to hold the output in the linear operating region. This offset passes on any power-supply noise to the output with a gain of approximately −20dB, so good supply decoupling is recommended on the power-supply pin. 図 8-8 shows the frequency response for the circuit of 図 8-7. This plot shows the 8Hz low-frequency high-pass pole and a high-end cutoff at approximately 100MHz.

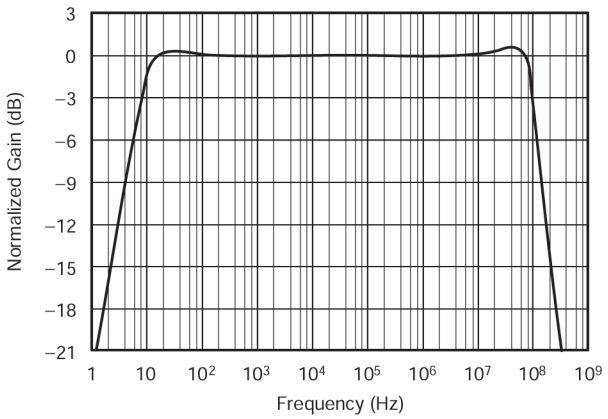


図 8-8. Video Line Driver Response to Matched Load

8.2.3 Noninverting Amplifier With Reduced Peaking

図 8-9 shows a noninverting amplifier that reduces peaking at low gains. Resistor R_C compensates the OPA830 to have greater noise gain (NG), which reduces the ac response peaking (typically 5dB at G = +1 without R_C) without changing the dc gain. V_{IN} must be a low impedance source, such as an op amp. The resistor values are low to reduce noise. Using both R_T and R_F helps minimize the impact of parasitic impedances.

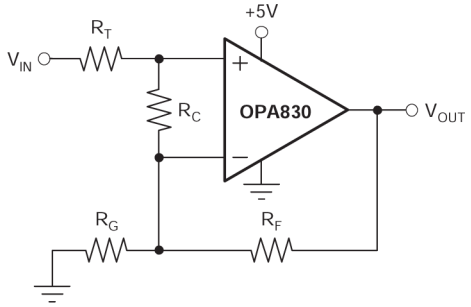


図 8-9. Compensated Noninverting Amplifier

The noise gain is calculated as follows:

$$G_1 = 1 + \frac{R_F}{R_G} \quad (1)$$

$$G_2 = 1 + \frac{R_T + \frac{R_F}{G_1}}{R_C} \quad (2)$$

$$NG = G_1 \times G_2 \quad (3)$$

A unity-gain buffer can be designed by selecting $R_T = R_F = 20.0\Omega$ and $R_C = 40.2\Omega$ (do not use R_G). This configuration gives a noise gain of 2, so the response is similar to the characteristics plots with G = +2. Decreasing R_C to 20.0Ω increases the noise gain to 3, which typically gives a flat frequency response, but with less bandwidth.

The circuit in 図 8-1 can be redesigned to have less peaking by increasing the noise gain to 3. This redesign is accomplished by adding $R_C = 2.55k\Omega$ across the op amp inputs.

8.2.4 Single-Supply Active Filter

The OPA830, while operating on a single 3V or 5V supply, works well with high-frequency active filter designs. Again, the key additional requirement is to establish the dc operating point of the signal near the supply midpoint for highest dynamic range. 図 8-10 shows an example design of a 1MHz low-pass Butterworth filter using the Sallen-Key topology.

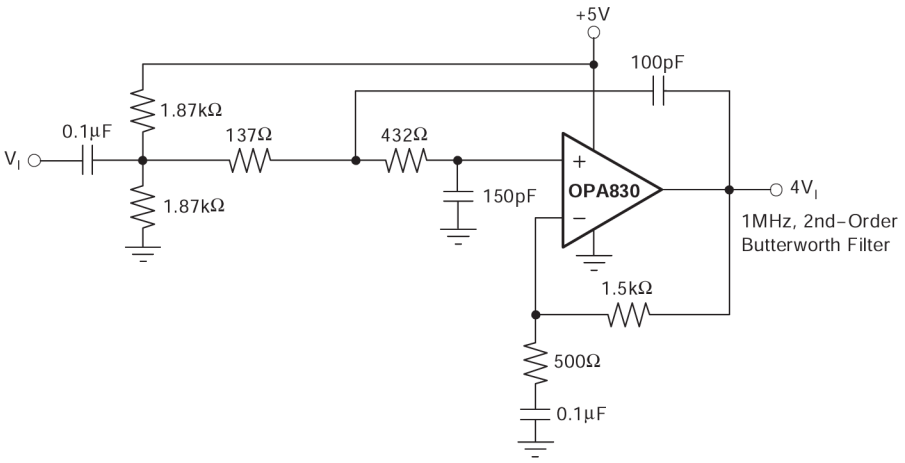


図 8-10. Single-Supply, High-Frequency Active Filter

Both the input signal and the gain setting resistor are ac-coupled using 0.1µF blocking capacitors (actually giving bandpass response with the low-frequency pole set to 32kHz for the component values shown). As discussed for 図 8-1, this configuration allows the midpoint bias formed by the two 1.87kΩ resistors to appear at both the input and output pins. The midband signal gain is set to +4 (12dB) in this case. The capacitor to ground on the noninverting input is intentionally set larger to dominate input parasitic terms. At a gain of +4, the OPA830 on a single supply shows 30MHz small- and large-signal bandwidth. The resistor values are slightly adjusted to account for this limited bandwidth in the amplifier stage. Tests of this circuit show a precise 1MHz, –3dB point with a maximally flat pass band (greater than the 32kHz ac-coupling corner), and a maximum stop-band attenuation of 36dB at the amplifier –3dB bandwidth of 30MHz.

8.3 Layout

8.3.1 Layout Guidelines

Achieving optimized performance with a high-frequency amplifier such as the OPA830 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

1. **Minimize parasitic capacitance** to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, open a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.25”) from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, do not place the ground and power-plane layout in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Always decouple each power-supply connection with one of these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Use larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, on the main supply pins. Place these capacitors somewhat farther from the device. These capacitors can be shared among several devices in the same area of the PCB.
3. **Carefully select and place external components to preserve the high-frequency performance.** Use very low reactance type resistors. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB traces as short as possible. Never use wire-wound type resistors in a high-frequency application. The output pin and inverting input pin are the most sensitive to parasitic capacitance; therefore, always position the feedback and series output resistor, if any, as close as possible to the output pin. Place other network components, such as noninverting input termination resistors, close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole, zero below 500MHz, or both, that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 750Ω feedback used in the *Typical Characteristics* is a good starting point for design.
4. **Make connections to other wideband devices on the board with short direct traces or through onboard transmission lines**. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50mils to 100mils), preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the typical characteristic curve *Recommended R_S vs Capacitive Load*. R_S is not always needed for low parasitic capacitive loads (< 5pF) because the OPA830 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment improves distortion; see also the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA830 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; set this total effective impedance to match the trace impedance. If the 6dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the typical characteristic curve *Recommended R_S vs Capacitive Load*. This configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low,

some signal attenuation occurs due to the voltage divider formed by the series output into the terminating impedance.

5. **Do not socket a high-speed device.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the OPA830 onto the board.

8.3.1.1 Input and ESD Protection

The OPA830 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings*. All device pins are protected with internal ESD protection diodes to the power supplies, as in 図 8-11.

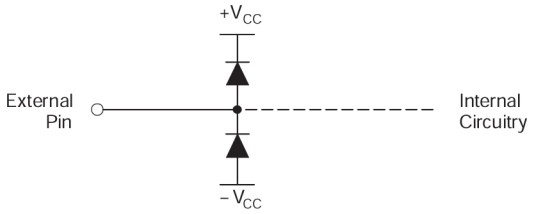


図 8-11. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages greater than the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (that is, in systems with ±15V supply parts driving into the OPA830), add current-limiting series resistors into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Demonstration Boards

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA830 in two package options. Both of these PCBs are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in 表 9-1.

表 9-1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA830ID	SO-8	DEM-OPA-SO-1A	SBOU009
OPA830IDBV	SOT23-5	DEM-OPA-SOT-1A	SBOU010

Request demonstration fixtures at the Texas Instruments web site through the OPA830 product folder.

9.1.1.2 Macromodel and Applications Support

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA830 and circuit designs. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA830 is available through the TI web page. The applications department is also available for design assistance. These models predict typical small signal ac, transient steps, dc performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in small-signal ac performance.

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (November 2024) to Revision H (December 2024)	Page
• Updated power supply for DBV package in *Absolute Maximum Ratings*	4
• Added D package electrical characteristics back into *Specifications*	13
• Moved electrical characteristics for DBV and D packages into separate tables	13

Changes from Revision F (August 2008) to Revision G (November 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 「目次」、「ピン構成および機能」、「仕様」、「ESD 定格」、「推奨動作条件」、「熱に関する情報」、「パラメータ測定情報」、「アプリケーションと実装」、「代表的なアプリケーション」、「レイアウト」、「レイアウトのガイドライン」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」の各セクションを追加	1
• 「概要」セクションに「パッケージ情報」表を追加	1
• Updated electrical characteristics to match device performance	13
• Updated plots in *Typical Characteristics*	19
• Updated θ_{JA} in *Thermal Analysis*	40

Changes from Revision E (August 2007) to Revision F (August 2008)	Page
• Changed Storage temperature minimum value from −40°C to −65°C in *Absolute Maximum Ratings*	4

Changes from Revision D (March 2006) to Revision E (August 2007)	Page
• 「特長」で 550V/ns を 550V/µs に変更	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA830ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 830	Samples
OPA830IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A72	Samples
OPA830IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A72	Samples
OPA830IDBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	A72	
OPA830IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 830	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA830 :

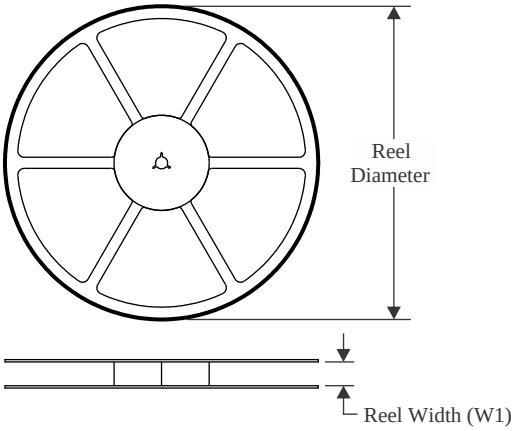
- Enhanced Product : OPA830-EP

NOTE: Qualified Version Definitions:

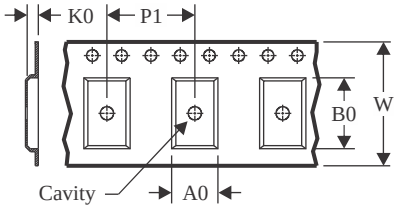
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

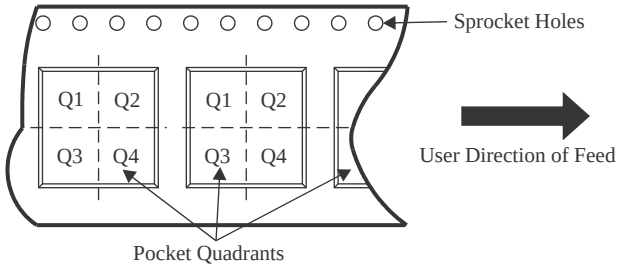


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

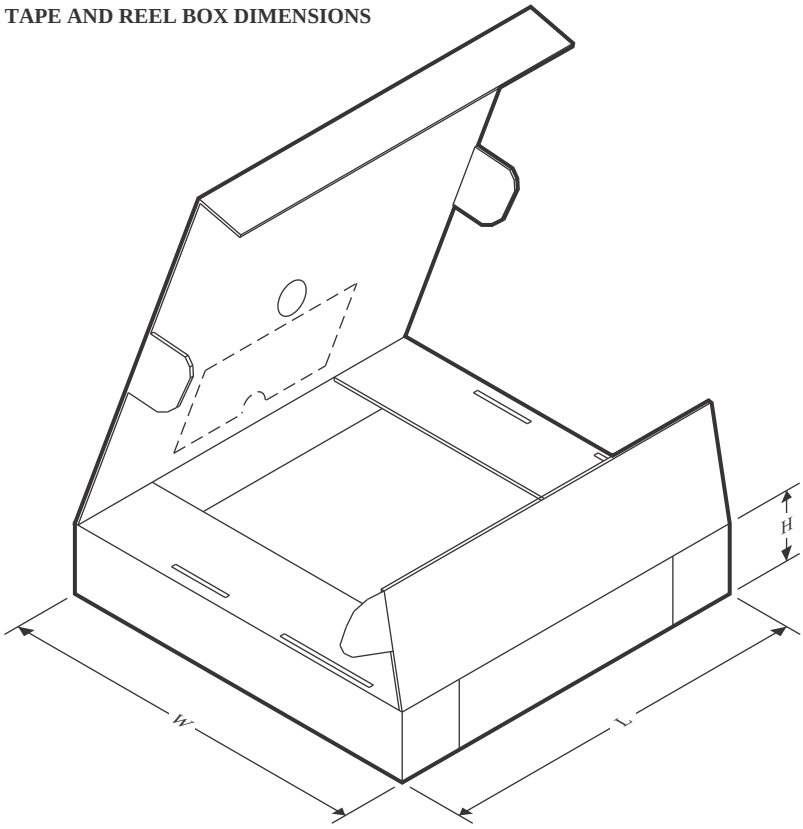
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA830IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

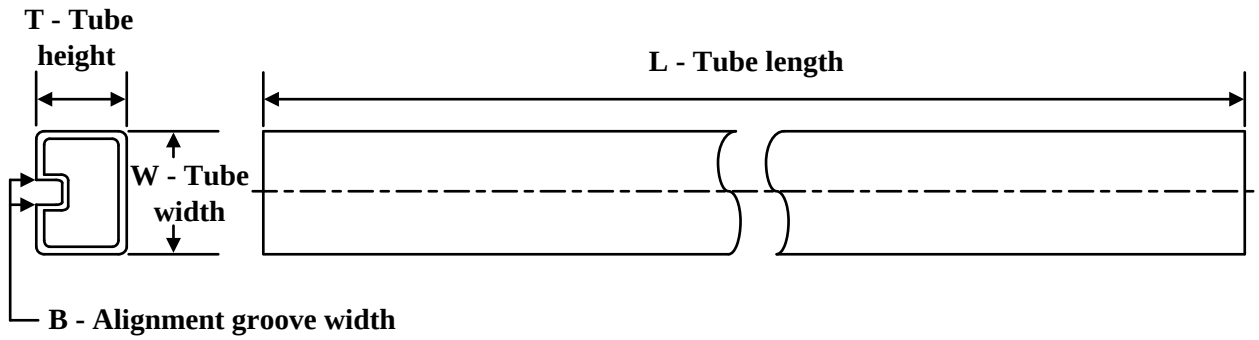
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

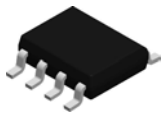
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA830IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA830ID	D	SOIC	8	75	506.6	8	3940	4.32

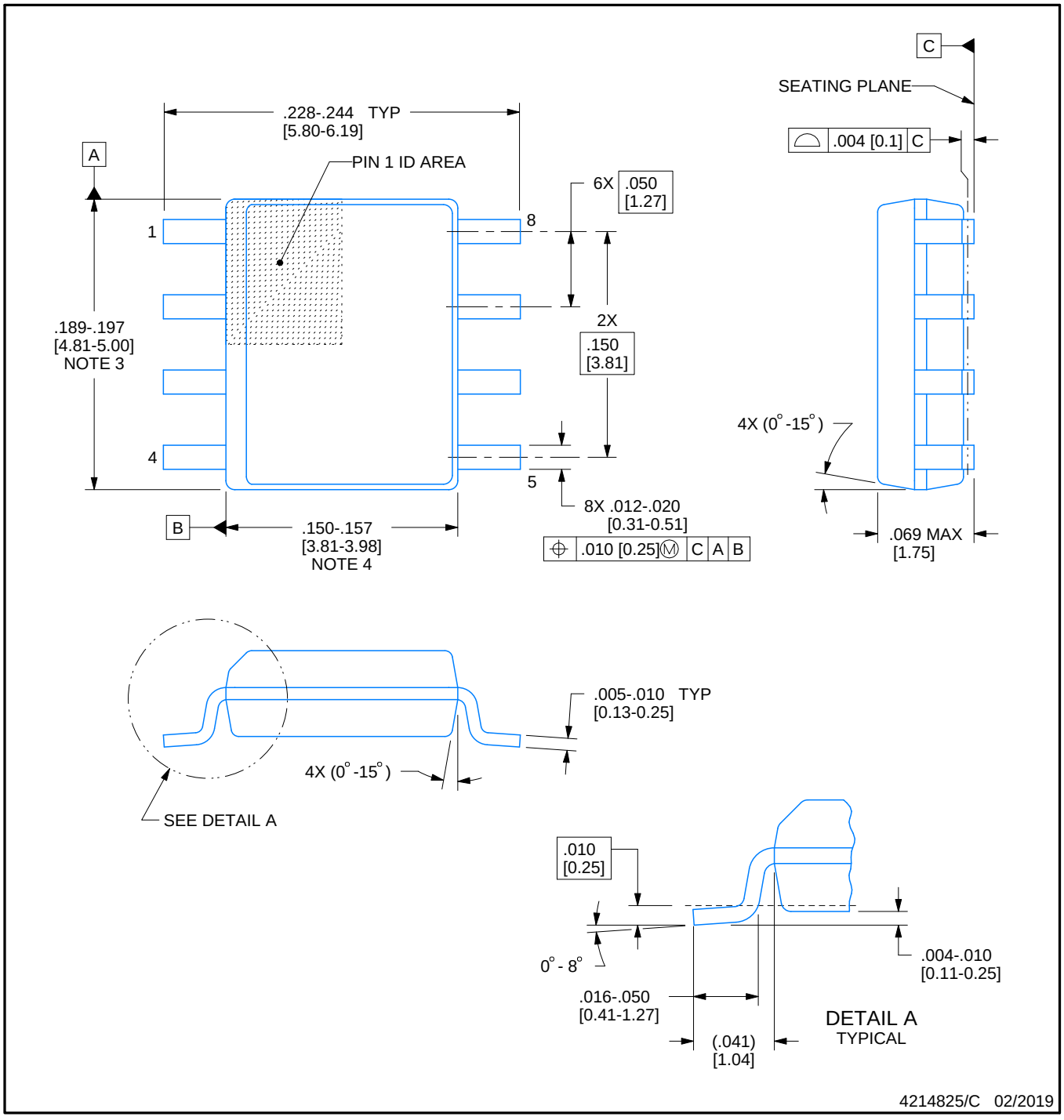


PACKAGE OUTLINE

D0008A

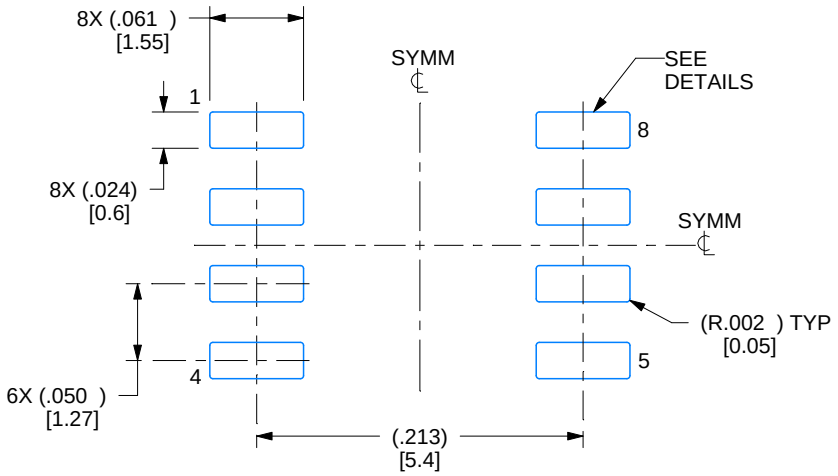
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

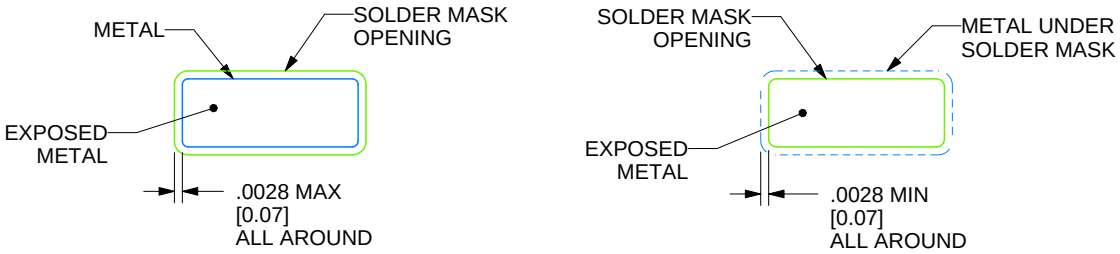


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

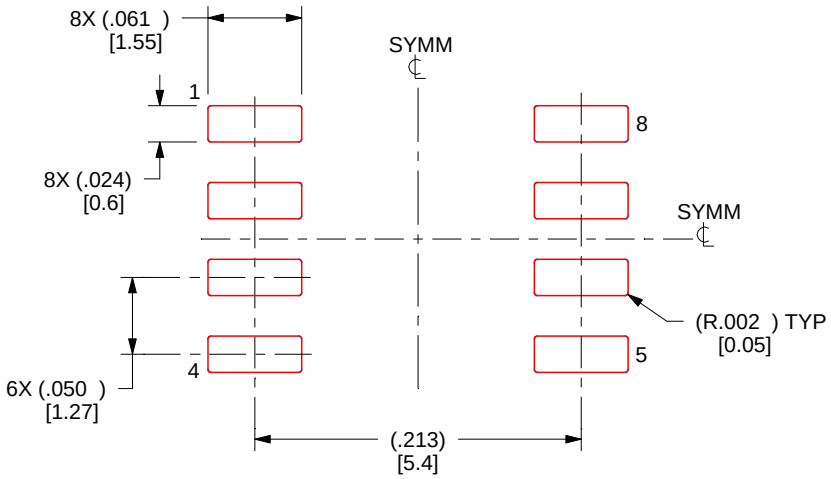
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

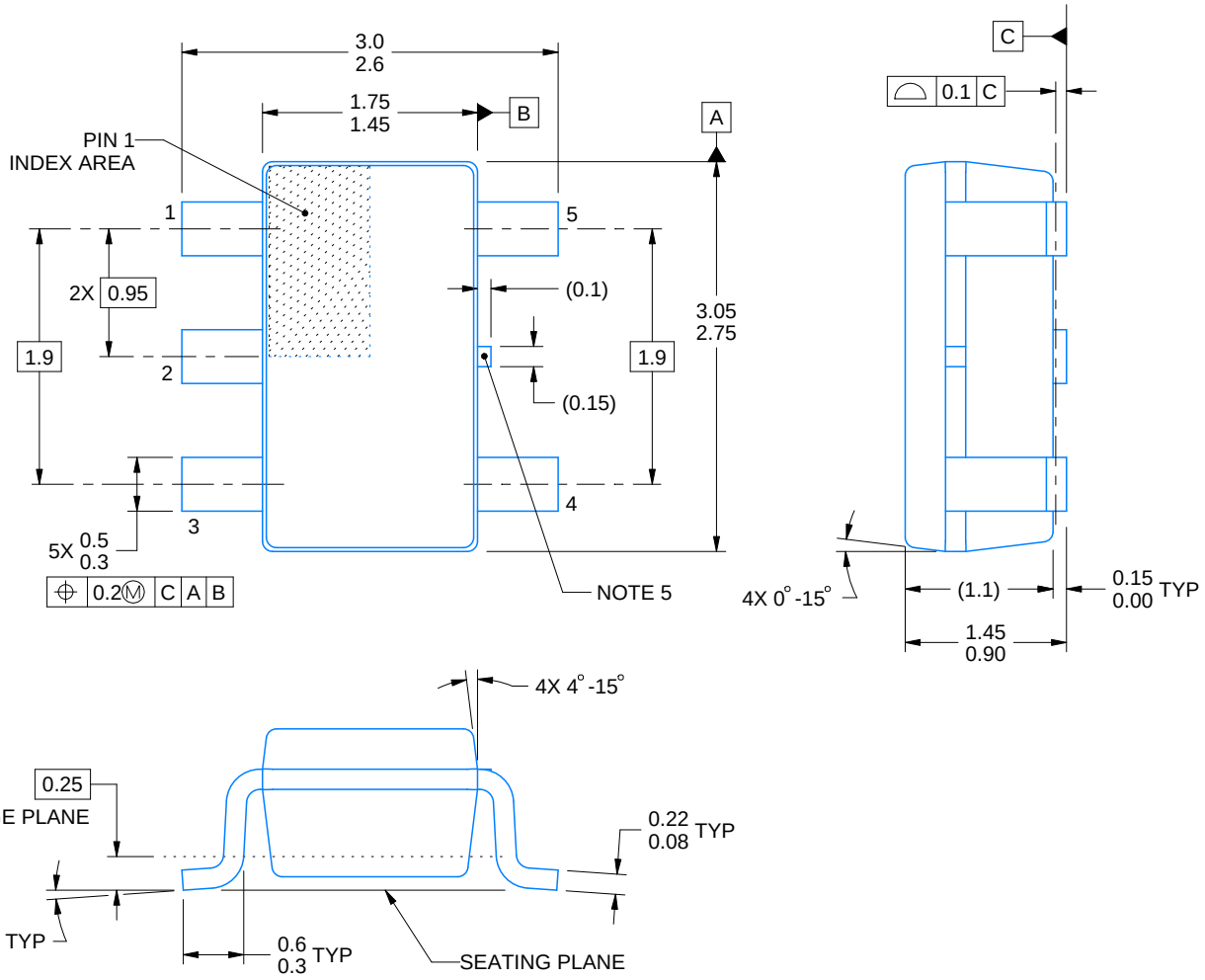
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

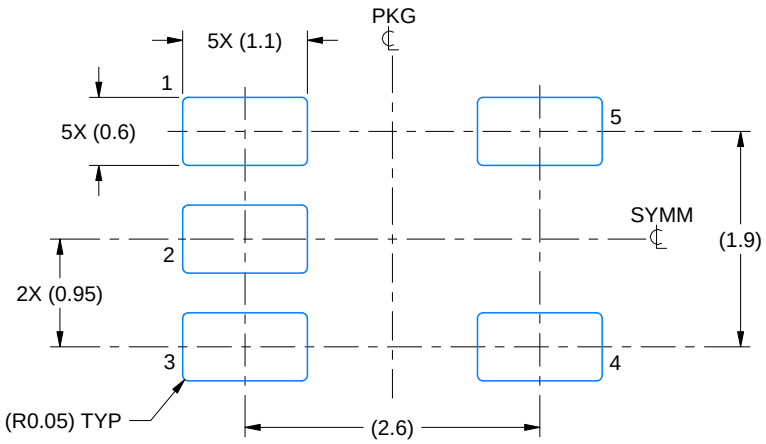
SMALL OUTLINE TRANSISTOR



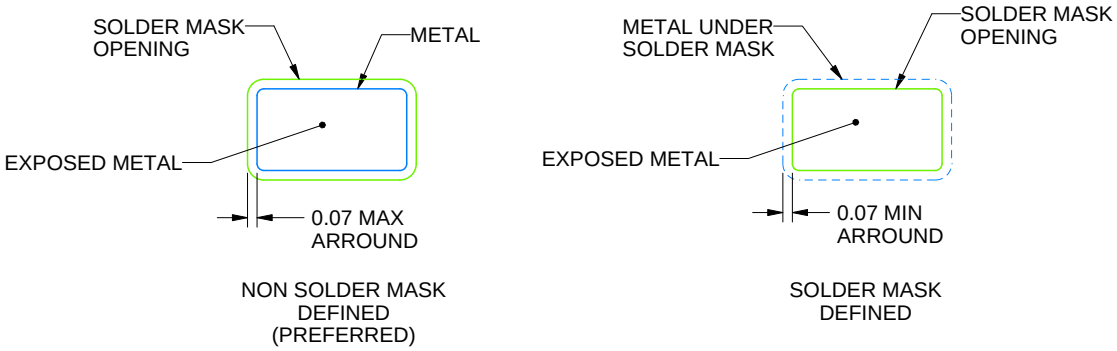
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

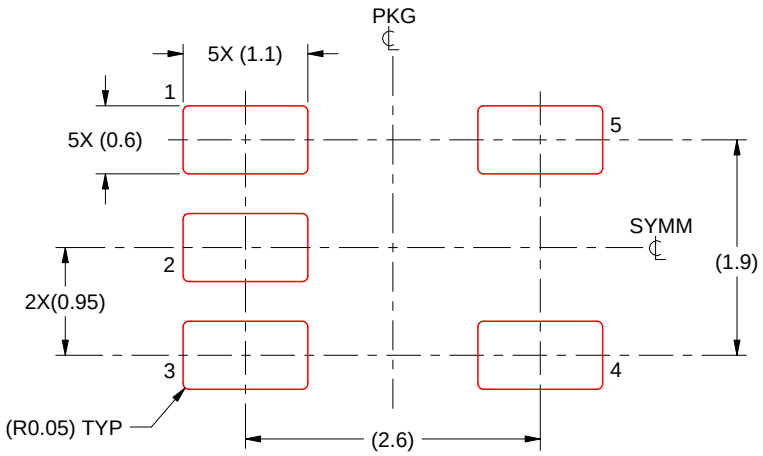


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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