

RC4580 デュアル オーディオ オペアンプ

1 特長

- 動作電圧 $\pm 2V \sim \pm 18V$
- 低いノイズ電圧: $0.8\mu V_{rms}$
- ゲイン帯域幅積: $12MHz$
- 全高調波歪み: 0.0005%
- スルーレート: $5V/\mu s$
- NJM4580 のドロップイン代替品
- LM833、NE5532、NJM4558/9、NJM4560/2/5 デバイスとピンおよび機能が互換

2 アプリケーション

- オーディオ プリアンプ
- アクティブ フィルタ
- ヘッドホン アンプ
- 産業用の測定機器

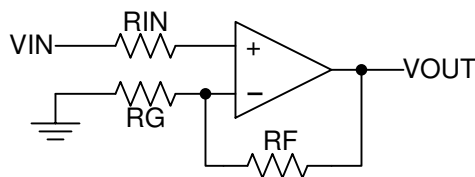
3 概要

RC4580 デバイスは、トーン制御の改善など、オーディオアプリケーション向けに最適化された設計のデュアル オペアンプです。このデバイスはノイズが低く、ゲイン帯域幅が高く、高調波歪みが小さく、出力電流が大きくて、プリアンプ、アクティブ フィルタ、産業用測定機器などのオーディオ エレクトロニクス用に設計されています。大きな出力電流が必要な場合、RC4580 デバイスをヘッドホン アンプとして使用できます。RC4580 デバイスはデバイスの動作電源電圧範囲が広いと、低電圧アプリケーションでも使用できます。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	本体サイズ ⁽²⁾
RC4580	D (SOIC, 8)	3.9mm × 4.9mm
	P (PDIP, 8)	9.81mm × 9.43mm
	PW (TSSOP, 8)	3.0mm × 4.4mm
	DGK (VSSOP, 8)	3.0mm × 3.0mm
	DDF (SOT-23, 8)	1.6mm × 2.9mm

- (1) 供給されているすべてのパッケージについては、[セクション 10](#) を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



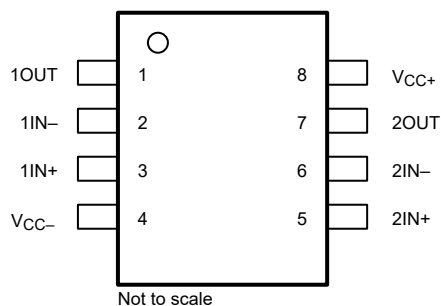
非反転アンプの回路図



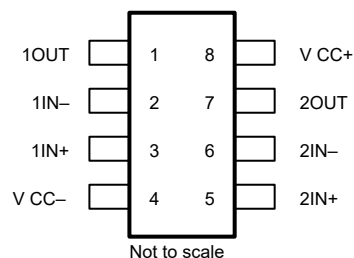
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4 Pin Configuration and Functions



**図 4-1. D, PW, and DGK Packages
8-Pin SOIC, TSSOP, and VSSOP
(Top View)**



**図 4-2. DDF Package
8-Pin SOT-23
(Top View)**

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN-	2	I	Inverting input
1OUT	1	O	Output
2IN+	5	I	Noninverting input
2IN-	6	I	Inverting input
2OUT	7	O	Output
V _{CC} +	8	—	Positive supply
V _{CC} -	4	—	Negative supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage		±18	V
V _I	Input voltage (any input)		±15	V
V _{ID}	Differential input voltage		±30	V
I _O	Output current		±50	mA
T _A	Ambient temperature range	–40	125	°C
T _{stg}	Storage temperature range	–60	125	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			MIN	MAX	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC+}	Supply voltage	2	16	V
V _{CC–}		–2	–16	
V _{ICR}	Input common-mode voltage range	–13.5	13.5	V
T _A	Operating free-air temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		RC4580					UNIT
		D (SOIC)	P (PDIP)	PW (TSSOP)	DGK (VSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	109	99.2	163	160.5	177.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	55.7	78.8	38	70.2	96.5	
R _{θJB}	Junction-to-board thermal resistance	49	61.9	90.6	95.6	95.2	
ψ _{JT}	Junction-to-top characterization parameter	10.6	44.8	1.3	8.8	9.5	
ψ _{JB}	Junction-to-board characterization parameter	48.6	61.2	88.9	94.0	95.0	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

$V_{CC\pm} = \pm 15\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$R_S = < 10\text{ k}\Omega$		0.5	3	mV
I_{IO} Input offset current			5	200	nA
I_{IB} Input bias current			100	500	nA
A_{VD} Large-signal differential voltage amplification	$R_L \geq 2\text{ k}\Omega$, $V_O = \pm 10\text{ V}$	90	110		dB
V_{CM} Output voltage swing	$R_L \geq 2\text{ k}\Omega$	± 12	± 13.5		V
V_{ICR} Common-mode input voltage		± 12	± 13.5		V
CMRR Common-mode rejection ratio	$R_S \leq 10\text{ k}\Omega$	80	110		dB
k_{SVR} Supply-voltage rejection ratio ⁽¹⁾	$R_S \leq 10\text{ k}\Omega$	80	110		dB
I_{CC} Total supply current (all amplifiers)			6	9	mA

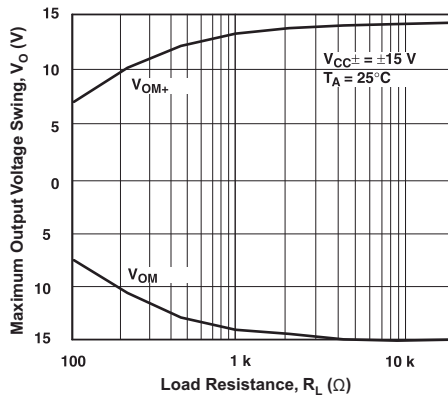
(1) Measured with $V_{CC\pm}$ varied simultaneously

5.6 Operating Characteristics

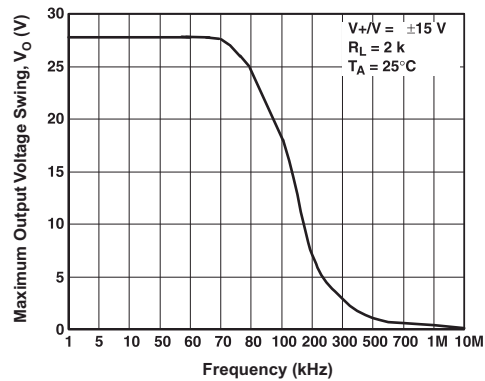
$V_{CC\pm} = \pm 15\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
SR Slew rate at unity gain	$R_L \geq 2\text{ k}\Omega$	5	V/ μs
GBW Gain-bandwidth product	$f = 10\text{ kHz}$	12	MHz
THD Total harmonic distortion	$V_O = 5\text{ V}$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $A_{VD} = 20\text{ dB}$	0.0005%	
V_n Equivalent input noise voltage	RIAA, $R_S \leq 2.2\text{ k}\Omega$, 30kHz LPF	0.8	μVrms

5.7 Typical Characteristics



5-1. Maximum Output Voltage Swing vs Load Resistance



5-2. Maximum Output Voltage Swing vs Frequency

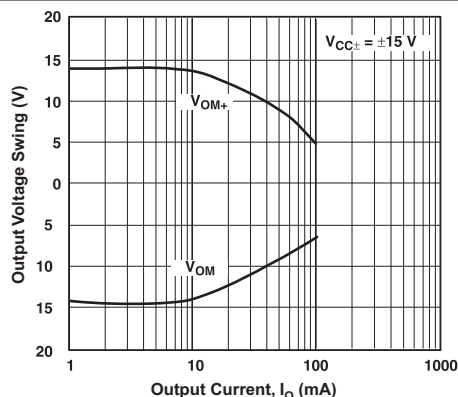


図 5-3. Output Voltage Swing vs Output Current

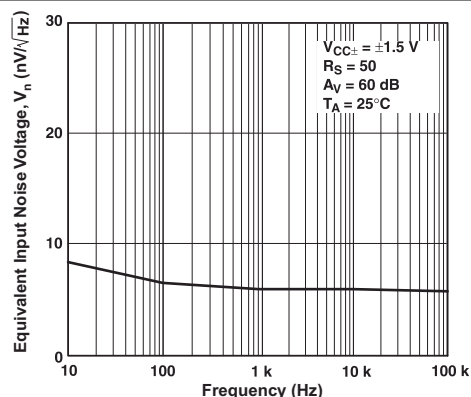


図 5-4. Equivalent Input Noise Voltage vs Frequency

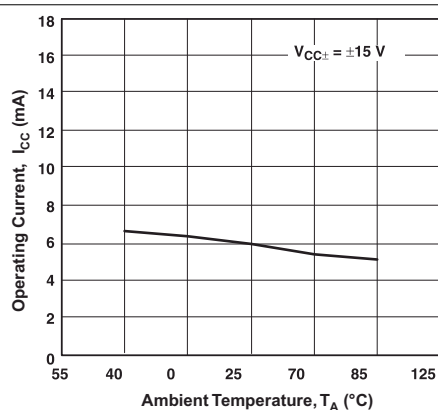


図 5-5. Operating Current vs Temperature

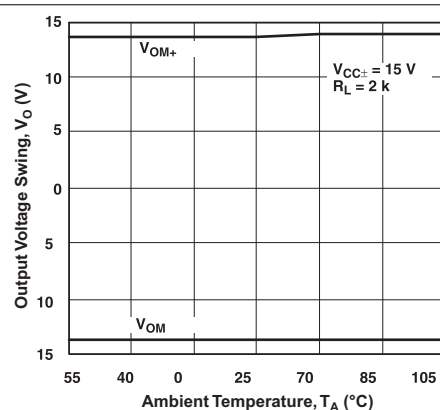


図 5-6. Output Voltage Swing vs Temperature

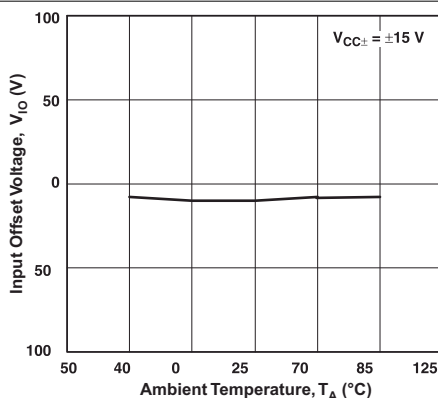


図 5-7. Input Offset Voltage vs Temperature

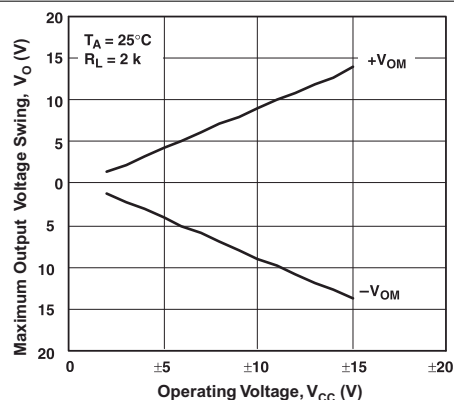


図 5-8. Input Bias Current vs Temperature

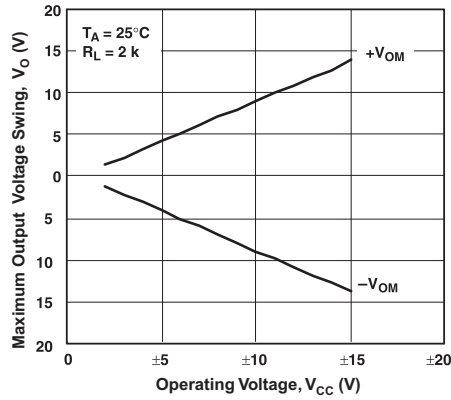


図 5-9. Maximum Output Voltage Swing vs Operating Voltage

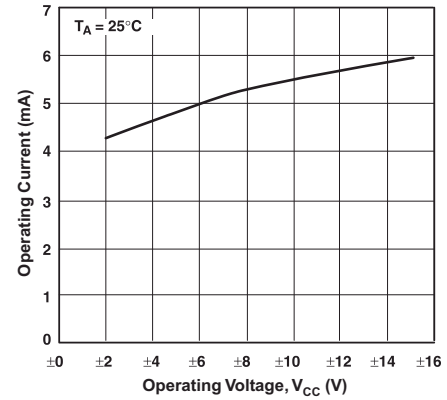


図 5-10. Operating Current vs Operating Voltage

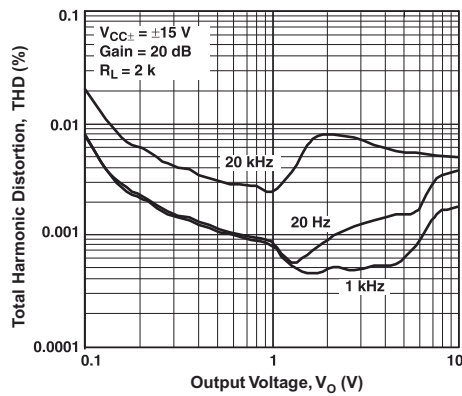


図 5-11. Total Harmonic Distortion vs Output Voltage

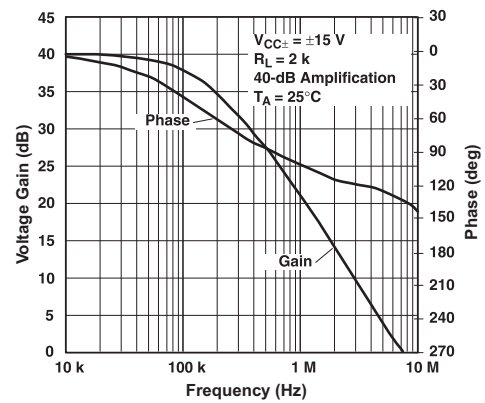


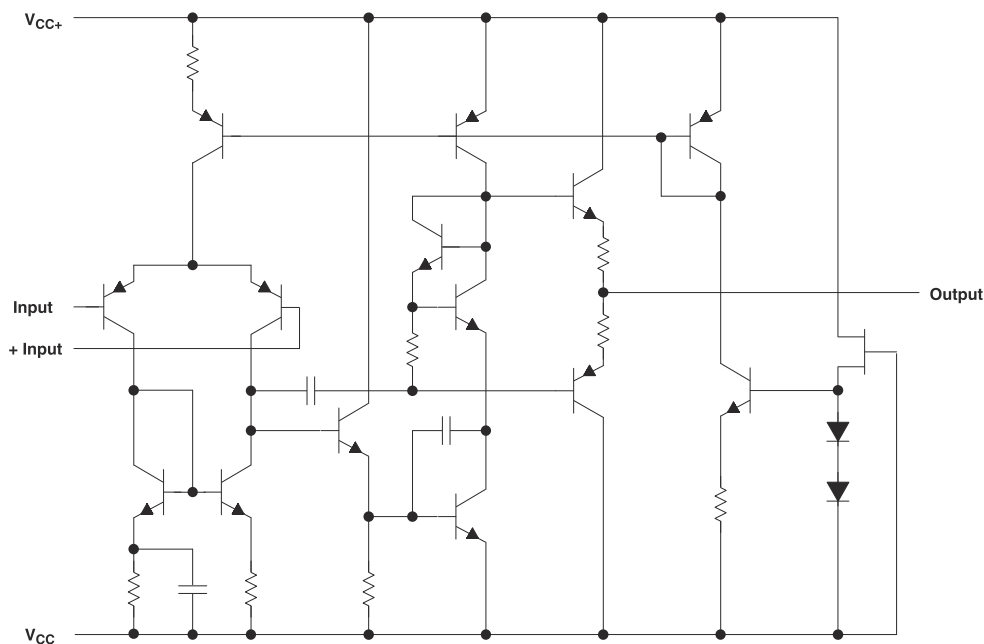
図 5-12. Voltage Gain, Phase vs Frequency

6 Detailed Description

6.1 Overview

The RC4580 device is a dual operational amplifier that has been designed optimally for audio applications, such as improving tone control. The device offers low noise, high gain bandwidth, low harmonic distortion, and high output current. When high output current is required, the RC4580 device can be used as a headphone amplifier. Due to the wide operating supply voltage of the device, the RC4580 device can also be used in low-voltage applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The RC4580 device has a 12MHz unity-gain bandwidth.

6.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. The CMRR is found by taking the ratio of the change in input offset voltage to the change in the input voltage, then converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have the CMRR as high as possible. The CMRR of the RC4580 device is 110dB.

6.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change the op amp output when there is a change on the input. The RC4580 device has a 5V/μs slew rate.

6.4 Device Functional Mode

The RC4580 device is powered on when the supply is connected. Each device can operate as a single-supply operational amplifier or dual-supply amplifier depending on the application.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Typical Application

Some applications require differential signals. 図 7-1 shows a simple circuit to convert a single-ended input of 2V to 10V into differential output of $\pm 8V$ on a single 15V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+} . The second amplifier inverts the input and adds a reference voltage to generate V_{OUT-} . Both V_{OUT+} and V_{OUT-} range from 2V to 10V. The difference, V_{DIFF} , is the difference between V_{OUT+} and V_{OUT-} .

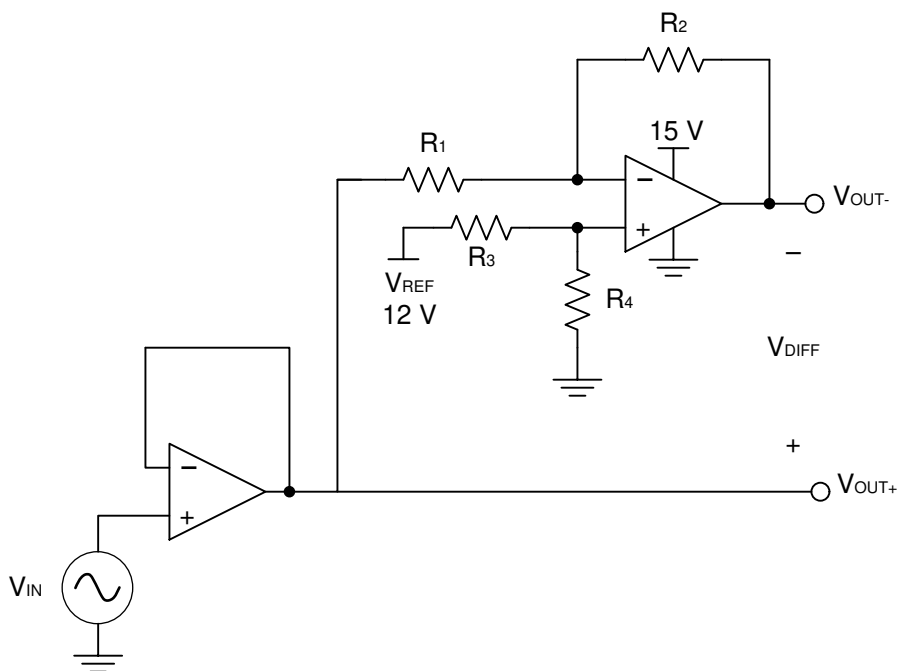


図 7-1. Schematic for Single-Ended Input to Differential Output Conversion

7.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15V
- Reference voltage: 12V
- Input: 2V to 10V
- Output differential: $\pm 8V$

7.1.2 Detailed Design Procedure

The circuit in [Figure 7-1](#) takes a single-ended input signal, V_{IN} , and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF} . V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (see [Equation 1](#)). V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is [Equation 2](#).

$$V_{OUT+} = V_{IN} \quad (1)$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4} \right) \times \left(1 + \frac{R_2}{R_1} \right) - V_{IN} \times \frac{R_2}{R_1} \quad (2)$$

The differential output signal, V_{DIFF} , is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-} . [Equation 3](#) shows the transfer function for V_{DIFF} . By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into [Equation 6](#). Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF} . The differential output range is $2 \times V_{REF}$. Furthermore, the common-mode voltage is one half of V_{REF} (see [Equation 7](#)).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1} \right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4} \right) \left(1 + \frac{R_2}{R_1} \right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2} \right) = \frac{1}{2} V_{REF} \quad (7)$$

7.1.2.1 Amplifier Selection

Linearity over the input range is key for good DC accuracy. The common-mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. The RC4580 device has a bandwidth of 12MHz, therefore this circuit is only be able to process signals with frequencies of less than 12MHz.

7.1.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} is heavily reliant on resistors (R_1 , R_2 , R_3 , and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36k Ω with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6k Ω or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

7.1.3 Application Curves

The measured transfer functions in [図 7-2](#), [図 7-3](#), and [図 7-4](#) were generated by sweeping the input voltage from 0V to 12V. However, this design should only be used between 2V and 10V for optimum linearity.

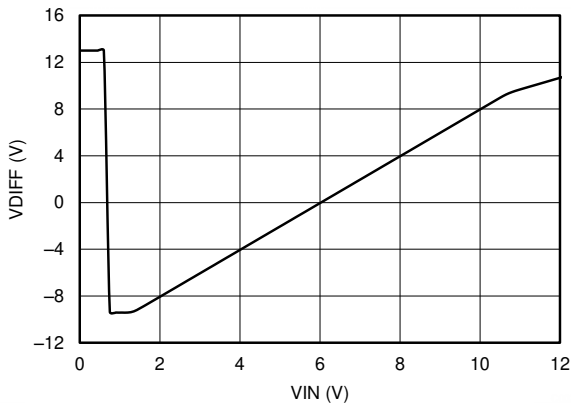


図 7-2. Differential Output Voltage vs Input Voltage

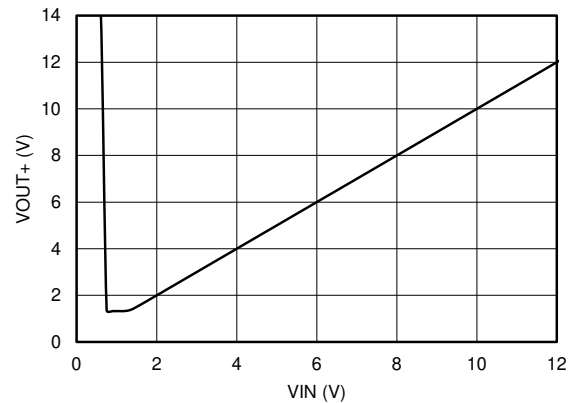


図 7-3. Positive Output Voltage vs Input Voltage

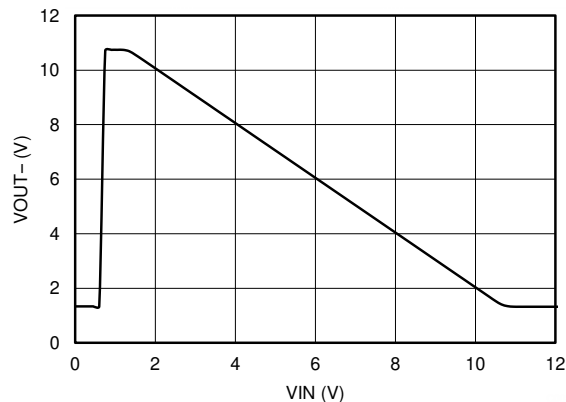


図 7-4. Positive Output Voltage vs Input Voltage

7.2 Power Supply Recommendations

The RC4580 device is specified for operation over the range of $\pm 2\text{V}$ to $\pm 16\text{V}$; many specifications apply from -40°C to 125°C . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

注意

Supply voltages outside of the $\pm 18\text{V}$ range can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place $0.1\mu\text{F}$ bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout Guidelines](#).

7.3 Layout

7.3.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1 μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V^+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

7.3.2 Layout Example

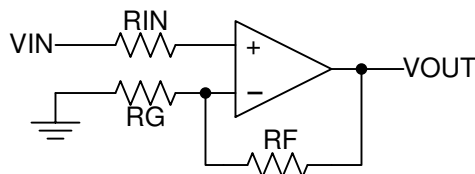


图 7-5. Operational Amplifier Schematic for Noninverting Configuration

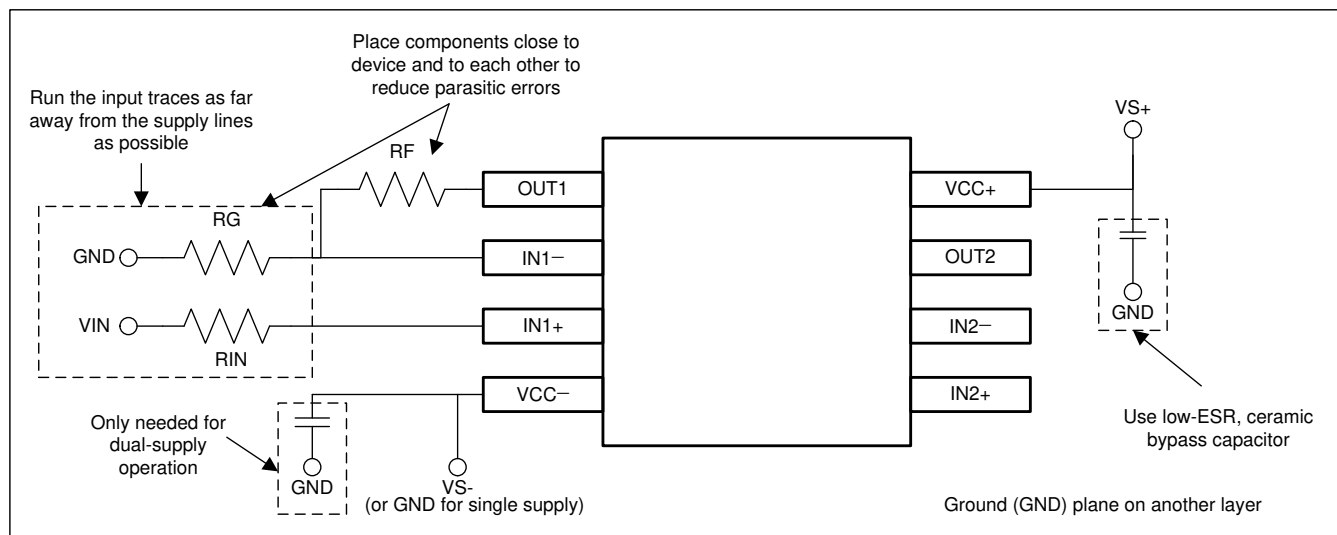


图 7-6. Operational Amplifier Board Layout for Noninverting Configuration

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

Changes from Revision D (November 2014) to Revision E (November 2024)	Page
ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
P (PDIP, 8)、DGK (VSSOP, 8)、DDF (SOT-23, 8) パッケージをデータシートに追加.....	1
Changed the slew rate value listed in the <i>Slew Rate</i> section from: 5V/ms to: 5V/μs to match the slew rate values listed in the <i>Features</i> section and <i>Electrical Characteristics</i> table.....	8
Deleted references to the <i>Circuit Board Layout Techniques</i> application note.....	11

Changes from Revision C (March 2004) to Revision D (November 2014)	Page
「アプリケーション」、「デバイス情報」表、「ピンの機能」表、「取り扱い定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。.....	1
「注文情報」表を削除。.....	1
Changed $T_A = 25^{\circ}\text{C}$ to $T_A = -40^{\circ}\text{C}$ to 125°C in condition statement for <i>Electrical Characteristics</i> table and <i>Operational Characteristics</i> table.....	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
RC4580IDDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4580F
RC4580IDDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4580F
RC4580IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4580
RC4580IDGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4580
RC4580IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580I
RC4580IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580I
RC4580IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	RC4580IP
RC4580IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	RC4580IP
RC4580IPW	Obsolete	Production	TSSOP (PW) 8	-	-	Call TI	Call TI	-40 to 125	R4580I
RC4580IPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580I
RC4580IPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R4580I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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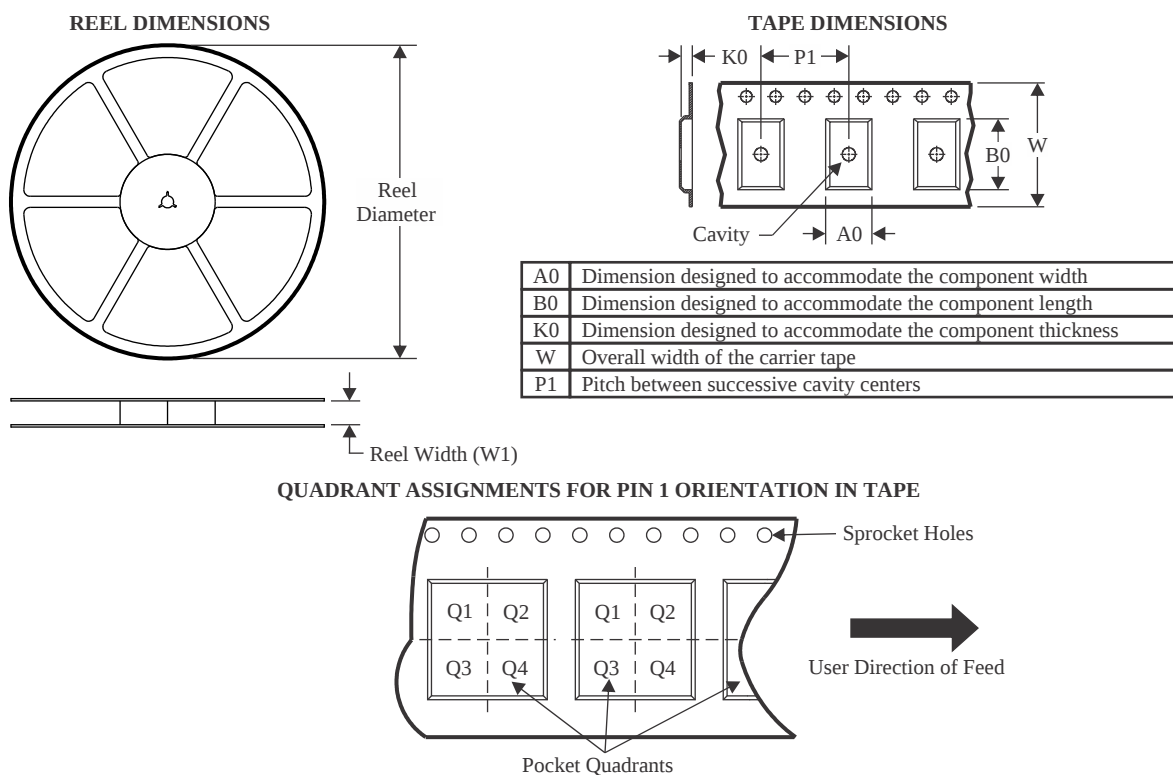
OTHER QUALIFIED VERSIONS OF RC4580 :

- Automotive : [RC4580-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

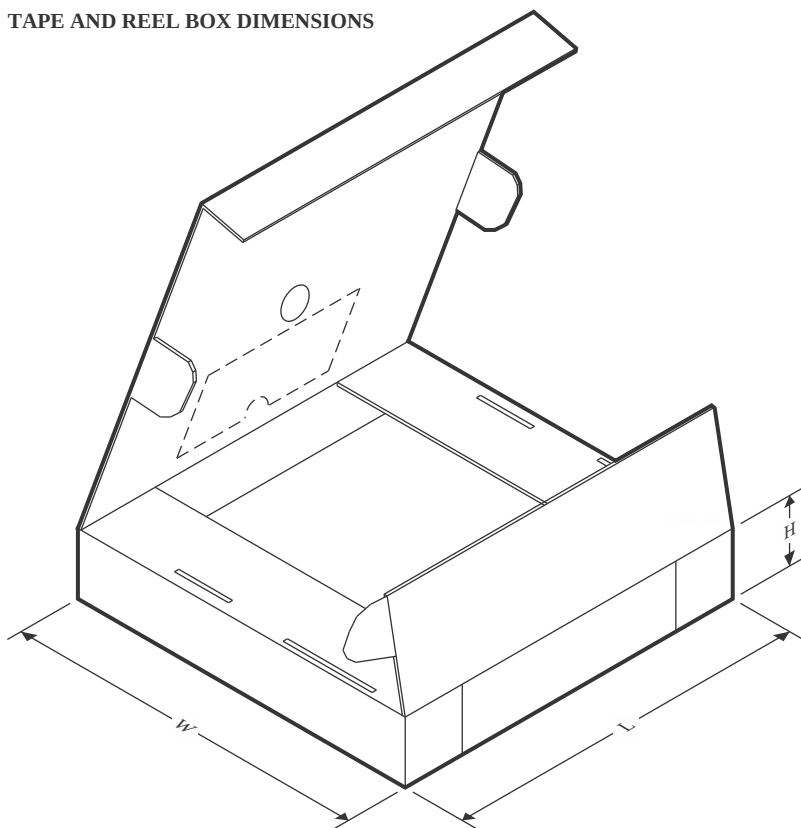
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4580IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
RC4580IDGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4580IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4580IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

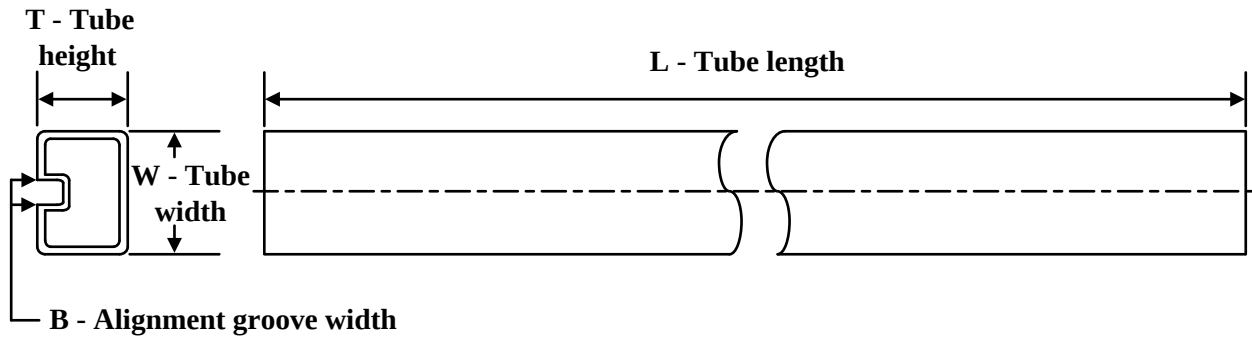
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4580IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
RC4580IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
RC4580IDR	SOIC	D	8	2500	353.0	353.0	32.0
RC4580IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

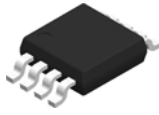
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
RC4580IP	P	PDIP	8	50	506	13.97	11230	4.32
RC4580IP.A	P	PDIP	8	50	506	13.97	11230	4.32

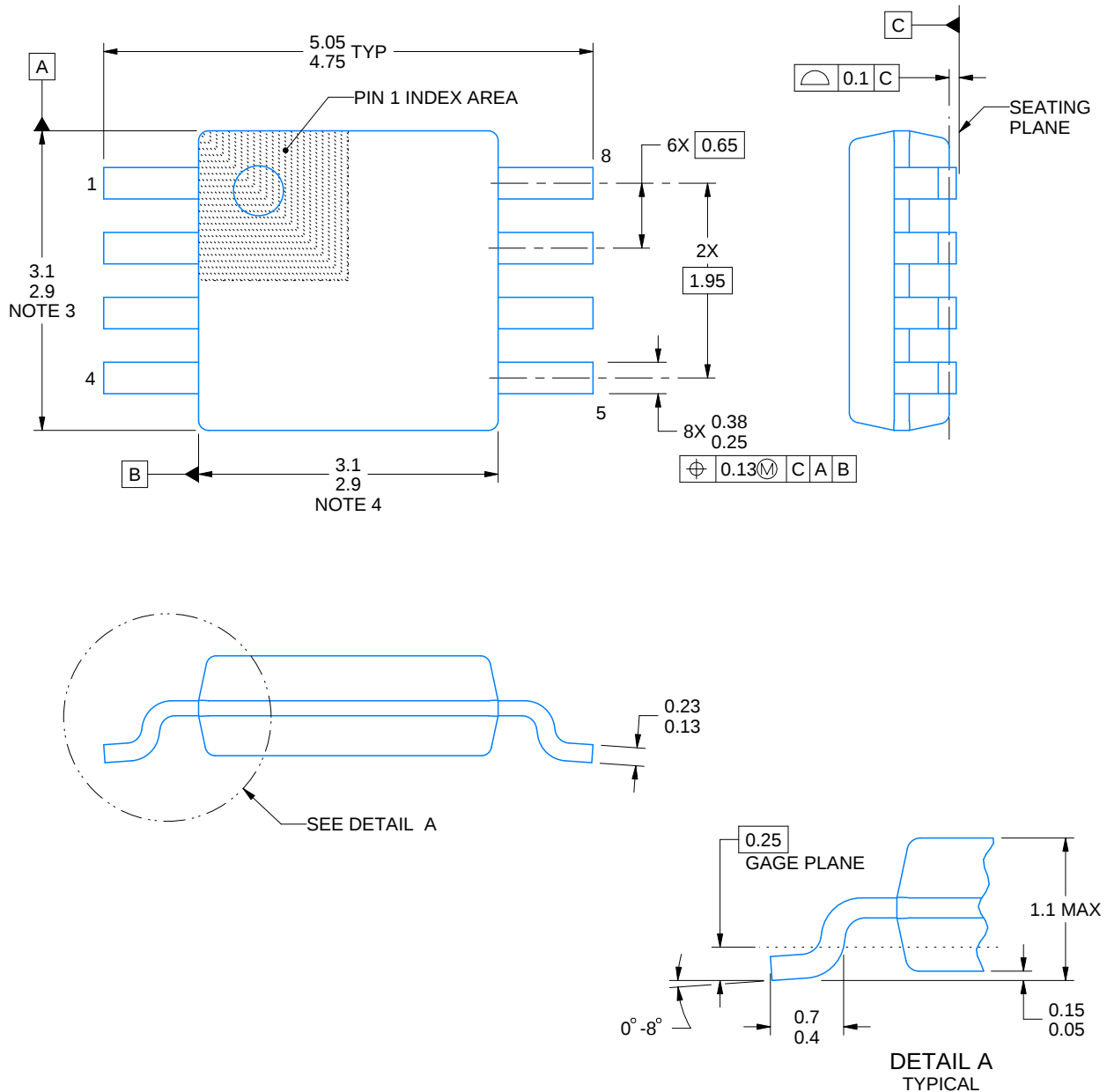
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

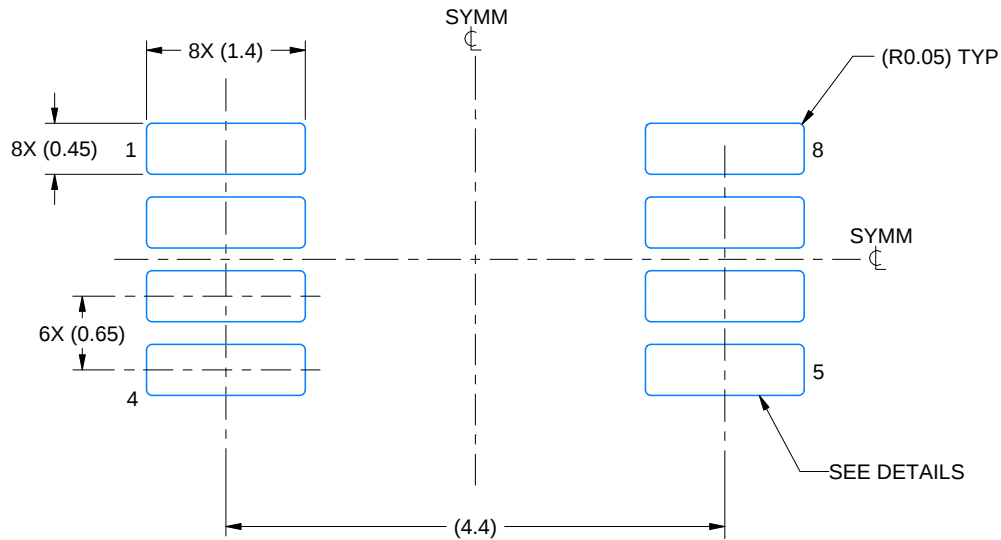
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

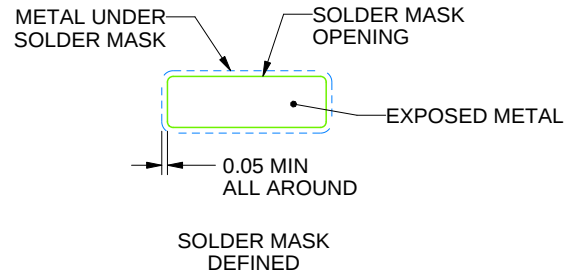
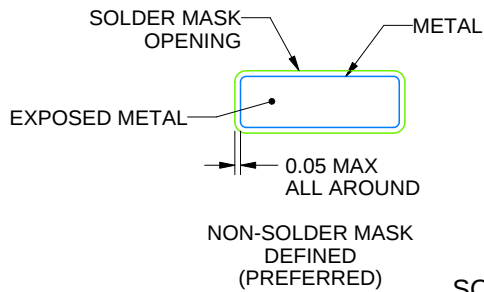
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

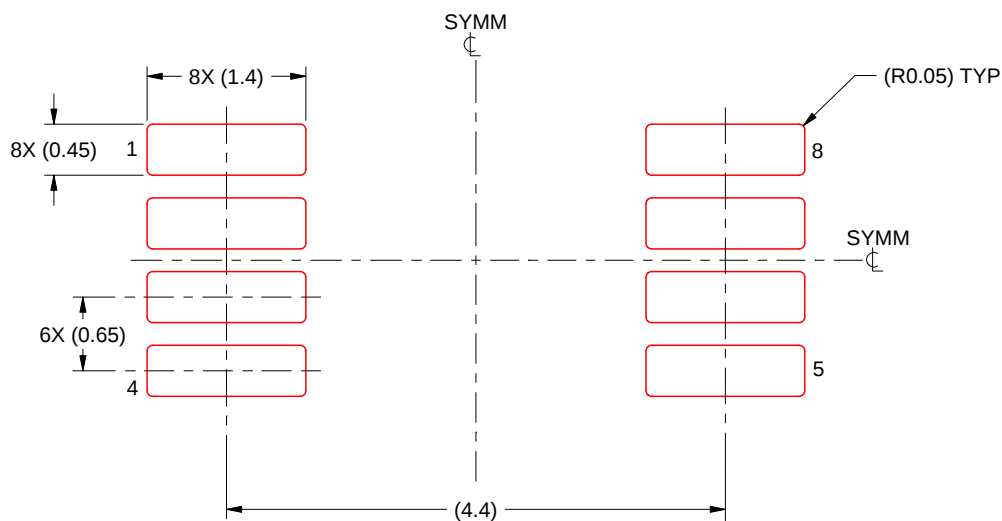
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

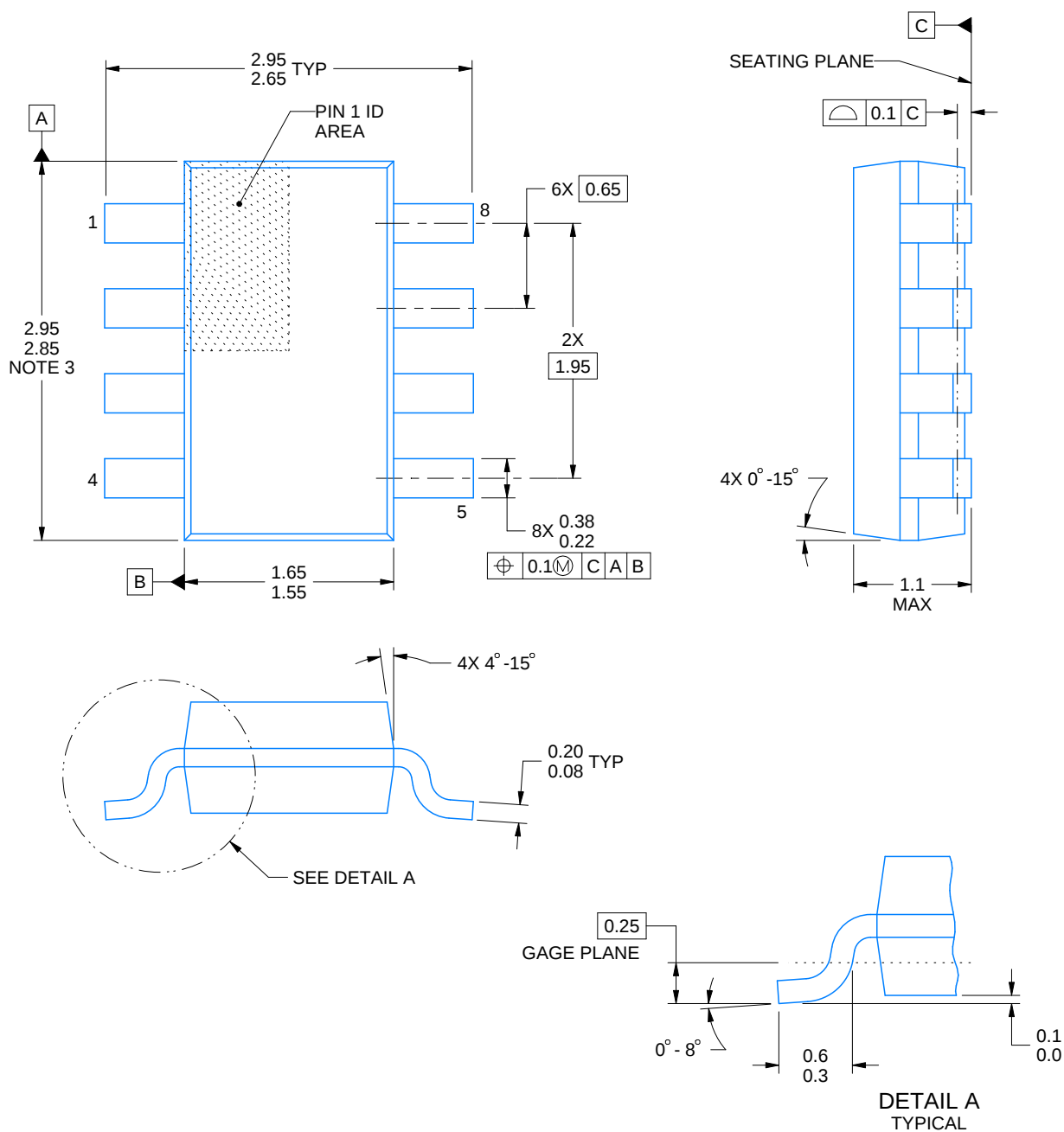
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

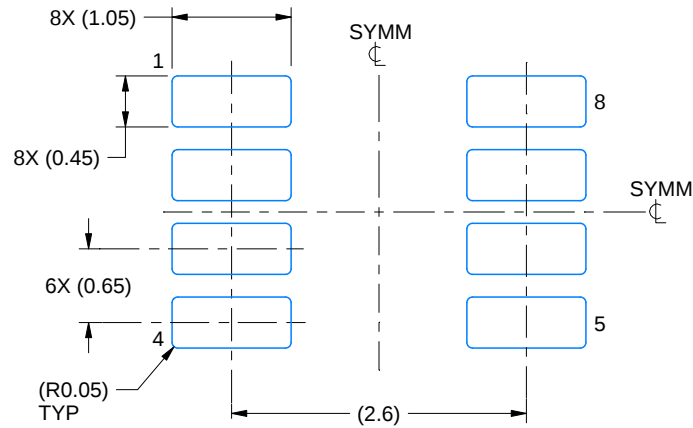
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

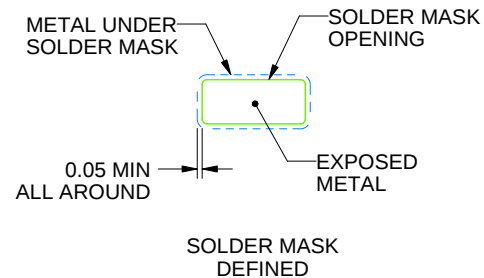
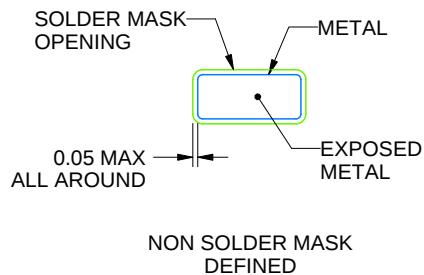
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

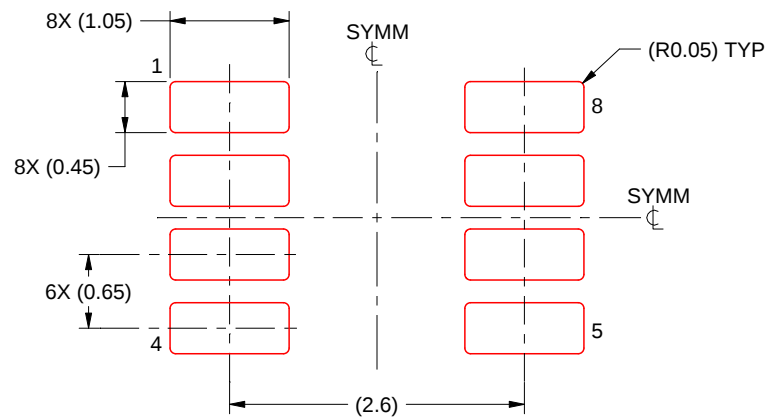
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



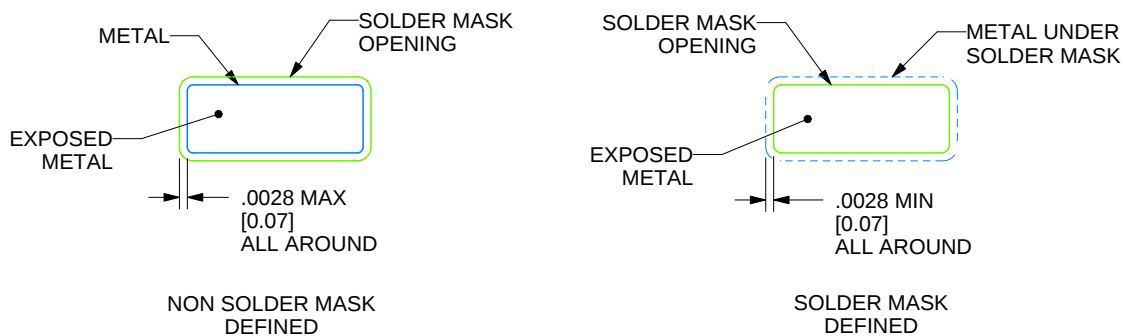
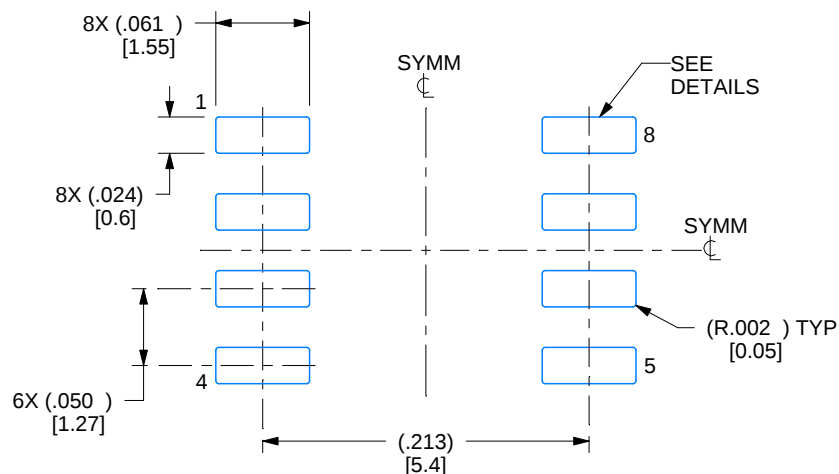
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

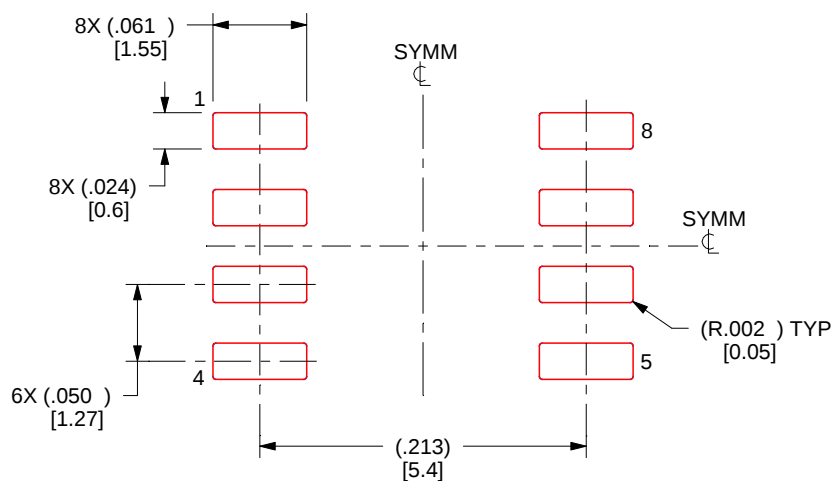
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

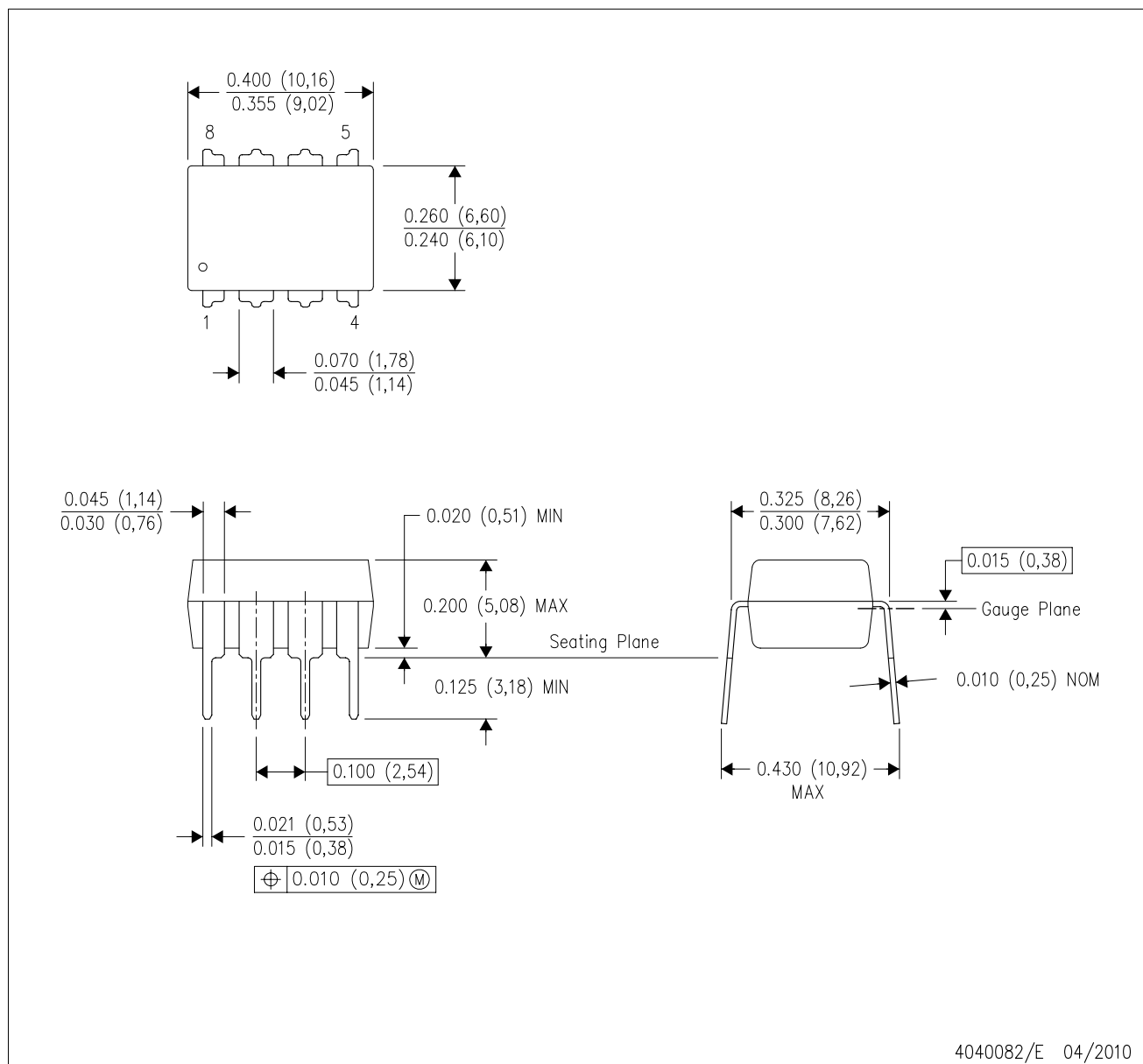
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



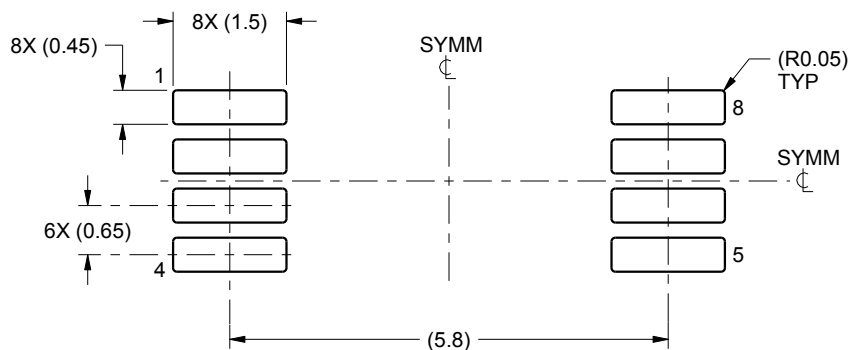
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

EXAMPLE BOARD LAYOUT

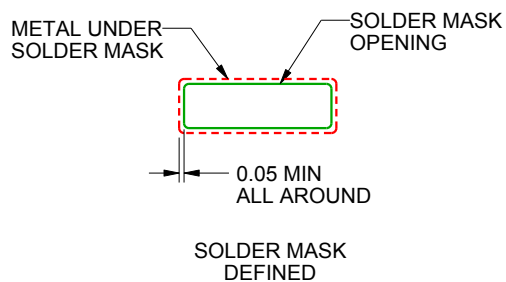
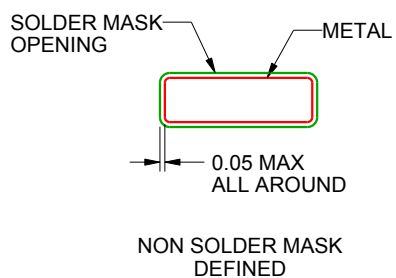
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

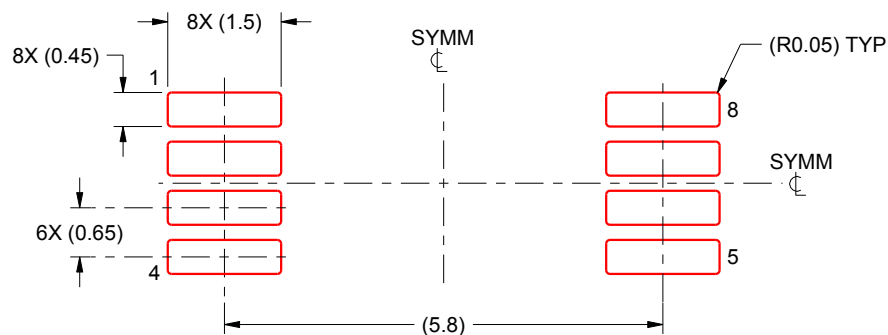
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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