

# SNx4AC373 3 ステート出力、オクタール D タイプ・トランスペアレント・ラッチ

## 1 特長

- 2V~6V の  $V_{CC}$  で動作
- 6V までの入力電圧に対応
- 最大  $t_{pd}$  9.5ns (5V 時)
- 3 ステート非反転出力はバスラインを直接駆動
- 読み込み時の完全並列アクセス

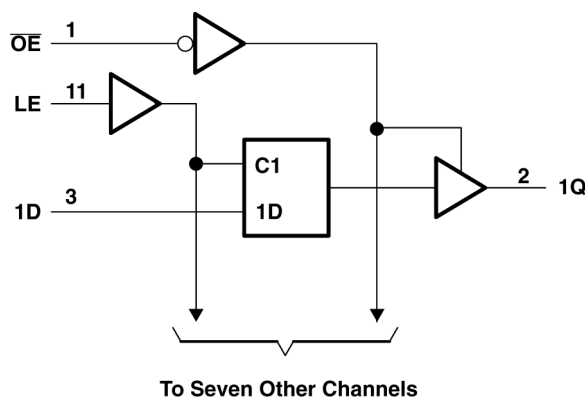
## 2 概要

これらの 8 ビット ラッチは、大きな容量性負荷または比較的低いインピーダンスの負荷の駆動用に設計された 3 ステート出力を備えています。本デバイスは、バッファレジスタ、I/O ポート、双方向バスドライバ、作業レジスタの実装に特に適しています。

### 製品情報

| 部品番号      | パッケージ <sup>(1)</sup> | パッケージサイズ <sup>(2)</sup> | 本体サイズ <sup>(3)</sup> |
|-----------|----------------------|-------------------------|----------------------|
| SNx4AC373 | DB (SSOP, 20)        | 7.2mm × 7.8mm           | 7.2mm × 5.30mm       |
|           | DW (SOIC, 20)        | 12.80mm × 10.3mm        | 12.80mm × 7.50mm     |
|           | N (PDIP, 20)         | 24.33mm × 9.4mm         | 24.33mm × 6.35mm     |
|           | NS (SOP, 20)         | 12.6mm × 7.8mm          | 12.6mm × 5.3mm       |
|           | PW (TSSOP, 20)       | 6.50mm × 6.4mm          | 6.50mm × 4.40mm      |

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) パッケージサイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



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### 3 Pin Configuration and Functions

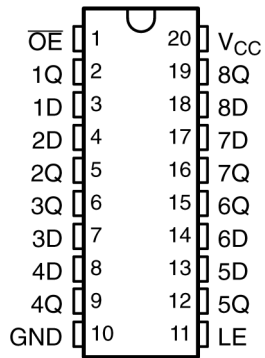


图 3-1. SN54AC373 J or W Package; SN74AC373 DB, DW, N, NS, or PW Package (Top View)

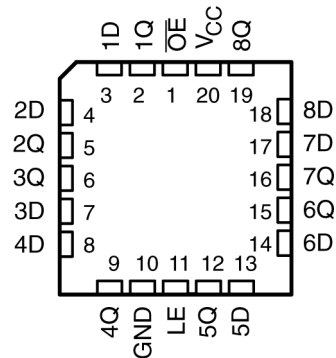


图 3-2. SN54AC373 FK Package (Top View)

表 3-1. Pin Functions

| NO. | PIN                             |                 | TYPE | DESCRIPTION                       |
|-----|---------------------------------|-----------------|------|-----------------------------------|
|     | SSOP, TVSOP, SOIC, SO, or TSSOP | VQFN            |      |                                   |
| 1   | OE                              | OE              | I    | Output Enable                     |
| 2   | 1Q                              | 1Q              | O    | 1Q Output                         |
| 3   | 1D                              | 1D              | I    | 1D Input                          |
| 4   | 2D                              | 2D              | I    | 2D Input                          |
| 5   | 2Q                              | 2Q              | O    | 2Q Output                         |
| 6   | 3Q                              | 3Q              | O    | 3Q Output                         |
| 7   | 3D                              | 3D              | I    | 3D Input                          |
| 8   | 4D                              | 4D              | I    | 4D Input                          |
| 9   | 4Q                              | 4Q              | O    | 4Q Output                         |
| 10  | GND                             | GND             | —    | Ground Pin                        |
| 11  | LE                              | LE              | I    | Latch Enable                      |
| 12  | 5Q                              | 5Q              | O    | 5Q Output                         |
| 13  | 5D                              | 5D              | I    | 5D Input                          |
| 14  | 6D                              | 6D              | I    | 6D Input                          |
| 15  | 6Q                              | 6Q              | O    | 6Q Output                         |
| 16  | 7Q                              | 7Q              | O    | 7Q Output                         |
| 17  | 7D                              | 7D              | I    | 7D Input                          |
| 18  | 8D                              | 8D              | I    | 8D Input                          |
| 19  | 8Q                              | 8Q              | O    | 8Q Output                         |
| 20  | V <sub>CC</sub>                 | V <sub>CC</sub> | —    | Power Pin                         |
| —   | —                               | Thermal Pad     | —    | Thermal Pad, normally tied to GND |

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>1</sup>

|   |                           | MIN   | MAX                   | UNIT    |
|---|---------------------------|---|-----------------------|---------|
| V <sub>CC</sub>                                   | Supply voltage range      | -0.5  | 7                     | V       |
| V <sub>I</sub> <sup>1</sup>                       | Input voltage range       | -0.5  | V <sub>CC</sub> + 0.5 | V       |
| V <sub>O</sub> <sup>1</sup>                       | Output voltage range      | -0.5  | V <sub>CC</sub> + 0.5 | V       |
| I <sub>IK</sub>                                   | Input clamp current       | (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> ) |                       | ±20 mA  |
| I <sub>OK</sub>                                   | Output clamp current      | (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) |                       | ±20 mA  |
| I <sub>O</sub>                                    | Continuous output current | (V <sub>O</sub> = 0 to V <sub>CC</sub> )                  |                       | ±50 mA  |
| Continuous current through V <sub>CC</sub> or GND |                           |   |                       | ±200 mA |
| T <sub>stg</sub>                                  | Storage temperature range | -65   | 150                   | °C      |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)<sup>1</sup>

|                 |                                    | SN54AC373               |                 | SN74AC373 |                 | UNIT |
|-----------------|------------------------------------|-------------------------|-----------------|-----------|-----------------|------|
|                 |                                    | MIN                     | MAX             | MIN       | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     | 2                       | 6               | 2         | 6               | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 3 V   | 2.1             | 2.1       |                 | V    |
|                 |                                    | V <sub>CC</sub> = 4.5 V | 3.15            | 3.15      |                 |      |
|                 |                                    | V <sub>CC</sub> = 5.5 V | 3.85            | 3.85      |                 |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 3 V   |                 | 0.9       | 0.9             | V    |
|                 |                                    | V <sub>CC</sub> = 4.5 V |                 | 1.35      | 1.35            |      |
|                 |                                    | V <sub>CC</sub> = 5.5 V |                 | 1.65      | 1.65            |      |
| V <sub>I</sub>  | Input voltage                      | 0                       | V <sub>CC</sub> | 0         | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                     | 0                       | V <sub>CC</sub> | 0         | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 3 V   |                 | -12       | -12             | mA   |
|                 |                                    | V <sub>CC</sub> = 4.5 V |                 | -24       | -24             |      |
|                 |                                    | V <sub>CC</sub> = 5.5 V |                 | -24       | -24             |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 3 V   |                 | 12        | 12              | mA   |
|                 |                                    | V <sub>CC</sub> = 4.5 V |                 | 24        | 24              |      |
|                 |                                    | V <sub>CC</sub> = 5.5 V |                 | 24        | 24              |      |
| Δt/Δv           | Input transition rise or fall rate |                         | 8               |           | 8               | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     | -55                     | 125             | -40       | 85              | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 4.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup>                           | SNx4AC373 |           |    |         |            | UNIT |
|---|-----------|-----------|----|---------|------------|------|
|   | DB (SSOP) | DW (SOIC) | N  | NS (SO) | PW (TSSOP) |      |
|   | 20 PINS   |           |    |         |            |      |
| R <sub>θJA</sub> Junction-to-ambient thermal resistance | 70        | 101.2     | 69 | 60      | 126.2      | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS   | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54AC373 |      | SN74AC373 |     | UNIT |
|-----------------|---|-----------------|-----------------------|-----|-----|-----------|------|-----------|-----|------|
|                 |   |                 | MIN                   | TYP | MAX | MIN       | MAX  | MIN       | MAX |      |
| V <sub>OH</sub> | I <sub>OH</sub> = -50μA                                     | 3 V             | 2.9                   |     |     | 2.9       | 2.9  |           | V   |      |
|                 |   | 4.5 V           | 4.4                   |     |     | 4.4       | 4.4  |           |     |      |
|                 |   | 5.5 V           | 5.4                   |     |     | 5.4       | 5.4  |           |     |      |
|                 | I <sub>OH</sub> = -12 mA                                    | 3 V             | 2.56                  |     |     | 2.4       | 2.46 |           |     |      |
|                 |   | 4.5 V           | 3.86                  |     |     | 3.7       | 3.76 |           |     |      |
|                 |   | 5.5 V           | 4.86                  |     |     | 4.7       | 4.76 |           |     |      |
| V <sub>OL</sub> | I <sub>OL</sub> = 50μA                                      | 3 V             | 0.1                   |     |     | 0.1       | 0.1  |           | V   |      |
|                 |   | 4.5 V           | 0.1                   |     |     | 0.1       | 0.1  |           |     |      |
|                 |   | 5.5 V           | 0.1                   |     |     | 0.1       | 0.1  |           |     |      |
|                 | I <sub>OL</sub> = 12 mA                                     | 3 V             | 0.36                  |     |     | 0.5       | 0.44 |           |     |      |
|                 |   | 4.5 V           | 0.36                  |     |     | 0.5       | 0.44 |           |     |      |
|                 |   | 5.5 V           | 0.36                  |     |     | 0.5       | 0.44 |           |     |      |
| I <sub>I</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5.5 V           | ±0.1                  |     |     | ±1        | ±1   |           | μA  |      |
| I <sub>OZ</sub> | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V           | ±0.25                 |     |     | ±5        | ±2.5 |           | μA  |      |
| I <sub>CC</sub> | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           | 4                     |     |     | 80        | 40   |           | μA  |      |
| C <sub>i</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             | 4.5                   |     |     |           |      |           | pF  |      |

### 4.5 Timing Requirements, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

|                 |                              | T <sub>A</sub> = 25°C |     | SN54AC373 |     | SN74AC373 |     | UNIT |
|-----------------|------------------------------|-----------------------|-----|-----------|-----|-----------|-----|------|
|                 |                              | MIN                   | MAX | MIN       | MAX | MIN       | MAX |      |
| t <sub>w</sub>  | Pulse duration, LE high      | 5.5                   |     | 6.5       |     | 6         |     | ns   |
| t <sub>su</sub> | Setup time, data before LE ↓ | 5.5                   |     | 6.5       |     | 6         |     | ns   |
| t <sub>h</sub>  | Hold time, data after LE ↓   | 1                     |     | 1         |     | 1         |     | ns   |

### 4.6 Timing Requirements, V<sub>CC</sub> = 5 V ± 0.5 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

|                 |                              | T <sub>A</sub> = 25°C |     | SN54AC373 |     | SN74AC373 |     | UNIT |
|-----------------|------------------------------|-----------------------|-----|-----------|-----|-----------|-----|------|
|                 |                              | MIN                   | MAX | MIN       | MAX | MIN       | MAX |      |
| t <sub>w</sub>  | Pulse duration, LE high      | 4                     |     | 5         |     | 4.5       |     | ns   |
| t <sub>su</sub> | Setup time, data before LE ↓ | 4                     |     | 5         |     | 4.5       |     | ns   |
| t <sub>h</sub>  | Hold time, data after LE ↓   | 1                     |     | 1         |     | 1         |     | ns   |

#### 4.7 Switching Characteristics, $V_{CC} = 3.3 V \pm 0.3 V$

over recommended operating free-air temperature range,  $V_{CC} = 3.3 V \pm 0.3 V$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | TO (INPUT)      | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ |     |      | SN54AC373 |      | SN74AC373 |      | UNIT |
|-----------|-----------------|-------------|--------------------------|-----|------|-----------|------|-----------|------|------|
|           |                 |             | MIN                      | TYP | MAX  | MIN       | MAX  | MIN       | MAX  |      |
| $t_{PLH}$ | D               | Q           | 1.5                      | 10  | 13.5 | 1         | 16.5 | 1.5       | 15   | ns   |
| $t_{PHL}$ |                 |             | 1.5                      | 9.5 | 13.0 | 1         | 16   | 1.5       | 14.5 |      |
| $t_{PLH}$ | LE              | Q           | 1.5                      | 10  | 13.5 | 1         | 16.5 | 1.5       | 15   | ns   |
| $t_{PHL}$ |                 |             | 1.5                      | 9.5 | 12.5 | 1         | 15   | 1.5       | 14   |      |
| $t_{PZH}$ | $\overline{OE}$ | Q           | 1.5                      | 9   | 11.5 | 1         | 14   | 1         | 13   | ns   |
| $t_{PZL}$ |                 |             | 1.5                      | 8.5 | 11.5 | 1         | 13.5 | 1         | 13   |      |
| $t_{PHZ}$ | $\overline{OE}$ | Q           | 1.5                      | 10  | 12.5 | 1         | 16   | 1         | 14.5 | ns   |
| $t_{PLZ}$ |                 |             | 1.5                      | 8   | 11.5 | 1         | 13   | 1         | 12.5 |      |

#### 4.8 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

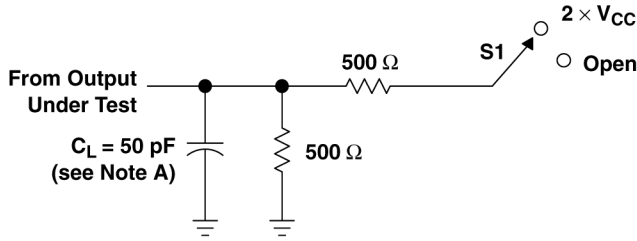
| PARAMETER | TO (INPUT)      | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ |     |     | SN54AC373 |      | SN74AC373 |      | UNIT |
|-----------|-----------------|-------------|--------------------------|-----|-----|-----------|------|-----------|------|------|
|           |                 |             | MIN                      | TYP | MAX | MIN       | MAX  | MIN       | MAX  |      |
| $t_{PLH}$ | D               | Q           | 1.5                      | 7   | 9.5 | 1         | 11.5 | 1.5       | 10.5 | ns   |
| $t_{PHL}$ |                 |             | 1.5                      | 7   | 9.5 | 1         | 11.5 | 1.5       | 10.5 |      |
| $t_{PLH}$ | LE              | Q           | 1.5                      | 7.5 | 9.5 | 1         | 12   | 1.5       | 10.5 | ns   |
| $t_{PHL}$ |                 |             | 1.5                      | 7   | 9.5 | 1         | 11   | 1.5       | 10.5 |      |
| $t_{PZH}$ | $\overline{OE}$ | Q           | 1.5                      | 7   | 8.5 | 1         | 10.5 | 1         | 9.5  | ns   |
| $t_{PZL}$ |                 |             | 1.5                      | 6.5 | 8.5 | 1         | 10   | 1         | 9.5  |      |
| $t_{PHZ}$ | $\overline{OE}$ | Q           | 1.5                      | 8   | 11  | 1         | 13.5 | 1         | 12.5 | ns   |
| $t_{PLZ}$ |                 |             | 1.5                      | 6.5 | 8.5 | 1         | 10.5 | 1         | 10   |      |

#### 4.9 Operating Characteristics

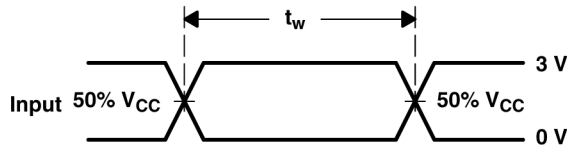
$V_{CC} = 5 V$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER                              | TEST CONDITIONS                             | TYP | UNIT |
|--|---|-----|------|
| $C_{pd}$ Power dissipation capacitance | $C_L = 50 \text{ pF}$ , $f = 1 \text{ MHz}$ | 40  | pF   |

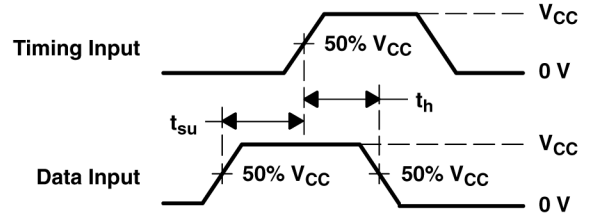
## 5 Parameter Measurement Information



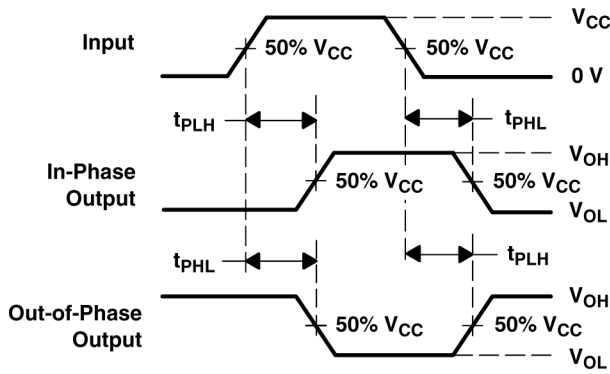
LOAD CIRCUIT



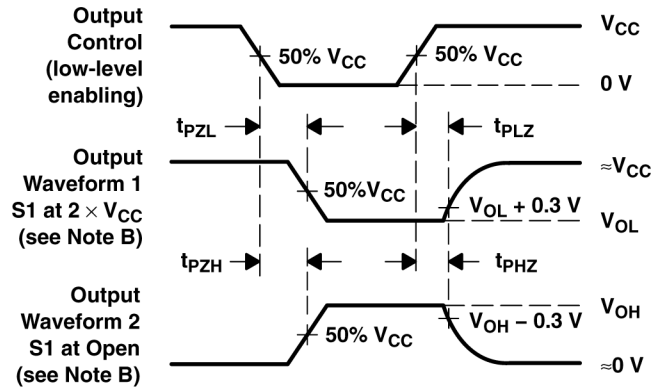
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- The outputs are measured one at a time with one input transition per measurement.

图 5-1. Load Circuit and Voltage Waveforms

| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open              |

## 6 Detailed Description

### 6.1 Overview

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

For specified high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 6.2 Functional Block Diagram

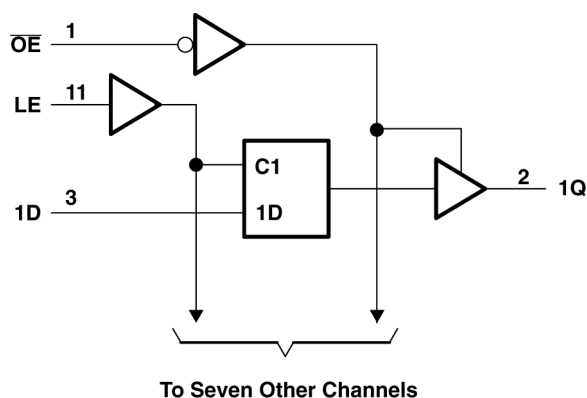


図 6-1. Logic Diagram (Positive Logic)

### 6.3 Device Functional Modes

表 6-1. Function Table (Each Latch)

| INPUTS          |    |   | OUTPUT Q |
|-----------------|----|---|----------|
| $\overline{OE}$ | LE | D |          |
| L               | H  | H | H        |
| L               | H  | L | L        |
| L               | L  | X | $Q_0$    |
| H               | X  | X | Z        |



## 7 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 7.1 Power Supply Recommendations

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Layout Diagram](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

#### 7.2.2 Layout Example

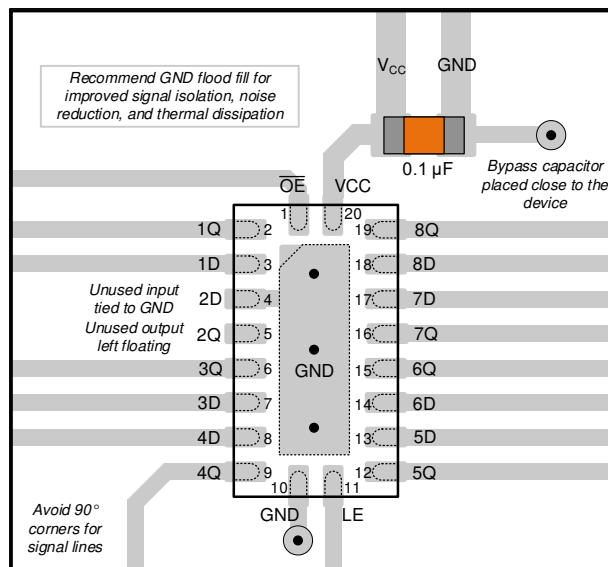


図 7-1. Layout example for the SNx4AC373

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

| PARTS     | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54AC373 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| SN74AC373 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

### 8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision E (August 2023) to Revision F (February 2024)                 | Page |
|---|------|
| • Updated RθJA values: DW = 58 to 101.2, PW = 83 to 126.2, all values in °C/W ..... | 5    |
| • Added <i>Application and Implementation</i> section.....                          | 9    |

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**Changes from Revision D (October 2003) to Revision E (August 2023)**

**Page**

- 「製品情報」表、「ピンの機能」表、「熱に関する情報」表、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ..... **1**
-

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)  | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)            | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| 5962-87555012A   | ACTIVE        | LCCC         | FK              | 20   | 55          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-87555012A<br>SNJ54AC<br>373FK | <a href="#">Samples</a> |
| 5962-8755501RA   | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8755501RA<br>SNJ54AC373J      | <a href="#">Samples</a> |
| 5962-8755501SA   | ACTIVE        | CFP          | W               | 20   | 25          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8755501SA<br>SNJ54AC373W      | <a href="#">Samples</a> |
| 5962-8755501VSA  | ACTIVE        | CFP          | W               | 20   | 25          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8755501VSA<br>SNV54AC373W     | <a href="#">Samples</a> |
| SN74AC373DBR     | ACTIVE        | SSOP         | DB              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AC373                              | <a href="#">Samples</a> |
| SN74AC373DW      | OBSOLETE      | SOIC         | DW              | 20   |             | TBD              | Call TI                              | Call TI              | -40 to 85    | AC373                              |                         |
| SN74AC373DWR     | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AC373                              | <a href="#">Samples</a> |
| SN74AC373DWRE4   | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AC373                              | <a href="#">Samples</a> |
| SN74AC373N       | ACTIVE        | PDIP         | N               | 20   | 20          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74AC373N                         | <a href="#">Samples</a> |
| SN74AC373NE4     | ACTIVE        | PDIP         | N               | 20   | 20          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74AC373N                         | <a href="#">Samples</a> |
| SN74AC373NSR     | ACTIVE        | SOP          | NS              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AC373                              | <a href="#">Samples</a> |
| SN74AC373PW      | OBSOLETE      | TSSOP        | PW              | 20   |             | TBD              | Call TI                              | Call TI              | -40 to 85    | AC373                              |                         |
| SN74AC373PWR     | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AC373                              | <a href="#">Samples</a> |
| SNJ54AC373FK     | ACTIVE        | LCCC         | FK              | 20   | 55          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-87555012A<br>SNJ54AC<br>373FK | <a href="#">Samples</a> |
| SNJ54AC373J      | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8755501RA<br>SNJ54AC373J      | <a href="#">Samples</a> |
| SNJ54AC373W      | ACTIVE        | CFP          | W               | 20   | 25          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8755501SA<br>SNJ54AC373W      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AC373, SN54AC373-SP, SN74AC373 :**

● Catalog : [SN74AC373](#), [SN54AC373](#)

● Enhanced Product : [SN74AC373-EP](#), [SN74AC373-EP](#)

● Military : [SN54AC373](#)

- Space : [SN54AC373-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AC373DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74AC373DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74AC373DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.9    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74AC373NSR | SOP          | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74AC373PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74AC373PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AC373DBR | SSOP         | DB              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AC373DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74AC373DWR | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74AC373NSR | SOP          | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74AC373PWR | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AC373PWR | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-87555012A  | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-8755501SA  | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| 5962-8755501VSA | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74AC373N      | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74AC373NE4    | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54AC373FK    | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54AC373W     | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

# PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

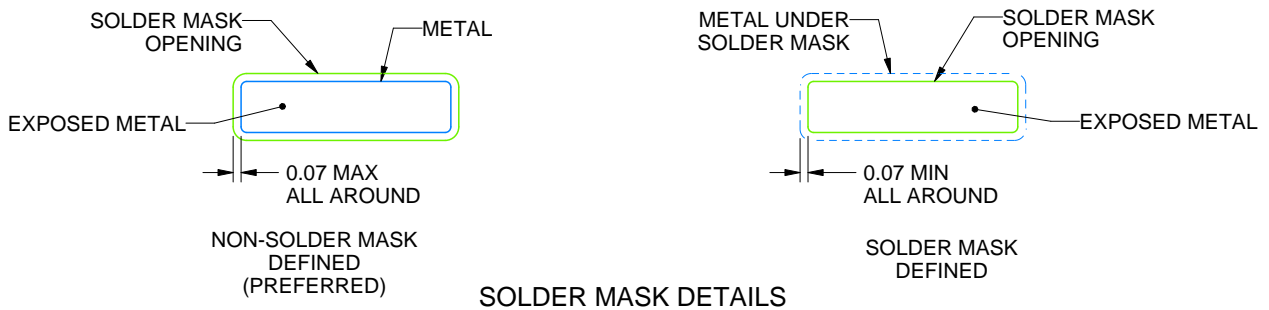
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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