

SNx4ACT11 トリプル 3 入力正論理 AND ゲート

1 特長

- 4.5V~5.5V の V_{CC} で動作
- 5.5V までの入力電圧に対応
- 最大 t_{pd} 10.5ns (5V 時)
- 入力は TTL 電圧互換

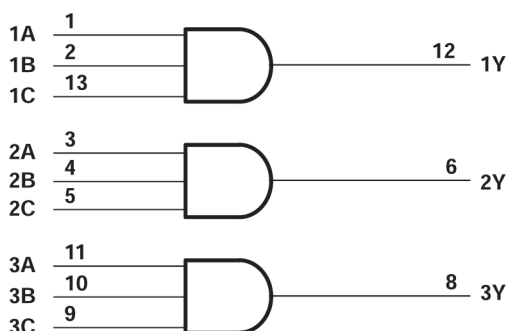
2 概要

'ACT11 デバイスには、3 つの独立した 3 入力 AND ゲートが内蔵されています。ブール関数 $Y = A \cdot B \cdot C$ つまり、 $Y = \bar{A} + \bar{B} + \bar{C}$ を正論理で実行します。

製品情報

部品番号	パッケージ ⁽¹⁾	パッケージサイズ ⁽²⁾	本体サイズ ⁽³⁾
SNx4ACT11	DB (SSOP, 14)	6.2mm × 7.8mm	6.2mm × 5.3mm
	D (SOIC, 14)	8.65mm × 6mm	8.65 mm × 3.9mm
	N (PDIP, 14)	19.3mm × 9.4mm	19.3mm × 6.3 mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm
	W (CFP, 14)	9.21mm × 9mm	9.21mm × 6.28mm
	FK (LCCC, 14)	8.9mm × 8.9mm	8.9mm × 8.9mm

- (1) 詳細については、[セクション 10](#) を参照してください。
- (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
- (3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



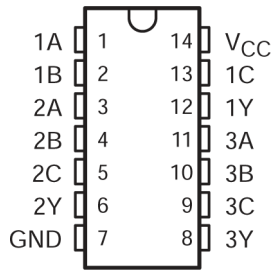
各ゲートの論理図 (正論理)



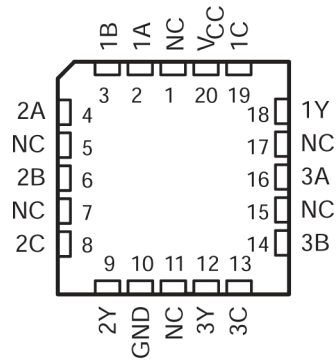
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3 Pin Configuration and Functions




3-1. SN54ACT11 W Package; SN74ACT11 D, DB, N, or PW Package (Top View)



NC – No internal connection

3-2. SN54ACT11 FK Package (Top View)

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
2A	3	Input	Channel 2, Input A
2B	4	Input	Channel 2, Input B
2C	5	Input	Channel 2, Input C
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3C	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
3A	11	Input	Channel 3, Input C
1Y	12	Output	Channel 1, Output Y
1C	13	Input	Channel 1, Input C
V _{CC}	14	—	Positive Supply

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I ⁽²⁾	Input voltage range	-0.5	V _{CC} + 0.5	V
V _O ⁽²⁾	Output voltage range	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0 or V _I > V _{CC})		±20
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})		±20
I _O	Continuous output current	(V _O = 0 or V _{CC})		±50
Continuous current through V _{CC} or GND				±200
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54ACT11		SN74ACT11		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-24	mA
I _{OL}	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate		8		8	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.3 Thermal Information

THERMAL METRIC ⁽¹⁾		SNx4ACT11					UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	119.9	96	80	76	145.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT11		SN74ACT11		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5V	4.4	4.49		4.4		4.4	V	
		5.5V	5.4	5.49		5.4		5.4		
	I _{OH} = -24 mA	4.5V	3.86			3.7		3.76		
		5.5V	4.86			4.7		4.76		
	I _{OH} = -50 mA ⁽¹⁾	5.5V				3.85				
I _{OH} = -75 mA ⁽¹⁾	5.5V						3.85			
V _{OL}	I _{OL} = 50 μA	4.5V		0.001	0.1		0.1		0.1	
		5.5V		0.001	0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5V			0.36		0.5		0.44	
		5.5V			0.36		0.5		0.44	
	I _{OL} = 50 mA ⁽¹⁾	5.5V					1.65			
I _{OL} = 75 mA ⁽¹⁾	5.5V							1.65		
I _I	V _I = V _{CC} or GND	5.5V			±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5V			2		40		20	μA
ΔI _{CC} ⁽²⁾	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.6		1.6		1.5	mA
C _i	V _I = V _{CC} or GND	5V			2.6					pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

4.5 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

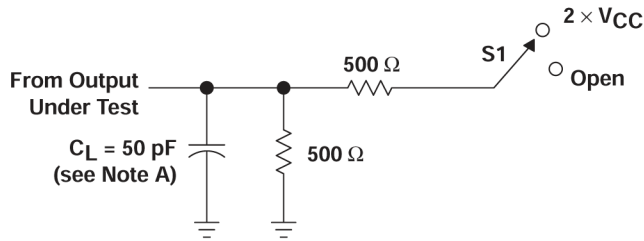
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			SN54ACT11		SN74ACT11		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A, B, or C	Y	1.5	6	9.5	1	10.5	1	10.5	ns
t _{PHL}			1.5	6	9.5	1	10.5	1	10.5	

4.6 Operating Characteristics

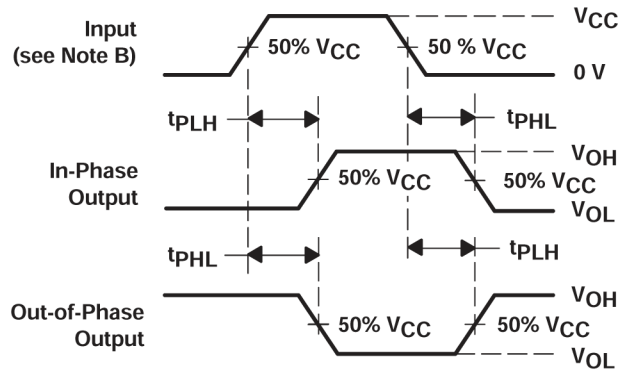
V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance C _L = 50 pF, f = 1 MHz	20	pF

5 Parameter Measurement Information



LOAD CIRCUIT



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- C. The outputs are measured one at a time with one input transition per measurement.

☒ 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open

6 Detailed Description

6.1 Functional Block Diagram

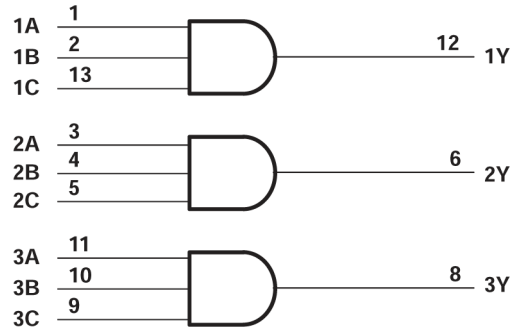


図 6-1. Logic Diagram, Each Gate (Positive Logic)

Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

6.2 Device Functional Modes

表 6-1. Function Table (Each Gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#). Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54ACT11	Click here	Click here	Click here	Click here	Click here
SN74ACT11	Click here	Click here	Click here	Click here	Click here

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2003) to Revision D (July 2024)	Page
<ul style="list-style-type: none"> 「製品情報」表、「ピンの機能」表、「熱に関する情報」表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加..... Updated RθJA values: D = 86 to 119.9, PW = 113 to 145.7, all values in °C/W..... 	<p>1</p> <p>4</p>

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9077201Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9077201Q2A SNJ54ACT11FK	Samples
5962-9077201QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9077201QDA SNJ54ACT11W	Samples
SN74ACT11BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD11	Samples
SN74ACT11D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	ACT11	
SN74ACT11DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD11	Samples
SN74ACT11DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11	Samples
SN74ACT11DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11	Samples
SN74ACT11N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ACT11N	Samples
SN74ACT11PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	AD11	
SN74ACT11PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD11	Samples
SNJ54ACT11FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9077201Q2A SNJ54ACT11FK	Samples
SNJ54ACT11W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9077201QDA SNJ54ACT11W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ACT11, SN74ACT11 :

- Catalog : [SN74ACT11](#)

- Automotive : [SN74ACT11-Q1](#), [SN74ACT11-Q1](#)

- Military : [SN54ACT11](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT11BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74ACT11DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ACT11DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT11PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT11PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT11BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74ACT11DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74ACT11DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74ACT11PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74ACT11PWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9077201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9077201QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74ACT11N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT11N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54ACT11FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT11W	W	CFP	14	25	506.98	26.16	6220	NA

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

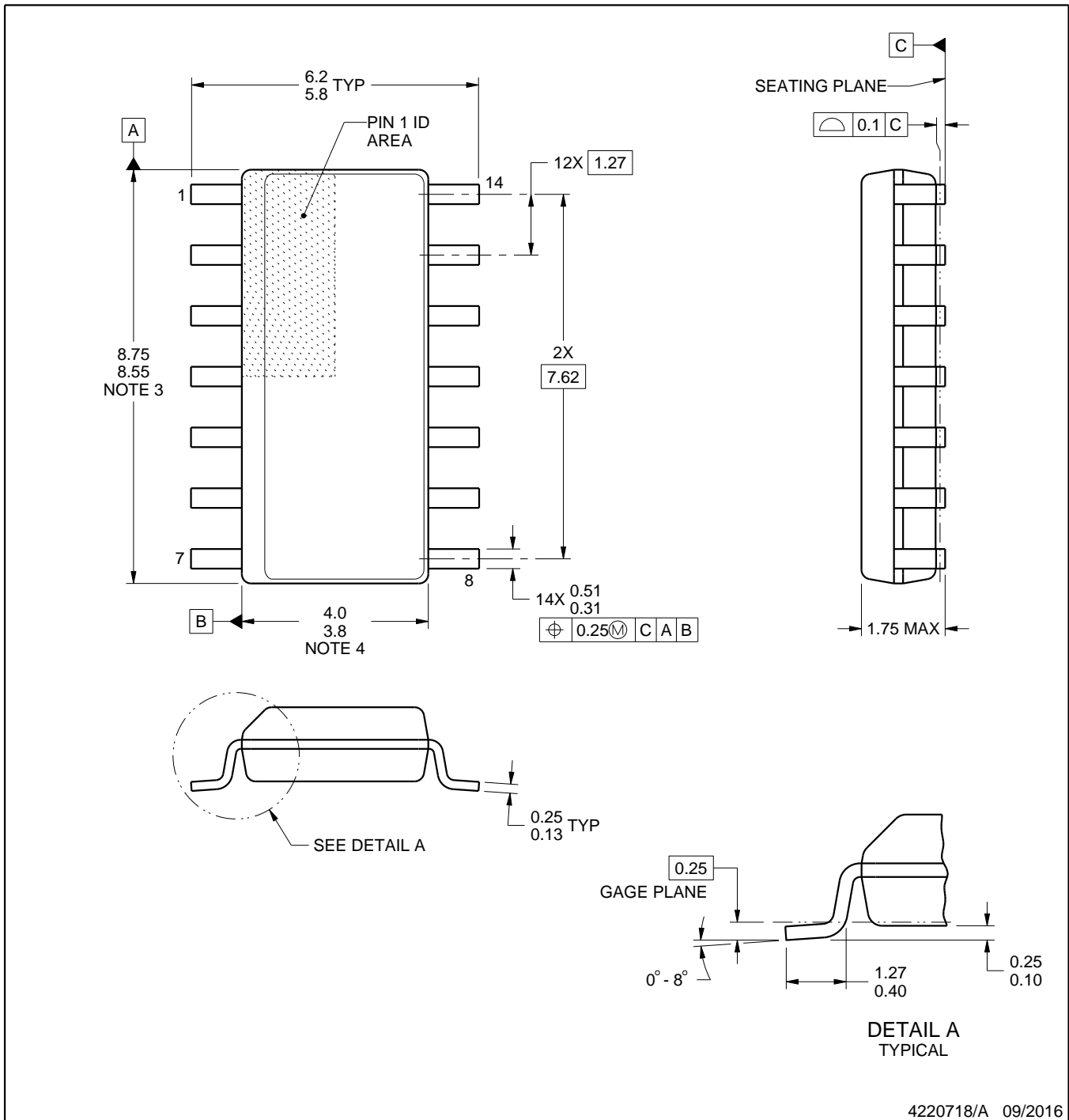
D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

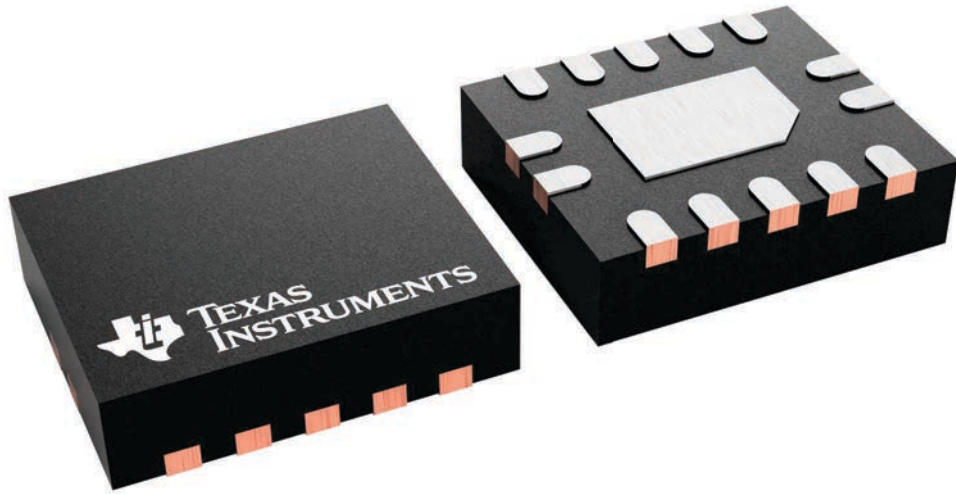
BQA 14

WQFN - 0.8 mm max height

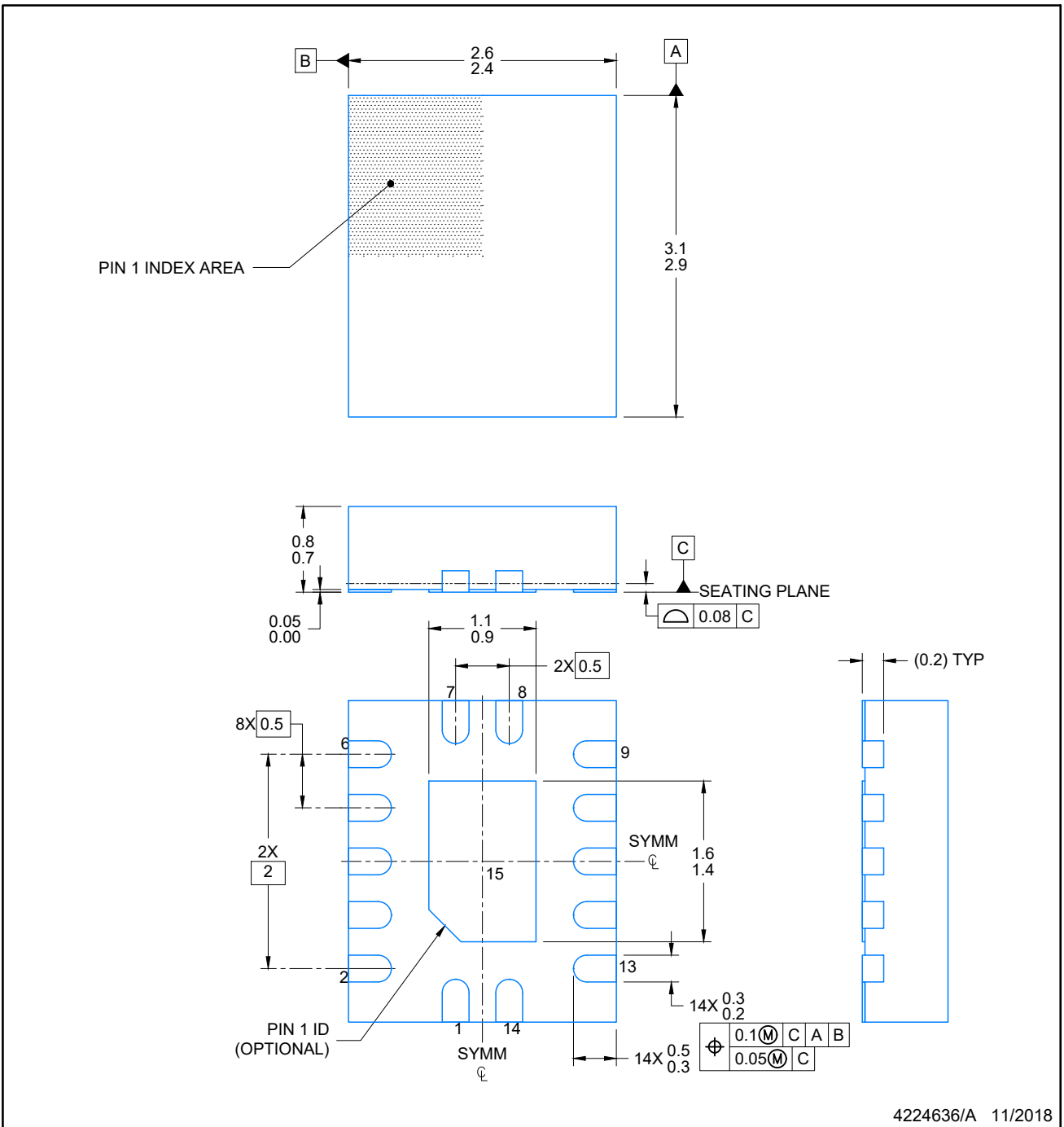
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

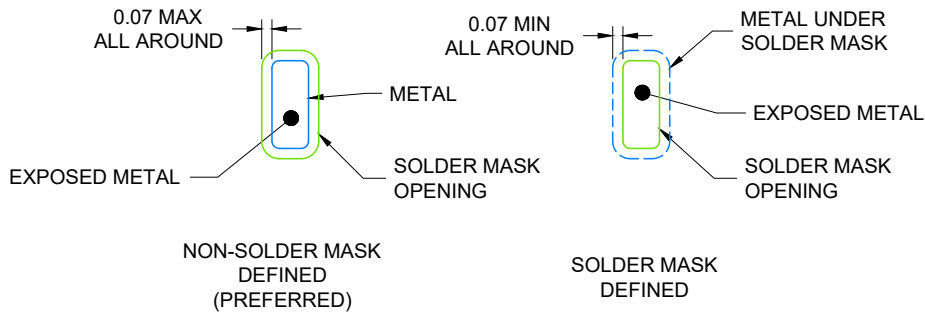
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220762/A 05/2024

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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