SN54ACT245, SN74ACT245
JAJSPN7H – SEPTEMBER 1994 – REVISED APRIL 2024

# SNx4ACT245 オクタル バストランシーバ、3 ステート出力

## 1 特長

- 4.5V ~ 5.5V の $V_{CC}$ で動作
- 5.5V までの入力電圧に対応
- 最大 $t_{pd}$ 8ns (5V 時)
- 入力は TTL 電圧互換

## 2 アプリケーション

- 業務用オーディオ
- ビデオとサイネージ
- 家電製品
- ファクトリ・オートメーション / 制御

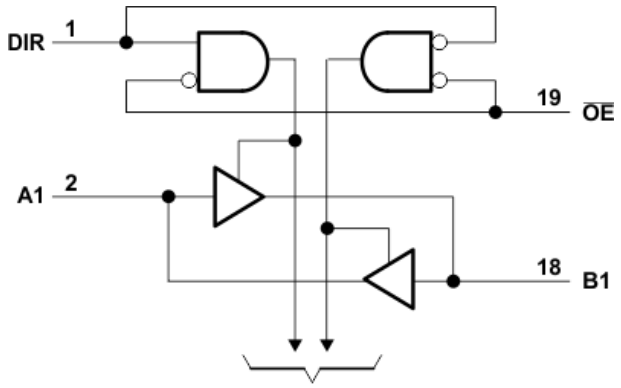
## 3 概要

'AC245 オクタル バス トランシーバは、データ バス間の非同期双方向通信用に設計されています。制御機能を実装しているため、外部のタイミング要件は最小限です。

**製品情報**

| 部品番号 | パッケージ (1) | パッケージ サイズ (2) | 本体サイズ (3) |
|---|---|---|---|
| SNx4ACT245 | DB (SSOP、20) | 7.2mm × 7.8mm | 7.2mm × 5.3mm |
| | DGS (VSSOP、20) | 5.1mm × 4.9mm | 5.1mm × 3mm |
| | DW (SOIC、20) | 12.8mm × 10.3mm | 12.8mm × 7.5mm |
| | N (PDIP、20) | 24.33mm × 9.4mm | 24.33mm × 6.35mm |
| | NS (SO、20) | 12.6mm × 7.8mm | 12.6mm × 5.3mm |
| | PW (TSSOP、20) | 6.5mm × 6.4mm | 6.5mm × 4.4mm |
| | RKS (VQFN、20) | 4.5mm × 2.5mm | 4.5mm × 2.5mm |

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。




論理図 (正論理)

# Table of Contents

## 4 Pin Configuration and Functions

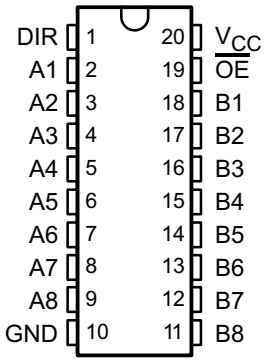



**図 4-1. SN54ACT245 J or W Package; SN74ACT245 DB, DGS, DW, N, NS, or PW Package Top View**

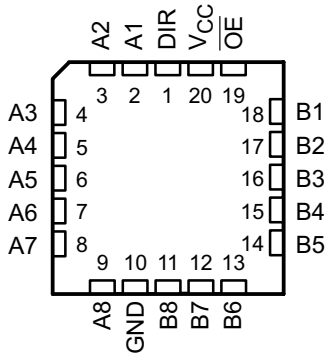



**図 4-2. SN54ACT245 FK Package Top View**

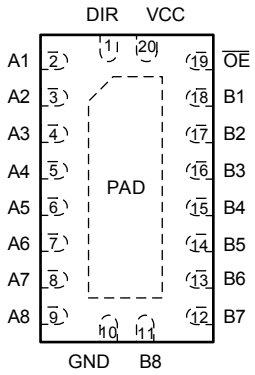



**図 4-3. SN54ACT245 RKS Package Top View**

## Pin Functions

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | DIR | I/O | Direction Pin |
| 2 | A1 | I/O | A1 Input/Output |
| 3 | A2 | I/O | A2 Input/Output |
| 4 | A3 | I/O | A3 Input/Output |
| 5 | A4 | I/O | A4 Input/Output |
| 6 | A5 | I/O | A5 Input/Output |
| 7 | A6 | I/O | A6 Input/Output |
| 8 | A7 | I/O | A7 Input/Output |
| 9 | A8 | I/O | A8 Input/Output |
| 10 | GND | — | Ground Pin |
| 11 | B8 | I/O | B8 Input/Output |
| 12 | B7 | I/O | B7 Input/Output |
| 13 | B6 | I/O | B6 Input/Output |
| 14 | B5 | I/O | B5 Input/Output |
| 15 | B4 | I/O | B4 Input/Output |
| 16 | B3 | I/O | B3 Input/Output |
| 17 | B2 | I/O | B2 Input/Output |
| 18 | B1 | I/O | B1 Input/Output |
| 19 | OE | I/O | Output Enable |
| 20 | VCC | — | Power Pin |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $V_I$ | Input voltage (1) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ | Output voltage (1) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 or $V_I$ > $V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±200 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±3000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

| | | SN54ACT245 | | SN74ACT245 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –24 | mA |
| $I_{OL}$ | Low-level output current | | 24 | | 24 | mA |
| Δt/Δv | Input transition rise or fall rate | | 8 | | 8 | ns/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | SNx4ACT245 | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | DB (SSOP) | DGS (VSSOP) | DW (SOIC) | N (PDIP) | NS (SOP) | PW (TSSOP) | RKS (VQFN) | |
| | | 20 PINS | | | | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 105.4 | 123.5 | 98.6 | 69 | 99.7 | 126.6 | 67.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54ACT245 | | SN74ACT245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.49 | | 4.4 | | 4.4 | | V |
| | | | 5.5 V | 5.4 | 5.49 | | 5.4 | | 5.4 | | |
| | | $I_{OH}$ = –24 mA | 4.5 V | 3.88 | | | 3.7 | | 3.76 | | |
| | | | 5.5 V | 4.86 | | | 4.7 | | 4.76 | | |
| | | $I_{OH}$ = –50 mA(1) | 5.5 V | | | | 3.85 | | | | |
| | | $I_{OH}$ = –75 mA(1) | 5.5 V | | | | | | 3.85 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 µA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 5.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 50 mA(1) | 5.5 V | | | | | 1.65 | | | |
| | | $I_{OL}$ = 75 mA(1) | 5.5 V | | | | | | | 1.65 | |
| $I_{OZ}$ | A or B ports(2) | $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.5 | | ±10 | | ±5 | µA |
| $I_I$ | $\overline{OE}$ or DIR | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 80 | | 40 | µA |
| $\Delta I_{CC}$ (3) | | One input at 3.4 V, Other inputs at GND or $V_{CC}$ | 5.5 V | | 0.6 | | | 1.6 | | 1.5 | mA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | 5 V | | 4.5 | | | | | | pF |
| $C_{io}$ | | $V_O$ = $V_{CC}$ or GND | 5 V | | 15 | | | | | | pF |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.
(2) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(3) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see 図 6-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | SN54ACT245 | | SN74ACT245 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 1 | 4 | 7.5 | 1 | 9 | 1.5 | 8 | ns |
| $t_{PHL}$ | | | 1 | 4 | 8 | 1 | 10 | 1 | 9 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 1 | 5 | 10 | 1 | 12 | 1.5 | 11 | ns |
| $t_{PZL}$ | | | 1 | 5.5 | 10 | 1 | 13 | 1.5 | 12 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 1 | 5.5 | 10 | 1 | 12 | 1 | 11 | ns |
| $t_{PLZ}$ | | | 1 | 5 | 10 | 1 | 12 | 1.5 | 11 | |

## 5.7 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, | f = 1 MHz | 45 | pF |

## 5.8 Typical Characteristics

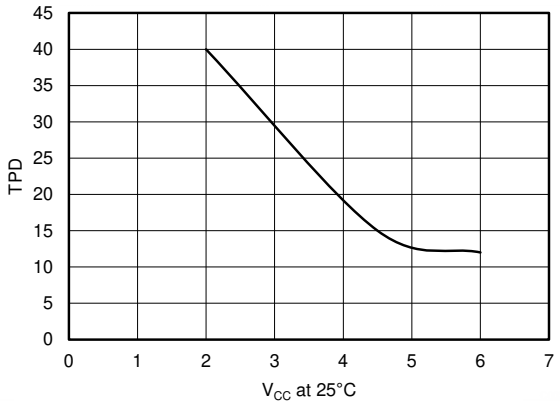



**図 5-1. TPD vs $V_{CC}$ at 25°C**

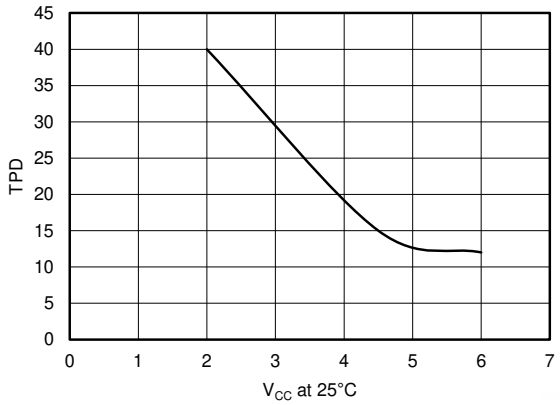
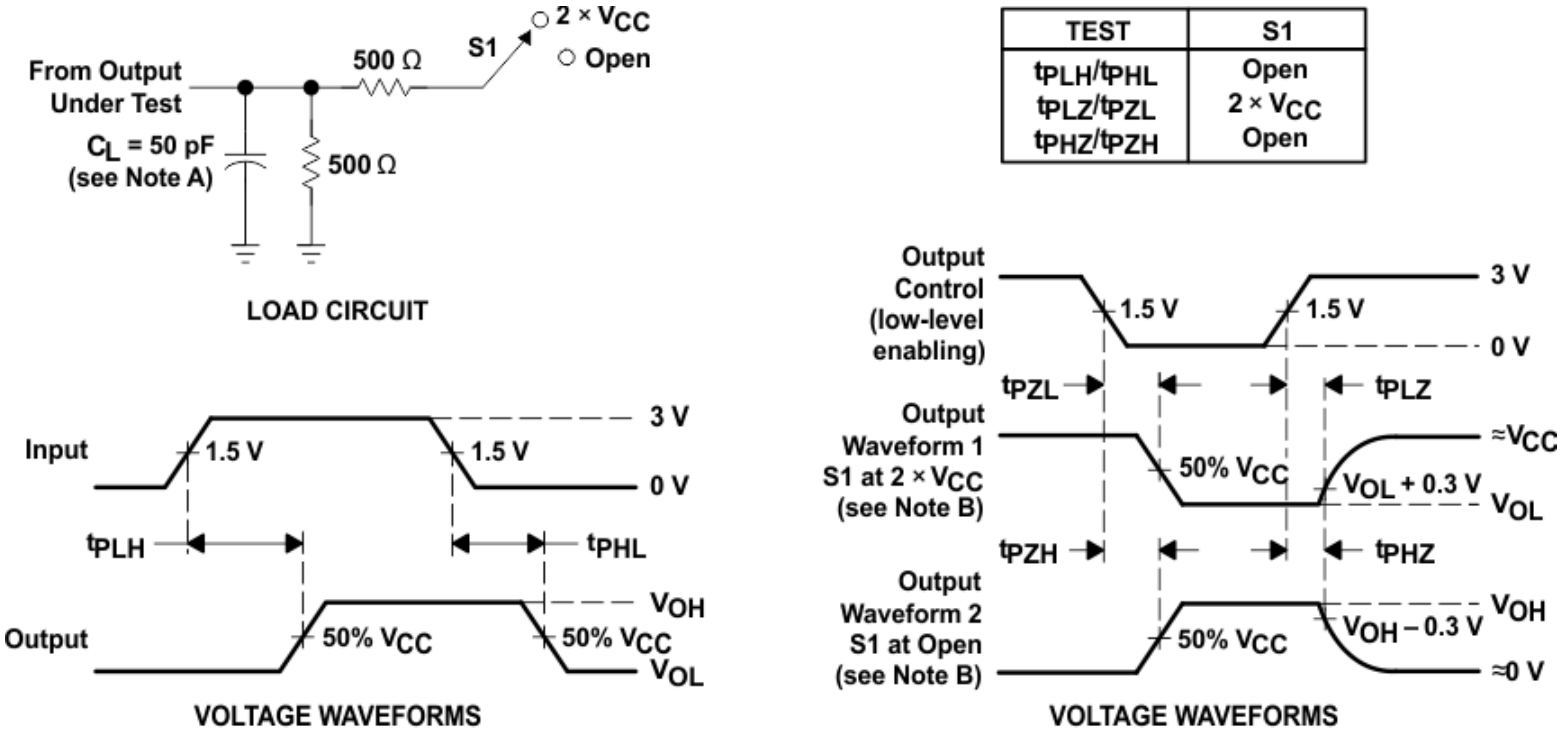



**図 5-2. TPD vs $V_{CC}$ at 25°C**

# 6 Parameter Measurement Information

## 6.1




NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤2.5 ns, $t_f$ ≤2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**図 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

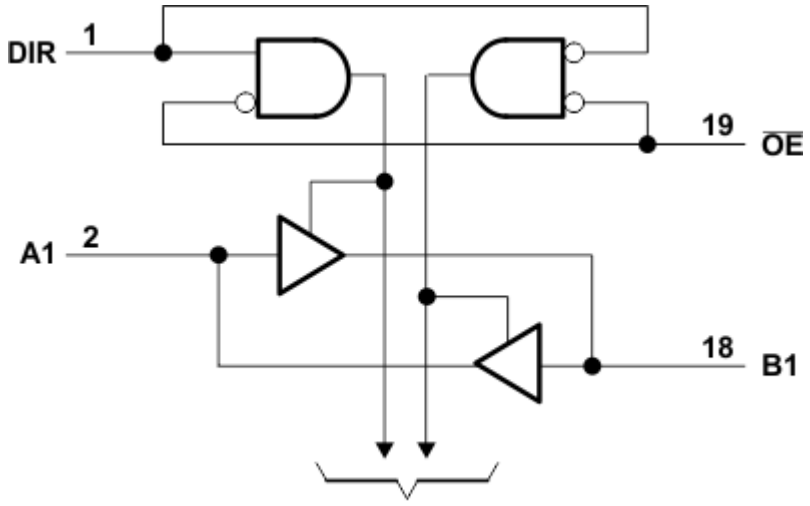
## 7.1 Overview

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

When the output-enable ( $\overline{OE}$) is low, the device passes noninverted data from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. A high on $\overline{OE}$ disables the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 7.2 Functional Block Diagram




**Logic Diagram (Positive Logic)**

## 7.3 Feature Description

The SNx4ACT245 devices have a wide operating $V_{CC}$ range from 4.5 V to 5.5 V with slower edge rates to minimize output ringing.

## 7.4 Device Functional Modes

セクション 7.4 lists the function modes of the SNx4ACT245.

**表 7-1. Function Table**

| INPUTS(1) | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

# 8 アプリケーション情報に関する免責事項

**注**

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 8.1 Application Information

The SNx4ACT245 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

## 8.2 Typical Application

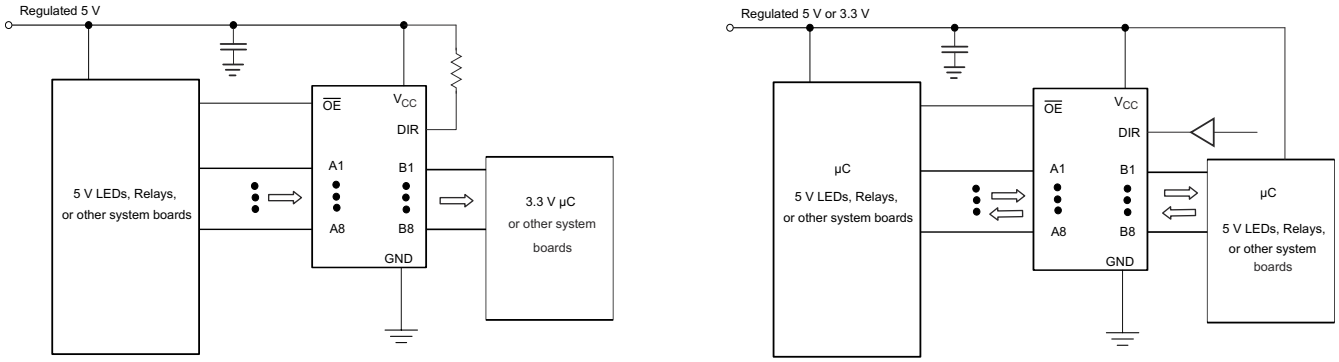



**図 8-1. Typical Application Schematic**

### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### 8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *セクション 5.3* table.
   - For specified High and low levels, see $V_{IH}$ and $V_{IL}$ in the *セクション 5.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommend Output Conditions
   - Load currents should not exceed 35 mA per output and 70 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.

### 8.2.3 Application Curve

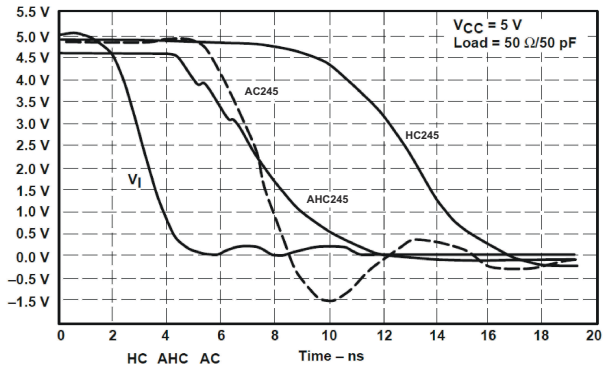



**図 8-2. Switching Characteristics Comparison**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *セクション 5.3*.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple $V_{CC}$ pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. セクション 8.4.2 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

### 8.4.2 Layout Example

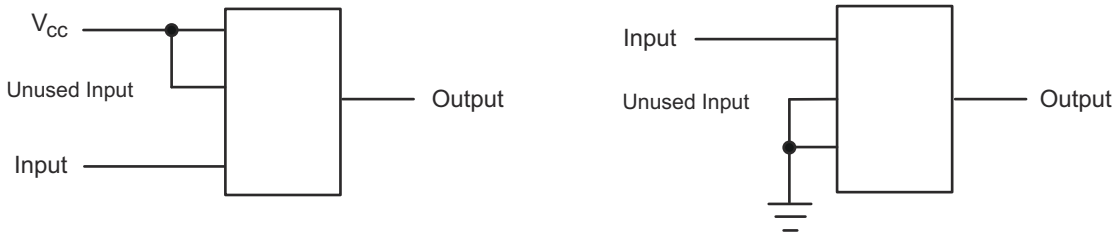



**図 8-3. Layout Diagram**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 9-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54ACT245 | Click here | Click here | Click here | Click here | Click here |
| SN74ACT245 | Click here | Click here | Click here | Click here | Click here |

## 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 9.3 サポート・リソース

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## 9.4 Trademarks

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## 9.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision G (March 2024) to Revision H (April 2024) | Page |
|---|---|
| • Updated RθJA values: DB = 70 to 105.4, DW = 58 to 98.6, NS = 60 to 99.7, PW = 83 to 126.6, all values in °C/W | 5 |

| Changes from Revision F (January 2023) to Revision G (March 2024) | Page |
|---|---|
| • 「製品情報」表、「ピン構成および機能」セクション、および「熱に関する情報」表に DGS および RKS パッケージを追加 | 1 |
| • 「パッケージ情報」を「製品情報」に変更し、表にパッケージサイズを追加 | 1 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8766301M2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8766301M2A SNJ54ACT245FK | Samples |
| 5962-8766301MRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8766301MRA SNJ54ACT245J | Samples |
| 5962-8766301MSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8766301MSA SNJ54ACT245W | Samples |
| SN74ACT245DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (ACT245, AD245) | Samples |
| SN74ACT245DGSR | ACTIVE | VSSOP | DGS | 20 | 5000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT245 | Samples |
| SN74ACT245DW | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | -40 to 85 | ACT245 | |
| SN74ACT245DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT245 | Samples |
| SN74ACT245DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT245 | Samples |
| SN74ACT245DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT245 | Samples |
| SN74ACT245N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74ACT245N | Samples |
| SN74ACT245NE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74ACT245N | Samples |
| SN74ACT245NS | ACTIVE | SOP | NS | 20 | | TBD | Call TI | Call TI | -40 to 85 | ACT245 | Samples |
| SN74ACT245NSR | ACTIVE | SOP | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT245 | Samples |
| SN74ACT245PW | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 85 | AD245 | |
| SN74ACT245PWG4 | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74ACT245PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (ACT245, AD245) | Samples |
| SN74ACT245PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (ACT245, AD245) | Samples |
| SN74ACT245RKSR | ACTIVE | VQFN | RKS | 20 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT245 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54ACT245FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8766301M2A SNJ54 ACT245FK | Samples |
| SNJ54ACT245J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8766301MR A SNJ54ACT245J | Samples |
| SNJ54ACT245W | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8766301MS A SNJ54ACT245W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ACT245, SN74ACT245 :**

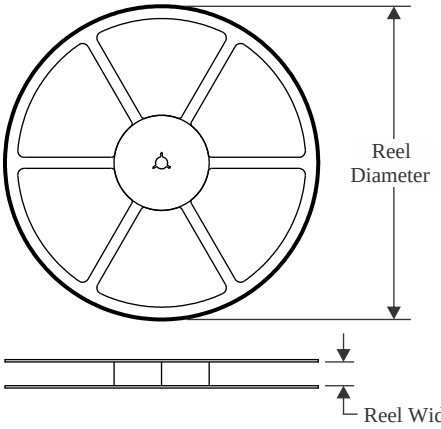
- Catalog : SN74ACT245
- Automotive : SN74ACT245-Q1, SN74ACT245-Q1
- Military : SN54ACT245
- Space : SN54ACT245-SP

NOTE: Qualified Version Definitions:

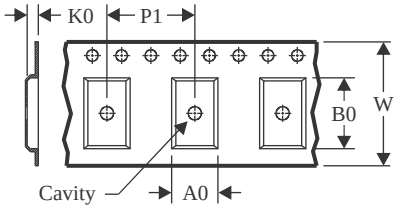
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

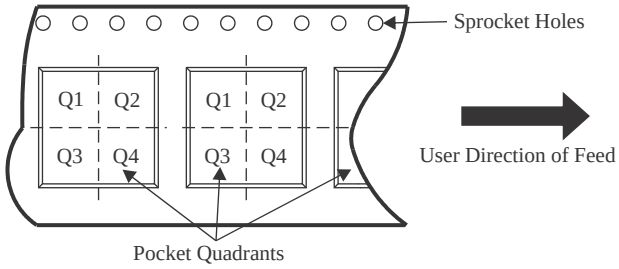



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

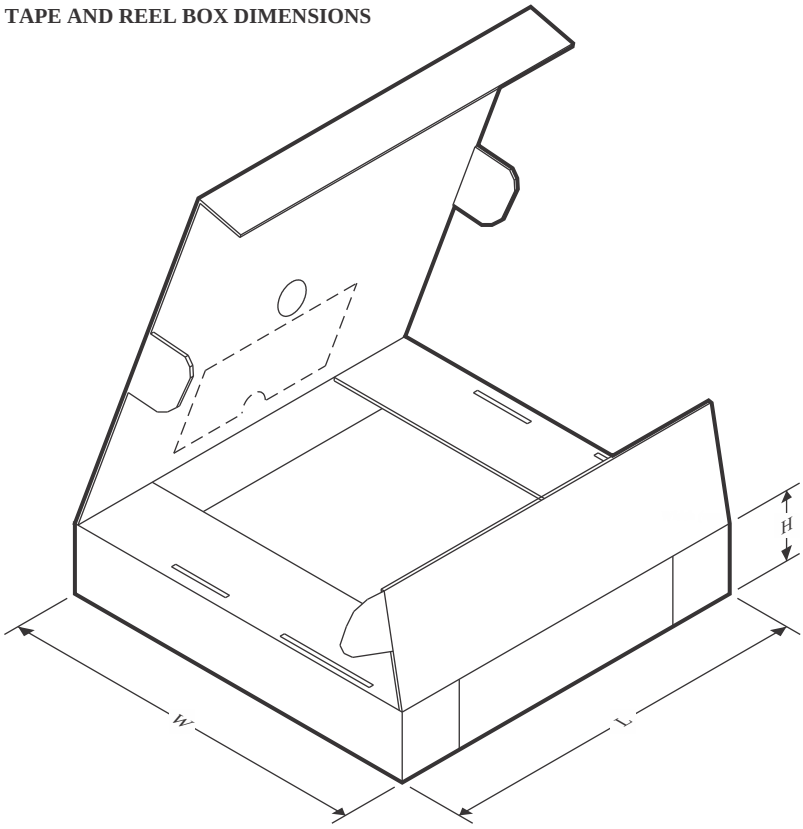
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ACT245DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ACT245DGSR | VSSOP | DGS | 20 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |
| SN74ACT245DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ACT245DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ACT245NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74ACT245NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74ACT245PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74ACT245PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74ACT245RKSR | VQFN | RKS | 20 | 3000 | 180.0 | 12.4 | 2.8 | 4.8 | 1.2 | 4.0 | 12.0 | Q1 |

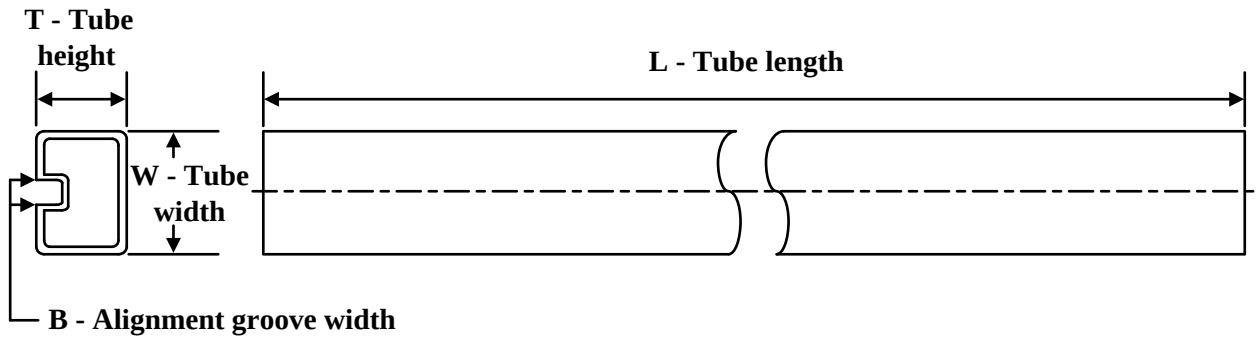
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ACT245DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74ACT245DGSR | VSSOP | DGS | 20 | 5000 | 353.0 | 353.0 | 32.0 |
| SN74ACT245DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ACT245DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74ACT245NSR | SOP | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ACT245NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74ACT245PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74ACT245PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74ACT245RKSR | VQFN | RKS | 20 | 3000 | 210.0 | 185.0 | 35.0 |

## TUBE




*All dimensions are nominal

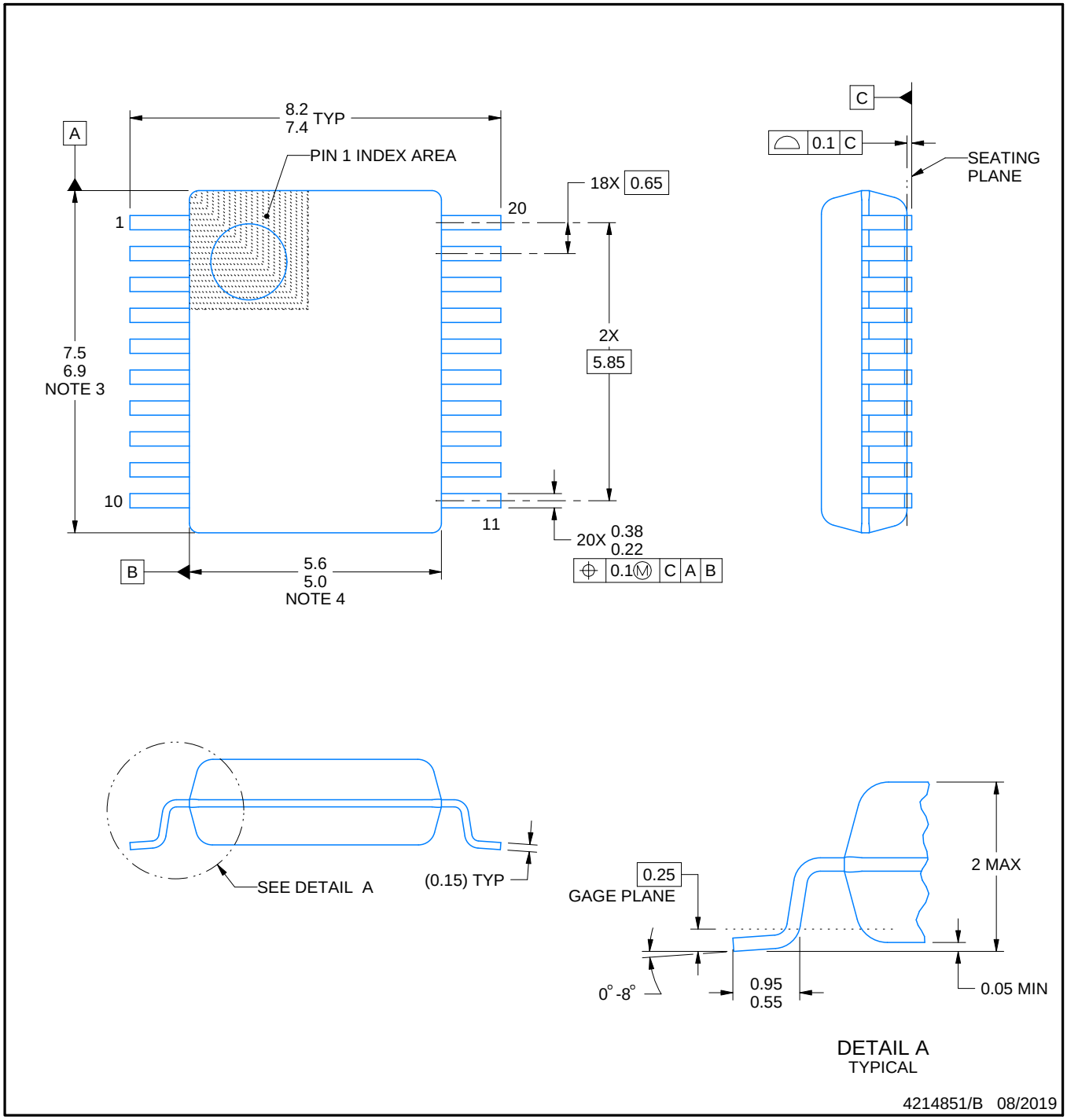
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-8766301M2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8766301MSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74ACT245N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74ACT245NE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54ACT245FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ACT245W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

# PACKAGE OUTLINE

## DB0020A

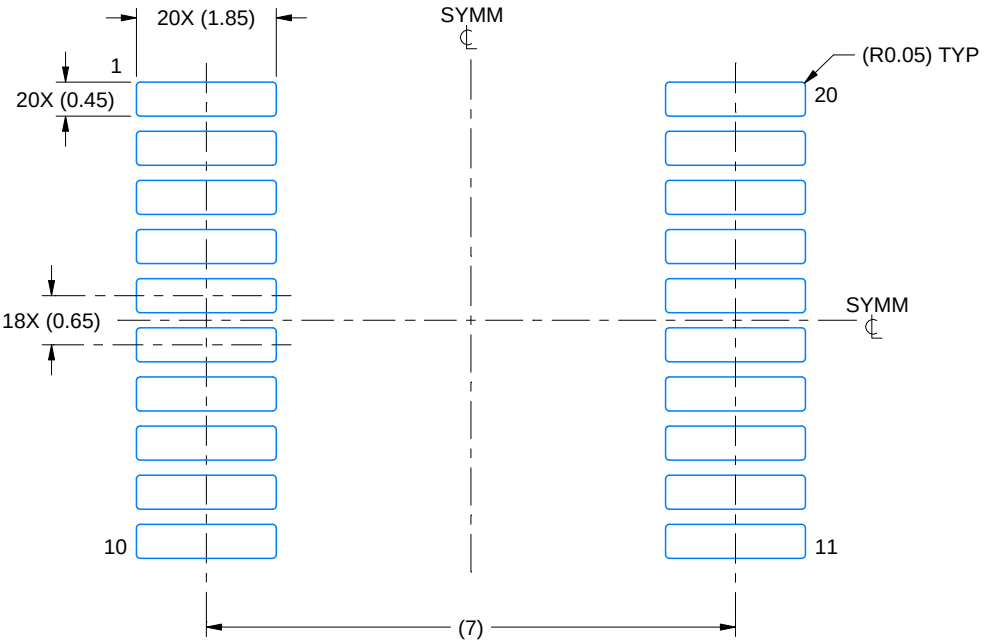
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

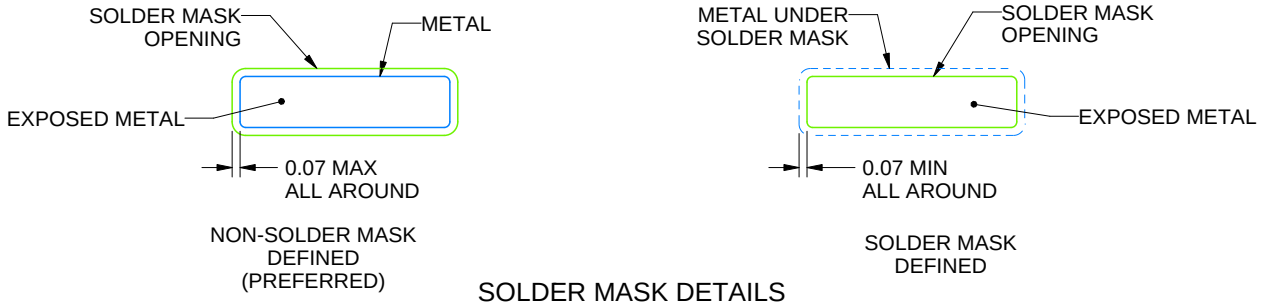



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

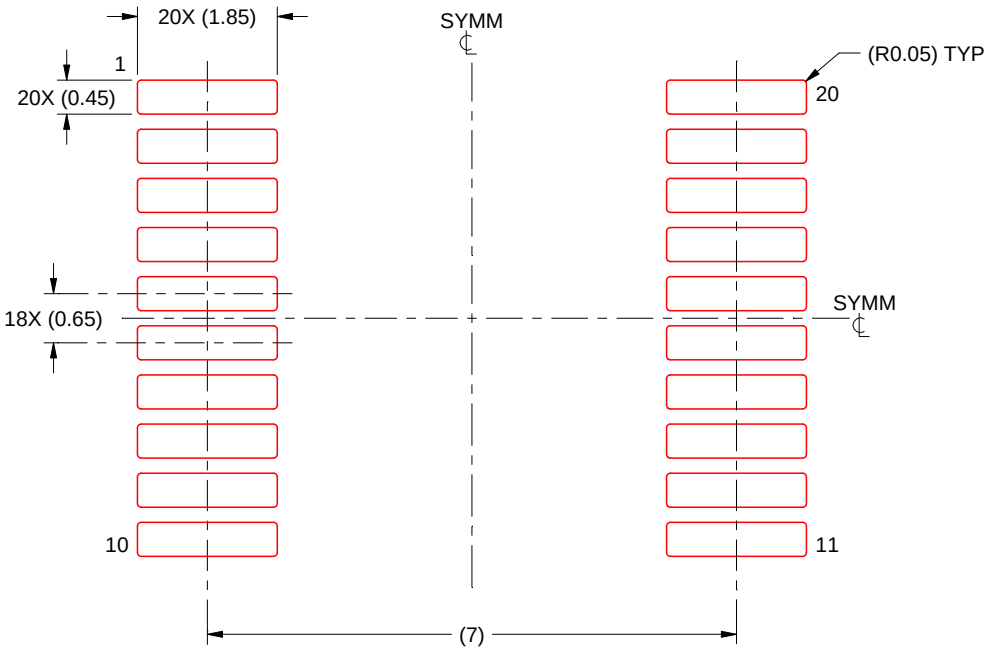
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0020A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

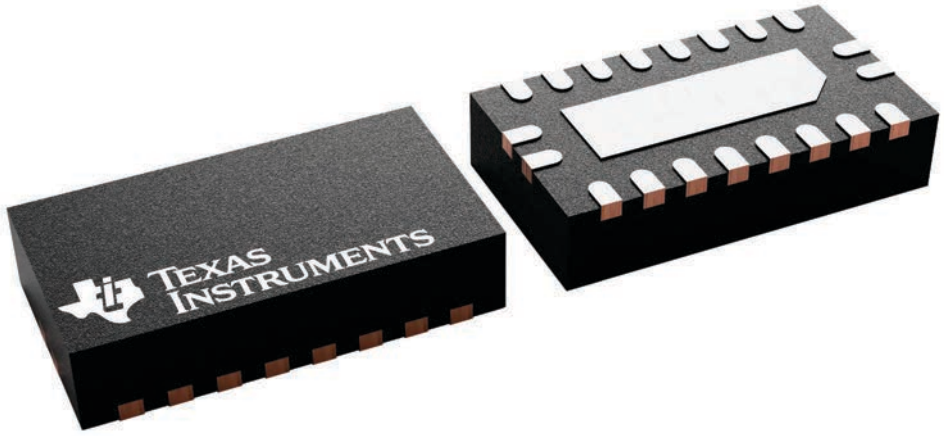
## RKS 20

## VQFN - 1 mm max height

**2.5 x 4.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

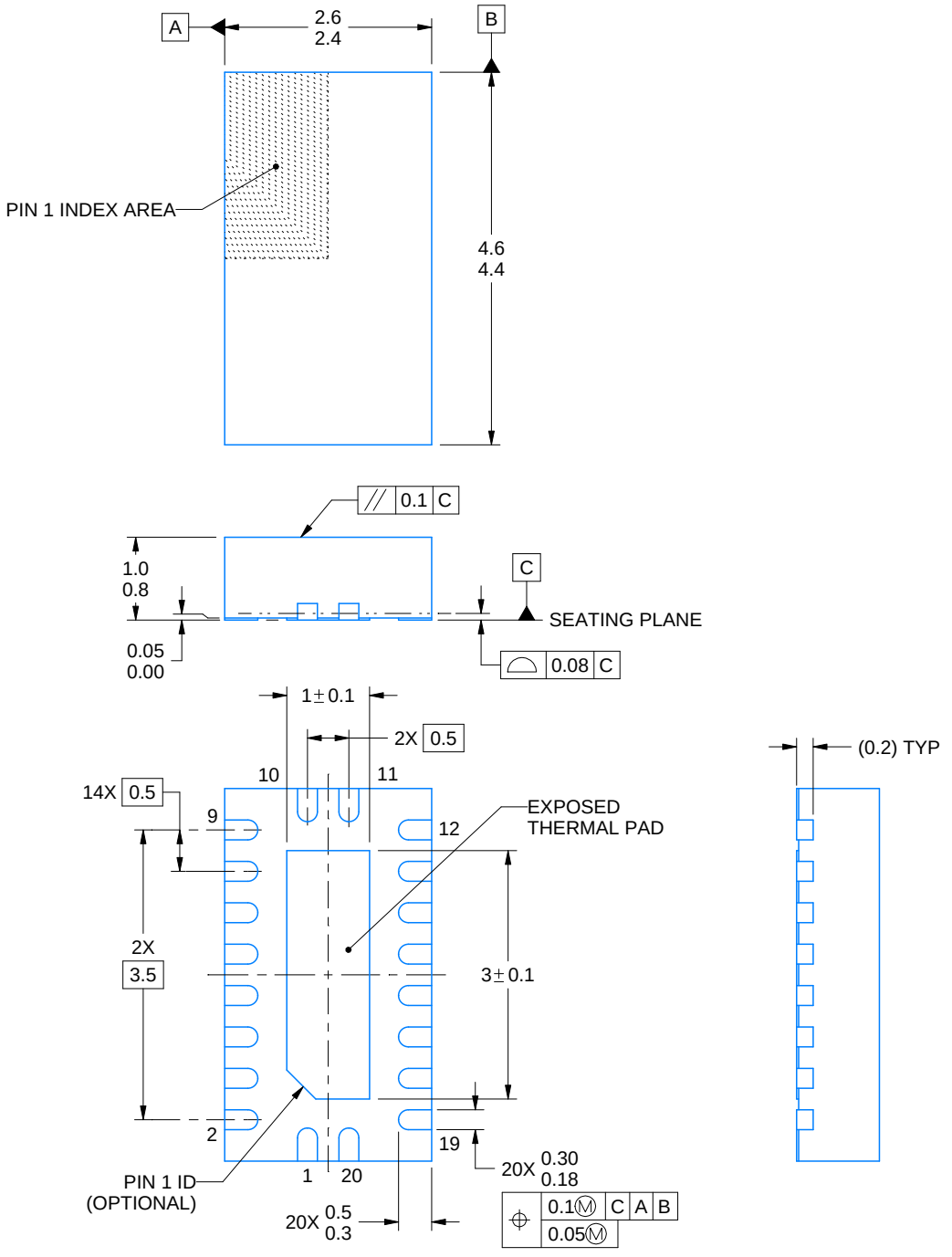


# PACKAGE OUTLINE

## RKS0020A

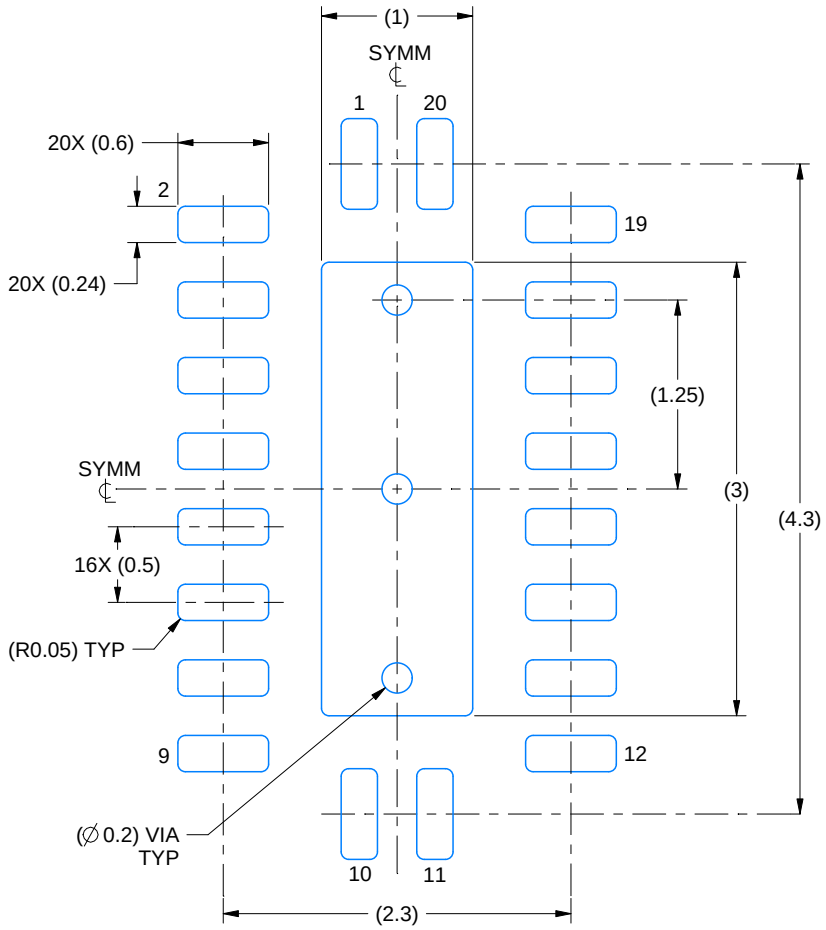
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

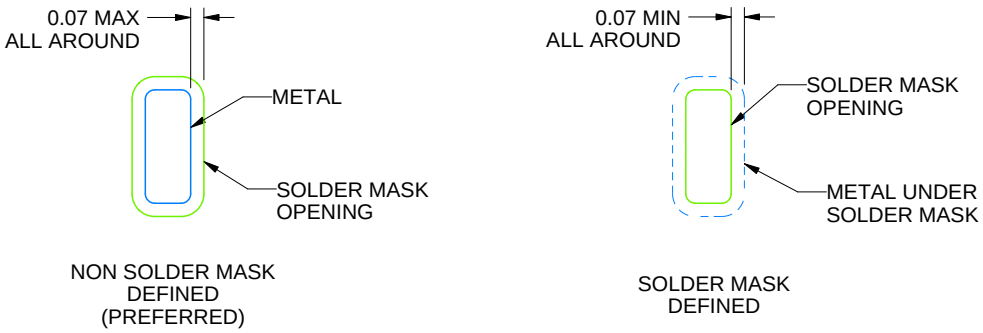



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

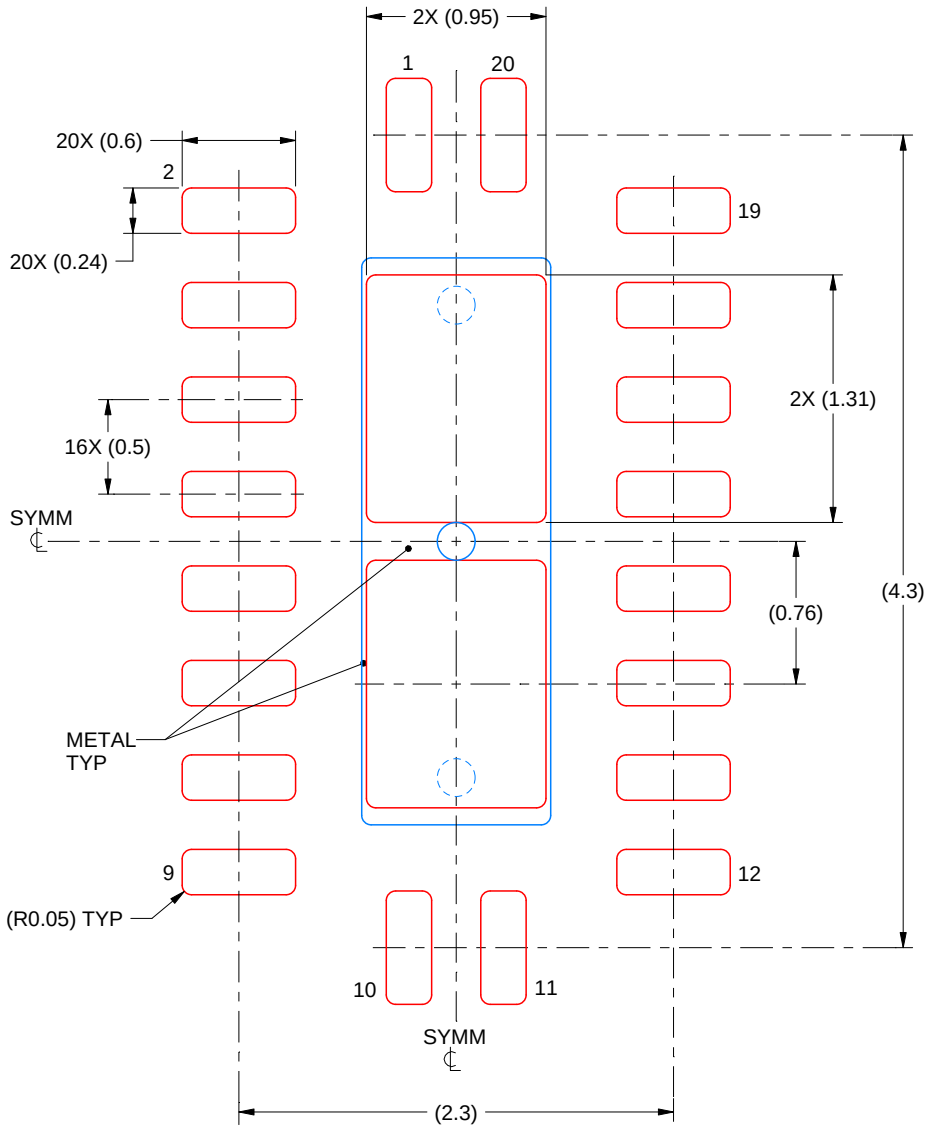



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

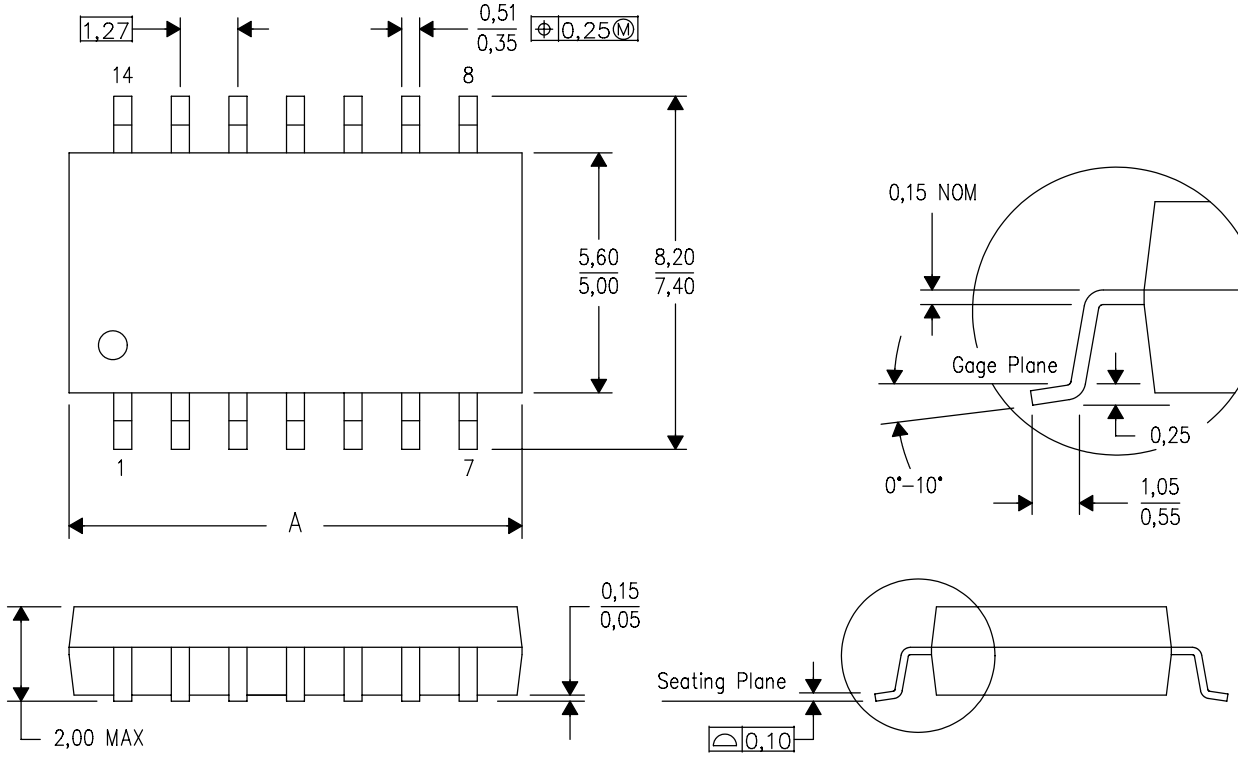
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

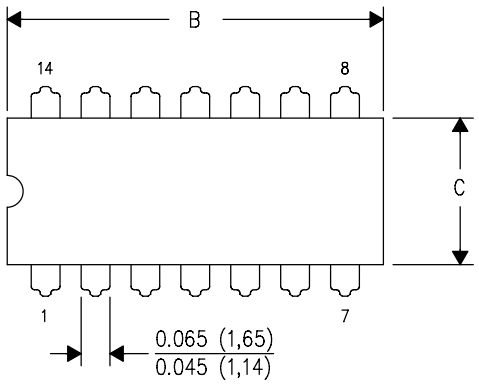
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

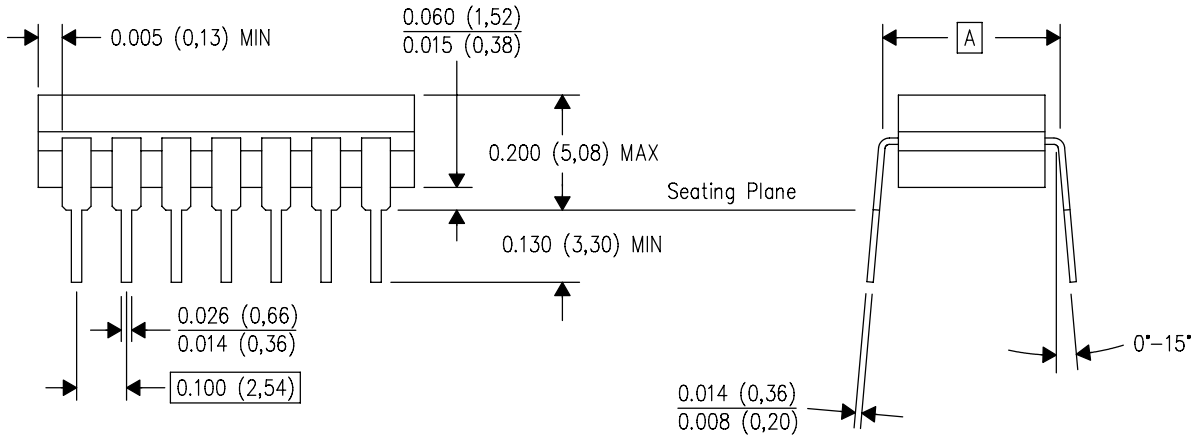
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# GENERIC PACKAGE VIEW

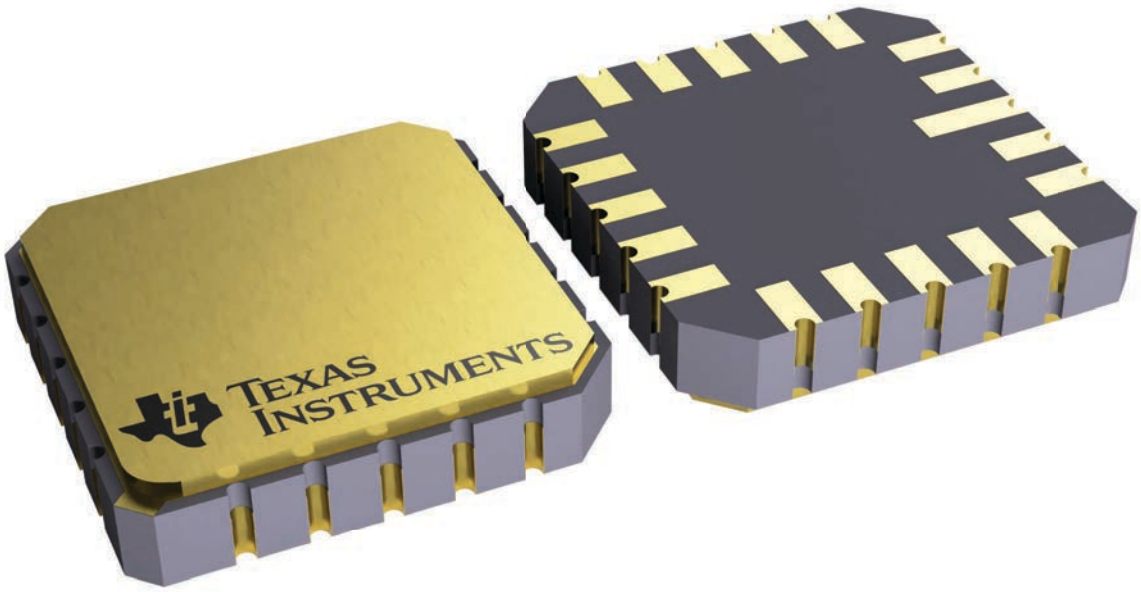
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

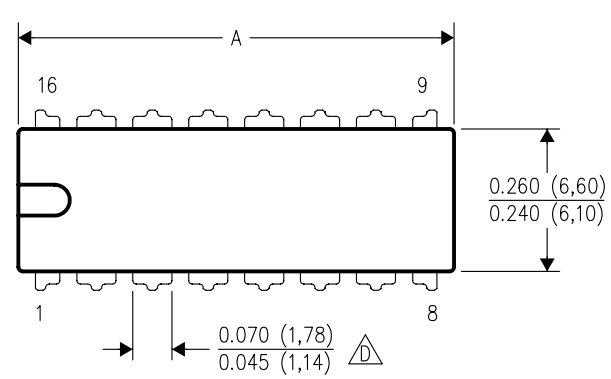



4229370VA\

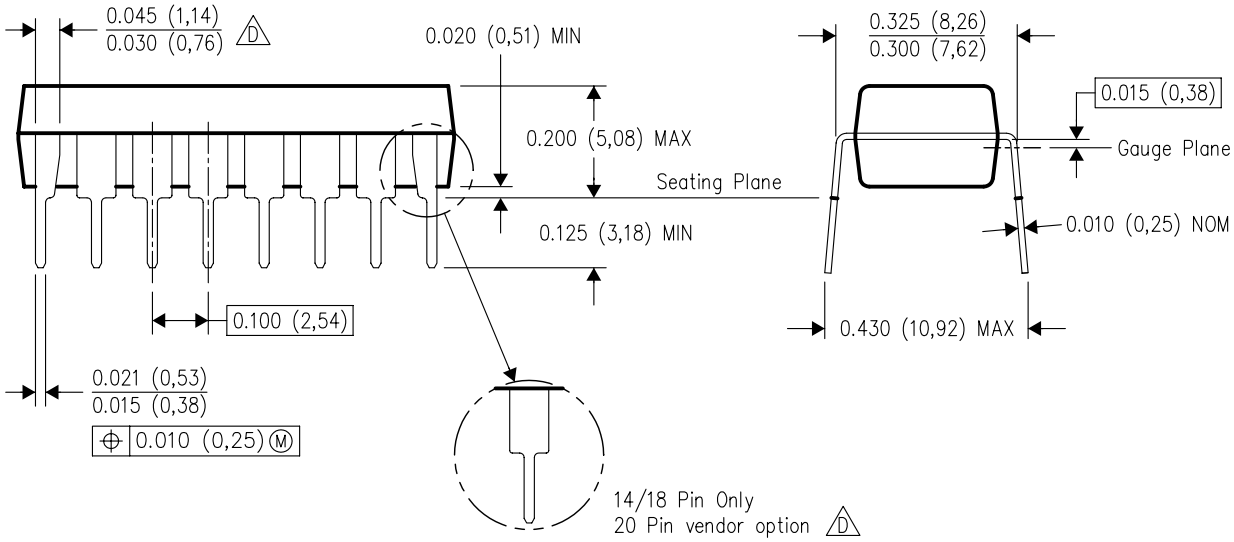
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

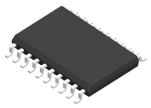



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

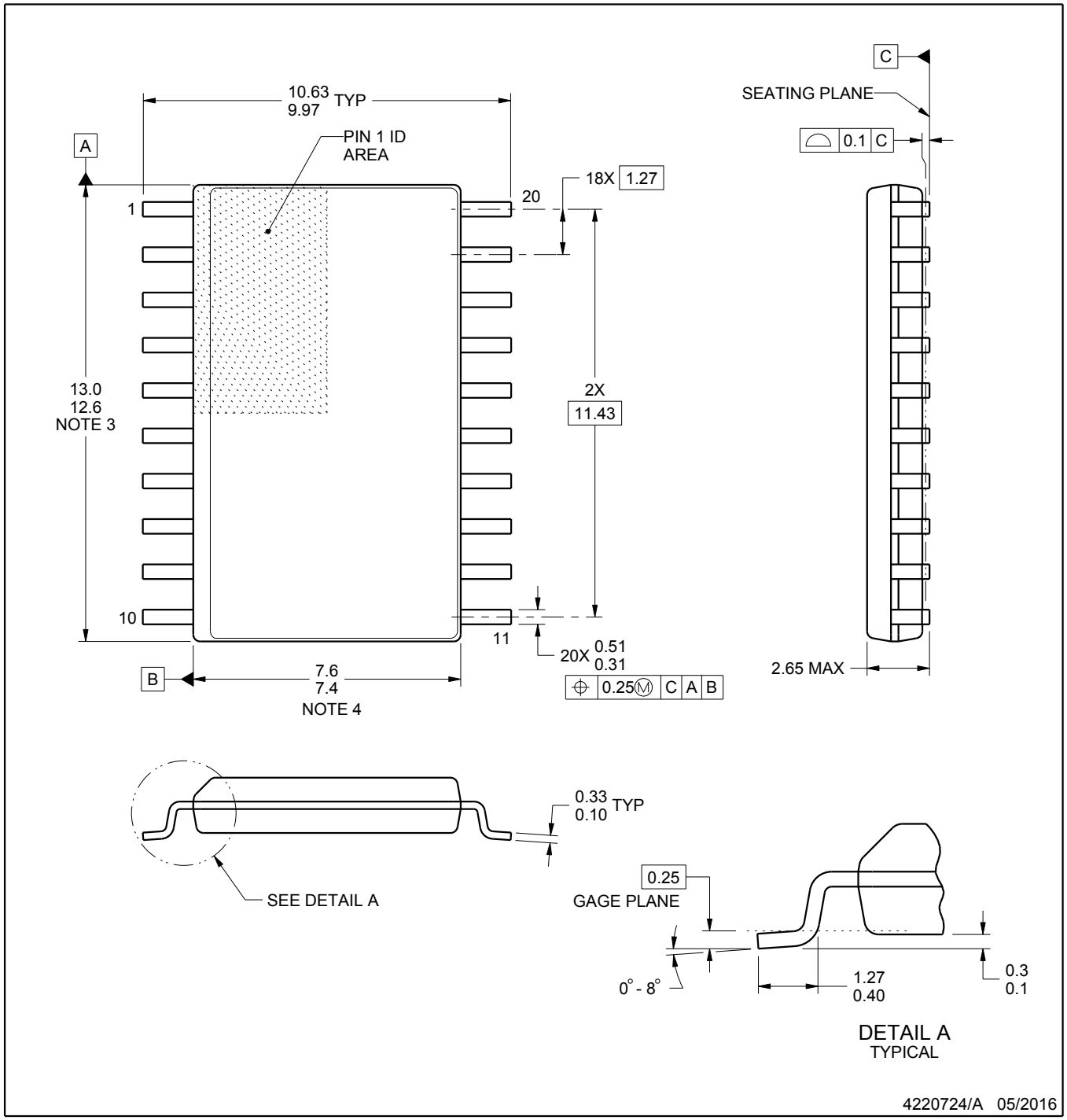


# PACKAGE OUTLINE

## DW0020A

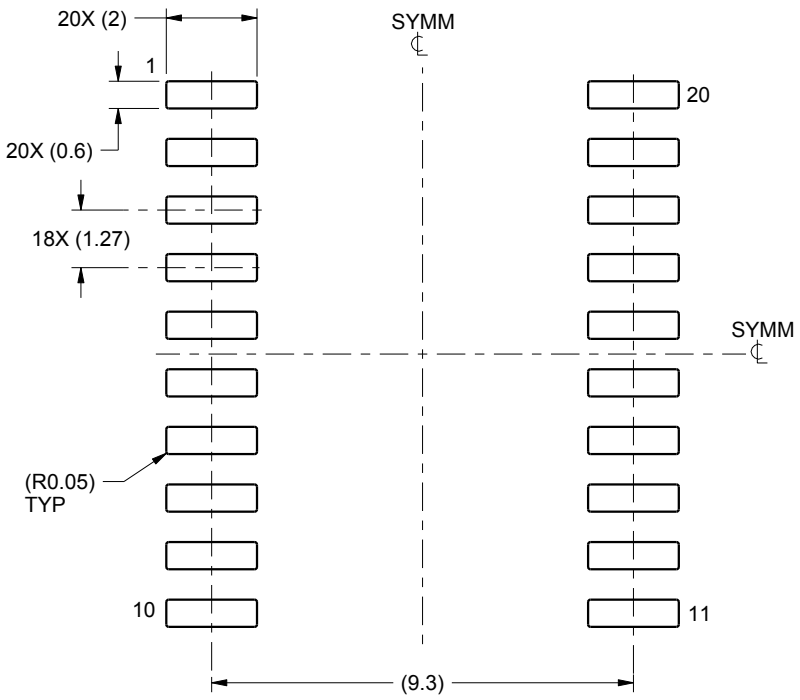
## SOIC - 2.65 mm max height

SOIC

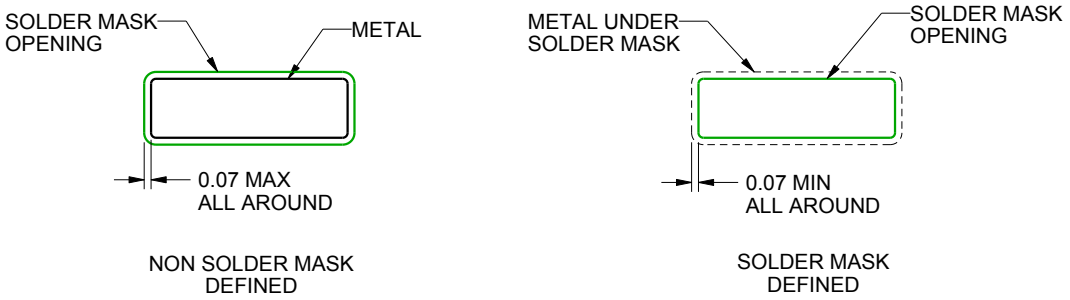



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

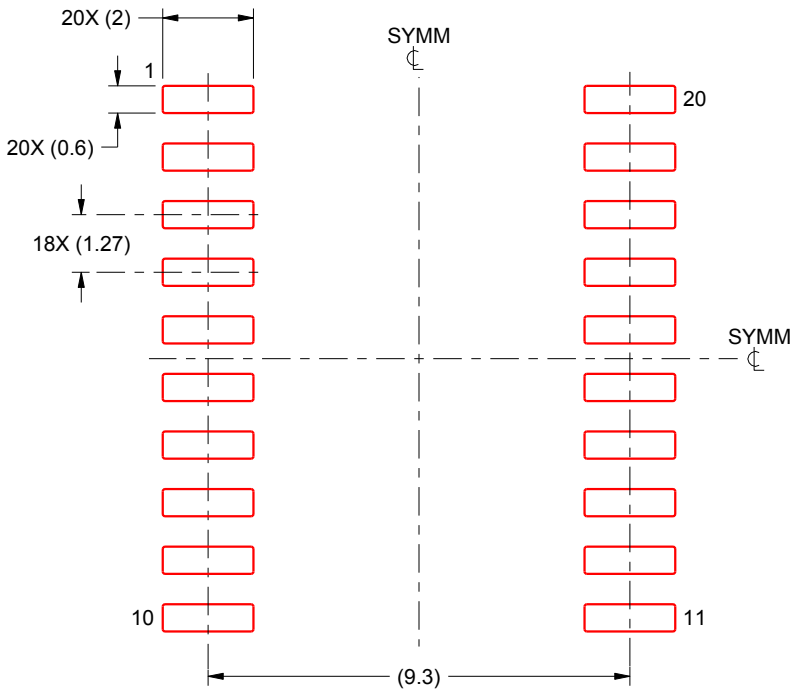



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



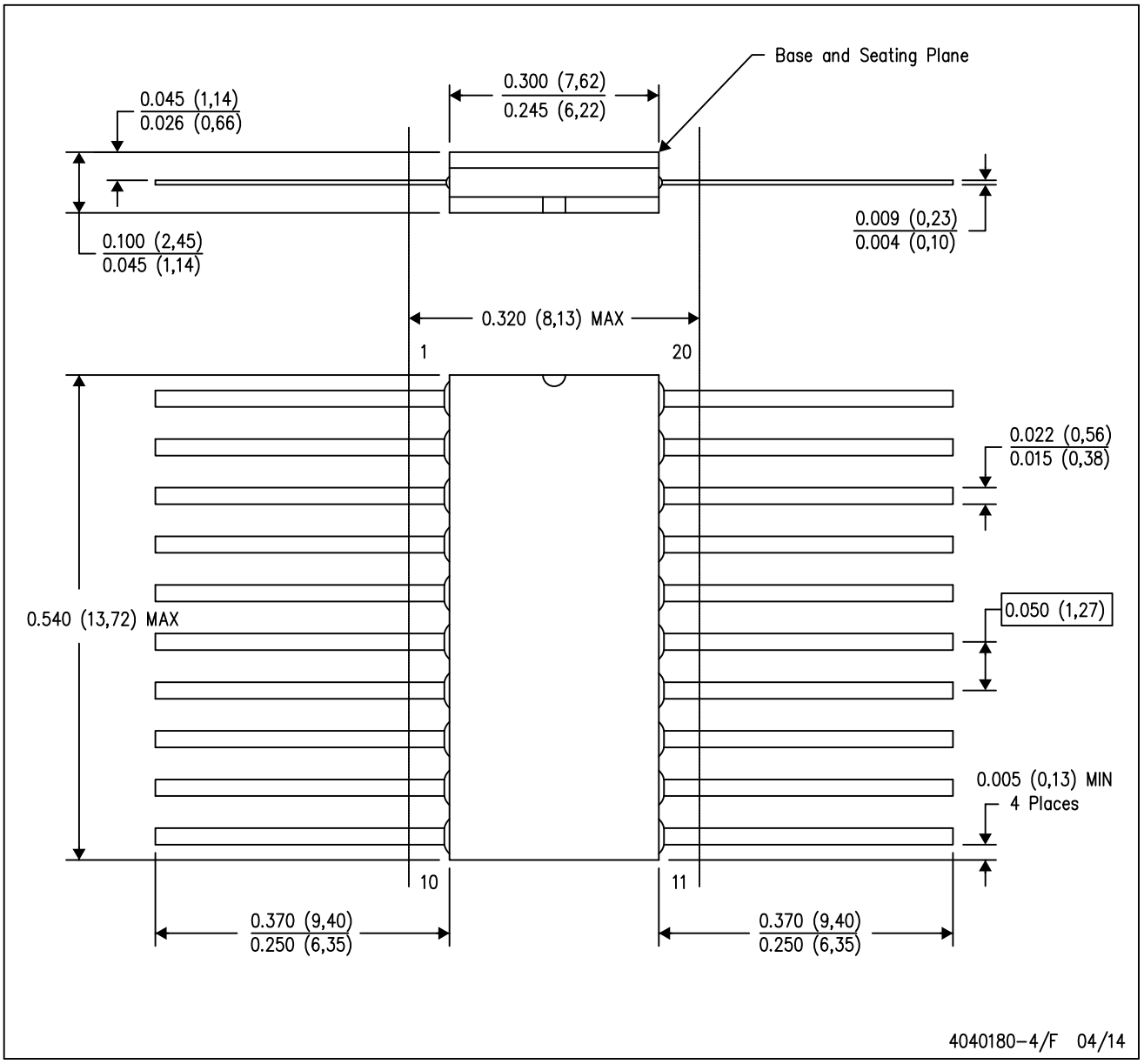

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



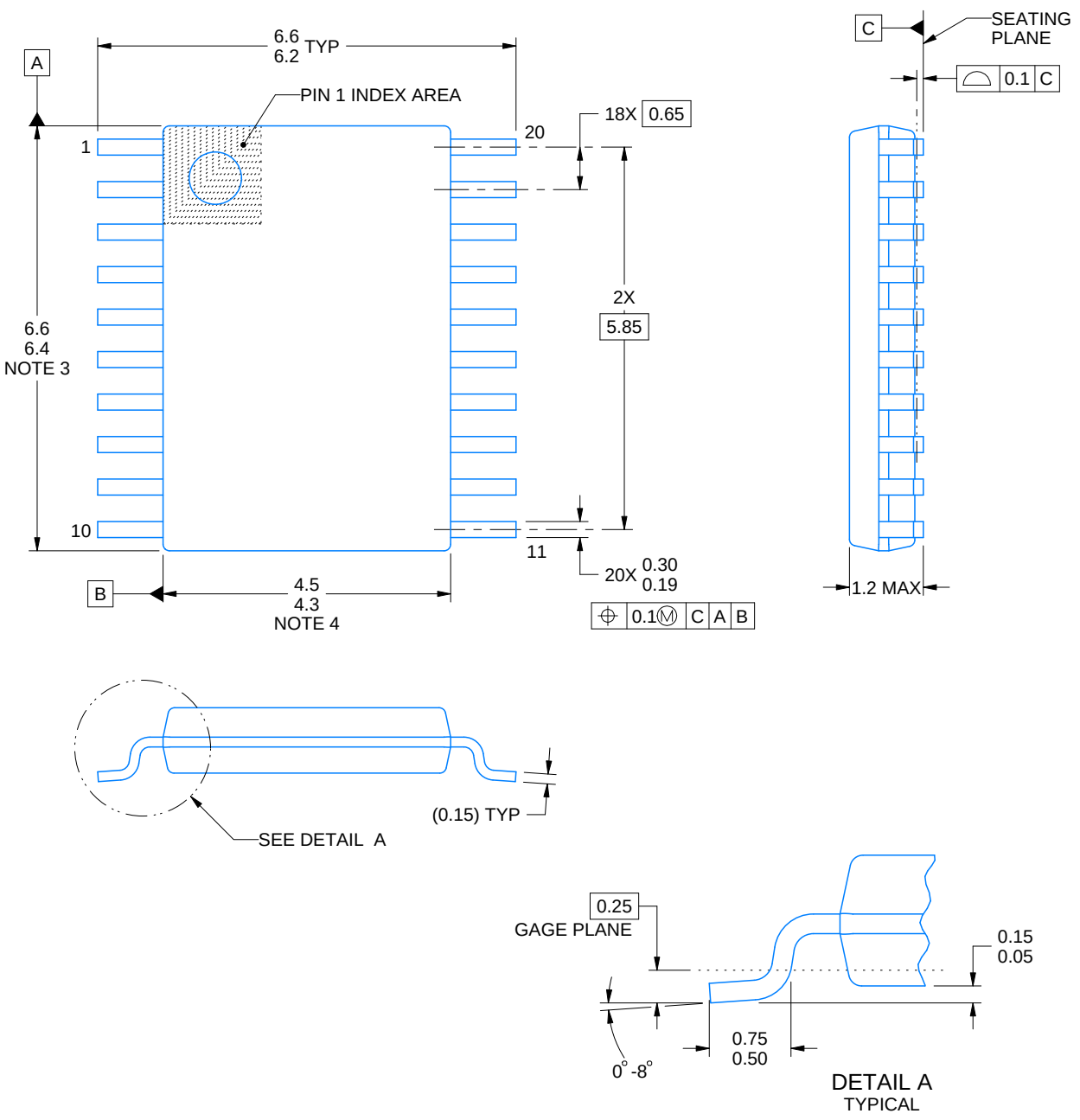

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

# PACKAGE OUTLINE

## PW0020A

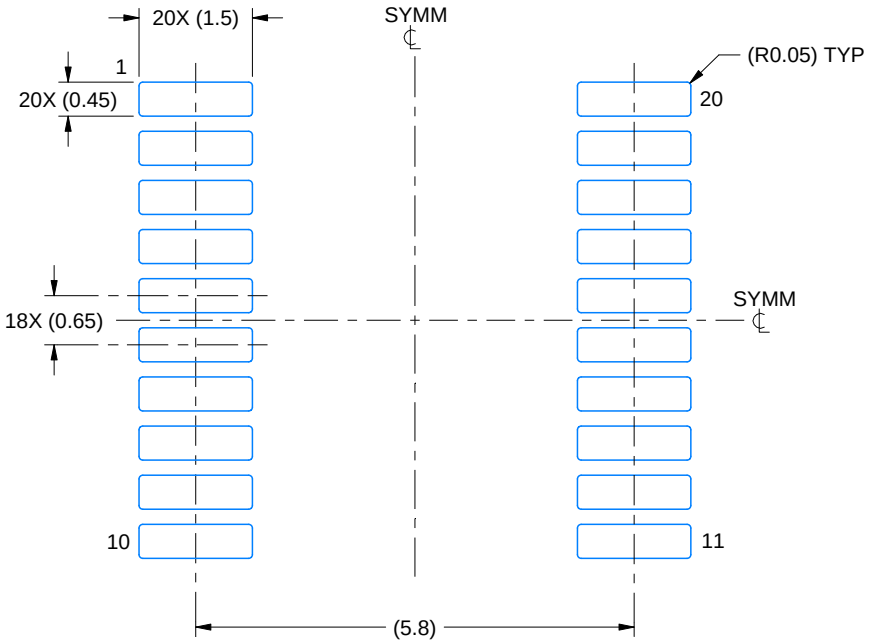
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



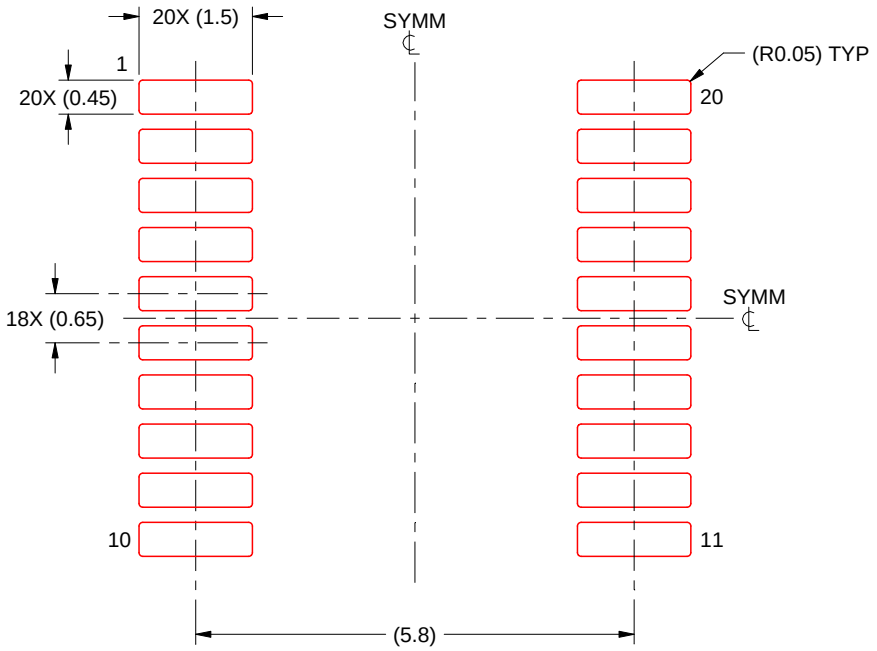

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

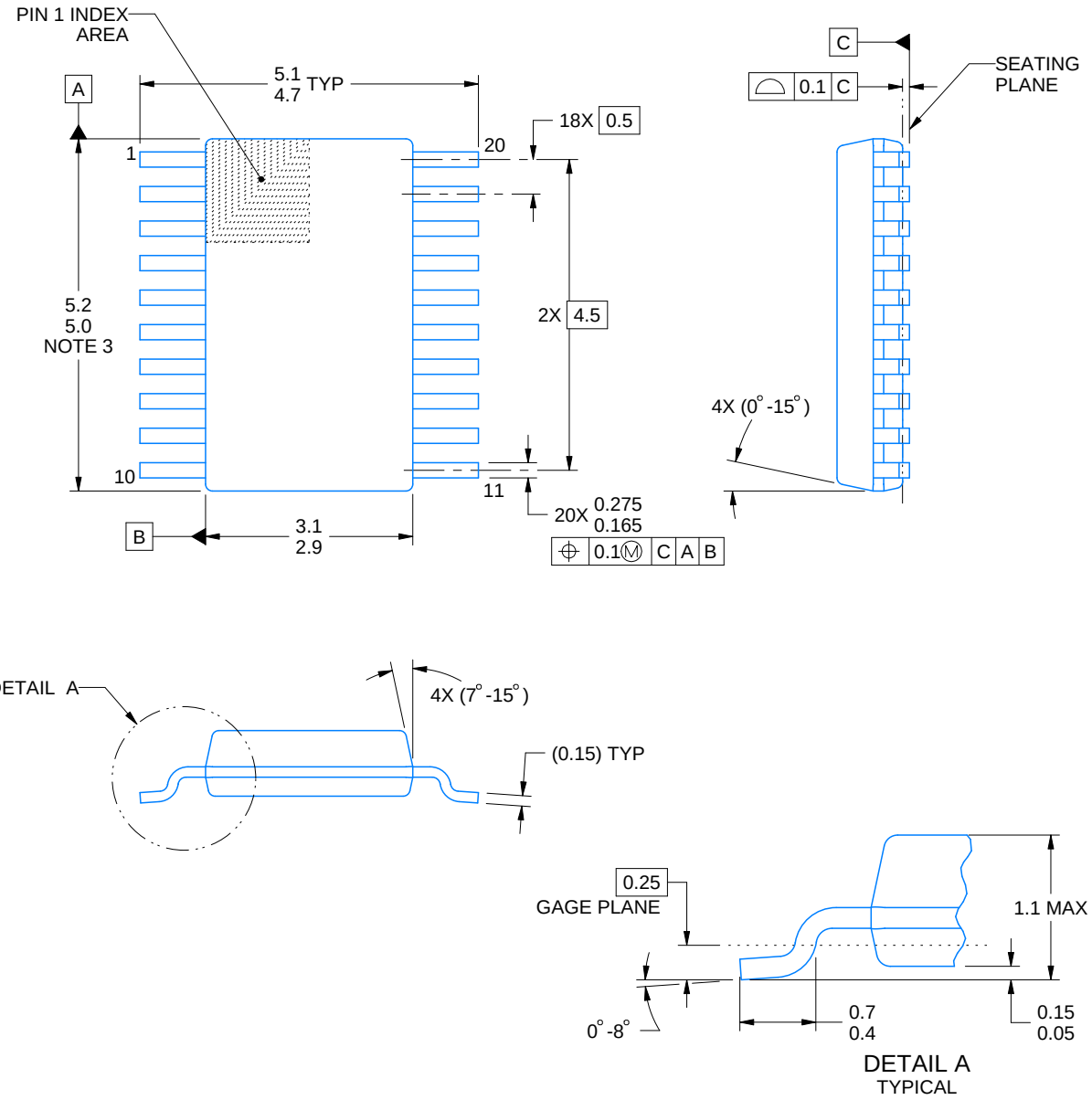
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGS0020A

## VSSOP - 1.1 mm max height

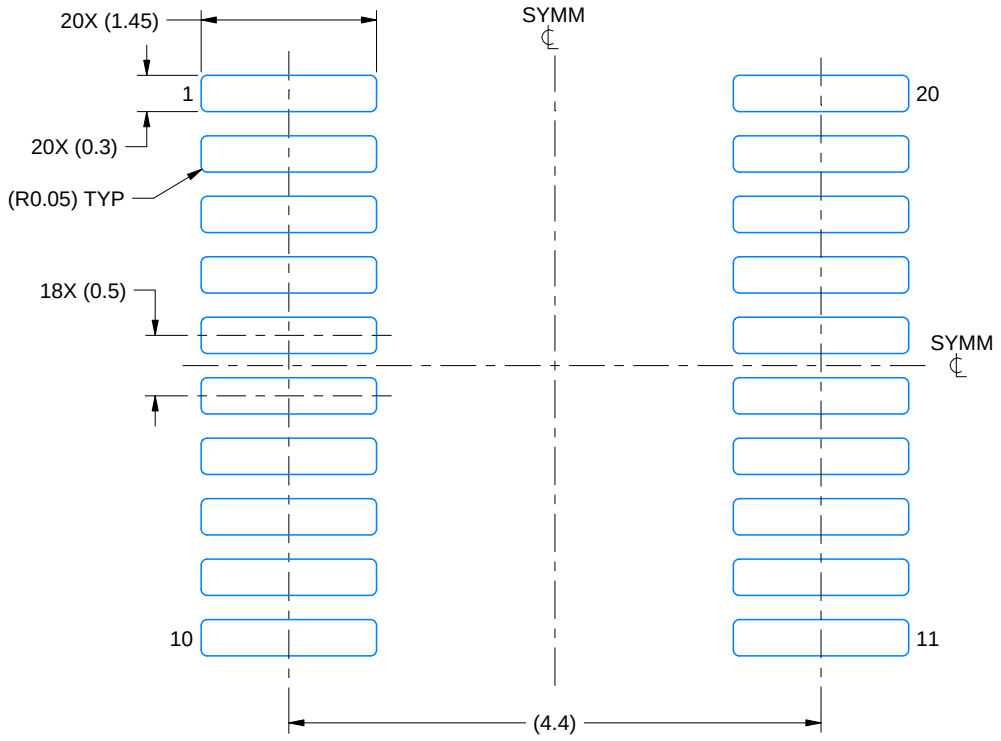
SMALL OUTLINE PACKAGE



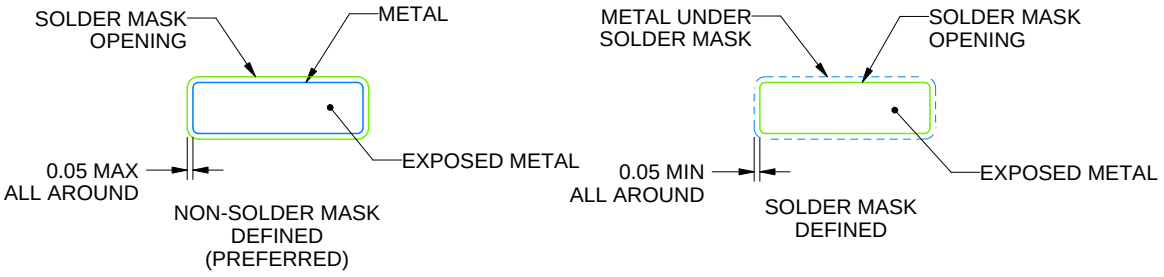

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
SCALE: 16X

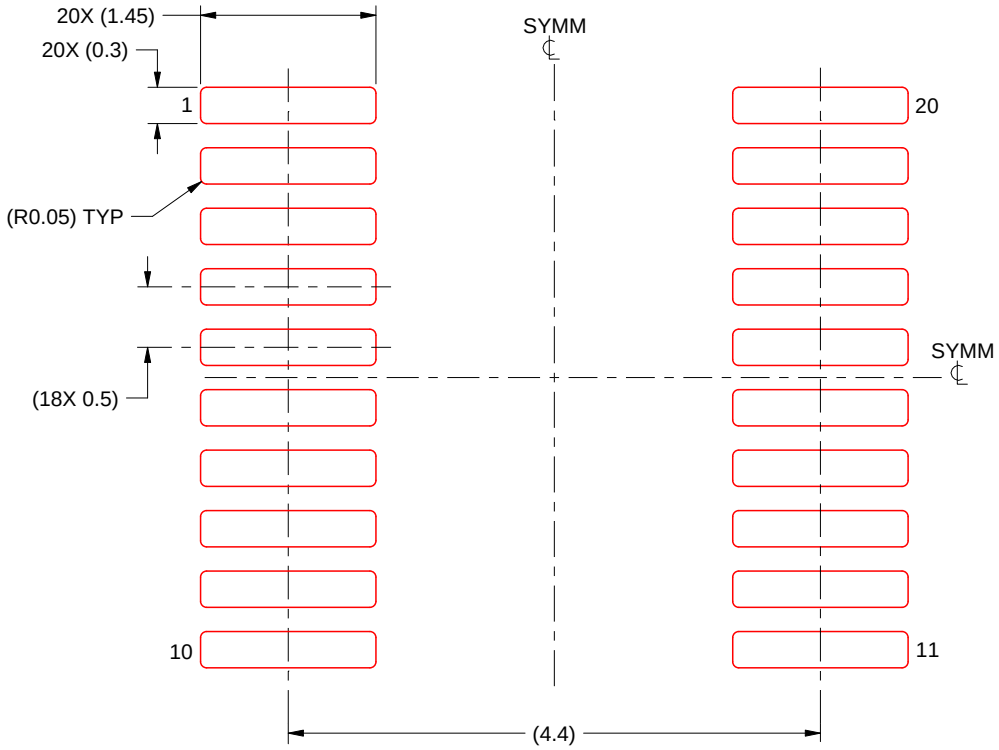



SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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