SNx4BCT374 3 ステート出力、オクタル・エッジトリガ D タイプ・ラッチ

1 特長

- 4.5V～5.5V の動作電源電圧範囲
- BiCMOS 設計 により TTL 設計よりも I_{CCZ} が大幅に削減
- 読み込み時のフル・パラレル・アクセス
- バッファ付き制御入力
- バス・ラインまたはバッファ・メモリ・アドレス・レジスタを駆動できる 3 ステート出力

2 アプリケーション

- バッファ・レジスタ
- I/O ポート
- バス・ドライバ
- 作業レジスタ

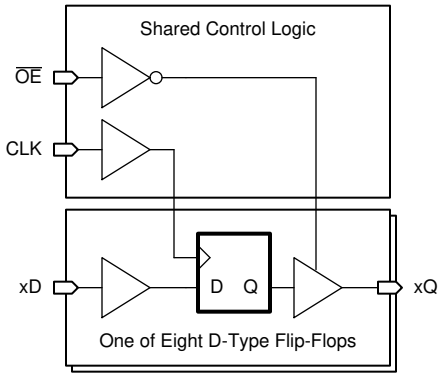
3 概要

SNx4BCT374 デバイスには、8 チャネルの D タイプ・フリップ・フロップが搭載されており、共通のクロック (CLK) および出力イネーブル ($\overline{OE}$) ピンがあります。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
SN74BCT374N	PDIP (20)	25.40mm × 6.35mm
SN74BCT374DW	SOIC (20)	12.80mm × 7.50mm
SN74BCT374NS	SOP (20)	12.60mm × 5.30mm
SN74BCT374DB	SSOP (20)	7.20mm × 5.30mm
SN54BCT374J	CDIP (20)	26.92mm × 6.92mm
SN54BCT374W	CFP (20)	13.72mm × 6.92mm
SN54BCT374FK	LCCC (20)	8.89mm × 8.89mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (March 2003) to Revision D (February 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「*アプリケーション*」セクションに新しいアプリケーションを追加 ... 1
- 「*概要*」セクションから「*注文情報*」と「*機能*」表を削除 ... 1
- 「*概要*」セクションに「*製品情報*」表を追加 ... 1
- Moved package thermal impedance, Θ_{JA} for the DW, N, and NS packages to セクション 6.4 ... 5
- Added *ESD Ratings* section ... 5
- Added *Thermal Information* section ... 6
- Changed I_{OS}(min) value From: *–100 mA* To: *–50 mA* ... 6
- Added *Timing Requirements*, *Switching Characteristics*, and *Typical Characteristics* sections ... 7
- Added *Detailed Description* section ... 10
- Added *Application and Implementation* section ... 12
- Added *Power Supply Recommendations* and *Layout* sections ... 14

Changes from Revision B (April 1994) to Revision C (March 2003) — **Page**

- 「*概要*」セクションに「*注文情報*」表を追加 ... 1
- Added package thermal impedance, Θ_{JA} for the DW, N, and NS packages ... 5

Changes from Revision A (November 1993) to Revision B (April 1994) — **Page**

- 完全なデータシートの最初の公開リリース ... 1

5 Pin Configuration and Functions

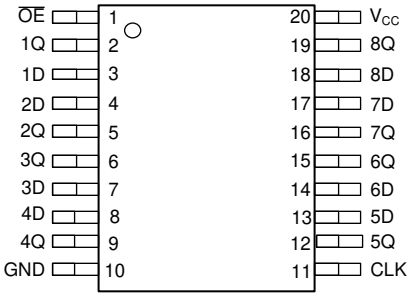


図 5-1. DB, DW, N, NS, J, or W Package 20-Pin SSOP, SOIC, PDIP, SO, CDIP, or CFP Top View

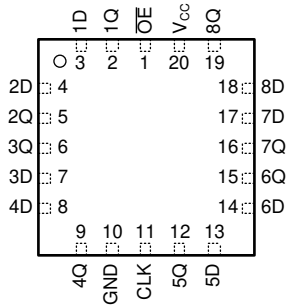


図 5-2. FK Package 20-Pin LCCC Transparent Top View

表 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	I	Output enable, active low
1Q	2	O	Channel 1 output
1D	3	I	Channel 1 input
2D	4	I	Channel 2 input
2Q	5	O	Channel 2 output
3Q	6	O	Channel 3 output
3D	7	I	Channel 3 input
4D	8	I	Channel 4 input
4Q	9	O	Channel 4 output
GND	10	G	Ground
CLK	11	I	Clock, rising edge triggered
5Q	12	O	Channel 5 output
5D	13	I	Channel 5 input
6D	14	I	Channel 6 input
6Q	15	O	Channel 6 output
7Q	16	O	Channel 7 output
7D	17	I	Channel 7 input
8D	18	I	Channel 8 input
8Q	19	O	Channel 8 output
V_{CC}	20	P	Positive supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the disabled or power-off state		–0.5	5.5	V
V_O	Voltage range applied to any output in the high state		–0.5	V_{CC}	V
I_{IK}	Input clamp current			–30	mA
I_{OL}	Current into any output in the low state	SN54BCT374		96	mA
		SN74BCT374		128	
T_{stg}	Storage temperature range(3)		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The negative input voltage rating may be exceeded if the input clamp current rating is observed.
(3) Long-term high-temperature storage and extended use at maximum recommended operating conditions or both may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

6.3 Recommended Operating Conditions(1)

		Operating free-air temperature (T_A)						UNIT
		–55°C to 125°C(2)			0°C to 70°C(3)			
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}				–2			–15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.
(2) Applies to SN54BCT374 devices only
(3) Applies to SN74BCT374 devices only

6.4 Thermal Information

THERMAL METRIC[1]		SN74BCT374				UNIT
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)	
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.4	73.4	59.7	71.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.1	41.9	40.6	36.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.2	14.6	24.9	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.5	41.4	40.3	35.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	38.8	50.0	34.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		Operating free-air temperature (T_A)						UNIT
			–55°C to 125°C[3]			0°C to 70°C[4]			
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = –12 mA	2	3.2					
		I_{OH} = –15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.4			0.4	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				–0.6			–0.6	mA
I_{OS} [2]	V_{CC} = 5.5 V, V_O = 0 V		–50		–225	–50		–225	mA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	µA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				–50			–50	µA
I_{CCL}	V_{CC} = 5.5 V			37	60		37	60	mA
I_{CCH}	V_{CC} = 5.5 V			2	5		2	5	mA
I_{CCZ}	V_{CC} = 5.5 V			5	8		5	8	mA
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			6		pF
C_o	V_{CC} = 5 V, V_O = 2.5 V or 0.5 V			10			10		pF

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
(3) Applies to SN54BCT374 devices only
(4) Applies to SN74BCT374 devices only

6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			Operating free-air temperature (T_A)						UNIT
			25°C[1]		–55°C to 125°C[2]		0°C to 70°C[3]		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			70		70		70	MHz
t_w	Pulse duration	CLK high	7		8		7		ns
t_{su}	Setup time before CLK ↑	Data high or low	6.5		6.5		6.5		ns
t_h	Hold time after CLK ↑	Data high or low	0		0		0		ns

(1) V_{CC} = 5 V, T_A = 25°C, applies to all SN54BCT374 and SN74BCT374 devices
(2) Applies to SN54BCT374 devices only
(3) Applies to SN74BCT374 devices only

6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Operating free-air temperature (T_A)							UNIT
			25°C[1]			–55°C to 125°C[2] [3]		0°C to 70°C[2] [4]		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			70			70		70		MHz
t_{PLH}	CLK	Q	2	7.2	9.1	2	11.6	2	10.6	ns
t_{PHL}			2	7.1	8.8	2	10.6	2	10	
t_{PZH}	$\overline{OE}$	Q	1	8.3	10.1	1	12.7	1	12.3	ns
t_{PZL}			1	8.6	10.6	1	13	1	12.7	
t_{PHZ}	OE	Q	1	4.7	6.3	1	7.1	1	6.8	ns
t_{PLZ}			1	4.8	6.3	1	7.5	1	6.8	

(1) V_{CC} = 5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = 25°C, applies to all SN54BCT374 and SN74BCT374 devices
(2) V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω
(3) Applies to SN54BCT374 devices only
(4) Applies to SN74BCT374 devices only

6.8 Typical Characteristics

T_A = 25°C

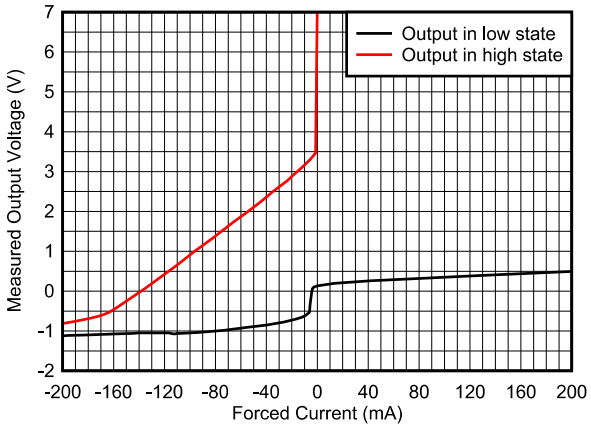
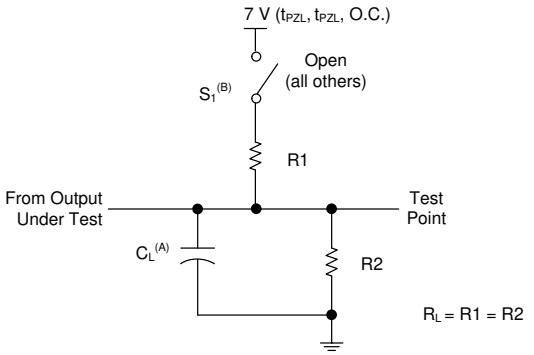


図 6-1. Typical output voltage versus output current for BCT family drivers

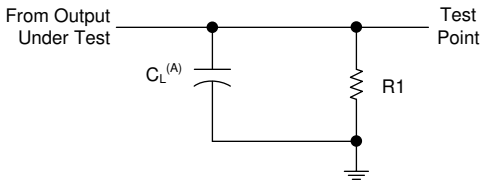
7 Parameter Measurement Information

All parameters and waveforms are not applicable to all devices.



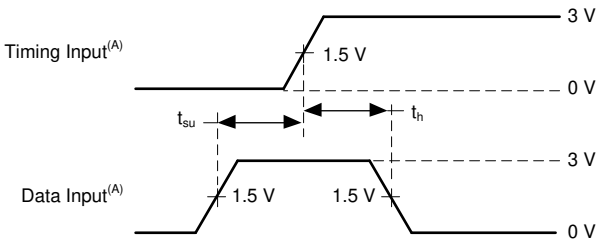
A. C_L includes probe and jig capacitance.
B. When measuring propagation delay times of 3-state outputs, switch S1 is open.

図 7-1. Load circuit for 3-state and open-collector outputs



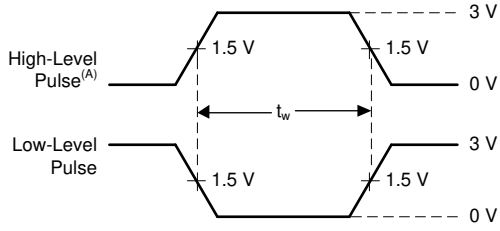
A. C_L includes probe and jig capacitance.

図 7-2. Load circuit for push-pull outputs



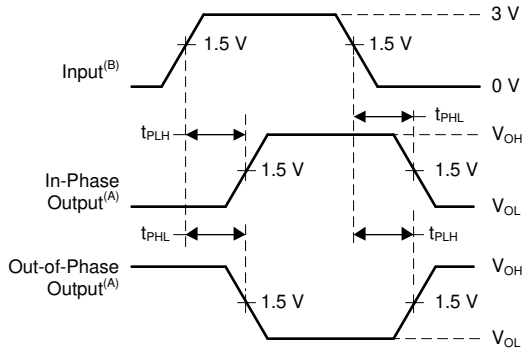
A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.

図 7-3. Voltage waveforms Setup and hold times



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.

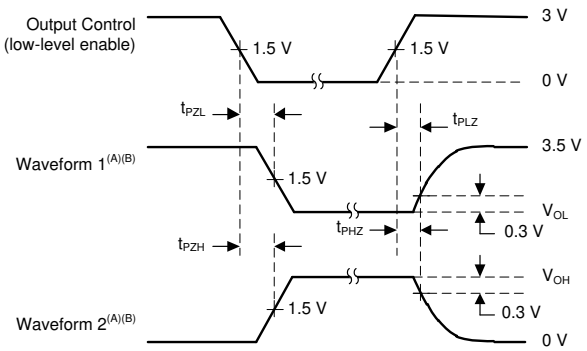
図 7-4. Voltage waveforms Pulse duration



A. The outputs are measured one at a time with one transition per measurement.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.

図 7-5. Voltage waveforms Propagation delay times



A. The outputs are measured one at a time with one transition per measurement.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

図 7-6. Voltage waveforms Enable and disable times, 3-state outputs

8 Detailed Description

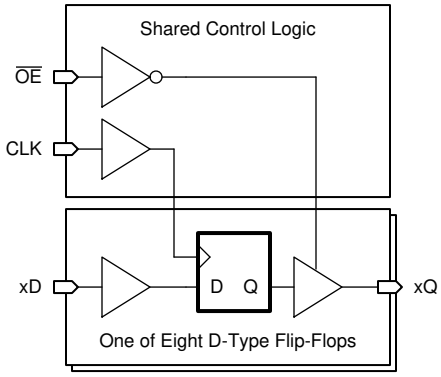
8.1 Overview

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the SNx4BCT374 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bipolar Push-Pull Outputs

This device includes bipolar push-pull outputs. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused bipolar push-pull outputs should be left disconnected.

8.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in Implications of Slow or Floating CMOS Inputs.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors, however a 10-kΩ resistor is recommended and will typically meet all requirements.

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have negative clamping diodes only as depicted in 図 8-1.

> **注意**
>
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

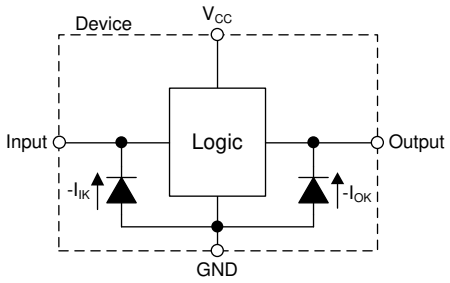


図 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

The *Function Table* below lists the functional modes of the SNx4BCT374.

表 8-1. Function Table

INPUTS(1)			OUTPUT(2)
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

(1) L = Low input, H = High input, ↑ = Low to high transition, X = Do not care.
(2) L = Low output, H = High output, Q_0 = Previous state, Z = High impedance.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SNx4BCT374 contains multiple D-type flip-flops that are operated by the same clock. By connecting multiple channels together in series, a shift register can be formed. This produces a delay of a specific number of clock cycles for incoming data. The application schematic shown below gives an example of using three channels of the SNx4BCT374 to produce a delay of three clock cycles.

9.2 Typical Application

9.2.1 Application

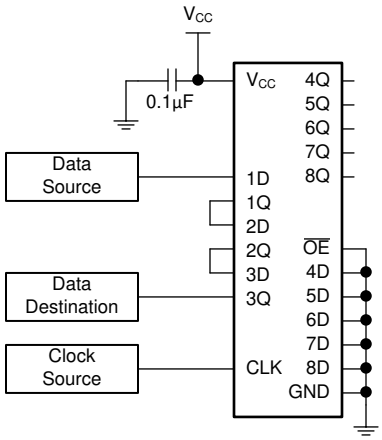


図 9-1. Typical application block diagram

9.2.2 Design Requirements

9.2.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SNx4BCT374 plus the maximum static supply current, I_{CC}, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4BCT374 plus the maximum supply current, I_{CC}, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection.

The SNx4BCT374 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SNx4BCT374 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

9.2.2.2 Output Considerations

The positive supply voltage is used to produce the output high voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output low voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull bipolar outputs should never be connected directly together. This can cause excessive current and damage to the device.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

9.2.2.3 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic low, and $V_{IH(min)}$ to be considered a logic high. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly connected if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of high, and a pull-down resistor is used for a default state of low. The resistor size is limited by drive current of the controller, leakage current into the SNx4BCT374, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SNx4BCT374 has CMOS inputs and thus requires fast input transitions to operate correctly. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.3 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the SNx4BCT374 and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SNx4BCT374 to the receiving device(s).
3. Ensure the resistive load at the output is larger than ($V_{CC} / I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.
5. This device includes D-type flip-flop circuits. The output of these circuits is unknown at system startup. Data must be clocked into each D-type flip-flop to initialize it into a known state.

9.2.4 Application Curves

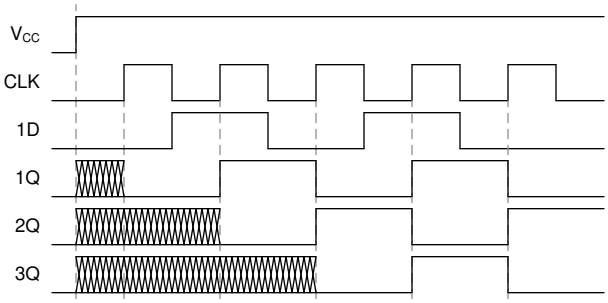


図 9-2. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

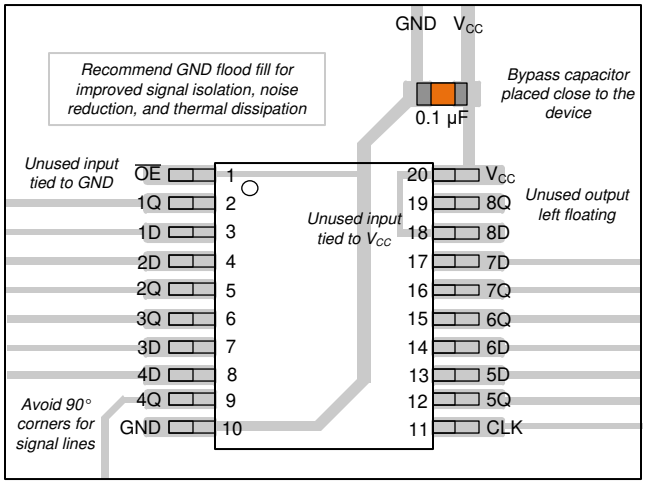


図 11-1. Example layout for the SN74BCT374.

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Input and Output Characteristics of Digital Integrated Circuits* application report
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Understanding and Interpreting Standard-Logic Data Sheets* application report

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9051601M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9051601M2A SNJ54BCT374FK
5962-9051601MRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9051601MRA SNJ54BCT374J
5962-9051601MSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9051601MSA SNJ54BCT374W
SN74BCT374DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT374
SN74BCT374DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT374
SN74BCT374N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74BCT374N
SN74BCT374N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74BCT374N
SN74BCT374NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT374
SN74BCT374NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT374
SNJ54BCT374FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9051601M2A SNJ54BCT374FK
SNJ54BCT374FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9051601M2A SNJ54BCT374FK
SNJ54BCT374J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9051601MRA SNJ54BCT374J
SNJ54BCT374J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9051601MRA SNJ54BCT374J
SNJ54BCT374W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9051601MSA SNJ54BCT374W

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54BCT374W.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9051601MSA SNJ54BCT374W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN54BCT374, SN74BCT374 :

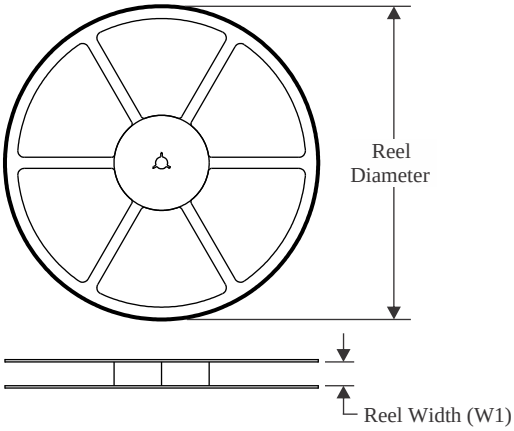
- Catalog : SN74BCT374
- Military : SN54BCT374

NOTE: Qualified Version Definitions:

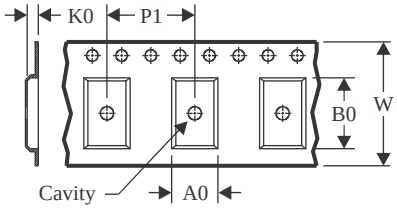
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

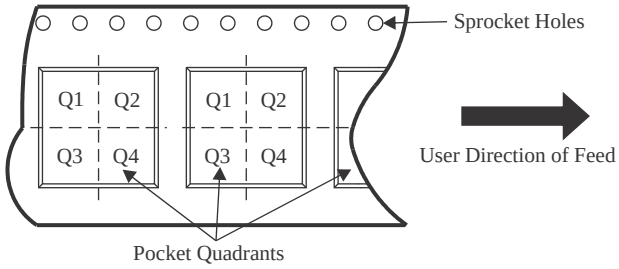


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

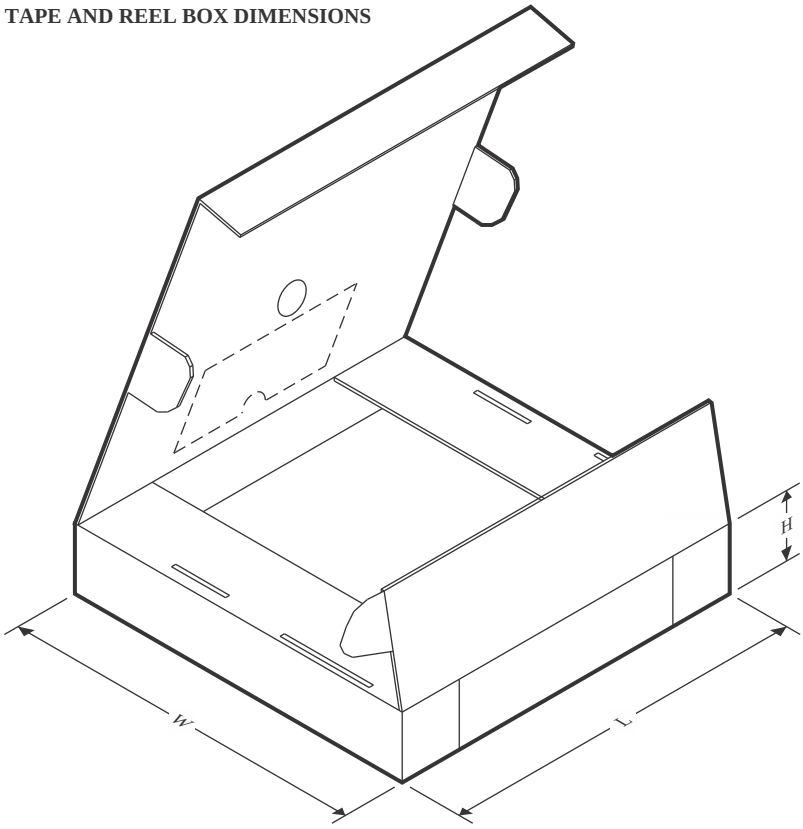
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT374NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

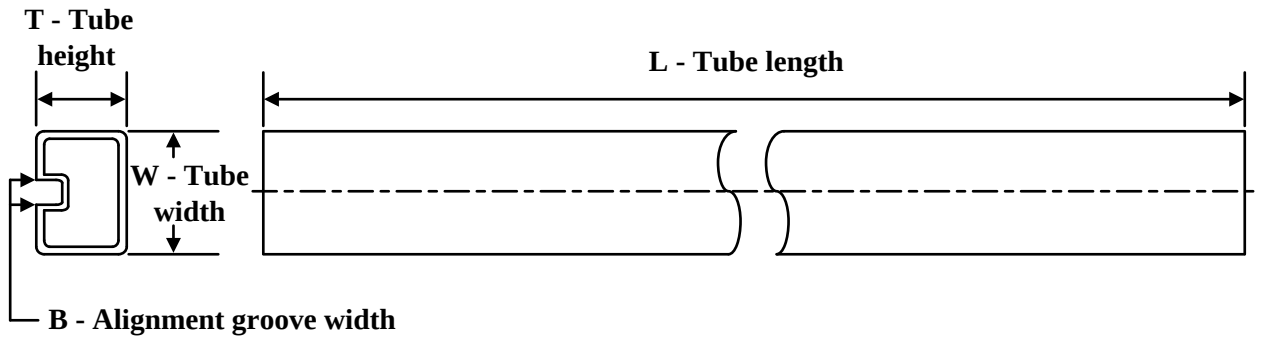
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74BCT374NSR	SOP	NS	20	2000	356.0	356.0	45.0

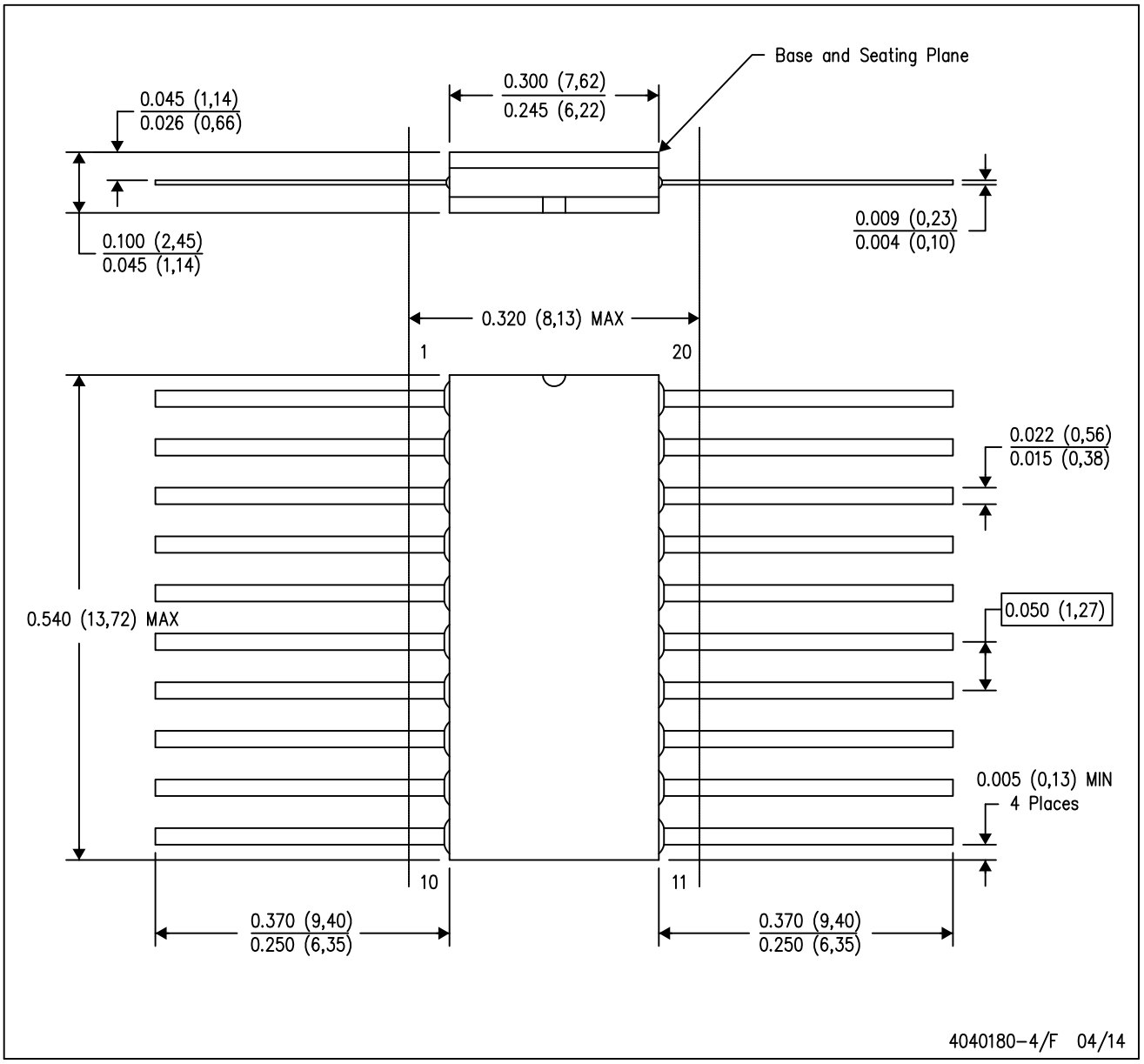
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9051601M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9051601MSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74BCT374DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74BCT374DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74BCT374N	N	PDIP	20	20	506	13.97	11230	4.32
SN74BCT374N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54BCT374FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT374FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT374W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54BCT374W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R–GDFP–F20) CERAMIC DUAL FLATPACK

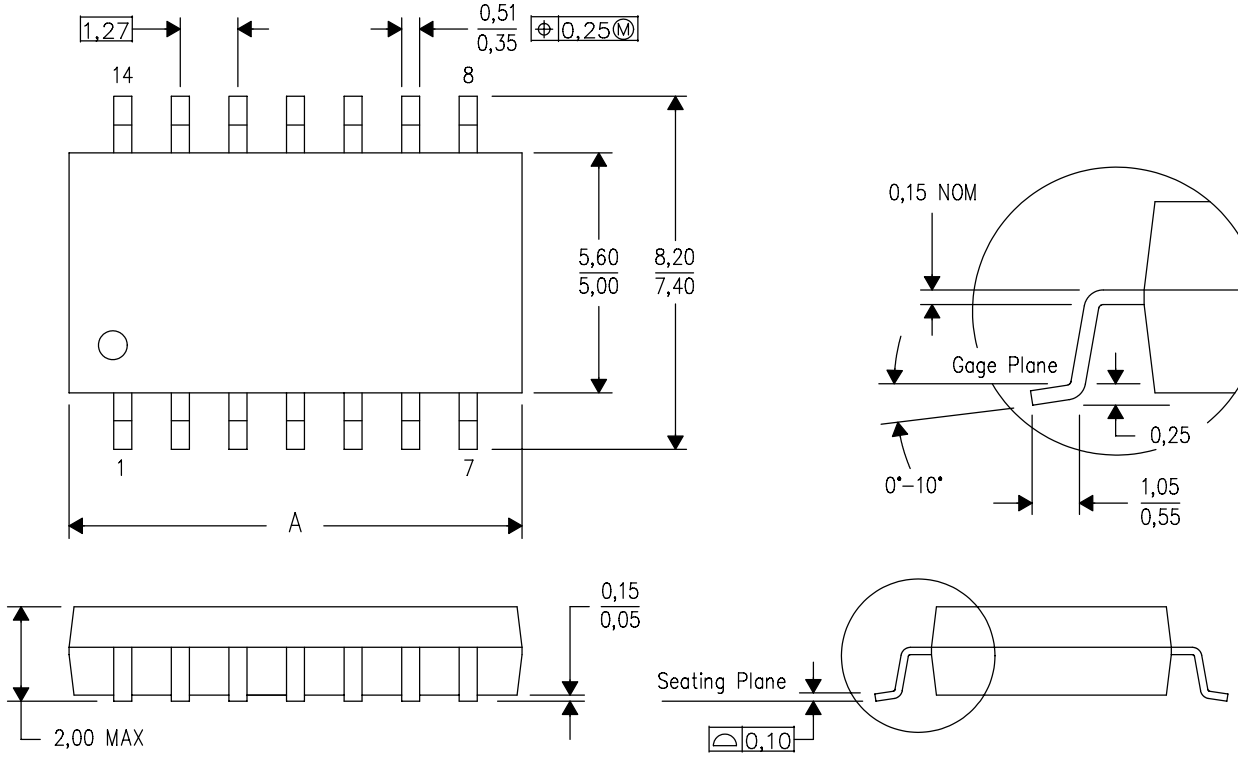


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

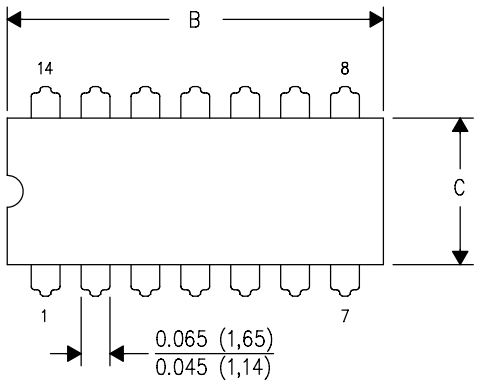
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

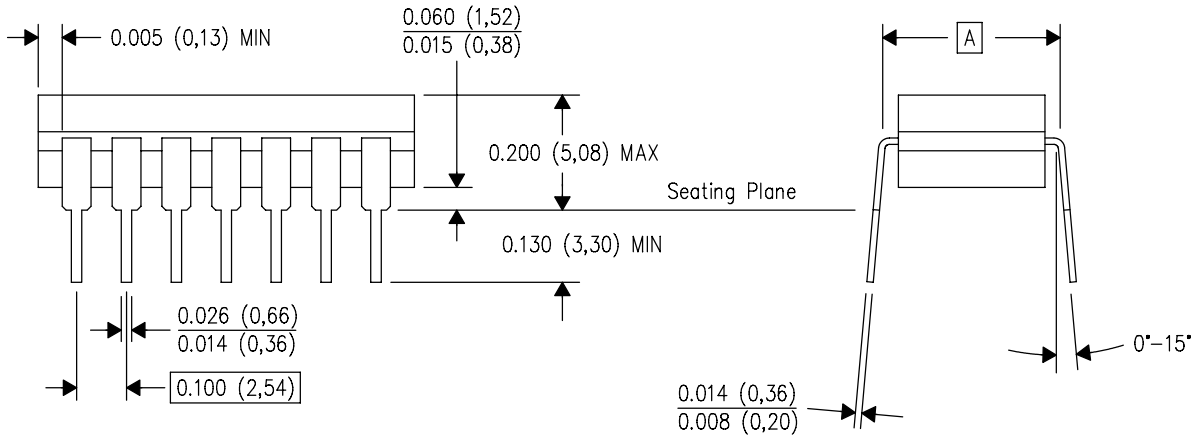
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

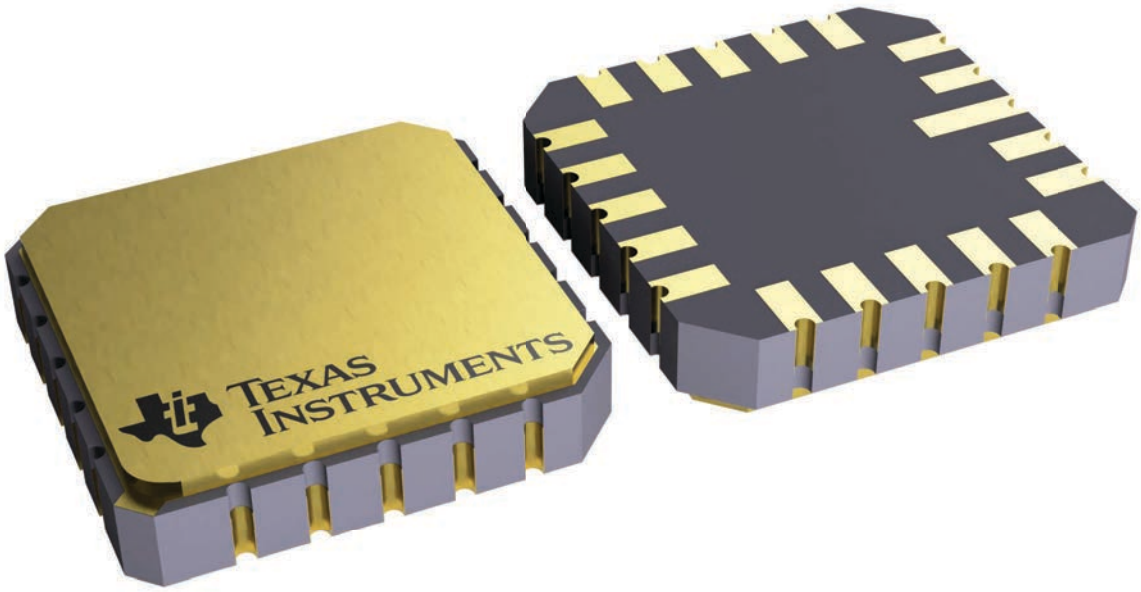
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

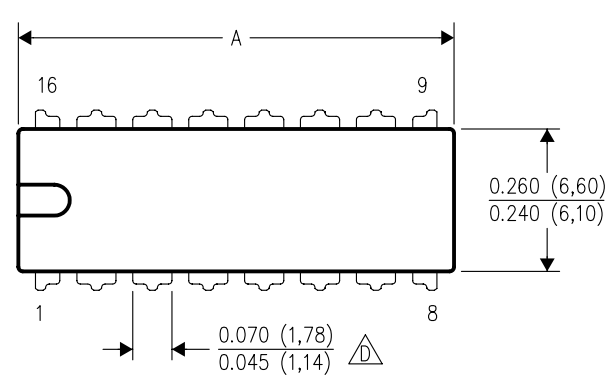


4229370VA\

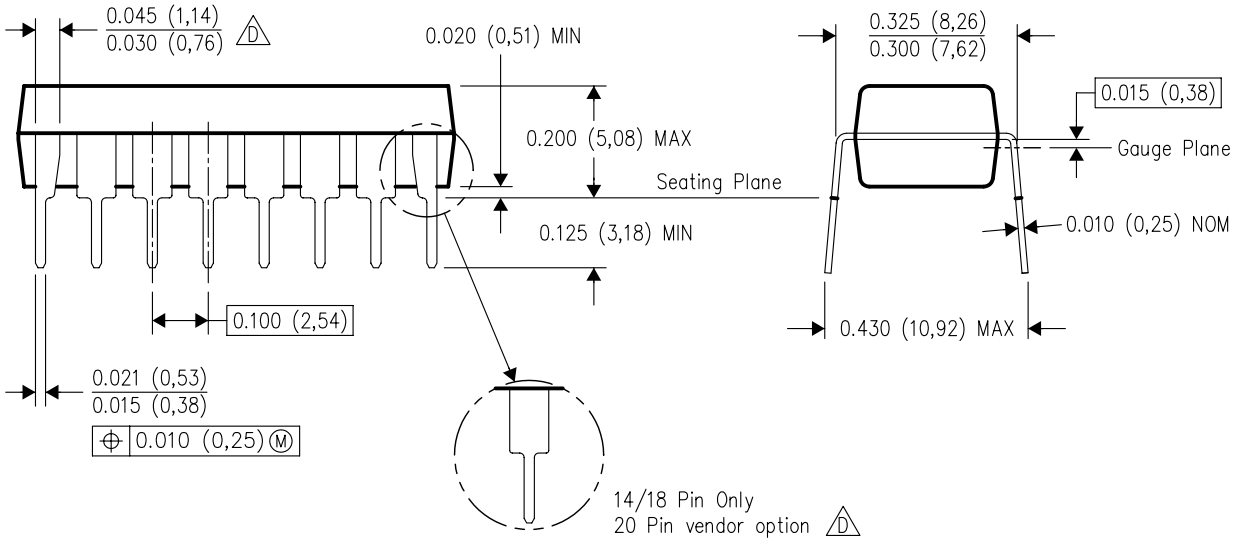
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

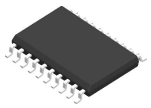


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

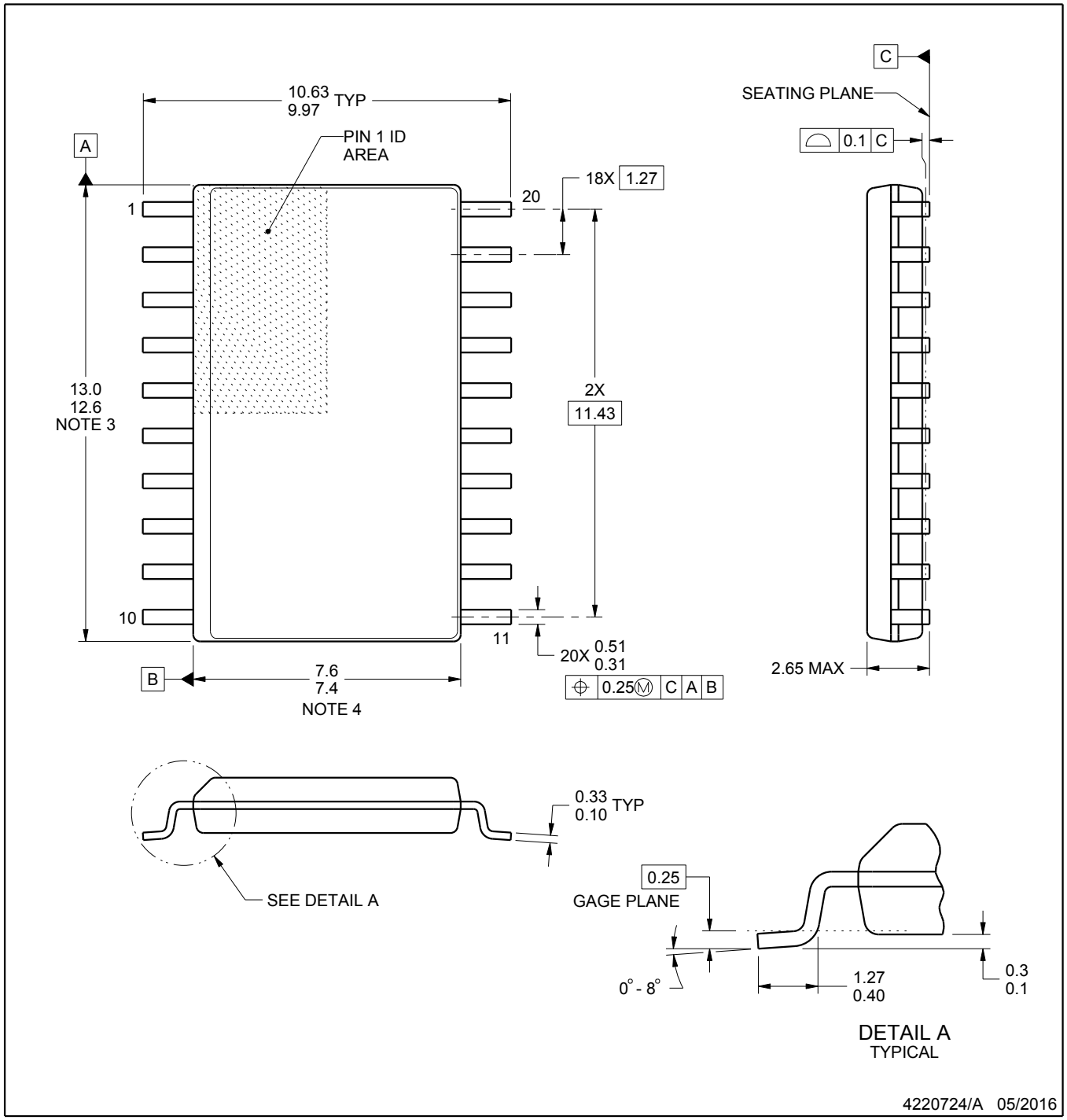


PACKAGE OUTLINE

DW0020A

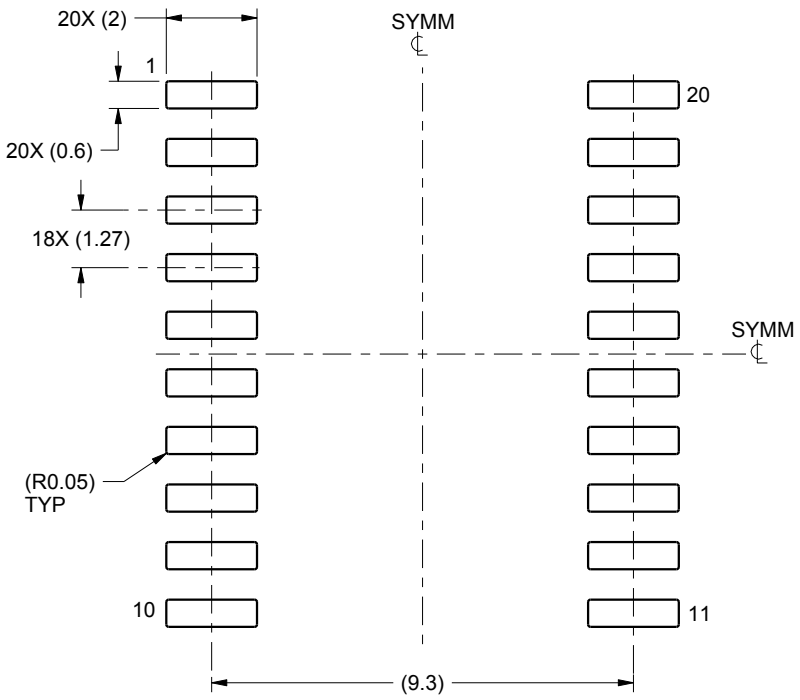
SOIC - 2.65 mm max height

SOIC

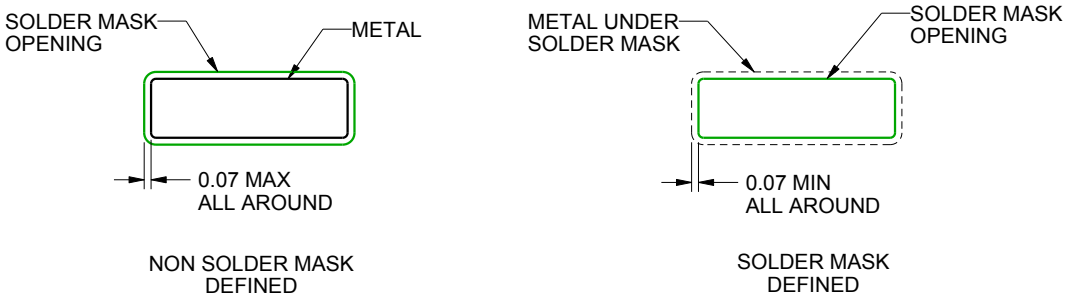


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

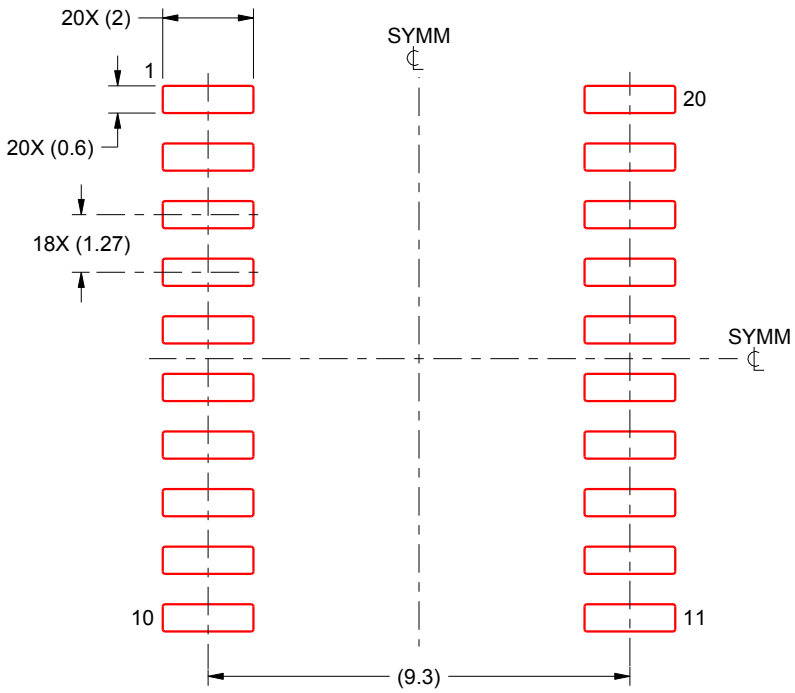


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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最終更新日：2025 年 10 月