

## SN74AHC1G14 シングル・シュミット・トリガ・インバータ・ゲート

## 1 特長

- 動作範囲 : 2V ~ 5.5V
- 最大  $t_{pd}$  10ns (5V 時)
- 低消費電力、最大  $I_{CC}$  10 $\mu$ A
- $\pm 8mA$  の出力駆動能力 (5V 時)
- JESD 17 準拠で 250mA 超のラッチアップ性能

## 2 アプリケーション

- バーコード・スキャナ
- ケーブル・ソリューション
- eBook (電子書籍)
- 組み込み用 PC
- フィールド・トランスマッタ : 温度センサ、圧力センサ
- 指紋認証
- HVAC : 暖房、換気、空調
- ネットワーク接続ストレージ (NAS)
- サーバーのマザーボードおよび PSU
- ソフトウェア定義無線 (SDR)
- テレビ : 高解像度 (HDTV)、LCD、デジタル
- ビデオ通信システム
- ワイヤレス・データ・アクセス・カード、ヘッドセット、キーボード、マウス、LAN カード

## 3 概要

SN74AHC1G14 デバイスはシングル・インバータ・ゲートです。このデバイスは、ブール関数  $Y = \bar{A}$  を実行します。

## パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)	本体サイズ (3)
SN74AHC1G14	DBV (SOT-23, 5)	2.8mm × 2.8mm	2.9mm × 1.6mm
	DCK (SC-70, 5)	2mm × 2.1mm	2mm × 1.25mm
	DRL (SOT-553, 5)	1.6mm × 1.6mm	1.6mm × 1.2mm

- 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- パッケージ・サイズ(長さ×幅)は公称値であり、該当する場合はピンも含まれます。
- 本体サイズ(長さ×幅)は公称値であり、ピンは含まれません。



論理図 (正論理)



このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール(機械翻訳)を使用していることがあります。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.comで必ず最新の英語版をご参照くださいますようお願いいたします。

## Table of Contents

1 特長.....	1	7.2 Functional Block Diagram.....	8
2 アプリケーション.....	1	7.3 Feature Description.....	8
3 概要.....	1	7.4 Device Functional Modes.....	8
4 Pin Configuration and Functions.....	3	8 Application and Implementation.....	9
5 Specifications.....	4	8.1 Application Information.....	9
5.1 Absolute Maximum Ratings.....	4	8.2 Typical Application.....	9
5.2 ESD Ratings.....	4	8.3 Power Supply Recommendations.....	10
5.3 Recommended Operating Conditions.....	4	8.4 Layout.....	10
5.4 Thermal Information.....	5	9 Device and Documentation Support.....	12
5.5 Electrical Characteristics.....	5	9.1 Documentation Support (Analog).....	12
5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	6	9.2 サポート・リソース.....	12
5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	6	9.3 Trademarks.....	12
5.8 Operating Characteristics.....	6	9.4 静電気放電に関する注意事項.....	12
5.9 Typical Characteristics.....	6	9.5 用語集.....	12
6 Parameter Measurement Information.....	7	10 Revision History.....	12
7 Detailed Description.....	8	11 Mechanical, Packaging, and Orderable	
7.1 Overview.....	8	Information.....	12

## 4 Pin Configuration and Functions

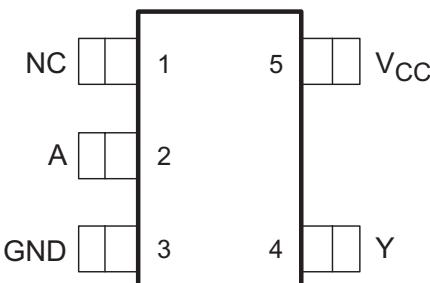


図 4-1. DBV Package 5-Pin SOT-23 Top View

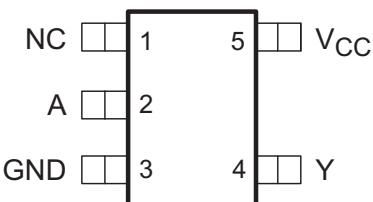


図 4-2. DCK Package 5-Pin SC70 Top View

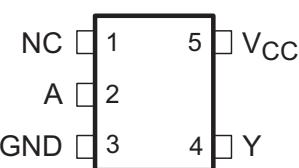


図 4-3. DRL Package 5-Pin SOT Top View

表 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	NC	—	No connect
2	A	I	Data Input
3	GND	—	Ground
4	Y	O	Data Output
5	VCC	—	Power

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		-0.5	7	V
$V_I$	Input voltage <sup>(2)</sup>		-0.5	7	V
$V_O$	Output voltage <sup>(2)</sup>		-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		-20	mA
$I_{OK}$	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		$\pm 20$	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		$\pm 25$	mA
	Continuous current through $V_{CC}$ or GND			$\pm 50$	mA
$T_j$	Maximum junction temperature			150	°C
$T_{stg}$	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	$\pm 1500$
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	5.5	V
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V		-50	μA
		$V_{CC} = 3.3$ V $\pm 0.3$ V		-4	mA
		$V_{CC} = 5$ V $\pm 0.5$ V		-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V		50	μA
		$V_{CC} = 3.3$ V $\pm 0.3$ V		4	mA
		$V_{CC} = 5$ V $\pm 0.5$ V		8	
$T_A$	Operating free-air temperature		-40	125	°C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>			SN74AHC1G14			UNIT
			DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
			5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance		278	289.2	271.8	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance		180.5	205.8	116.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		184.4	176.2	89.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter		115.4	117.6	17.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter		183.4	175.1	89.4	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bot) thermal resistance		N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$			RECOMMENDED			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{T+}$	Positive-going input threshold voltage		3 V	1.2	2.2	1.2	2.2	2.2	1.2	2.2	2.2	V
			4.5 V	1.75	3.15	1.75	3.15	3.15	1.75	3.15	3.15	
			5.5 V	2.15	3.85	2.15	2.85	2.15	2.15	3.85	3.85	
$V_{T-}$	Negative-going input threshold voltage		3 V	0.9	1.9	0.9	1.9	0.9	0.9	1.9	1.9	V
			4.5 V	1.35	2.75	1.35	2.75	1.35	1.35	2.75	2.75	
			5.5 V	1.65	3.35	1.65	3.35	1.65	1.65	3.35	3.35	
$\Delta V_T$	Hysteresis ( $V_{T+} - V_{T-}$ )		3 V	0.3	1.2	0.3	1.2	1.2	0.25	1.2	1.2	V
			4.5 V	0.4	1.4	0.4	1.4	1.4	0.35	1.4	1.4	
			5.5 V	0.5	1.6	0.5	1.6	1.6	0.45	1.6	1.6	
$V_{OH}$	High level output voltage	$I_{OH} = -50 \mu\text{A}$	2 V	1.9	2	1.9			1.9			V
			3 V	2.9	3	2.9			2.9			
			4.5 V	4.4	4.5	4.4			4.4			
		$I_{OH} = -4 \text{ mA}$	3 V	2.58		2.48			2.4			
		$I_{OL} = -8 \text{ mA}$	4.5 V	3.94		3.8			3.7			
$V_{OL}$	Low level output voltage	$I_{OH} = 50 \mu\text{A}$	2 V		0.1		0.1		0.1		0.1	V
			3 V		0.1		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1		0.1	
		$I_{OH} = 4 \text{ mA}$	3 V		0.36		0.44		0.55			
		$I_{OL} = 8 \text{ mA}$	4.5 V		0.36		0.44		0.55			
$I_I$	Input leakage current	$V_I = 5.5 \text{ V}$ or GND	0 V to 5.5 V		±0.1		±1		±1		±1	µA
$I_{CC}$	Supply current	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		1		10		10		10	µA
$C_i$	Input Capacitance	$V_I = V_{CC}$ or GND	5 V	2	10		10		10		10	pF

## 5.6 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$		RECOMMENDED $T_A = -40^\circ\text{C} \text{ to } 125^\circ\text{C}$		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$	8.3	12.8	1	15	1	16	ns
$t_{PHL}$				8.3	12.8	1	15	1	16	ns
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$	10.8	16.3	1	18.5	1	19.5	ns
$t_{PHL}$				10.8	16.3	1	18.5	1	19.5	ns

## 5.7 Switching Characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

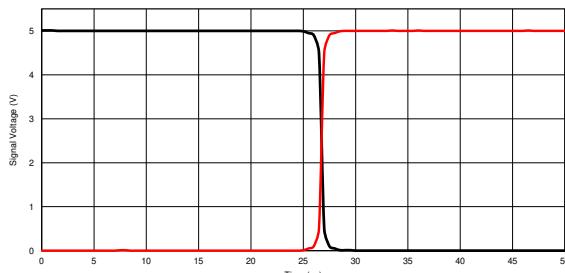
PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$		RECOMMENDED $T_A = -40^\circ\text{C} \text{ to } 125^\circ\text{C}$		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y	$C_L = 15 \text{ pF}$	5.5	8.6	1	10	1	11	ns
$t_{PHL}$				5.5	8.6	1	10	1	11	ns
$t_{PLH}$	A or B	Y	$C_L = 50 \text{ pF}$	7	10.6	1	12	1	11	ns
$t_{PHL}$				7	10.6	1	12	1	11	ns

## 5.8 Operating Characteristics

$V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1 \text{ MHz}$	9	pF

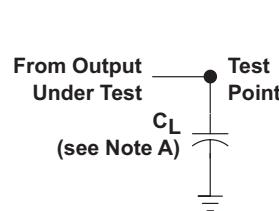
## 5.9 Typical Characteristics



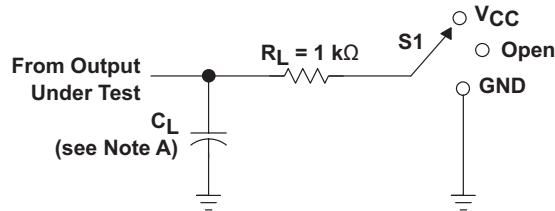
$T_A = 25^\circ\text{C}$ ,  $V_A = 5 \text{ V}$

図 5-1. Response Time vs Output Voltage

## 6 Parameter Measurement Information

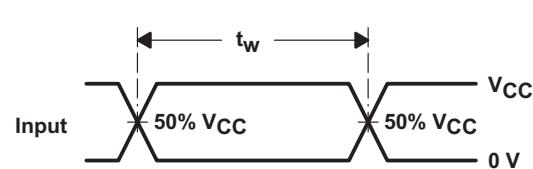


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

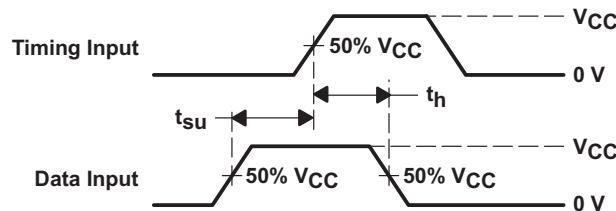


LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS

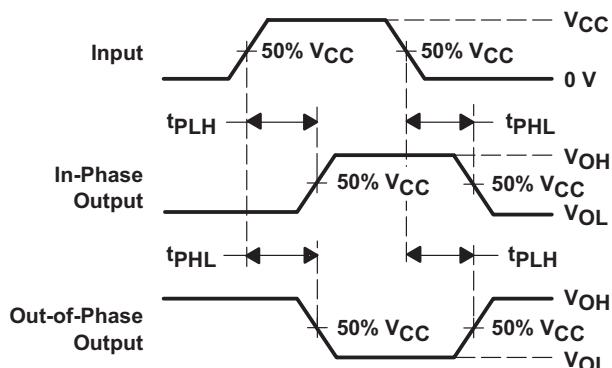
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND
Open Drain	$V_{CC}$



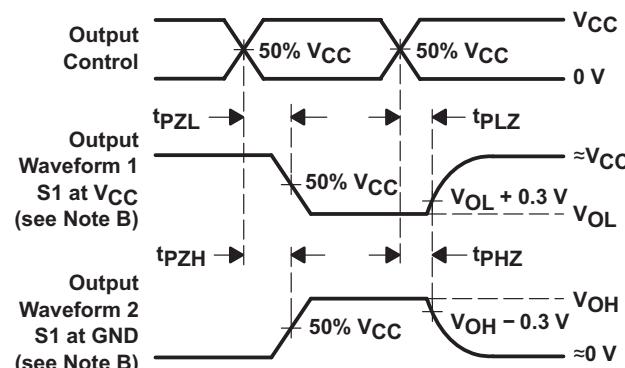
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_0 = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

図 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The SN74AHC1G14 device is a single inverter gate. The device performs the Boolean function  $Y = \bar{A}$ .

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

### 7.2 Functional Block Diagram

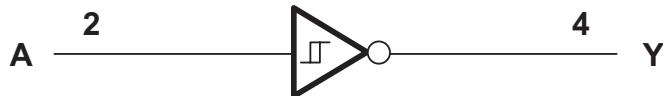


図 7-1. Logic Diagram (Positive Side)

### 7.3 Feature Description

The SN74AHC1G14 device has a wide operating  $V_{CC}$  range of 2 V to 5.5 V, which allows it to be used in a broad range of systems. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low-power consumption makes this device a good choice for portable and battery power-sensitive applications.

### 7.4 Device Functional Modes

表 7-1 lists the functional modes for SN74AHC1G14.

表 7-1. Function Table

INPUT <sup>(1)</sup> A	OUTPUT <sup>(2)</sup> Y
H	L
L	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 8.1 Application Information

Physically interactive interface elements like push buttons or rotary knobs offer simple and easy ways to interact with an electronic system. Many of these physical interface elements often have issues with bouncing, or where the physical conductive contact can connect and disconnect multiple times during a button push or release. This bouncing can cause one or more faulty transient signals to be passed during this transitional period. These faulty signals can be observed in many common applications, for example, a television remote with bouncing error can adjust the TV channel multiple times despite the button being pushed only once. To mitigate these faulty signals, we can use a Schmitt-trigger, or a device with hysteresis, to remove these faulty signals. Hysteresis allows a device to *remember* its history, and in this case, the SN74AHC1G14 uses this memory to debounce the signal of the physical element, or filter the faulty transient signals and pass only the valid signal each time the element is used. In this example, we show a push-button signal passed through an SN74AHC1G14 that is debounced and inverted to the microprocessor for push detection.

### 8.2 Typical Application

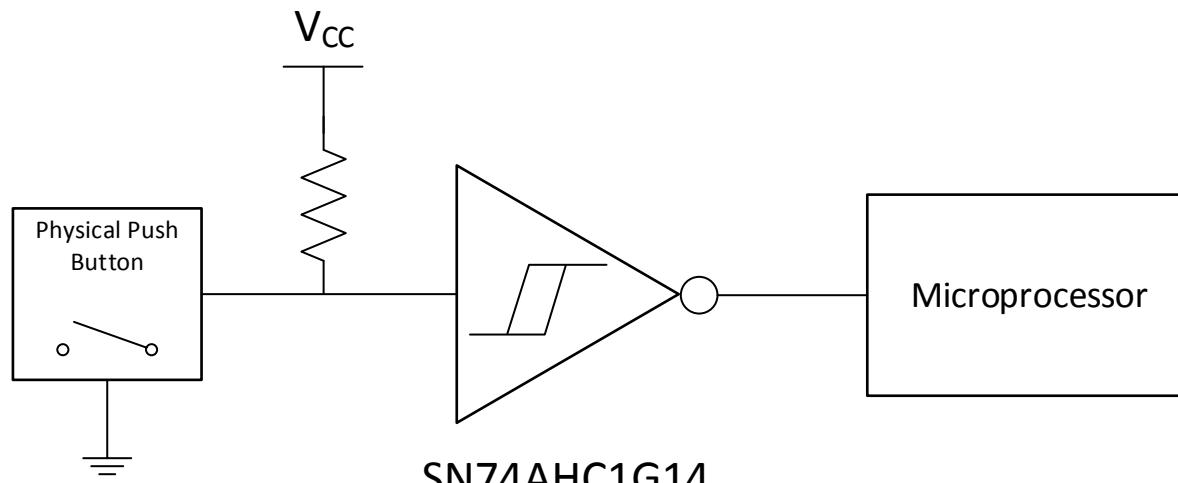


図 8-1. Switch Debouncer

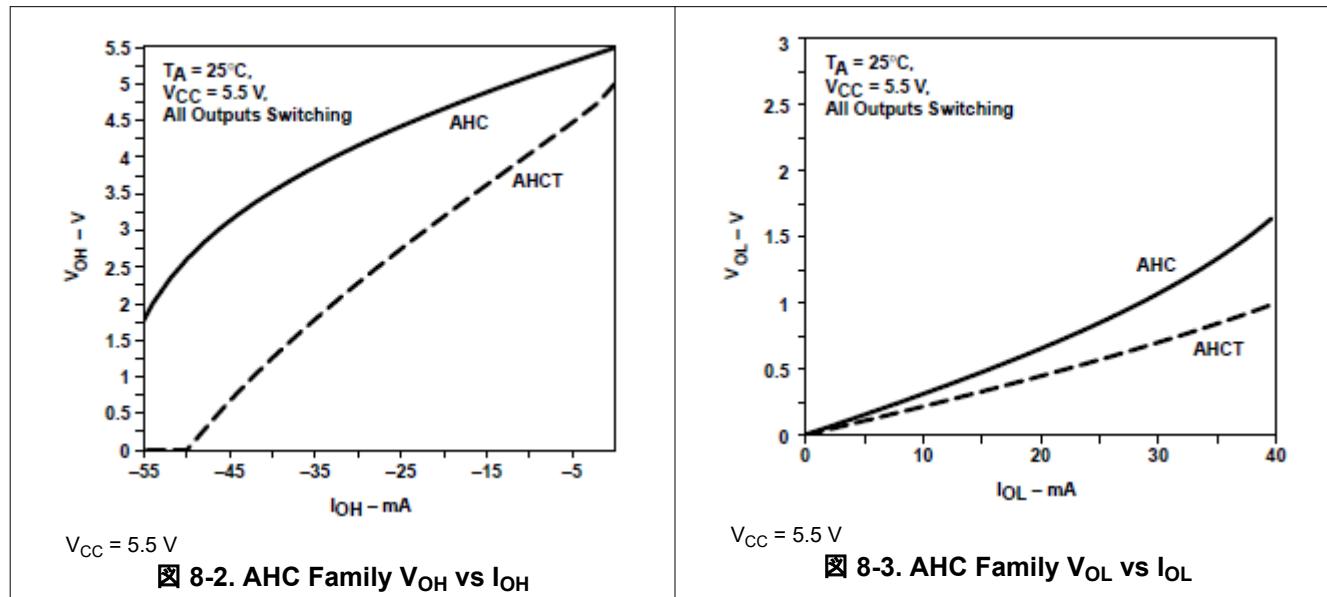
#### 8.2.1 Design Requirements

The SN74AHC1G14 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The SN74AHC1G14 allows for performing logical Boolean functions with hysteresis using digital signals. All input signals must remain as close as possible to either 0 V or VCC for optimal operation.

### 8.2.2 Detailed Design Procedure

1. Recommended input conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta v$  in the [セクション 5.3](#) table.
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [セクション 5.3](#) table.
  - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommended output conditions:
  - Load currents must not exceed  $\pm 50$  mA.
3. Frequency selection criterion:
  - The effects of frequency upon the power consumption of the device can be studied in *CMOS Power Consumption and CPD Calculation, SCAA035*.
  - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the [セクション 8.4.1](#) section.

### 8.2.3 Application Curves



## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [セクション 5.3](#) table.

Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  bypass capacitor is recommended. If multiple pins are labeled  $V_{CC}$ , then a 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu\text{F}$  bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed

capacitance and self-inductance of the trace, which results in the reflection. Not all PCB traces can be straight; therefore some traces must turn corners. **図 8-4** shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

#### 8.4.1.1 Layout Example

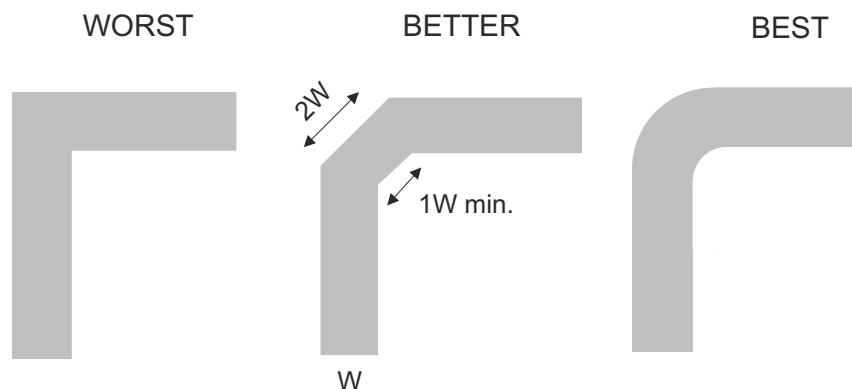


図 8-4. Trace Example

## 9 Device and Documentation Support

### 9.1 Documentation Support (Analog)

#### 9.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)
- *CMOS Power Consumption and CPD Calculation*, [SCAA035](#)
- *Selecting the Right Texas Instruments Signal Switch*, [SZZA030](#)

### 9.2 サポート・リソース

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### 9.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.5 用語集

テキサス・インスツルメンツ用語集 この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision R (October 2023) to Revision S (February 2024)</b>	<b>Page</b>
• Updated thermal values for DBV package from R <sub>θJA</sub> = 225.7 to 278, R <sub>θJC(top)</sub> = 160.3 to 180.5, R <sub>θJB</sub> = 59.4 to 184.4, Ψ <sub>JT</sub> = 41.0 to 115.4, Ψ <sub>JB</sub> = 58.7 to 183.4, R <sub>θJC(bot)</sub> = N/A, all values in °C/W .....	5

<b>Changes from Revision Q (February 2014) to Revision R (October 2023)</b>	<b>Page</b>
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Updated thermal values for DCK package: R <sub>θJA</sub> = 287.6 to 289.2, all values in °C/W .....	5
• Added thermal values for DCK package: R <sub>θJC(top)</sub> = 205.8, R <sub>θJB</sub> = 176.2, Ψ <sub>JT</sub> = 117.6, Ψ <sub>JB</sub> = 175.1, R <sub>θJC(bot)</sub> = N/A, all values in °C/W .....	5

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AHC1G14DBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(38SH, 3C2F, A143, A14G, A14J, A14L, A14S)
SN74AHC1G14DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(38SH, 3C2F, A143, A14G, A14J, A14L, A14S)
SN74AHC1G14DBVRE4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(3C1F, A14G)
<a href="#">SN74AHC1G14DBVRG4</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(3C1F, A14G)
SN74AHC1G14DBVRG4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(3C1F, A14G)
SN74AHC1G14DBVTG4.A	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A14G
<a href="#">SN74AHC1G14DCK3</a>	Obsolete	Production	SC70 (DCK)   5	-	-	Call TI	Call TI	-40 to 125	AFY
<a href="#">SN74AHC1G14DCKR</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1R9, AF3, AFG, AFJ, AFL, AFS)
SN74AHC1G14DCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1R9, AF3, AFG, AFJ, AFL, AFS)
<a href="#">SN74AHC1G14DCKRG4</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF3
SN74AHC1G14DCKRG4.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF3
<a href="#">SN74AHC1G14DCKT</a>	Obsolete	Production	SC70 (DCK)   5	-	-	Call TI	Call TI	-40 to 125	(AF3, AFG, AFJ, AF S)
SN74AHC1G14DCKTE4	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF3
<a href="#">SN74AHC1G14DCKTG4</a>	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF3
SN74AHC1G14DCKTG4.A	Active	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF3
<a href="#">SN74AHC1G14DRLR</a>	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AFS
SN74AHC1G14DRLR.A	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AFS
SN74AHC1G14DRLRG4	Active	Production	SOT-5X3 (DRL)   5	4000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	AFS

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

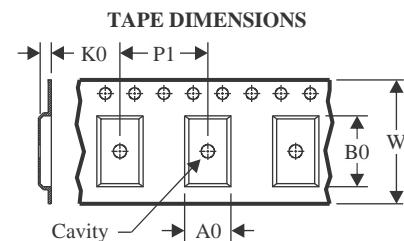
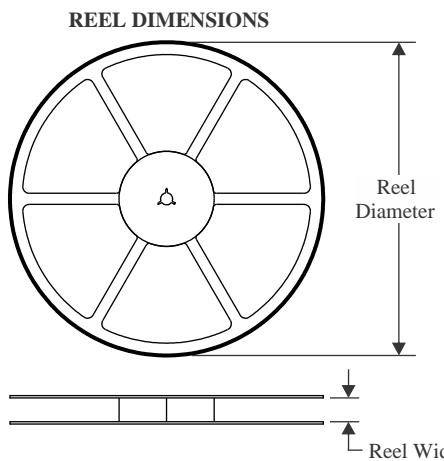
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AHC1G14 :**

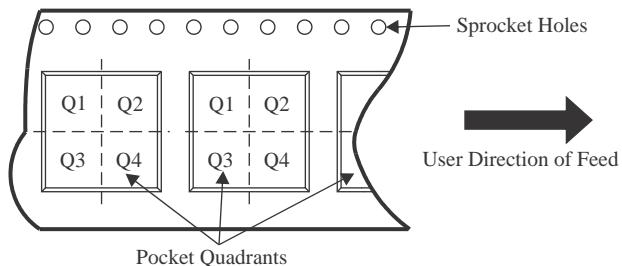
- Automotive : [SN74AHC1G14-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

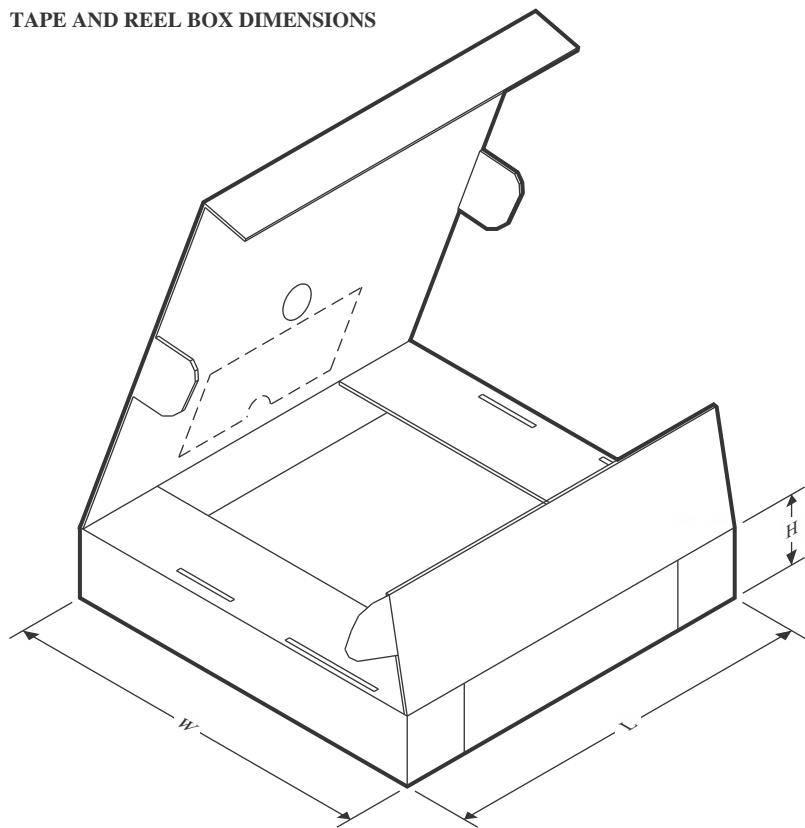
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G14DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G14DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G14DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AHC1G14DCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G14DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G14DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G14DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHC1G14DBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHC1G14DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AHC1G14DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G14DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G14DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0

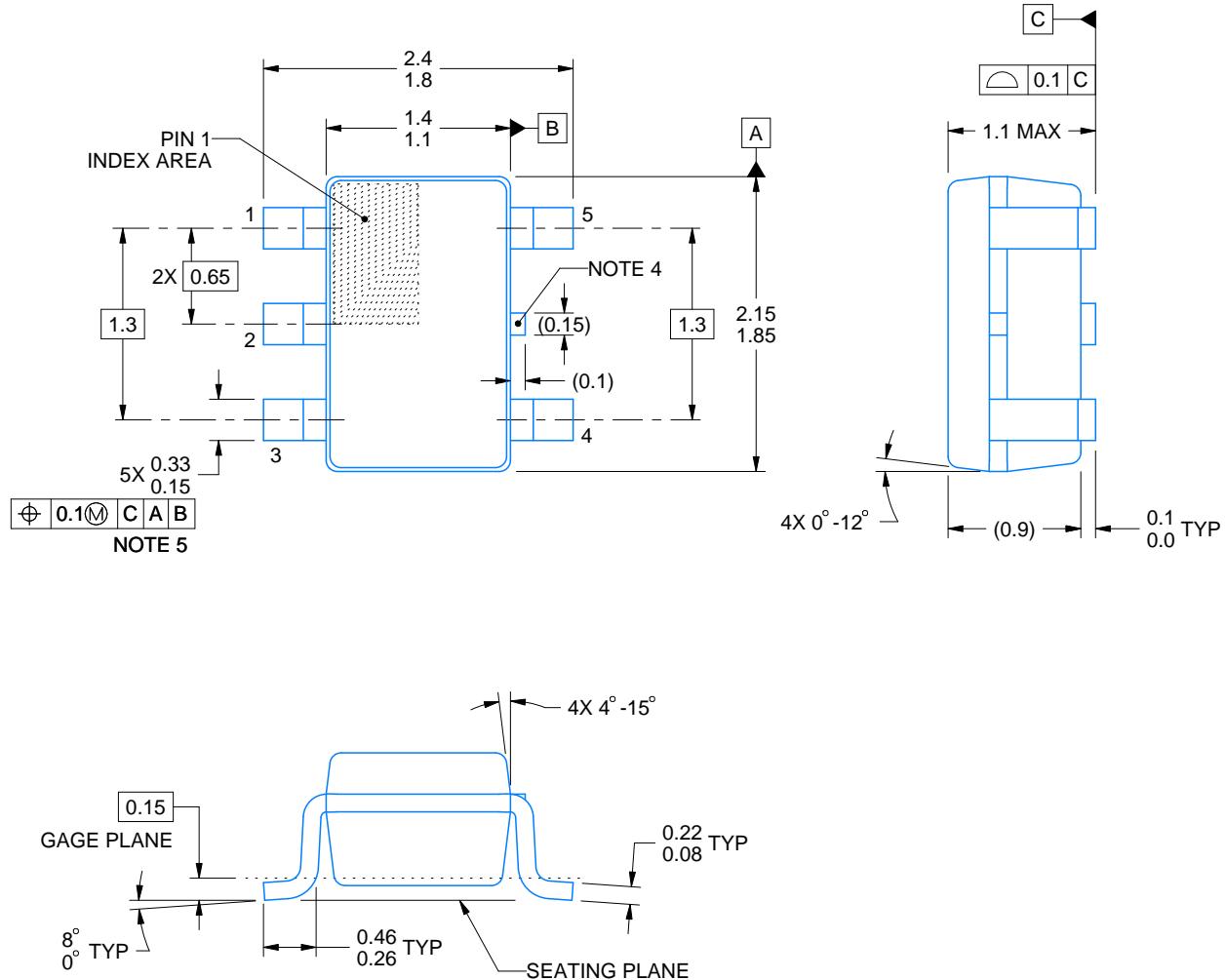
## PACKAGE OUTLINE

**DCK0005A**



## SOT - 1.1 max height

## SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

## NOTES:

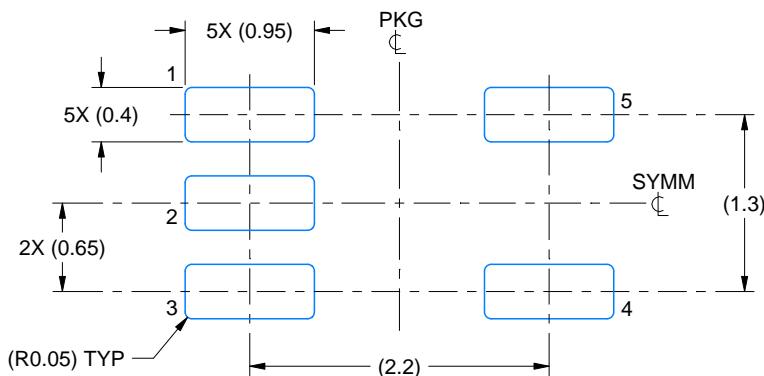
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

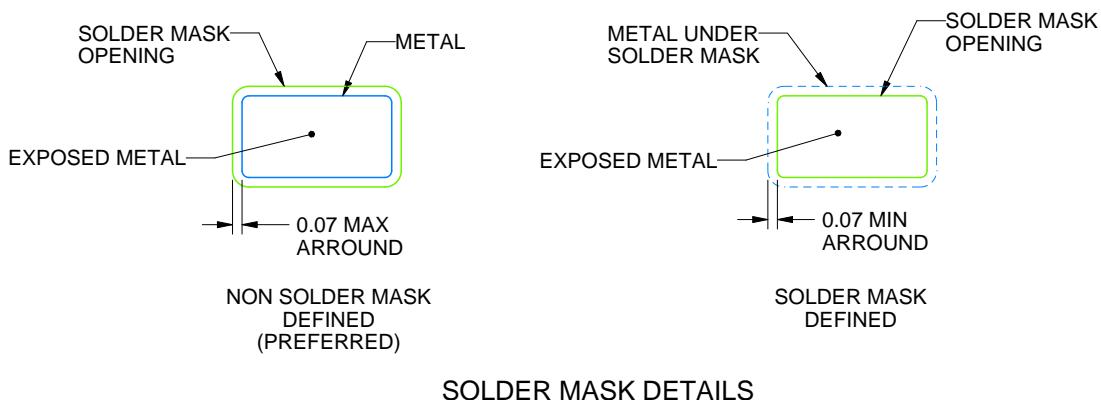
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



4214834/G 11/2024

NOTES: (continued)

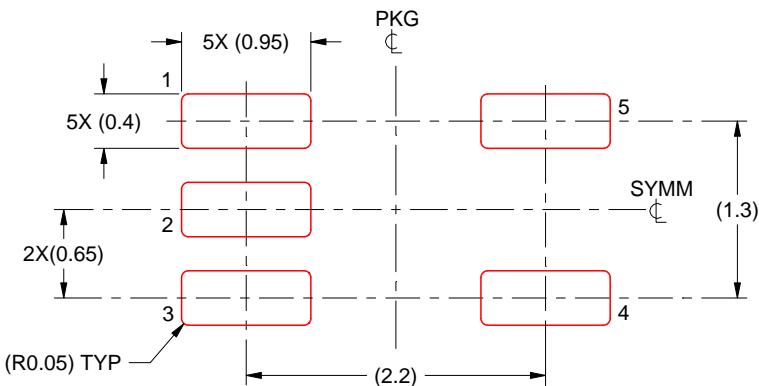
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

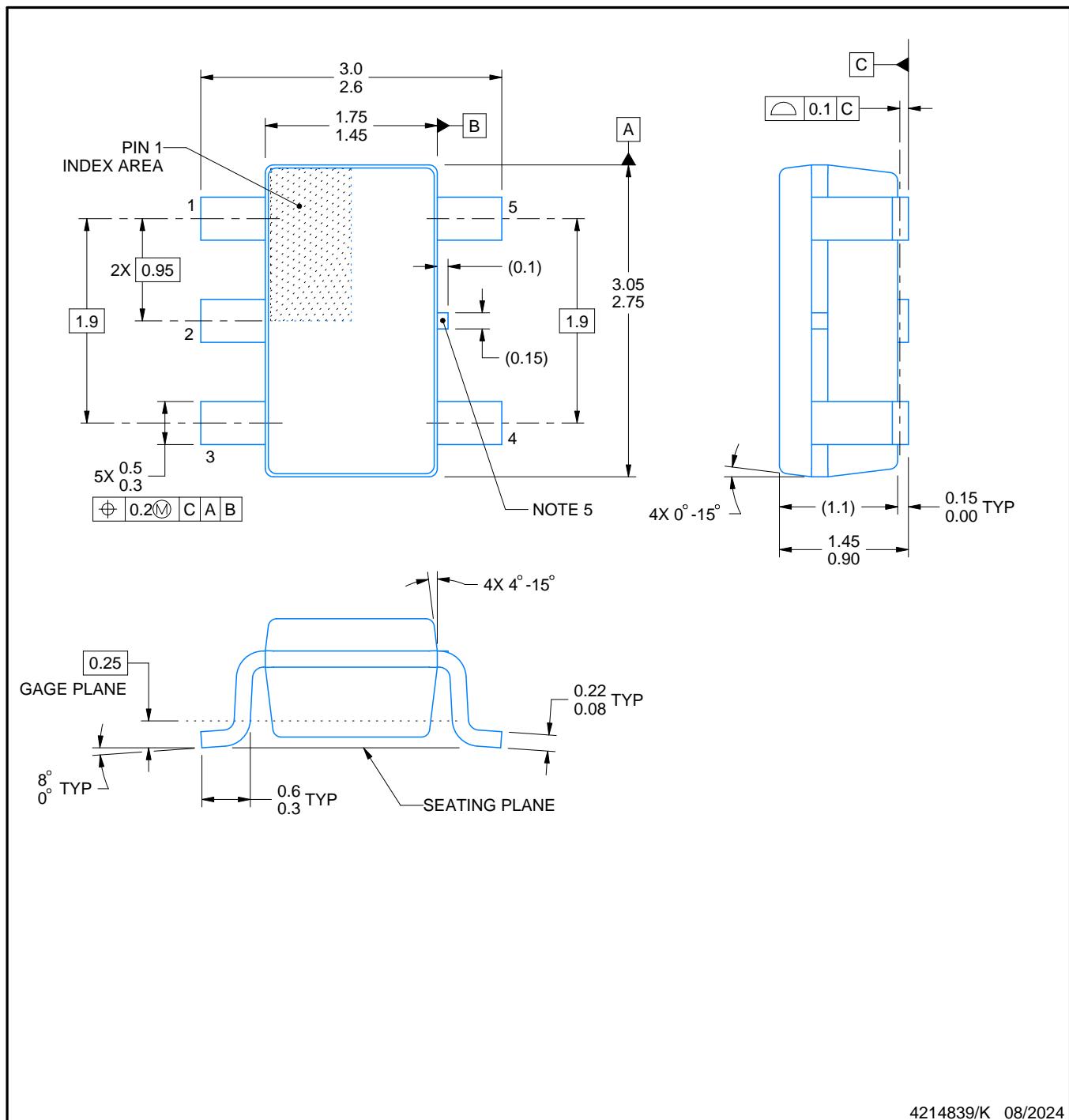
## PACKAGE OUTLINE

**DBV0005A**



## **SOT-23 - 1.45 mm max height**

## SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

## NOTES:

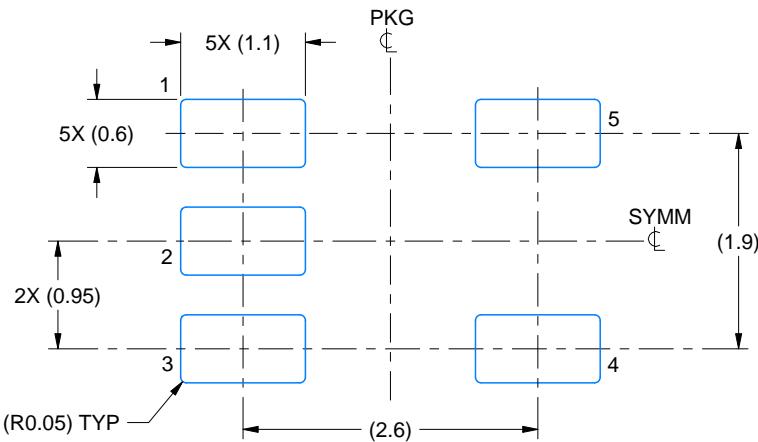
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

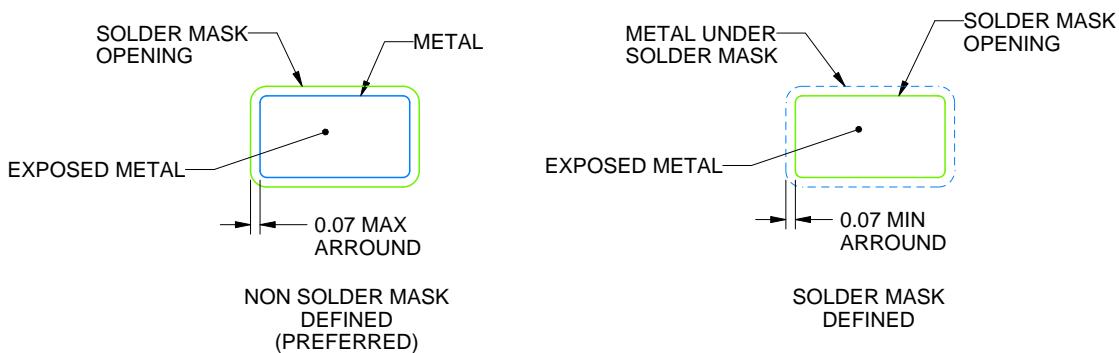
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

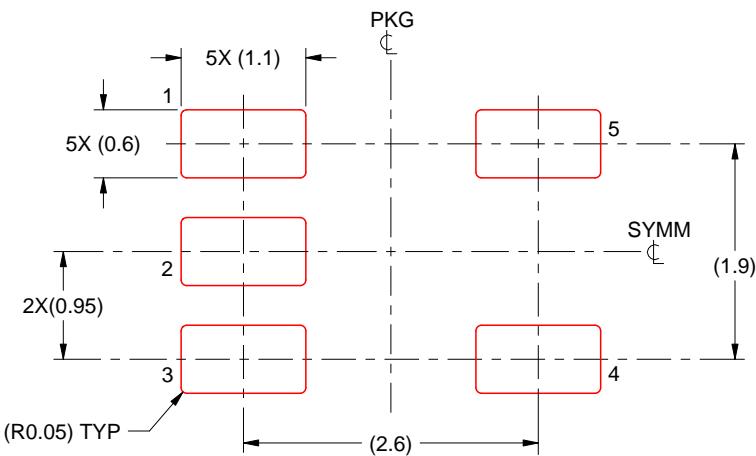
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

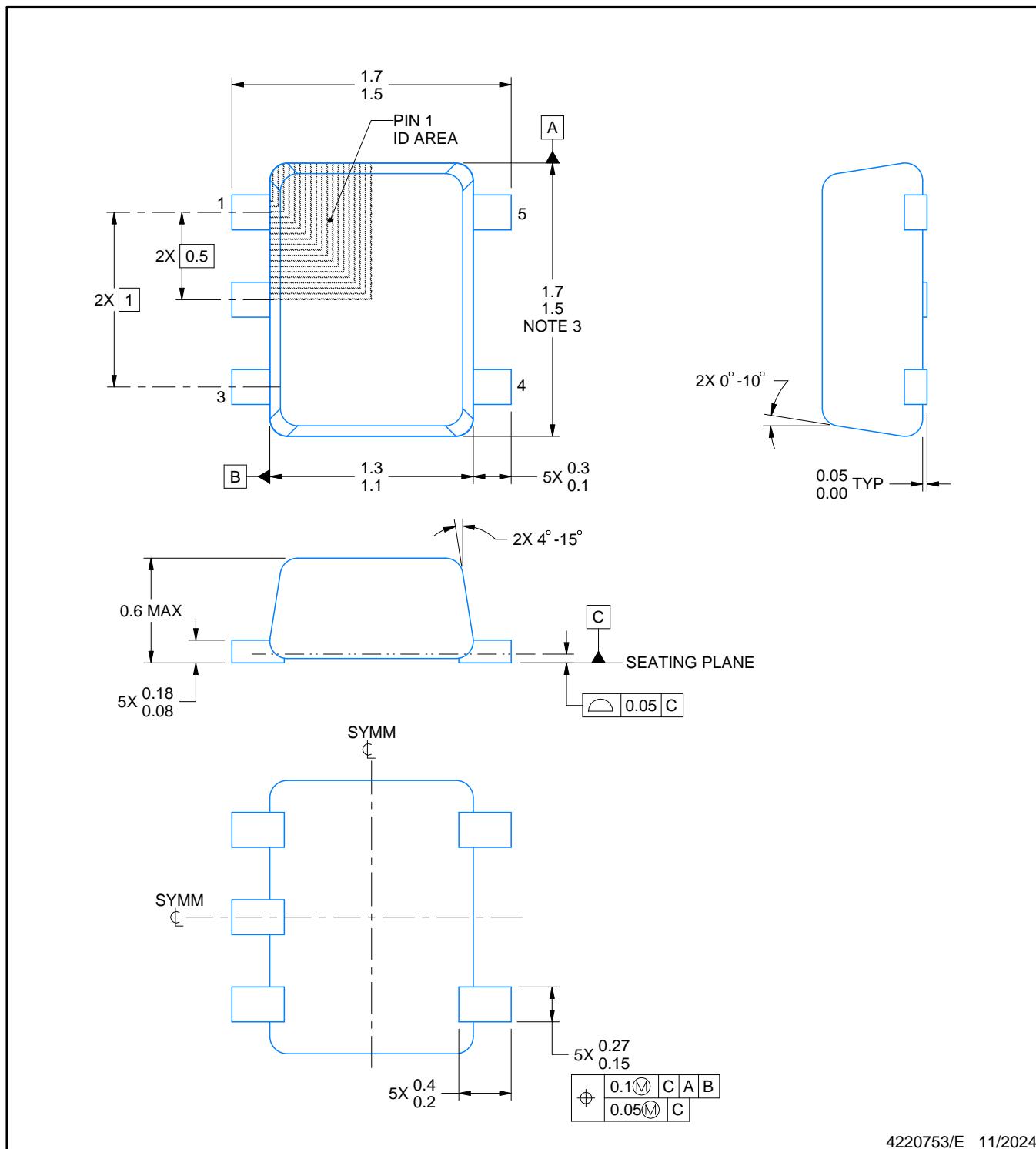
## PACKAGE OUTLINE

**DRL0005A**



## SOT - 0.6 mm max height

## PLASTIC SMALL OUTLINE



4220753/E 11/2024

## NOTES:

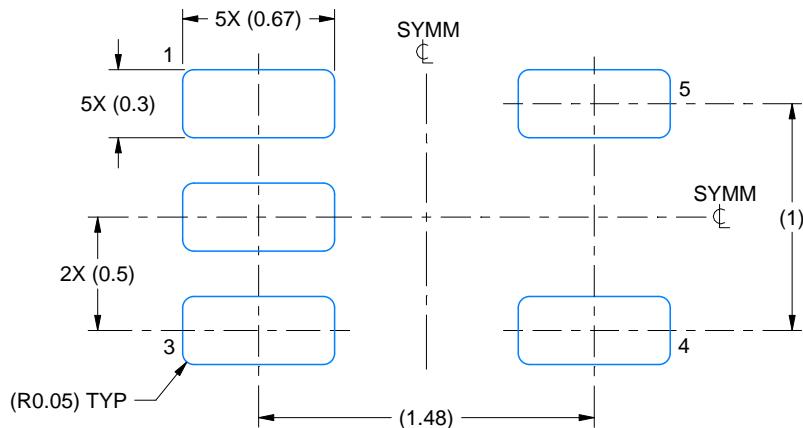
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

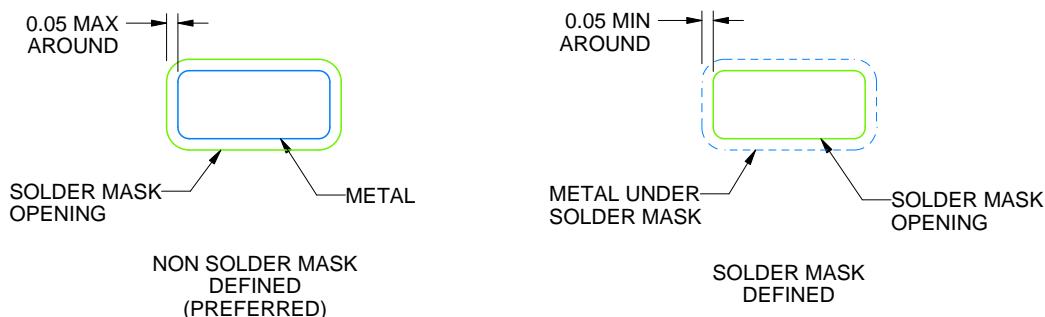
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

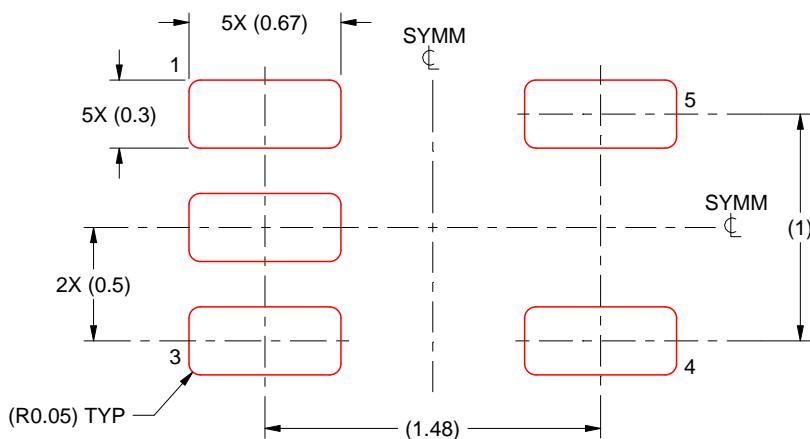
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月