

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- True Logic Outputs
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

### description

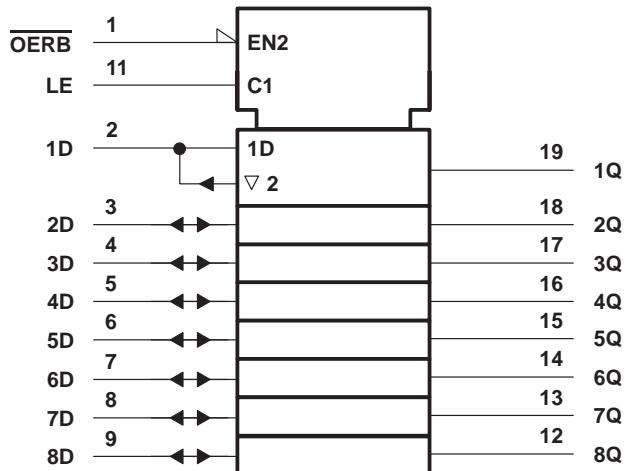
This 8-bit latch is designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus.

The eight latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs.

Read back is provided through the output-enable ( $\overline{OERB}$ ) input. When  $\overline{OERB}$  is taken low, the data present at the output of the data latches is allowed to pass back onto the input data bus. When  $\overline{OERB}$  is taken high, the output of the data latches is isolated from the D inputs.  $\overline{OERB}$  does not affect the internal operation of the latches; however, precautions should be taken not to create a bus conflict.

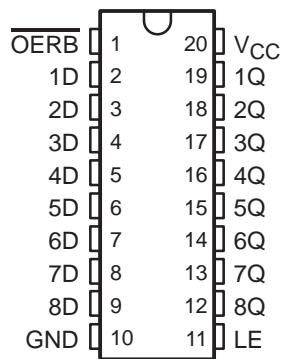
The SN74ALS990 is characterized for operation from 0°C to 70°C.

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### DW OR N PACKAGE (TOP VIEW)

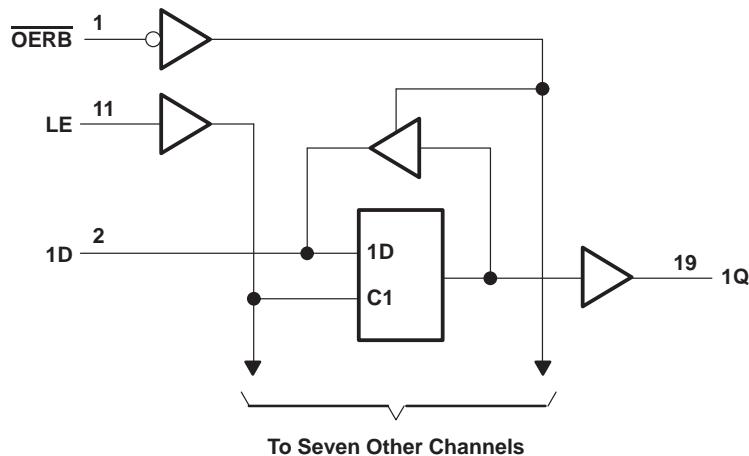


# SN74ALS990

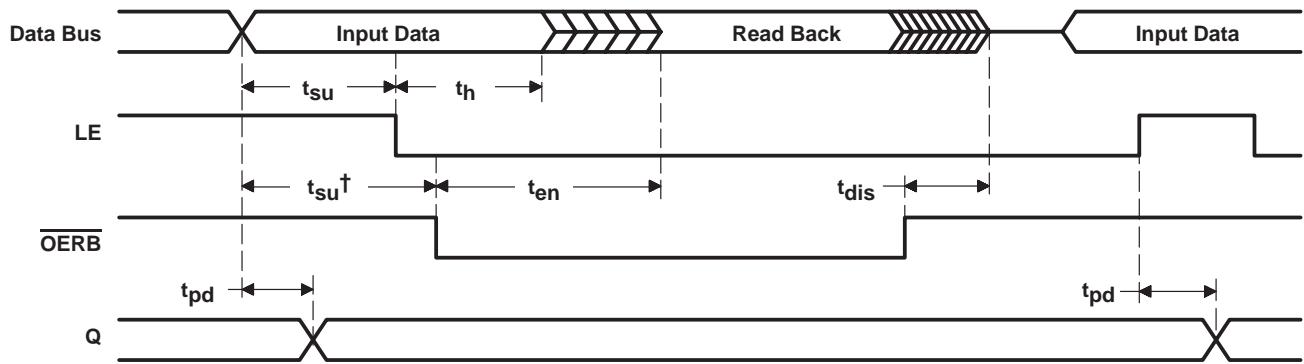
## 8-BIT D-TYPE TRANSPARENT READ-BACK LATCH

SDAS027B – APRIL 1984 – REVISED JANUARY 1995

### logic diagram (positive logic)



### timing diagram



† This setup time ensures that the read-back circuit will not create a conflict on the input data bus.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|                                                   |                |
|---------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ .....                    | 7 V            |
| Input voltage, $V_I$ (OERB and LE) .....          | 7 V            |
| Voltage applied to D inputs .....                 | 5.5 V          |
| Operating free-air temperature range, $T_A$ ..... | 0°C to 70°C    |
| Storage temperature range .....                   | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

|          |                                       | MIN                                      | NOM | MAX  | UNIT |
|----------|---------------------------------------|------------------------------------------|-----|------|------|
| $V_{CC}$ | Supply voltage                        | 4.5                                      | 5   | 5.5  | V    |
| $V_{IH}$ | High-level input voltage              |                                          | 2   |      | V    |
| $V_{IL}$ | Low-level input voltage               |                                          | 0.8 |      | V    |
| $I_{OH}$ | High-level output current             | Q                                        |     | -2.6 | mA   |
|          |                                       | D                                        |     | -0.4 |      |
| $I_{OL}$ | Low-level output current              | Q                                        |     | 24   | mA   |
|          |                                       | D                                        |     | 8    |      |
| $t_W$    | Pulse duration, LE high               |                                          | 10  |      | ns   |
| $t_{SU}$ | Setup time                            | Data before $LE \downarrow$              | 10  |      | ns   |
|          |                                       | Data before $\overline{OERB} \downarrow$ | 10  |      |      |
| $t_h$    | Hold time, data after $LE \downarrow$ |                                          | 5   |      | ns   |
| $T_A$    | Operating free-air temperature        | 0                                        | 70  | 70   | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS                  |                                               | MIN              | TYP†         | MAX  | UNIT    |
|-----------|----------------------------------|-----------------------------------------------|------------------|--------------|------|---------|
| $V_{IK}$  | $V_{CC} = 4.5$ V, $I_I = -18$ mA |                                               |                  |              | -1.2 | V       |
| $V_{OH}$  | All outputs                      | $V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA |                  | $V_{CC} - 2$ |      | V       |
|           | Q                                | $V_{CC} = 4.5$ V, $I_{OH} = -2.6$ mA          | 2.4              | 3.2          |      |         |
| $V_{OL}$  | D                                | $V_{CC} = 4.5$ V                              | $I_{OL} = 4$ mA  | 0.25         | 0.4  | V       |
|           |                                  |                                               | $I_{OL} = 8$ mA  | 0.35         | 0.5  |         |
|           | Q                                | $V_{CC} = 4.5$ V                              | $I_{OL} = 12$ mA | 0.25         | 0.4  |         |
|           |                                  |                                               | $I_{OL} = 24$ mA | 0.35         | 0.5  |         |
| $I_I$     | OERB, LE                         | $V_{CC} = 5.5$ V                              | $V_I = 5.5$ V    |              | 0.1  | mA      |
|           | D inputs                         |                                               | $V_I = 7$ V      |              | 0.1  |         |
| $I_{IH}$  | OERB, LE                         | $V_{CC} = 5.5$ V, $V_I = 2.7$ V               |                  |              | 20   | $\mu$ A |
|           | D inputs‡                        |                                               |                  |              | 20   |         |
| $I_{IL}$  | OERB, LE                         | $V_{CC} = 5.5$ V, $V_I = 0.4$ V               |                  |              | -0.1 | mA      |
|           | D inputs‡                        |                                               |                  |              | -0.1 |         |
| $I_O$ §   |                                  | $V_{CC} = 5.5$ V, $V_O = 2.25$ V              |                  | -30          | -112 | mA      |
| $I_{CC}$  | $V_{CC} = 5.5$ V, OERB high      | Outputs high                                  |                  | 27           | 50   | mA      |
|           |                                  | Outputs low                                   |                  | 40           | 70   |         |

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports (Q<sub>A</sub> thru Q<sub>H</sub>), the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

# SN74ALS990

## 8-BIT D-TYPE TRANSPARENT READ-BACK LATCH

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### switching characteristics (see Figure 1)

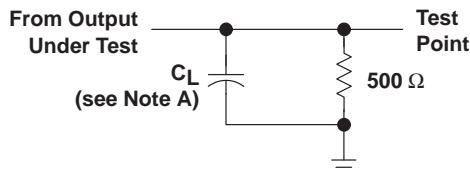
| PARAMETER         | FROM<br>(INPUT)   | TO<br>(OUTPUT) | $V_{CC} = 4.5\text{ V to }5.5\text{ V},$<br>$C_L = 50\text{ pF},$<br>$T_A = \text{MIN to MAX}^\dagger$ |     | UNIT |
|-------------------|-------------------|----------------|--------------------------------------------------------------------------------------------------------|-----|------|
|                   |                   |                | MIN                                                                                                    | MAX |      |
| $t_{PLH}$         | D                 | Q              | 4                                                                                                      | 17  | ns   |
| $t_{PHL}$         |                   |                | 5                                                                                                      | 24  |      |
| $t_{PLH}$         | LE                | Q              | 6                                                                                                      | 26  | ns   |
| $t_{PHL}$         |                   |                | 8                                                                                                      | 26  |      |
| $t_{en}^\ddagger$ | $\overline{OERB}$ | D              | 4                                                                                                      | 21  | ns   |
| $t_{dis}^\$$      | $\overline{OERB}$ | D              | 4                                                                                                      | 19  | ns   |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

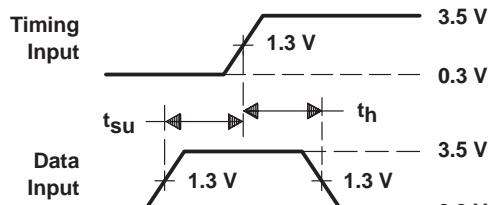
<sup>‡</sup>  $t_{en} = t_{PZH}$  or  $t_{PZL}$

<sup>§</sup>  $t_{dis} = t_{PHZ}$  or  $t_{PLZ}$

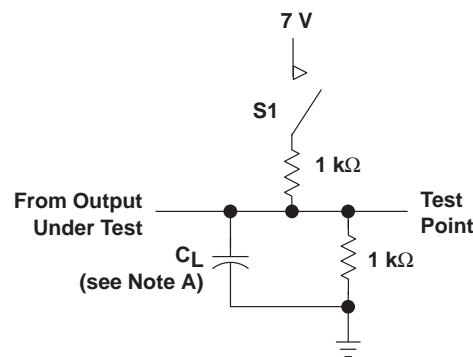
PARAMETER MEASUREMENT INFORMATION



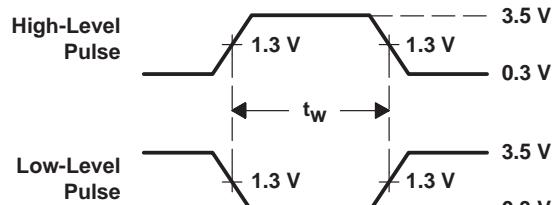
LOAD CIRCUIT FOR Q OUTPUTS



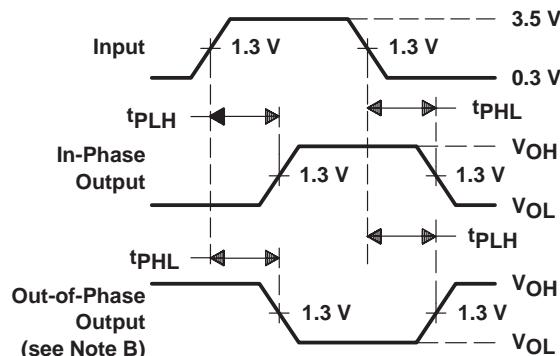
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



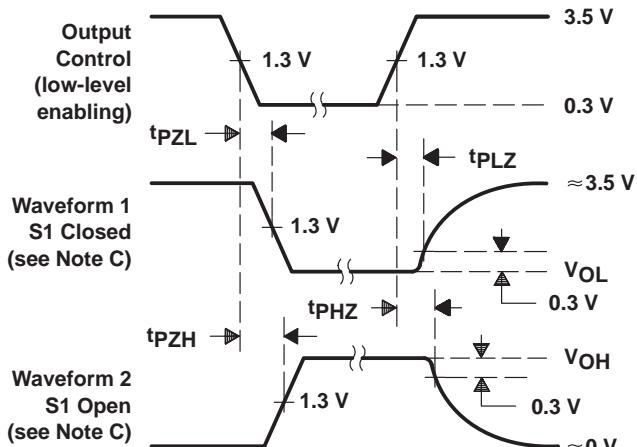
LOAD CIRCUIT FOR D OUTPUTS



VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:

- $C_L$  includes probe and jig capacitance.
- When measuring propagation delay times of 3-state outputs, switch S1 is open.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses have the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $t_r = t_f = 2 \text{ ns}$ , duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74ALS990DW</a>  | Obsolete      | Production           | SOIC (DW)   20 | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | ALS990              |
| <a href="#">SN74ALS990DWR</a> | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | ALS990              |
| SN74ALS990DWR.A               | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | ALS990              |
| <a href="#">SN74ALS990N</a>   | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74ALS990N         |
| SN74ALS990N.A                 | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74ALS990N         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

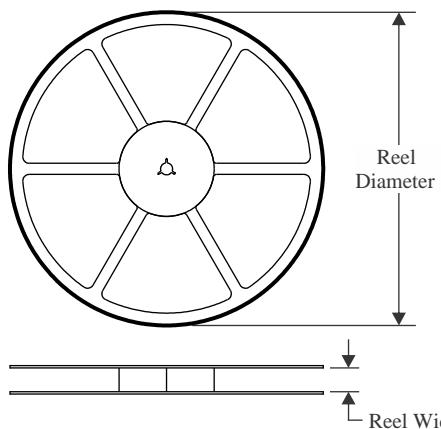
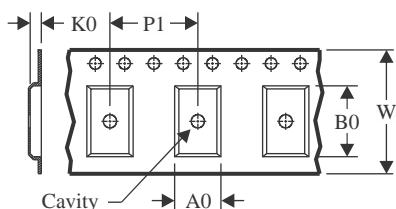
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

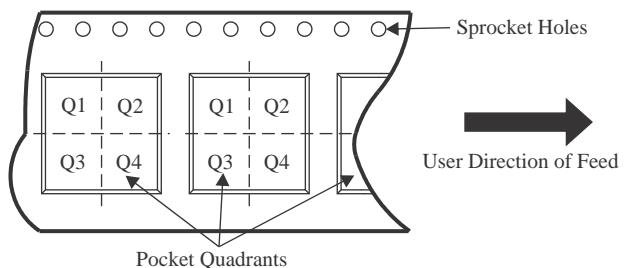
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


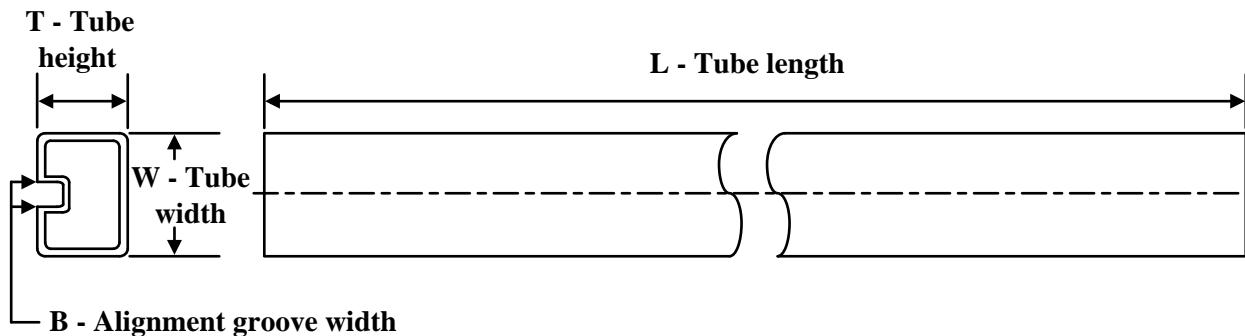
\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS990DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS990DWR | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |

**TUBE**


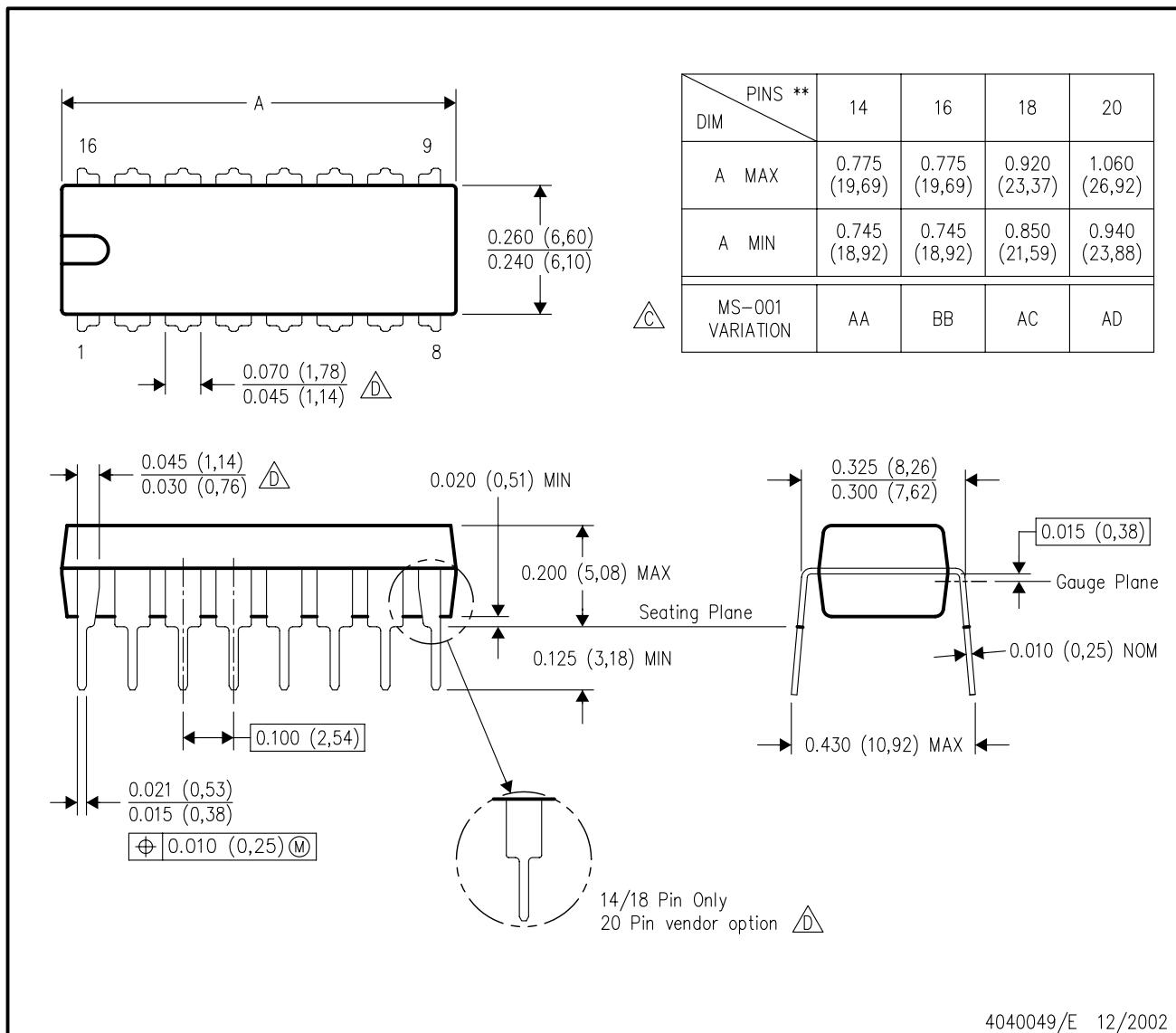
\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T ( $\mu$ m) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------------|--------|
| SN74ALS990N   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230        | 4.32   |
| SN74ALS990N.A | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230        | 4.32   |

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



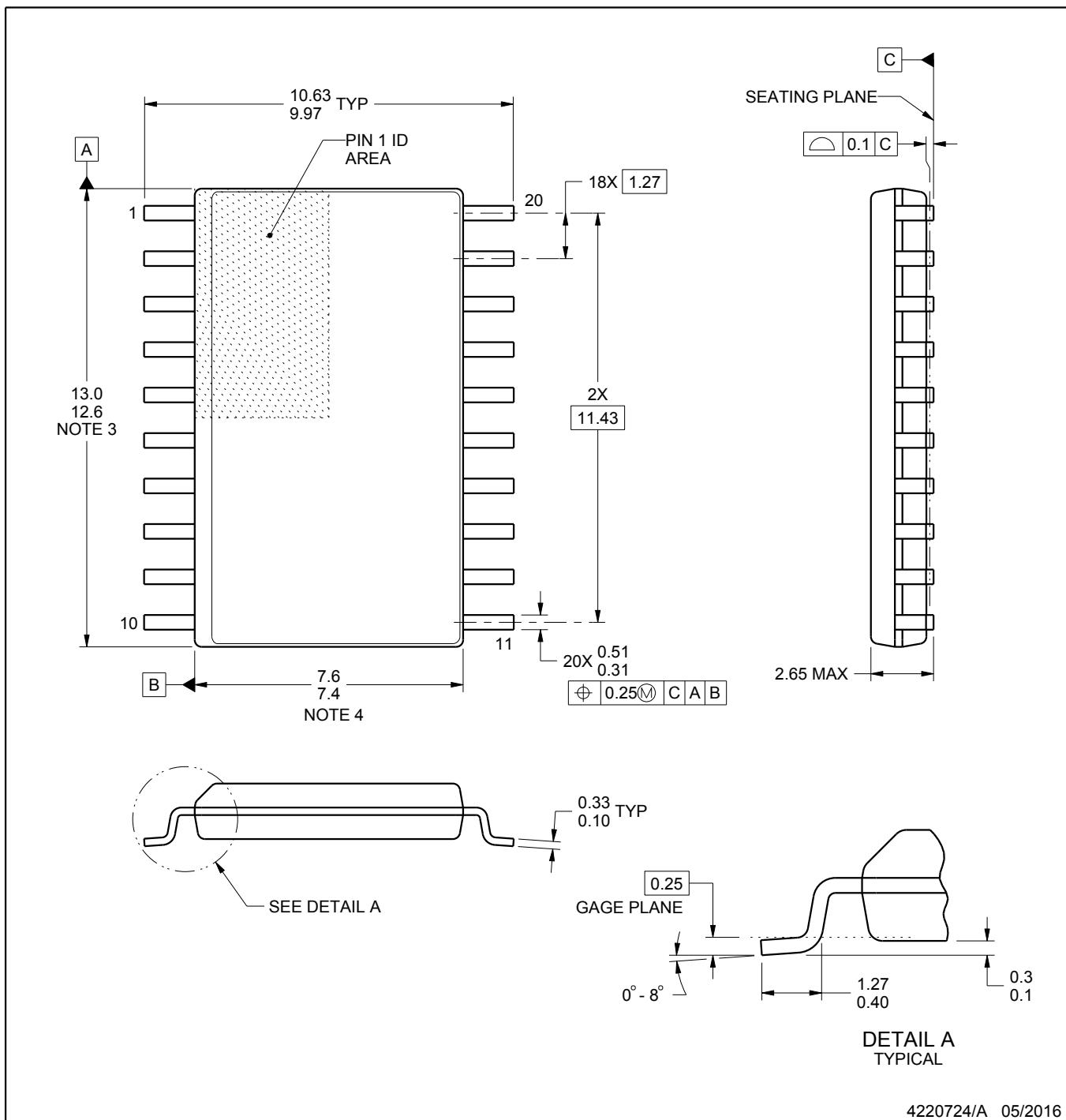
# PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

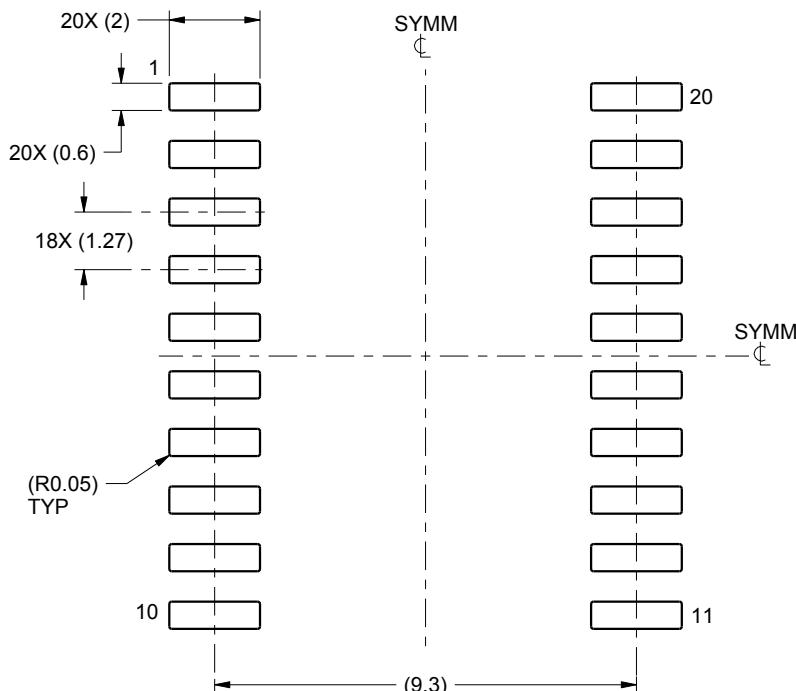
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

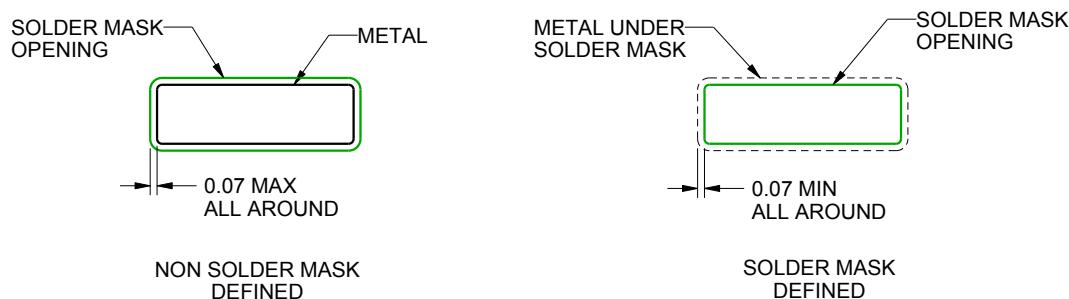
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

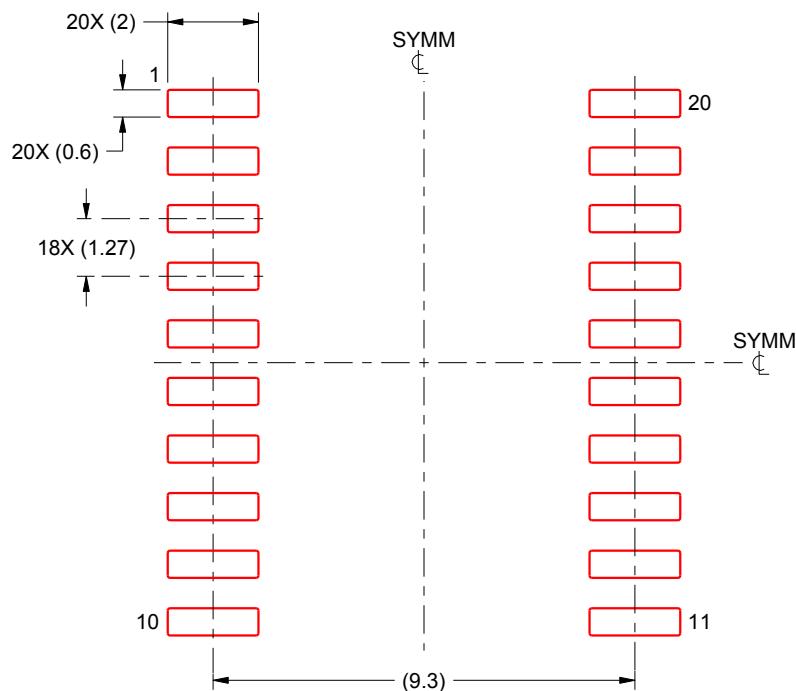
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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