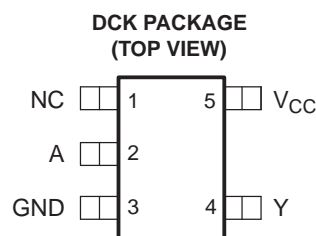


FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Low Static-Power Consumption**
($I_{CC} = 0.9 \mu\text{A Max}$)
- **Low Dynamic-Power Consumption**
($C_{pd} = 4.4 \text{ pF Typ at } 3.3 \text{ V}$)
- **Low Input Capacitance** ($C_i = 1.5 \text{ pF}$)
- **Low Noise – Overshoot and Undershoot**
<10% of V_{CC}
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Includes Schmitt-Trigger Inputs**
- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**
- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**

- $t_{pd} = 5.1 \text{ ns Max at } 3.3 \text{ V}$
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- **ESD Protection Exceeds 5000 V With Human-Body Model**



See mechanical drawings for dimensions.

- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

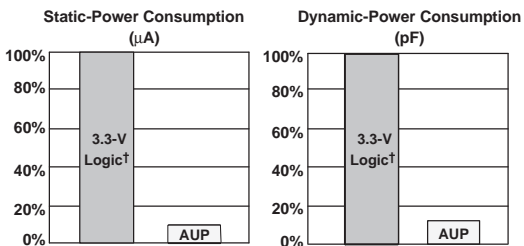
DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figures 1 and 2).



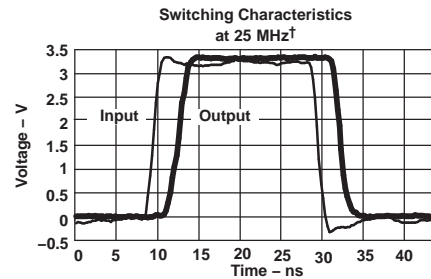
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.



† Single, dual, and triple gates

Figure 1. AUP - The Lowest-Power Family



† AUP1G08 data at $C_L = 15$ pF

Figure 2. Excellent Signal Integrity

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching noise immunity at the input.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

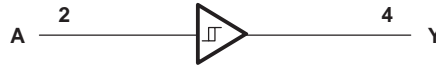
T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
-55°C to 125°C	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G17MDCKREP	BZU

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) DCK: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS A	OUTPUT Y
H	H
L	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range	-0.5	4.6	V	
V _I	Input voltage range ⁽²⁾	-0.5	4.6	V	
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V	
V _O	Output voltage range in the high or low state ⁽²⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0	-50	mA	
I _{OK}	Output clamp current	V _O < 0	-50	mA	
I _O	Continuous output current		±20	mA	
	Continuous current through V _{CC} or GND		±50	mA	
θ _{JA}	Package thermal impedance ⁽³⁾	DCK package	227	°C/W	
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	3.6	V
V _I	Input voltage	0	3.6	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	-20	μA
		V _{CC} = 1.1 V	-1.1	mA
		V _{CC} = 1.4 V	-1.7	
		V _{CC} = 1.65 V	-1.9	
		V _{CC} = 2.3 V	-3.1	
		V _{CC} = 3 V	-4	
I _{OL}	Low-level output current	V _{CC} = 0.8 V	20	μA
		V _{CC} = 1.1 V	1.1	mA
		V _{CC} = 1.4 V	1.7	
		V _{CC} = 1.65 V	1.9	
		V _{CC} = 2.3 V	3.1	
		V _{CC} = 3 V	4	
T _A	Operating free-air temperature	-55	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74AUP1G17-EP LOW-POWER SINGLE SCHMITT-TRIGGER BUFFER

SCES684–JANUARY 2007

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = -55°C to 125°C			UNIT
			MIN	TYP	MAX	
V _{T+} Positive-going input threshold voltage		0.8 V	0.3		0.6	V
		1.1 V	0.53		0.9	
		1.4 V	0.74		1.11	
		1.65 V	0.91		1.29	
		2.3 V	1.37		1.77	
		3 V	1.88		2.29	
V _{T-} Negative-going input threshold voltage		0.8 V	0.1		0.6	V
		1.1 V	0.26		0.65	
		1.4 V	0.39		0.75	
		1.65 V	0.47		0.84	
		2.3 V	0.69		1.04	
		3 V	0.88		1.24	
ΔV _T Hysteresis (V _{T+} - V _{T-})		0.8 V	0.07		0.5	V
		1.1 V	0.08		0.46	
		1.4 V	0.18		0.56	
		1.65 V	0.27		0.66	
		2.3 V	0.53		0.92	
		3 V	0.79		1.31	
V _{OH}	I _{OH} = -20 μA I _{OH} = -1.1 mA I _{OH} = -1.7 mA I _{OH} = -1.9 mA I _{OH} = -2.3 mA I _{OH} = -3.1 mA I _{OH} = -2.7 mA I _{OH} = -4 mA	0.8 V to 3.6 V	V _{CC} - 0.2			V
		1.1 V	0.7 × V _{CC}			
		1.4 V	1.03			
		1.65 V	1.3			
		2.3 V	1.97			
		2.3 V	1.85			
		3 V	2.67			
		3 V	2.55			
V _{OL}	I _{OL} = 20 μA I _{OL} = 1.1 mA I _{OL} = 1.7 mA I _{OL} = 1.9 mA I _{OL} = 2.3 mA I _{OL} = 3.1 mA I _{OL} = 2.7 mA I _{OL} = 4 mA	0.8 V to 3.6 V			0.1	V
		1.1 V			0.3 × V _{CC}	
		1.4 V			0.37	
		1.65 V			0.35	
		2.3 V			0.33	
		2.3 V			0.45	
		3 V			0.33	
		3 V			0.475	
I _I	All inputs V _I = GND to 3.6 V	0 V to 3.6 V			0.5	μA
I _{off}	V _I or V _O = 0 V to 3.6 V	0 V			5.0	μA
ΔI _{off}	V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V			5.0	μA
I _{CC}	V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V			0.9	μA
ΔI _{CC}	V _I = V _{CC} - 0.6 V, I _O = 0	3.3 V			50	μA
C _i	V _I = V _{CC} or GND	0 V		1.5		pF
		3.6 V		1.5		
C _o	V _O = GND	0 V		2.5		pF

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

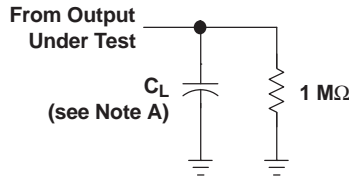
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = -55^\circ\text{C}$ to 125°C		UNIT
				MIN	MAX	
t_{pd}	A	Y	$1.2\text{ V} \pm 0.1\text{ V}$	7.5	28	ns
			$1.5\text{ V} \pm 0.1\text{ V}$	5.6	20	
			$1.8\text{ V} \pm 0.15\text{ V}$	4.8	17	
			$2.5\text{ V} \pm 0.2\text{ V}$	4	13	
			$3.3\text{ V} \pm 0.3\text{ V}$	3.6	11	

Operating Characteristics

$T_A = 25^\circ\text{C}$

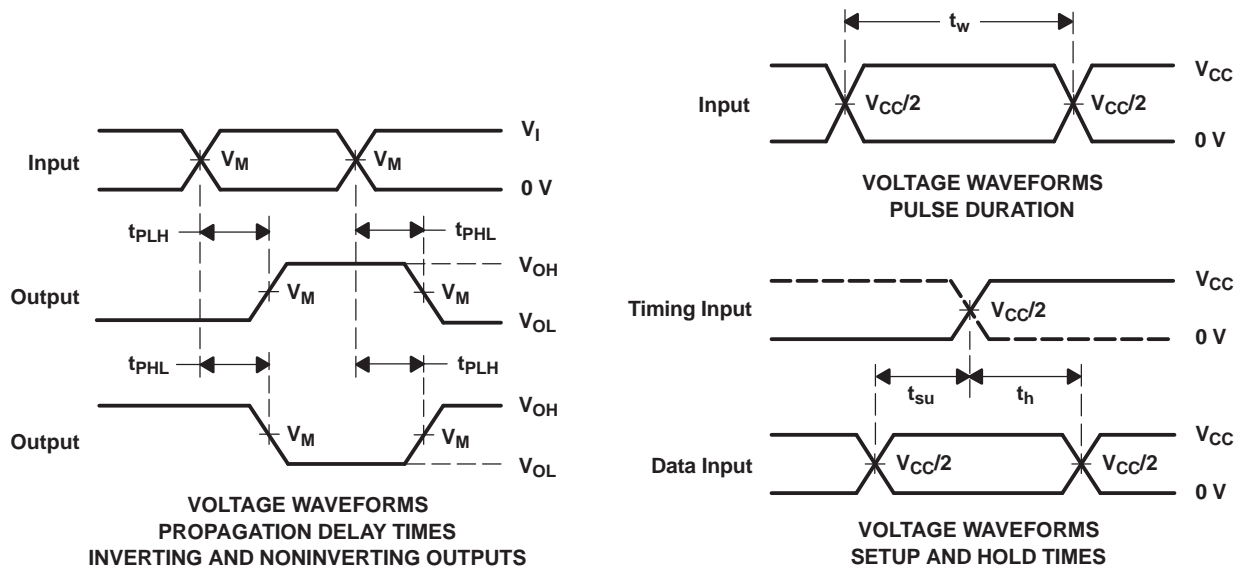
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	0.8 V	4	pF
		$1.2 \pm 0.1\text{ V}$	4	
		$1.5 \pm 0.1\text{ V}$	4	
		$1.8\text{ V} \pm 0.15\text{ V}$	4	
		$2.5\text{ V} \pm 0.2\text{ V}$	4.2	
		$3.3\text{ V} \pm 0.3\text{ V}$	4.4	

PARAMETER MEASUREMENT INFORMATION
 (Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

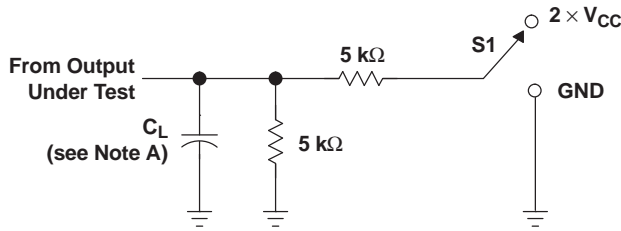
	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, for propagation delays $t_r/t_f = 3\text{ ns}$, for setup and hold times and pulse width $t_r/t_f = 1.2\text{ ns}$.
 - C. The outputs are measured one at a time, with one transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

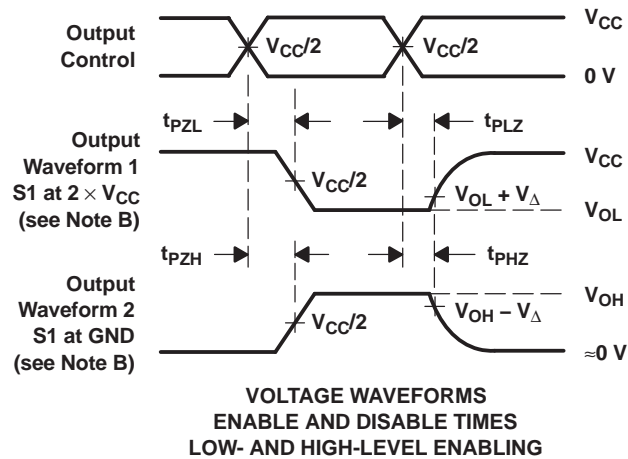
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP1G17MDCKREP	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BZU
V62/07623-01XE	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BZU

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AUP1G17-EP :

- Catalog : [SN74AUP1G17](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G17MDCKREP	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G17MDCKREP	SC70	DCK	5	3000	202.0	201.0	28.0

DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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