SN74AVC2T45-Q1 Automotive Dual-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-state Outputs

1 Features

- Qualified for automotive applications
- Control inputs V_{IH}/V_{IL} levels are referenced to V_{CCA} voltage
- Fully configurable dual-rail design allows each port to operate over the full 1.2V to 3.6V power-supply range
- Operating temperature from -40°C to 105°C
- I/Os are 4.6V tolerant
- I_{off} supports partial-power-down mode operation
- Maximum data rates
  - 500Mbps (1.8V to 3.3V translation)
  - 320Mbps (< 1.8V to 3.3V translation)
  - 320Mbps (translate to 2.5V or 1.8V)
  - 280Mbps (translate to 1.5V)
  - 240Mbps (translate to 1.2V)
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 8000V human-body model (A114-A)
  - 200V machine model (A115-A)
  - 1000V charged-device model (C101)

2 Applications

- Smartphones
- Servers
- Desktop PCs and notebooks
- Other portable devices

3 Description

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2V to 3.6V. This allows for universal low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The SN74AVC2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74AVC2T45 is designed so that the DIR input is powered by V_{CCA}.

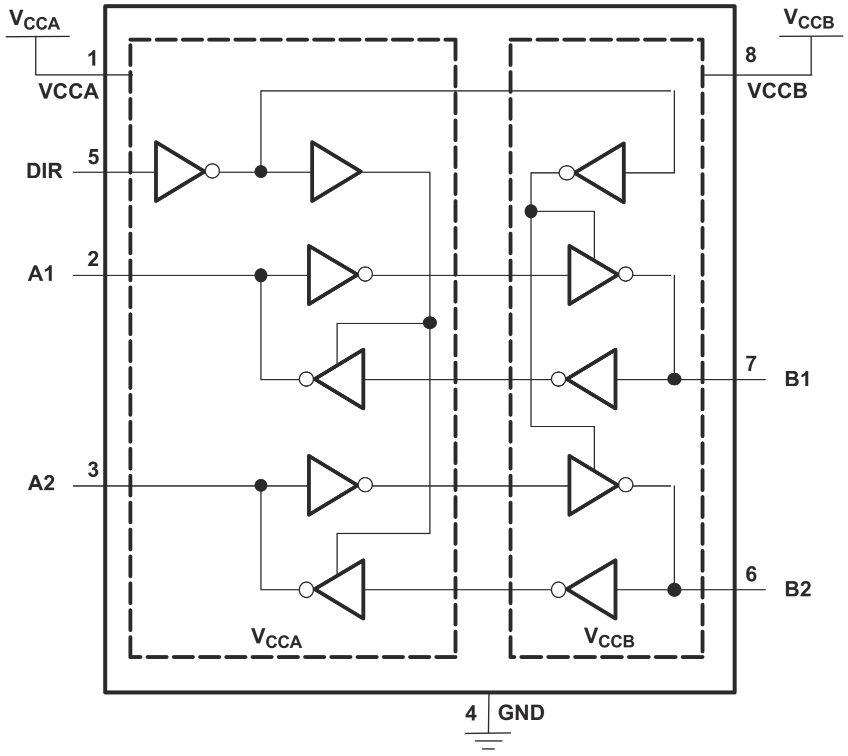
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

The V_{CC} isolation feature makes sure that if either V_{CC} input is at GND, both ports are in the high-impedance state.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74AVC2T45DCU	DCU (VSSOP, 8)	2mm × 3.1mm
SN74AVC2T45DTT	DTT (SON, 8)	1.95mm × 1.00mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

Figure 4-1. DCU (8-Pin VSSOP) and DTT (8-Pin SON) Package (Top View)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VCCA	1	—	Supply Voltage A
VCCB	8	—	Supply Voltage B
GND	4	—	Ground
A1	2	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA}.
A2	3	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA}.
B1	7	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB}.
B2	6	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB}.
DIR	5	I	Direction Pin, Connect to GND or to VCCA

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range (2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state (2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state (2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DCU package		227	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current ratings are observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model (MM), Per JEDEC specification JESD22-A115-A	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

See (1) (2) (3) (4) (5)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs (4)	1.2V to 1.95V		V_{CCI} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		
V_{IL}	Low-level input voltage	Data inputs (4)	1.2V to 1.95V			V_{CCI} × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 3.6V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(5)	1.2V to 1.95V		V_{CCA} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(5)	1.2V to 1.95V			V_{CCA} × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 3.6V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2V		–3	mA
				1.4V to 1.6V		–6	
				1.65V to 1.95V		–8	
				2.3V to 2.7V		–9	
				3V to 3.6V		–12	
I_{OL}	Low-level output current			1.2V		3	mA
				1.4V to 1.6V		6	
				1.65V to 1.95V		8	
				2.3V to 2.7V		9	
				3V to 3.6V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	105	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V.

5.4 Thermal Information

THERMAL METRIC(1)		SN74AVC2T45-Q1		UNIT
		DCU (VSSOP)	DTT (QFN)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	246.9	216.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.2	149.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	158.4	114.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	34.1	21.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	157.5	114.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 105°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100µA	$V_I = V_{IH}$	1.2V to 3.6V	1.2V to 3.6V				V_{CCO} – 0.2V		V
		I_{OH} = –3mA		1.2V	1.2V		0.95				
		I_{OH} = –6mA		1.4V	1.4V				1.05		
		I_{OH} = –8mA		1.65V	1.65V				1.2		
		I_{OH} = –9mA		2.3V	2.3V				1.75		
		I_{OH} = –12mA		3V	3V				2.3		
V_{OL}		I_{OL} = 100µA	$V_I = V_{IL}$	1.2V to 3.6V	1.2V to 3.6V					0.2	V
		I_{OL} = 3mA		1.2V	1.2V		0.25				
		I_{OL} = 6mA		1.4V	1.4V					0.35	
		I_{OL} = 8mA		1.65V	1.65V					0.45	
		I_{OL} = 9mA		2.3V	2.3V					0.55	
		I_{OL} = 12mA		3V	3V					0.7	
I_I	DIR	$V_I = V_{CCA}$ or GND		1.2V to 3.6V	1.2V to 3.6V		±0.025	±0.25		±1	µA
I_{off}	A port	V_I or V_O = 0 to 3.6V		0V	0 to 3.6V		±0.1	±1		±5	µA
	B port			0 to 3.6V	0V		±0.1	±1		±5	
I_{OZ}	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND		0V	3.6V		±0.5	±2.5		±5	µA
	A port			3.6V	0V		±0.5	±2.5		±5	
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V					10	µA
				0V	3.6V					–2	
				3.6V	0V					10	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V					10	µA
				0V	3.6V					10	
				3.6V	0V					–2	
$I_{CCA} + I_{CCB}$ (see Table 8-3)		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V					20	µA
C_I	Control inputs	V_I = 3.3V or GND		3.3V	3.3V		2.5				pF
C_{io}	A or B port	V_O = 3.3V or GND		3.3V	3.3V		6				pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

5.6 Switching Characteristics: VCCA = 1.2V

over recommended operating free-air temperature range, V_{CCA} = 1.2V (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2V	V_{CCB} = 1.5V	V_{CCB} = 1.8V	V_{CCB} = 2.5V	V_{CCB} = 3.3V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.1	2.6	2.4	2.2	2.2	ns
t_{PHL}			3.1	2.6	2.4	2.2	2.2	
t_{PLH}	B	A	3.4	3.1	3	2.9	2.9	ns
t_{PHL}			3.4	3.1	3	2.9	2.9	
t_{PHZ}	DIR	A	5.2	5.2	5.1	5	4.8	ns
t_{PLZ}			5.2	5.2	5.1	5	4.8	
t_{PHZ}	DIR	B	5	4	3.8	2.8	3.2	ns
t_{PLZ}			5	4	3.8	2.8	3.2	
t_{PZH} (1)	DIR	A	8.4	7.1	6.8	5.7	6.1	ns
t_{PZL} (1)			8.4	7.1	6.8	5.7	6.1	
t_{PZH} (1)	DIR	B	8.3	7.8	7.5	7.2	7	ns
t_{PZL} (1)			8.3	7.8	7.5	7.2	7	

(1) The enable time is a calculated value, derived using the formula shown in the Section 8.2.2.2.1 section.

5.7 Switching Characteristics: V_{CCA} = 1.5V

over recommended operating free-air temperature range, V_{CCA} = 1.5V ± 0.1V (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2V	V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.8	0.7	5.6	0.5	4.8	0.4	3.9	0.3	3.7	ns
t_{PHL}			2.8	0.7	5.6	0.5	4.8	0.4	3.9	0.3	3.7	
t_{PLH}	B	A	2.7	0.8	5.6	0.7	5.4	0.6	5.1	0.5	4.9	ns
t_{PHL}			2.7	0.8	5.6	0.7	5.4	0.6	5.1	0.5	4.9	
t_{PHZ}	DIR	A	3.9	1.3	8.7	1.3	8	1.1	7.9	1.4	7.8	ns
t_{PLZ}			3.9	1.3	8.7	1.3	8	1.1	7.9	1.4	7.8	
t_{PHZ}	DIR	B	4.7	1.1	7.2	1.4	7.1	1.2	7.1	1.7	7.3	ns
t_{PLZ}			4.7	1.1	7.2	1.4	7.1	1.2	7.1	1.7	7.3	
t_{PZH} (1)	DIR	A	7.4		12.6		12.3		12		12	ns
t_{PZL} (1)			7.4		12.6		12.3		12		12	
t_{PZH} (1)	DIR	B	6.7		14.1		12.6		11.6		11.3	ns
t_{PZL} (1)			6.7		14.1		12.6		11.6		11.3	

(1) The enable time is a calculated value, derived using the formula shown in the Section 8.2.2.2.1 section.

5.8 Switching Characteristics: V_{CCA} = 1.8V

over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2V	V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.7	0.5	5.4	0.4	4.5	0.2	3.6	0.2	3.3	ns
t_{PHL}			2.7	0.5	5.4	0.4	4.5	0.2	3.6	0.2	3.3	
t_{PLH}	B	A	2.4	0.7	4.9	0.5	4.6	0.5	4.2	0.4	4	ns
t_{PHL}			2.4	0.7	4.9	0.5	4.6	0.5	4.2	0.4	4	
t_{PHZ}	DIR	A	3.7	1.3	8.3	0.7	7.1	1.4	5.5	1.1	5.4	ns
t_{PLZ}			3.7	1.3	8.3	0.7	7.1	1.4	5.5	1.1	5.4	
t_{PHZ}	DIR	B	4.4	1.3	6	1.3	6.1	0.8	5.9	1.5	6.1	ns
t_{PLZ}			4.4	1.3	6	1.3	6.1	0.8	5.9	1.5	6.1	
t_{PZH} (1)	DIR	A	6.8		10.7		10.5		9.9		9.9	ns
t_{PZL} (1)			6.8		10.7		10.5		9.9		9.9	
t_{PZH} (1)	DIR	B	6.4		13.5		11.4		8.9		8.5	ns
t_{PZL} (1)			6.4		13.5		11.4		8.9		8.5	

(1) The enable time is a calculated value, derived using the formula shown in the Section 8.2.2.2.1 section.

5.9 Switching Characteristics: V_{CCA} = 2.5V

over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2V (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2V	V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.6	0.4	5.1	0.2	4.2	0.2	3.2	0.2	2.8	ns
t_{PHL}			2.6	0.4	5.1	0.2	4.2	0.2	3.2	0.2	2.8	
t_{PLH}	B	A	2.1	0.6	4	0.5	3.6	0.4	3.2	0.3	3	ns
t_{PHL}			2.1	0.6	4	0.5	3.6	0.4	3.2	0.3	3	
t_{PHZ}	DIR	A	2.4	0.7	8.1	0.8	6.6	0.8	5.2	0.5	4.5	ns
t_{PLZ}			2.4	0.7	8.1	0.8	6.6	0.8	5.2	0.5	4.5	
t_{PHZ}	DIR	B	3.8	1	4.5	0.6	4.5	0.5	4.4	1.1	4.3	ns
t_{PLZ}			3.8	1	4.5	0.6	4.5	0.5	4.4	1.1	4.3	
t_{PZH} (1)	DIR	A	5.9		8.7		7.9		7.4		7.1	ns
t_{PZL} (1)			5.9		8.7		7.9		7.4		7.1	
t_{PZH} (1)	DIR	B	5		13		10.6		8.2		7.1	ns
t_{PZL} (1)			5		13		10.6		8.2		7.1	

(1) The enable time is a calculated value, derived using the formula shown in the Section 8.2.2.2.1 section.

5.10 Switching Characteristics: V_{CCA} = 3.3V

over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3V (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2V	V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.5	0.3	4.9	0.2	4	0.2	3	0.2	2.6	ns
t_{PHL}			2.5	0.3	4.9	0.2	4	0.2	3	0.2	2.6	
t_{PLH}	B	A	2.1	0.6	3.8	0.4	3.3	0.3	2.8	0.3	2.6	ns
t_{PHL}			2.1	0.6	3.8	0.4	3.3	0.3	2.8	0.3	2.6	
t_{PHZ}	DIR	A	2.9	1.1	8.2	1	6.7	1.3	4.9	1.2	4.2	ns
t_{PLZ}			2.9	1.1	8.2	1	6.7	1.3	4.9	1.2	4.2	
t_{PHZ}	DIR	B	3.4	0.5	6.8	0.3	5.8	0.3	4.8	1.1	4.4	ns
t_{PLZ}			3.4	0.5	6.8	0.3	5.8	0.3	4.8	1.1	4.4	
t_{PZH} (1)	DIR	A	5.5		10.4		8.9		7.4		6.8	ns
t_{PZL} (1)			5.5		10.4		8.9		7.4		6.8	
t_{PZH} (1)	DIR	B	5.4		12.9		10.5		7.7		6.6	ns
t_{PZL} (1)			5.4		12.9		10.5		7.7		6.6	

(1) The enable time is a calculated value, derived using the formula shown in the Section 8.2.2.2.1 section.

5.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2V	V_{CCA} = V_{CCB} = 1.5V	V_{CCA} = V_{CCB} = 1.8V	V_{CCA} = V_{CCB} = 2.5V	V_{CCA} = V_{CCB} = 3.3V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10MHz, t_r = t_f = 1ns	3	3	3	3	4	pF
	B-port input, A-port output		12	13	13	14	15	
C_{pdB} (1)	A-port input, B-port output	C_L = 0, f = 10MHz, t_r = t_f = 1ns	12	13	13	14	15	pF
	B-port input, A-port output		3	3	3	3	4	

(1) Power-dissipation capacitance per transceiver

5.12 Typical Characteristics

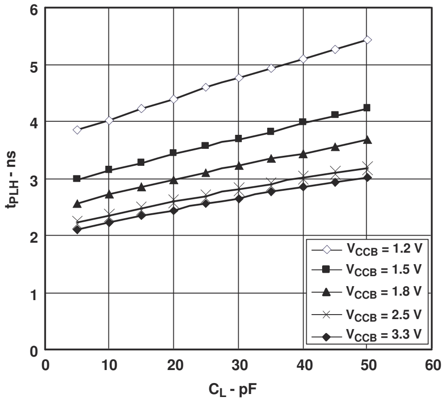


Figure 5-1. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 1.2V

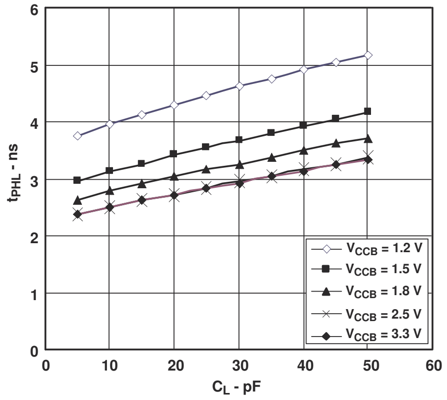


Figure 5-2. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 1.2V

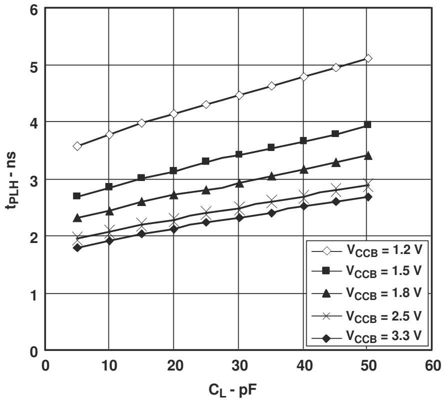


Figure 5-3. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 1.5V

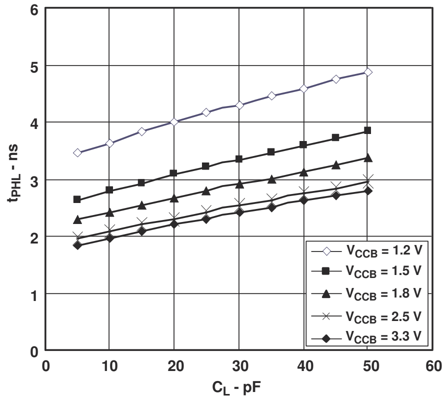


Figure 5-4. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 1.5V

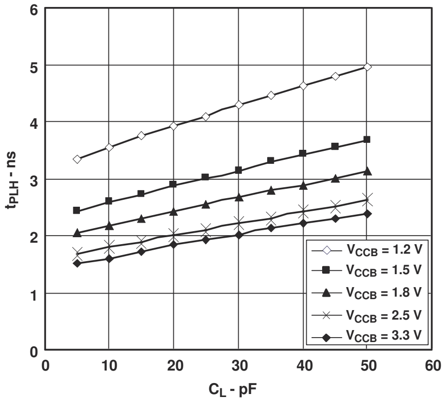


Figure 5-5. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 1.8V

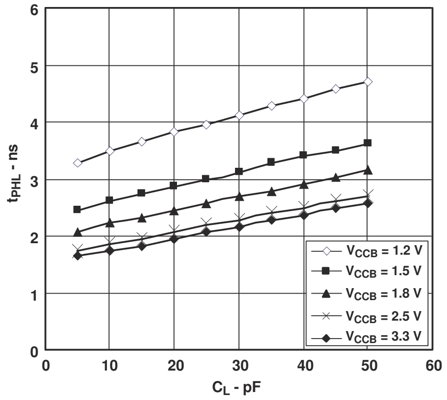


Figure 5-6. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 1.8V

5.12 Typical Characteristics (continued)

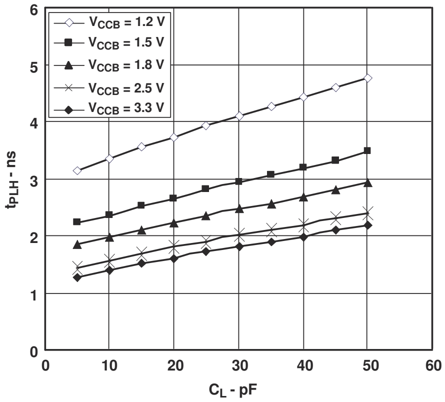


Figure 5-7. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 2.5V

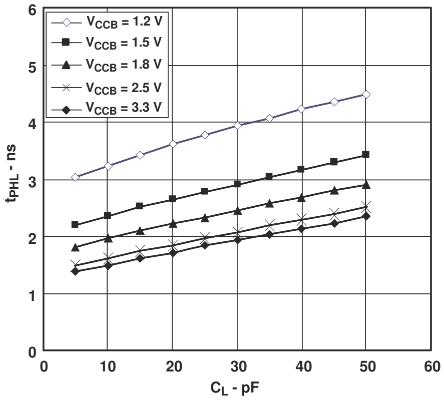


Figure 5-8. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 2.5V

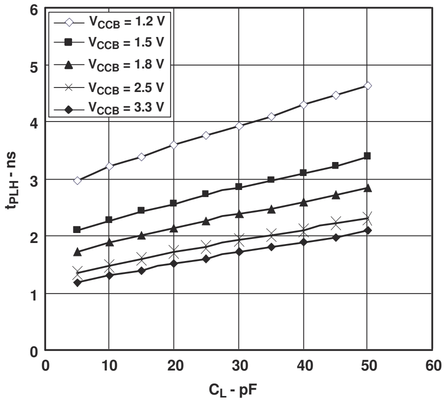


Figure 5-9. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 3.3V

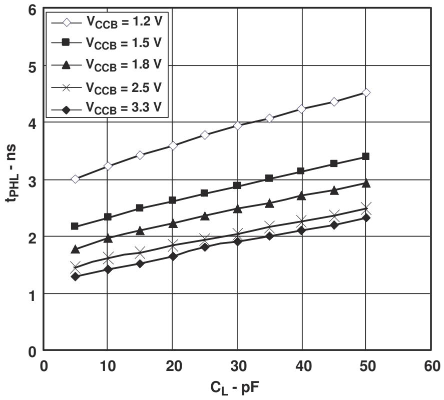
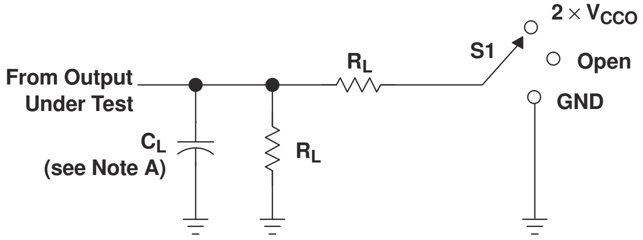


Figure 5-10. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 3.3V

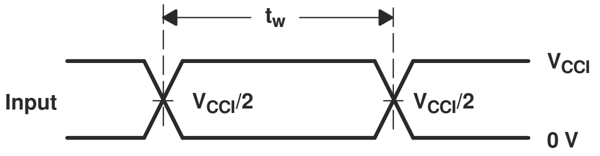
6 Parameter Measurement Information



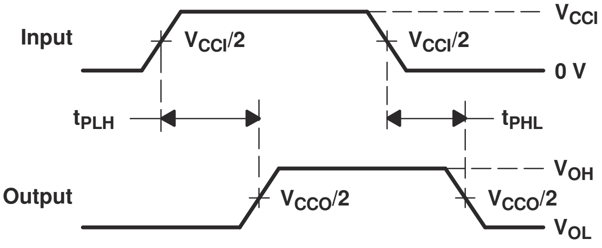
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

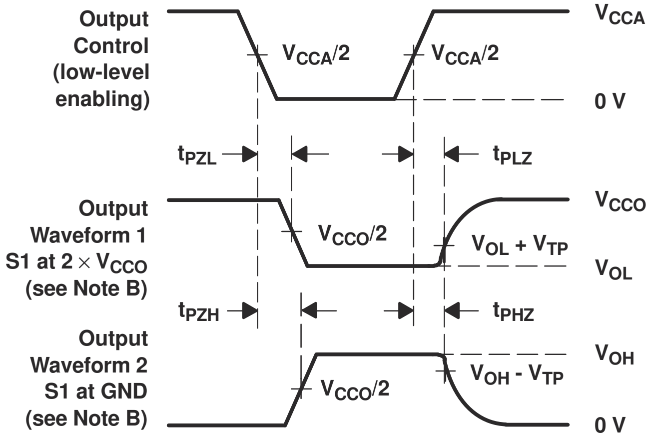
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} and accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB} and accepts any supply voltage from 1.2V to 3.6V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The device is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess internal leakage of the CMOS.

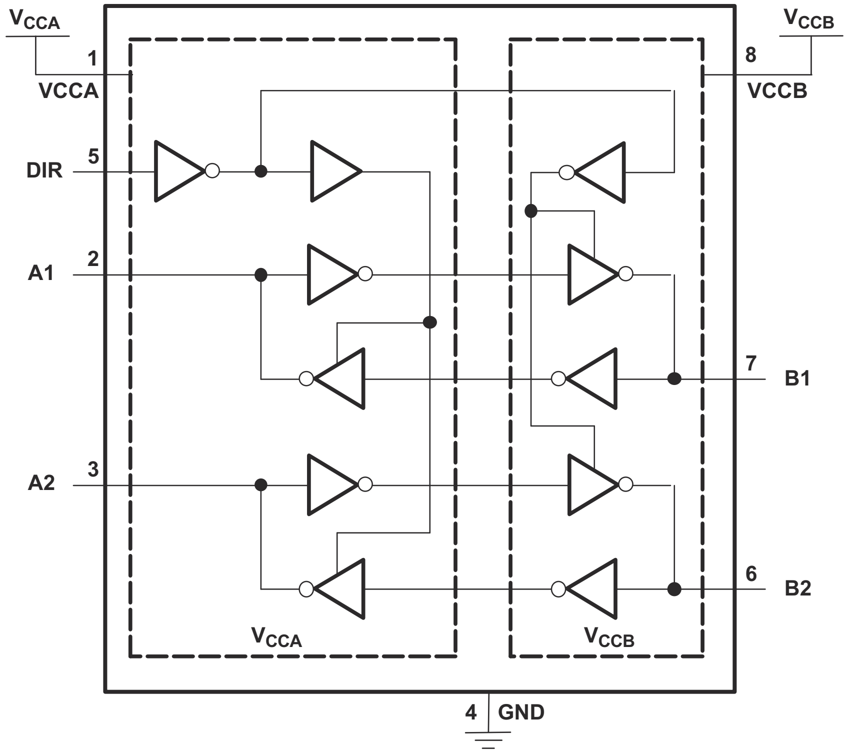
The device is designed so that the DIR input is powered by supply voltage from VCCA.

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

The V_{CC} isolation feature makes sure that if either VCC input is at GND, both ports are put in a high-impedance state. This action prevents a false high or low logic being presented at the output.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

7.2 Functional Block Diagram



Pin numbers are for the DCT and DCU packages only.

7.3 Feature Description

7.3.1 VCC Isolation

The V_{CC} isolation feature make sure that if either V_{CCA} or V_{CCB} are at GND, both ports are in a high-impedance state (I_{OZ} shown in *Section 5.5*). This action prevents false logic levels from being presented to either bus.

7.3.2 2-Rail Design

Fully configurable 2-rail design allows each port to operate over the full 1.2V to 3.6V power-supply range.

7.3.3 IO Ports are 4.6V Tolerant

The IO ports are up to 4.6V tolerant.

7.3.4 Partial-Power-Down Mode

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when the device is powered down.

7.4 Device Functional Modes

Table 7-1 shows the functional modes of the SN74AVC2T45-Q1.

Table 7-1. Function Table (Each Transceiver)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AVC2T45 is used to shift IO voltage levels from one voltage domain to another. Bus A and bus B have independent power supplies, and a direction pin is used to control the direction of data flow. Unused data ports must not be floating; tie the unused port input and output to ground directly.

8.2 Typical Applications

8.2.1 Unidirectional Logic Level-Shifting Application

Figure 8-1 is an example circuit of the SN74AVC2T45 used in a unidirectional logic level-shifting application.

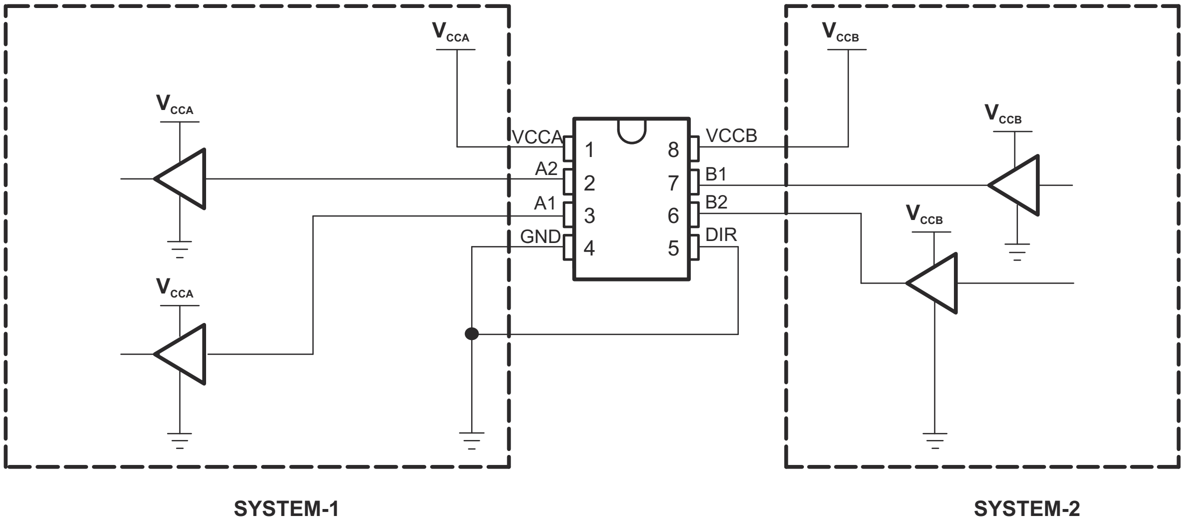


Figure 8-1. Unidirectional Logic Level-Shifting Application

8.2.1.1 Design Requirements

Table 8-1 lists the pins and pin descriptions of the SN74AVC2T45 connections with SYSTEM-1 and SYSTEM-2.

Table 8-1. SN74AVC2T45 Pin Connections With SYSTEM-1 and SYSTEM-2

PIN	NAME	DESCRIPTION
1	VCCA	SYSTEM-1 supply voltage (1.2V to 3.6V)
2	A1	Output level depends on V_{CCA}.
3	A2	Output level depends on V_{CCA}.
4	GND	Device GND
5	DIR	The GND (low-level) determines B-port to A-port direction.
6	B2	Input threshold value depends on V_{CCB}.
7	B1	Input threshold value depends on V_{CCB}.
8	VCCB	SYSTEM-2 supply voltage (1.2V to 3.6V)

8.2.1.2 Detailed Design Procedure

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Make sure to tie any unused input and output ports directly to ground.

8.2.1.3 Application Curve

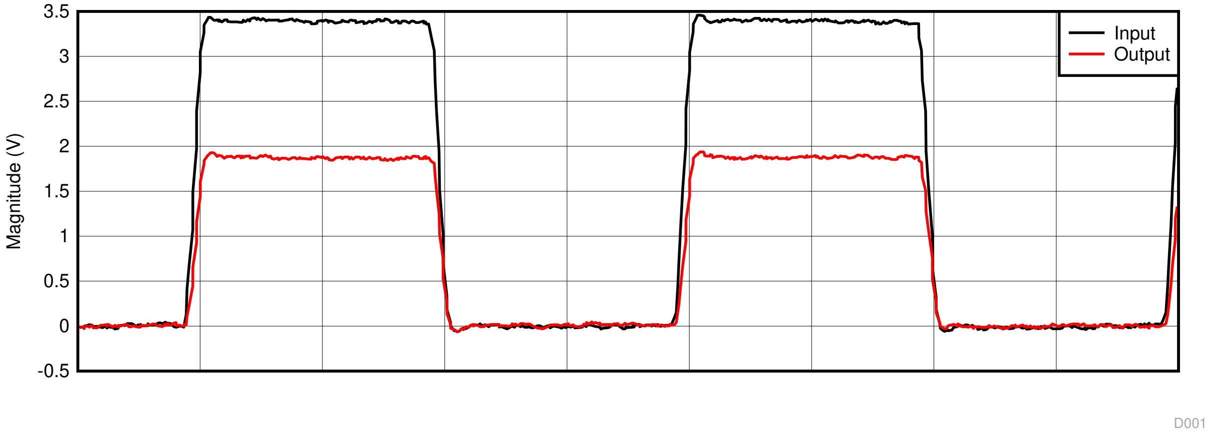


Figure 8-2. 3.3V to 1.8V Level-Shifting With 1MHz Square Wave

8.2.2 Bidirectional Logic Level-Shifting Application

Figure 8-3 shows the SN74AVC2T45 used in a bidirectional logic level-shifting application.

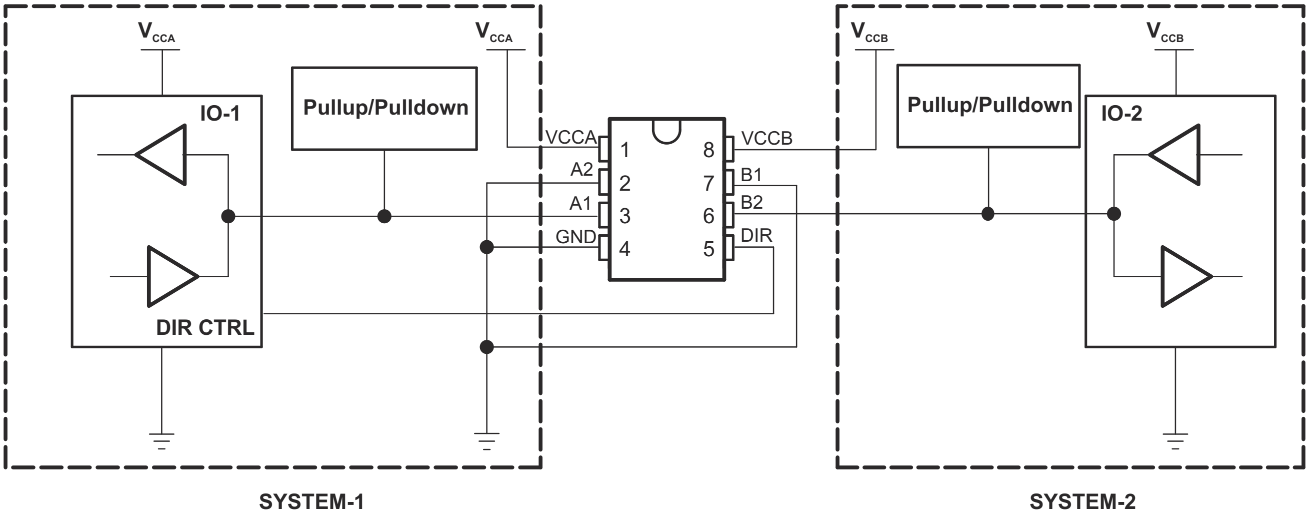


Figure 8-3. Bidirectional Logic Level-Shifting Application

8.2.2.1 Design Requirements

The SN74AVC2T45 does not have an output-enable (OE) pin, the system designer must take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

8.2.2.2 Detailed Design Procedure

Table 8-2 shows a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

Table 8-2. Data Transmission Sequence

STATE	DIR CTRL	IO-1	IO-2	DESCRIPTION
1	H	Output	Input	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. IO-1 and IO-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. IO-1 and IO-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)
4	L	Input	Output	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

8.2.2.2.1 Enable Times

Calculate the enable times for the SN74AVC2T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting the device with an input. After the B port has been disabled, an input signal applied to the port appears on the corresponding A port after the specified propagation delay.

8.3 Power Supply Recommendations

Follow a proper power-up sequence always to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

Table 8-3. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}						UNIT
	0V	1.2V	1.5V	1.8V	2.5V	3.3V	
0V	0	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	µA
1.2V	< 0.5	< 1	< 1	< 1	< 1	1	
1.5V	< 0.5	< 1	< 1	< 1	< 1	1	
1.8V	< 0.5	< 1	< 1	< 1	<1	< 1	
2.5V	< 0.5	1	< 1	< 1	<1	< 1	
3.3V	< 0.5	1	< 1	< 1	<1	< 1	

8.4 Layout

8.4.1 Layout Guidelines

To verify the reliability of the device, follow common printed-circuit board layout guidelines.

- Bypass capacitors can be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB pin and GND pin.
- Short trace lengths can be used to avoid excessive loading.

8.4.2 Layout Example

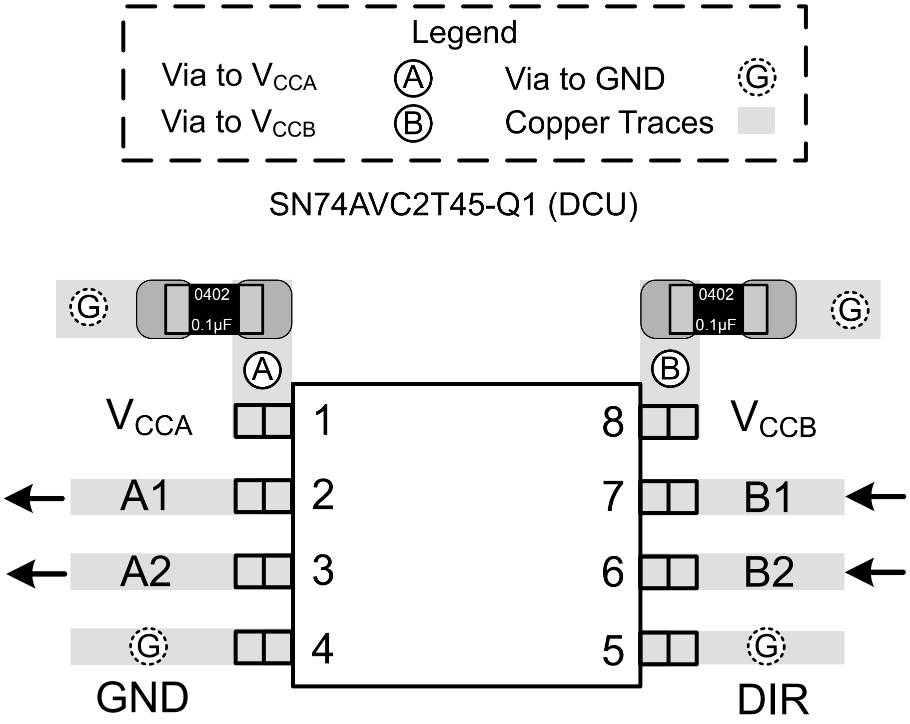


Figure 8-4. SN74AVC2T45-Q1 (DCU) Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2010) to Revision A (February 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the document to current TI format	1
• Added the DTT package option to the data sheet	1
• Updated DCU thermal information	7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAVC2T45TDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBUI	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AVC2T45-Q1 :

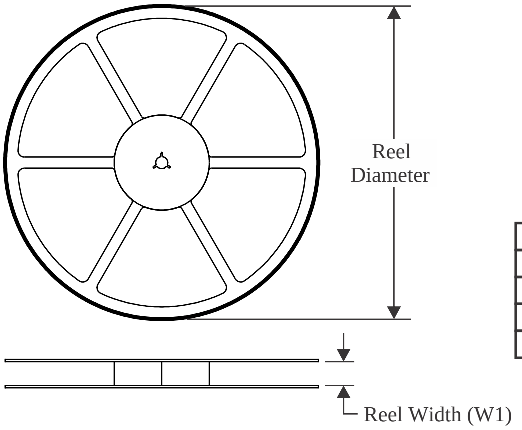
- Catalog : SN74AVC2T45

NOTE: Qualified Version Definitions:

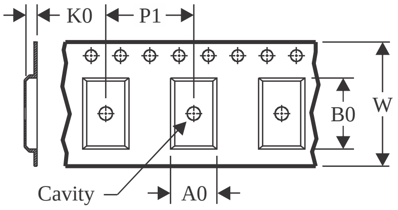
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

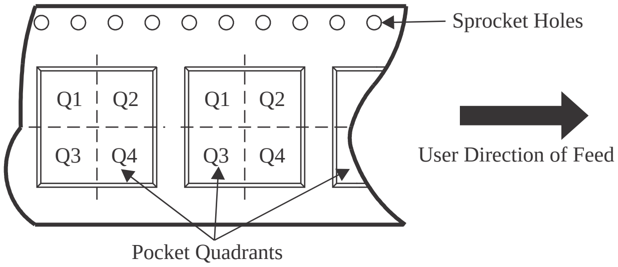


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

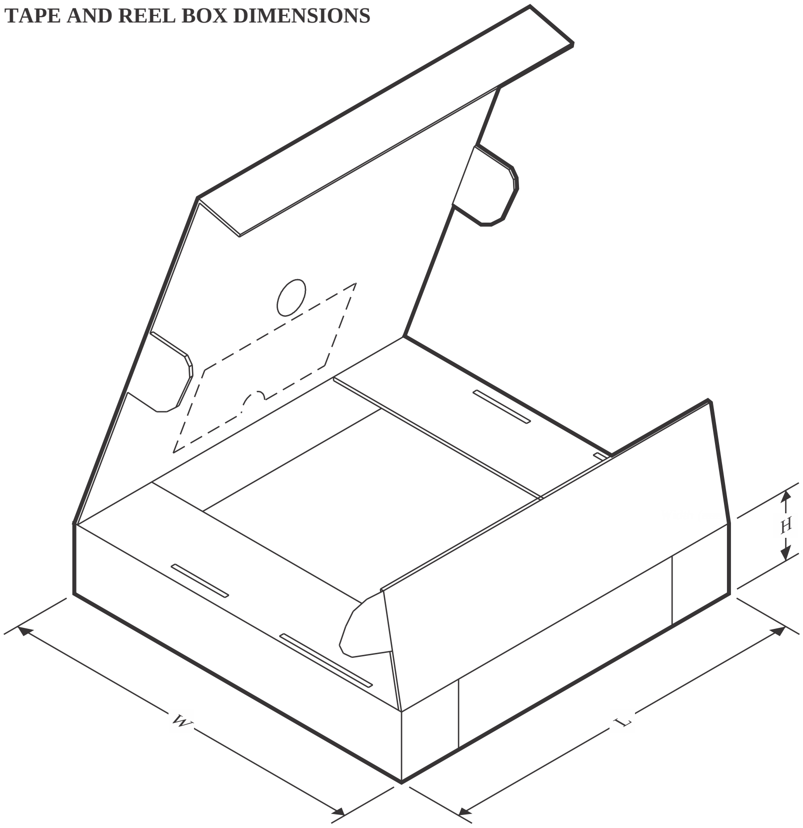
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAVC2T45TDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

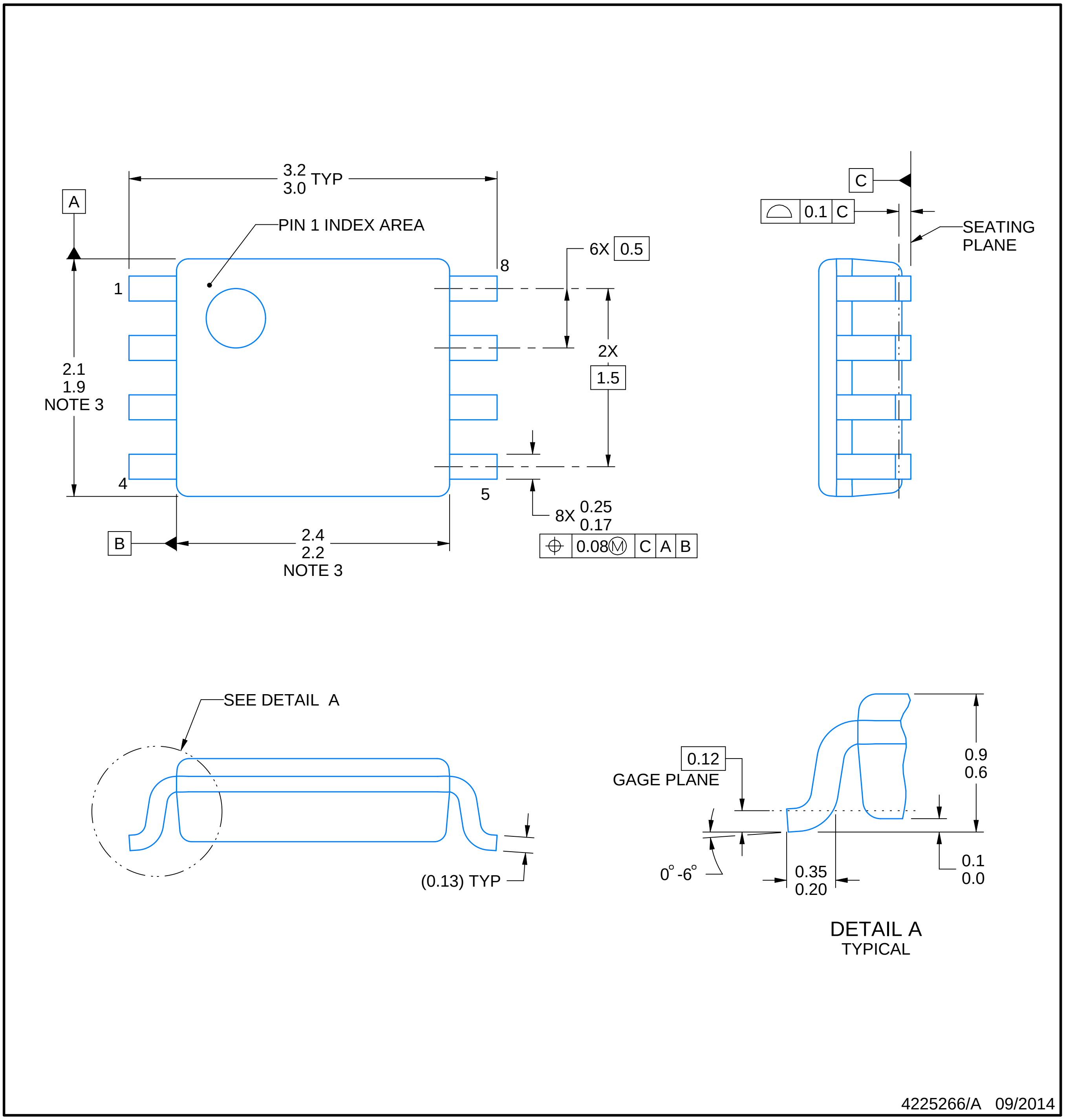
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAVC2T45TDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0

DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



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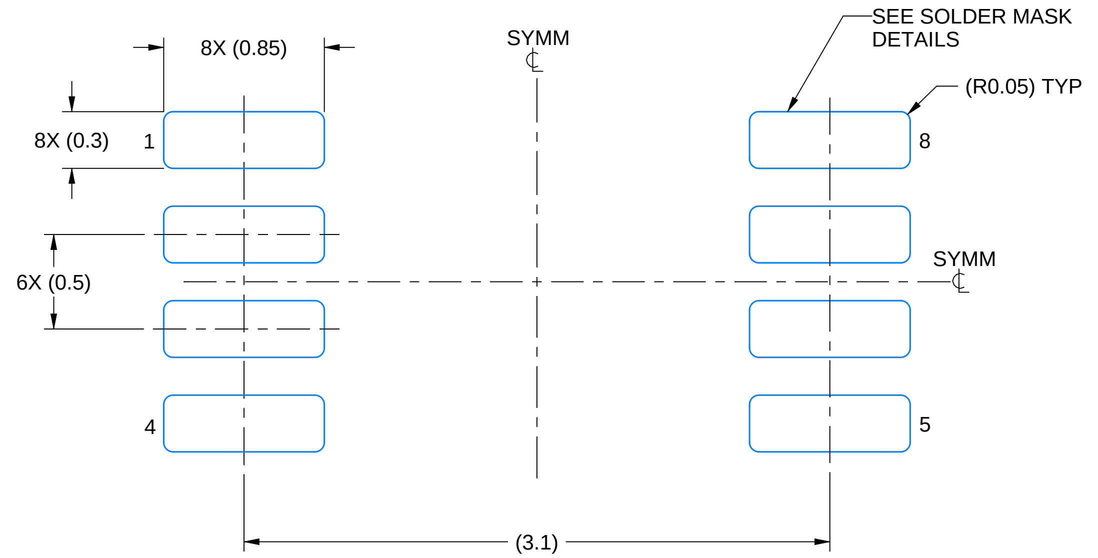
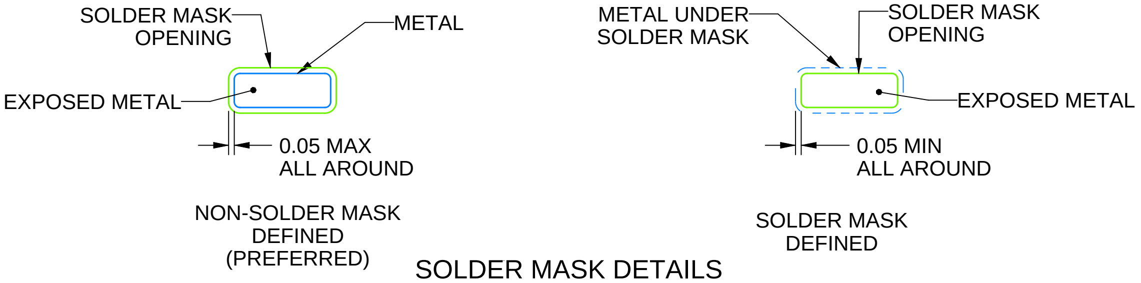
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

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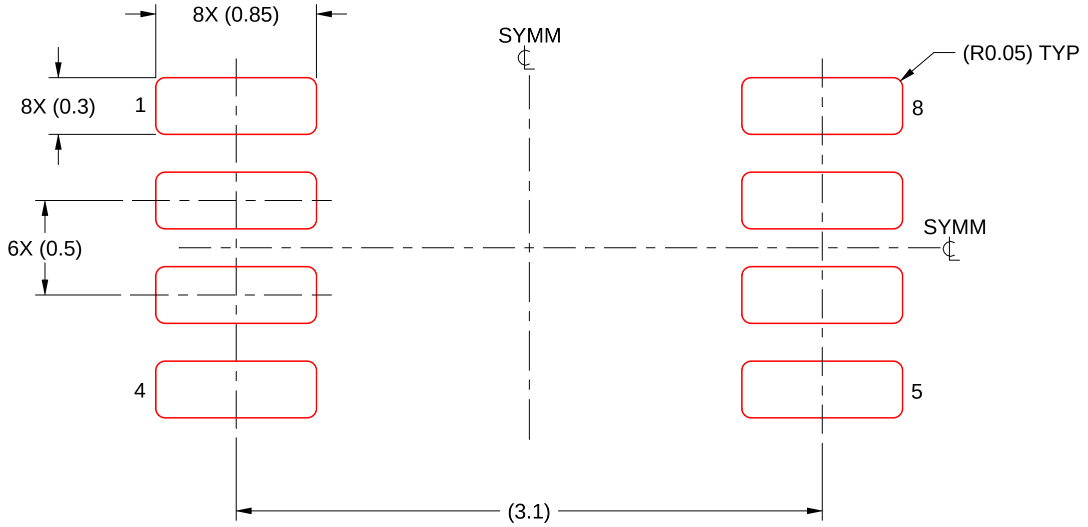
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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