SN74AVC4T245-Q1 構成可能な電圧レベル変換および 3 ステート出力搭載、車載用、4 ビット、デュアル電源、バス トランシーバ

1 特長

- 車載アプリケーション認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲 -40℃～125℃
  - デバイス HBM ESD 分類レベル H3B (JESD 22 A114-A)
  - デバイス CDM ESD 分類レベル C5 (JESD 22 C101)
- 機能安全対応
- V_{CCA} 電圧基準の制御入力 V_{IH}/V_{IL} レベル
- 完全に構成可能なデュアル レール設計により、1.2V～3.6V の電源電圧の全範囲にわたって各ポートが動作可能
- I/O は 4.6V 許容です
- I_{off} により部分的パワーダウン モードでの動作をサポート
- 最大データ レート:
  - 380Mbps (1.8V から 3.3V への変換)
  - 200Mbps (<1.8V から 3.3V への変換)
  - 200Mbps (2.5V または 1.8V への変換)
  - 150Mbps (1.5V への変換)
  - 100Mbps (1.2V への変換)
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- テレマティクス
- クラスタ
- ヘッド ユニット
- ナビゲーション システム

3 概要

この 4 ビット非反転バストランシーバは、設定可能な 2 本の独立した電源レールを使用します。A ポートは V_{CCA} に追従するように設計されています。V_{CCA} ピンには、1.2V～3.6V の電源電圧を入力できます。B ポートは、V_{CCB} に追従する設計になっています。V_{CCB} には、1.2V～3.6V の電源電圧を入力できます。

SN74AVC4T245-Q1 は、V_{CCA}/V_{CCB} を 1.4V～3.6V に設定した場合の動作用に最適化されています。最低 1.2V の V_{CCA}/V_{CCB} で動作します。これにより、1.2V、1.5V、1.8V、2.5V、3.3V の任意の電圧ノード間での自在な低電圧双方向変換が可能です。

SN74AVC4T245-Q1 は、2 つのデータ バス間の非同期通信用に設計されています。方向制御 (DIR) 入力および出力イネーブル ($\overline{OE}$) 入力のロジック レベルに応じて、B ポート出力もしくは A ポート出力のいずれかがアクティブになるか、または、両方の出力ポートが高インピーダンス モードになります。本デバイスは、B ポート出力がアクティブになった場合、A バスから B バスへデータを転送し、A ポート出力がアクティブになった場合、B バスから A バスへデータを転送します。A ポートと B ポートの入力回路はどちらも常にアクティブであるため、これらのポートには論理 High または Low レベルを印加して、I_{CC} と I_{CCZ} が過剰に流れないようにする必要があります。

SN74AVC4T245-Q1 は、制御ピン (1DIR、2DIR、1$\overline{OE}$、2 $\overline{OE}$) が V_{CCA} から電源を供給されるように設計されています。

このデバイスは、I_{off} を使用する部分的パワーダウン アプリケーション用の動作が完全に規定されています。I_{off} 回路で出力をディセーブルすることにより、電源切断時にデバイスに電流が逆流して損傷するのを回避できます。

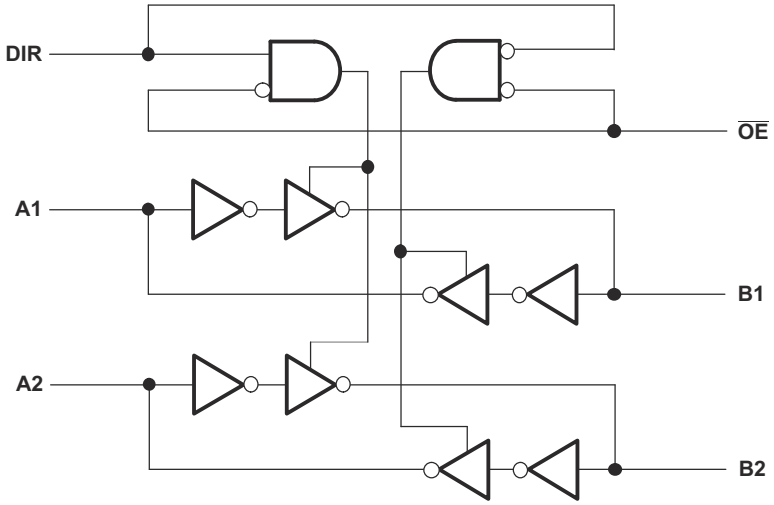
この V_{CC} 絶縁機能の設計により、いずれかの V_{CC} 入力が GND の場合、両方のポートが高インピーダンス状態になります。

電源投入または電源オフの間にデバイスを高インピーダンス状態にするには、$\overline{OE}$ をプルアップ抵抗を介して V_{CC} に接続します。この抵抗の最小値は、ドライバの電流シンク能力によって決まります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN74AVC4T245-Q1	RGY (VQFN、16)	4mm × 3.5mm
	PW (TSSOP、16)	5mm × 6.4mm
	BQB (WQFN、16)	3.5mm × 2.5mm
	DYY (SOT、16)	4.2mm × 2mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



SN74AVC4T245-Q1 の 1/2 の論理図 (正論理)

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4 Pin Configuration and Functions

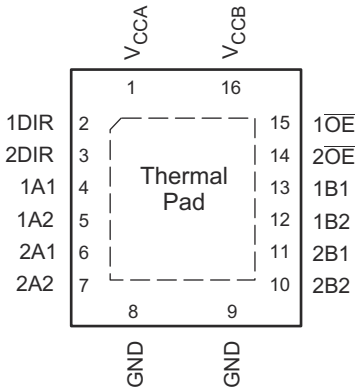


図 4-1. RGY Package 16-Pin VQFN With Exposed Thermal Pad (Top View)

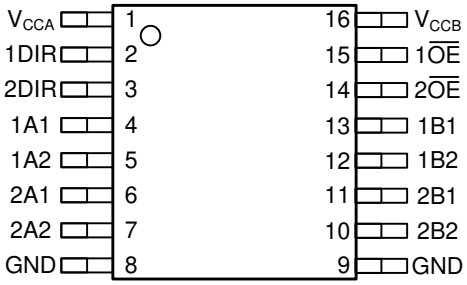


図 4-2. PW Package, 16-Pin TSSOP (Top View)

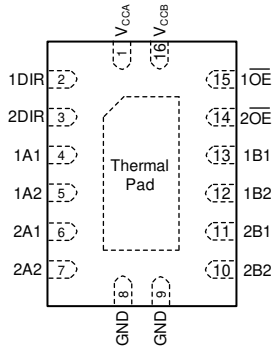


図 4-3. BQB/WBQB Package, 16-Pin WQFN (Transparent Top View)

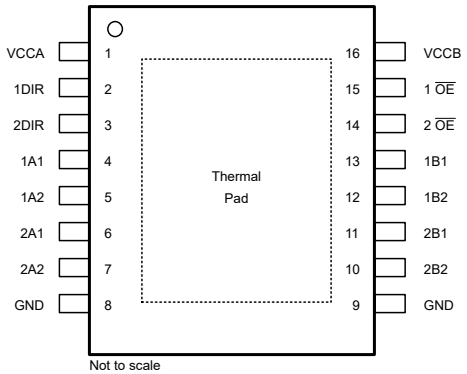


図 4-4. DYY Package, 16-Pin SOT (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A1	4	I/O	Input/output 1A1. Referenced to V_{CCA}.
1A2	5	I/O	Input/output 1A2. Referenced to V_{CCA}.
1B1	13	I/O	Input/output 1B1. Referenced to V_{CCB}.
1B2	12	I/O	Input/output 1B2. Referenced to V_{CCB}.
1DIR	2	I	Direction-control input for 1 ports
1 $\overline{OE}$	15	I	3-state output-mode enable. Pull $\overline{OE}$ high to place ‘1’ outputs in 3-state mode. Referenced to V_{CCA}.
2A1	6	I/O	Input/output 2A1. Referenced to V_{CCA}.
2A2	7	I/O	Input/output 2A2. Referenced to V_{CCA}.
2B1	11	I/O	Input/output 2B1. Referenced to V_{CCB}.
2B2	10	I/O	Input/output 2B2. Referenced to V_{CCB}.
2DIR	3	I	Direction-control input for 2 ports
2 $\overline{OE}$	14	I	3-state output-mode enable. Pull $\overline{OE}$ high to place ‘2’ outputs in 3-state mode. Referenced to V_{CCA}.
GND	8, 9	—	Ground
V_{CCA}	1	I	A-port power supply voltage. 1.2V ≤ V_{CCA} ≤ 3.6V
V_{CCB}	16	I	B-port power supply voltage. 1.2V ≤ V_{CCB} ≤ 3.6V
Thermal pad		—	The exposed thermal pad must be connected as a secondary GND or be left electrically open.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Machine model (C101)	±150	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs(1)	1.2V to 1.95V		V_{CCI} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		
V_{IL}	Low-level input voltage	Data inputs(1)	1.2V to 1.95V			V_{CCI} × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 3.6V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(2)	1.2V to 1.95V		V_{CCA} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		

5.3 Recommended Operating Conditions (続き)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(2)	1.2V to 1.95V			V_{CCA} × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 3.6V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2V		–3	mA
				1.4V to 1.6V		–6	
				1.65V to 1.95V		–8	
				2.3V to 2.7V		–9	
				3V to 3.6V		–12	
I_{OL}	Low-level output current			1.1V to 1.2V		3	mA
				1.4V to 1.6V		6	
				1.65V to 1.95V		8	
				2.3V to 2.7V		9	
				3V to 3.6V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating ambient temperature				–40	125	°C

(1) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V
(2) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V

5.4 Thermal Information

THERMAL METRIC(1)		SN74AVC4T245-Q1				UNIT
		RGY (VQFN)	PW (TSSOP)	BQB (WQFN)	DYY (SOT)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.5	101.8	80.8	163.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.5	37.2	77.9	90.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.6	60.6	50.7	93.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	1.6	7.4	10.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.8	60.0	50.6	92.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	N/A	28.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100µA	$V_I = V_{IH}$	1.2V to 3.6V	1.2V to 3.6V	T_A = –40°C to 125°C	V_{CCO} – 0.2			V
		I_{OH} = –3mA		1.2V	1.2V	T_A = 25°C		0.95		
		I_{OH} = –6mA		1.4V	1.4V	T_A = –40°C to 125°C	1.05			
		I_{OH} = –8mA		1.65V	1.65V	T_A = –40°C to 125°C	1.2			
		I_{OH} = –9mA		2.3V	2.3V	T_A = –40°C to 125°C	1.75			
		I_{OH} = –12mA		3V	3V	T_A = –40°C to 125°C	2.3			
V_{OL}		I_{OL} = 100µA	$V_I = V_{IL}$	1.2V to 3.6V	1.2V to 3.6V	T_A = –40°C to 125°C			0.2	V
		I_{OL} = 3mA		1.2V	1.2V	T_A = 25°C		0.25		
		I_{OL} = 6mA		1.4V	1.4V	T_A = –40°C to 125°C			0.35	
		I_{OL} = 8mA		1.65V	1.65V	T_A = –40°C to 125°C			0.45	
		I_{OL} = 9mA		2.3V	2.3V	T_A = –40°C to 125°C			0.55	
		I_{OL} = 12mA		3V	3V	T_A = –40°C to 125°C			0.7	
I_I [1]	Control inputs	$V_I = V_{CCA}$ or GND		1.2V to 3.6V	1.2V to 3.6V	T_A = 25°C		±0.025	±0.25	µA
						T_A = –40°C to 125°C			±1.5	
I_{off}	A or B port	V_I or V_O = 0 to 3.6V		0V	0V to 3.6V	T_A = 25°C		±0.1	±1	µA
						T_A = –40°C to 125°C			±5	
				0V to 3.6V	0V	T_A = 25°C		±0.1	±1	
						T_A = –40°C to 125°C			±5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6V	3.6V	T_A = 25°C		±0.5	±2.5	µA
						T_A = –40°C to 125°C			±5	
I_{CCA} [1]		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V	T_A = –40°C to 125°C			8	µA
				0V	0V to 3.6V	T_A = 25°C			–2	
						T_A = –40°C to 125°C			–11	
				0V to 3.6V	0V	T_A = –40°C to 125°C			8	
I_{CCB} [1]		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V	T_A = –40°C to 125°C			8	µA
				0V	0V to 3.6V	T_A = –40°C to 125°C			8	
				0V to 3.6V	0V	T_A = 25°C			–2	
						T_A = –40°C to 125°C			–11	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V	T_A = –40°C to 125°C			16	µA

5.5 Electrical Characteristics (続き)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
C_i	Control inputs	V_I = 3.3V or GND	3.3V	3.3V	T_A = 25°C		3.5	4.5	pF
					T_A = –40°C to 125°C			7	
C_{io}	A or B port	V_O = 3.3V or GND	3.3V	3.3V	T_A = 25°C		6		pF
					T_A = –40°C to 125°C				

(1) All unused data inputs of the device must be held at V_{CCI} or GND for proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.6 Switching Characteristics: V_{CCA} = 1.2V

over recommended operating ambient temperature range, V_{CCA} = 1.2V (unless otherwise noted) (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	TYP	UNIT
t_{PHL}, t_{PLH}	A	B	V_{CCB} = 1.2V	3.4	ns
			V_{CCB} = 1.5V ± 0.1V	2.9	
			V_{CCB} = 1.8V ± 0.15V	2.7	
			V_{CCB} = 2.5V ± 0.2V	2.6	
			V_{CCB} = 3.3V ± 0.3V	2.8	
t_{PHL}, t_{PLH}	B	A	V_{CCB} = 1.2V	3.6	ns
			V_{CCB} = 1.5V ± 0.1V	3.1	
			V_{CCB} = 1.8V ± 0.15V	2.8	
			V_{CCB} = 2.5V ± 0.2V	2.6	
			V_{CCB} = 3.3V ± 0.3V	2.6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V	5.6	ns
			V_{CCB} = 1.5V ± 0.1V	4.7	
			V_{CCB} = 1.8V ± 0.15V	4.3	
			V_{CCB} = 2.5V ± 0.2V	3.9	
			V_{CCB} = 3.3V ± 0.3V	3.7	
t_{PZH}	$\overline{OE}$	B	V_{CCB} = 1.2V	5	ns
			V_{CCB} = 1.5V ± 0.1V	4.3	
			V_{CCB} = 1.8V ± 0.15V	3.9	
			V_{CCB} = 2.5V ± 0.2V	3.6	
			V_{CCB} = 3.3V ± 0.3V	36.6	
t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V	5	
			V_{CCB} = 1.5V ± 0.1V	4.3	
			V_{CCB} = 1.8V ± 0.15V	3.9	
			V_{CCB} = 2.5V ± 0.2V	3.6	
			V_{CCB} = 3.3V ± 0.3V	3.6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V	6.2	ns
			V_{CCB} = 1.5V ± 0.1V	5.2	
			V_{CCB} = 1.8V ± 0.15V	5.2	
			V_{CCB} = 2.5V ± 0.2V	4.3	
			V_{CCB} = 3.3V ± 0.3V	4.8	

5.6 Switching Characteristics: V_{CCA} = 1.2V (続き)

over recommended operating ambient temperature range, V_{CCA} = 1.2V (unless otherwise noted) (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	TYP	UNIT
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V	5.9	ns
			V_{CCB} = 1.5V ± 0.1V	5.1	
			V_{CCB} = 1.8V ± 0.15V	5	
			V_{CCB} = 2.5V ± 0.2V	4.7	
			V_{CCB} = 3.3V ± 0.3V	5.5	

5.7 Switching Characteristics, V_{CCA} = 1.5V ± 0.1V

over recommended operating ambient temperature range, V_{CCA} = 1.5V ± 0.1V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V		3.2		ns
			V_{CCB} = 1.5V ± 0.1V			11.3	
			V_{CCB} = 1.8V ± 0.15V			10.2	
			V_{CCB} = 2.5V ± 0.2V			9.2	
			V_{CCB} = 3.3V ± 0.3V			9.2	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V		3.3		ns
			V_{CCB} = 1.5V ± 0.1V			11.3	
			V_{CCB} = 1.8V ± 0.15V			11	
			V_{CCB} = 2.5V ± 0.2V			10.7	
			V_{CCB} = 3.3V ± 0.3V			10.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V		4.9		ns
			V_{CCB} = 1.5V ± 0.1V			14.6	
			V_{CCB} = 1.8V ± 0.15V			14.5	
			V_{CCB} = 2.5V ± 0.2V			14.4	
			V_{CCB} = 3.3V ± 0.3V			14.4	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V		4.5		ns
			V_{CCB} = 1.5V ± 0.1V			14.6	
			V_{CCB} = 1.8V ± 0.15V			12.7	
			V_{CCB} = 2.5V ± 0.2V			10.8	
			V_{CCB} = 3.3V ± 0.3V			10.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V		5.6		ns
			V_{CCB} = 1.5V ± 0.1V			15.2	
			V_{CCB} = 1.8V ± 0.15V			15.2	
			V_{CCB} = 2.5V ± 0.2V			15.2	
			V_{CCB} = 3.3V ± 0.3V			15.2	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V		5.2		ns
			V_{CCB} = 1.5V ± 0.1V			15.3	
			V_{CCB} = 1.8V ± 0.15V			14.1	
			V_{CCB} = 2.5V ± 0.2V			12.4	
			V_{CCB} = 3.3V ± 0.3V			12.6	

5.8 Switching Characteristics: V_{CCA} = 1.8V ± 0.15V

over recommended operating ambient temperature range, V_{CCA} = 1.8V ± 0.15V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V		2.9		ns
			V_{CCB} = 1.5V ± 0.1V			11	
			V_{CCB} = 1.8V ± 0.15V			9.9	
			V_{CCB} = 2.5V ± 0.2V			8.9	
			V_{CCB} = 3.3V ± 0.3V			8.9	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V		3		ns
			V_{CCB} = 1.5V ± 0.1V			10.3	
			V_{CCB} = 1.8V ± 0.15V			9.9	
			V_{CCB} = 2.5V ± 0.2V			9.6	
			V_{CCB} = 3.3V ± 0.3V			9.5	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V		4.4		ns
			V_{CCB} = 1.5V ± 0.1V			12.4	
			V_{CCB} = 1.8V ± 0.15V			12.3	
			V_{CCB} = 2.5V ± 0.2V			12.3	
			V_{CCB} = 3.3V ± 0.3V			12.2	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V		4.1		ns
			V_{CCB} = 1.5V ± 0.1V			14.2	
			V_{CCB} = 1.8V ± 0.15V			12.4	
			V_{CCB} = 2.5V ± 0.2V			10.3	
			V_{CCB} = 3.3V ± 0.3V			9.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V		5.4		ns
			V_{CCB} = 1.5V ± 0.1V			13.6	
			V_{CCB} = 1.8V ± 0.15V			13.7	
			V_{CCB} = 2.5V ± 0.2V			13.7	
			V_{CCB} = 3.3V ± 0.3V			13.7	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V		5		ns
			V_{CCB} = 1.5V ± 0.1V			14.9	
			V_{CCB} = 1.8V ± 0.15V			13.7	
			V_{CCB} = 2.5V ± 0.2V			11.9	
			V_{CCB} = 3.3V ± 0.3V			11.9	

5.9 Switching Characteristics: V_{CCA} = 2.5V ± 0.2V

over recommended operating ambient temperature range, V_{CCA} = 2.5V ± 0.2V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V		2.8		ns
			V_{CCB} = 1.5V ± 0.1V			10.7	
			V_{CCB} = 1.8V ± 0.15V			9.6	
			V_{CCB} = 2.5V ± 0.2V			8.5	
			V_{CCB} = 3.3V ± 0.3V			8.6	

5.9 Switching Characteristics: V_{CCA} = 2.5V ± 0.2V (続き)

over recommended operating ambient temperature range, V_{CCA} = 2.5V ± 0.2V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V		2.7		ns
			V_{CCB} = 1.5V ± 0.1V			9.2	
			V_{CCB} = 1.8V ± 0.15V			8.9	
			V_{CCB} = 2.5V ± 0.2V			8.4	
			V_{CCB} = 3.3V ± 0.3V			8.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V		4		ns
			V_{CCB} = 1.5V ± 0.1V			11.5	
			V_{CCB} = 1.8V ± 0.15V			10.2	
			V_{CCB} = 2.5V ± 0.2V			9.8	
			V_{CCB} = 3.3V ± 0.3V			9.8	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V		3.8		ns
			V_{CCB} = 1.5V ± 0.1V			13.8	
			V_{CCB} = 1.8V ± 0.15V			12	
			V_{CCB} = 2.5V ± 0.2V			9.8	
			V_{CCB} = 3.3V ± 0.3V			9	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V		4.7		ns
			V_{CCB} = 1.5V ± 0.1V			13.4	
			V_{CCB} = 1.8V ± 0.15V			13.4	
			V_{CCB} = 2.5V ± 0.2V			11.2	
			V_{CCB} = 3.3V ± 0.3V			11.5	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V		4.5		ns
			V_{CCB} = 1.5V ± 0.1V			14.4	
			V_{CCB} = 1.8V ± 0.15V			13.2	
			V_{CCB} = 2.5V ± 0.2V			11.2	
			V_{CCB} = 3.3V ± 0.3V			10.2	

5.10 Switching Characteristics: V_{CCA} = 3.3V ± 0.3V

over recommended operating ambient temperature range, V_{CCA} = 3.3V ± 0.3V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V		2.9		ns
			V_{CCB} = 1.5V ± 0.1V			10.6	
			V_{CCB} = 1.8V ± 0.15V			9.5	
			V_{CCB} = 2.5V ± 0.2V			8.3	
			V_{CCB} = 3.3V ± 0.3V			7.9	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V		2.6		ns
			V_{CCB} = 1.5V ± 0.1V			9.2	
			V_{CCB} = 1.8V ± 0.15V			8.4	
			V_{CCB} = 2.5V ± 0.2V			8	
			V_{CCB} = 3.3V ± 0.3V			7.8	

5.10 Switching Characteristics: V_{CCA} = 3.3V ± 0.3V (続き)

over recommended operating ambient temperature range, V_{CCA} = 3.3V ± 0.3V (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V		3.8		ns
			V_{CCB} = 1.5V ± 0.1V			13.7	
			V_{CCB} = 1.8V ± 0.15V			10.2	
			V_{CCB} = 2.5V ± 0.2V			8.8	
			V_{CCB} = 3.3V ± 0.3V			8.8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V		3.7		ns
			V_{CCB} = 1.5V ± 0.1V			13.7	
			V_{CCB} = 1.8V ± 0.15V			11.8	
			V_{CCB} = 2.5V ± 0.2V			9.7	
			V_{CCB} = 3.3V ± 0.3V			8.8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V		4.8		ns
			V_{CCB} = 1.5V ± 0.1V			14.3	
			V_{CCB} = 1.8V ± 0.15V			13.3	
			V_{CCB} = 2.5V ± 0.2V			10.6	
			V_{CCB} = 3.3V ± 0.3V			11.6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V		5.3		ns
			V_{CCB} = 1.5V ± 0.1V			14.3	
			V_{CCB} = 1.8V ± 0.15V			13.1	
			V_{CCB} = 2.5V ± 0.2V			11.4	
			V_{CCB} = 3.3V ± 0.3V			11.2	

5.11 Operating Characteristics

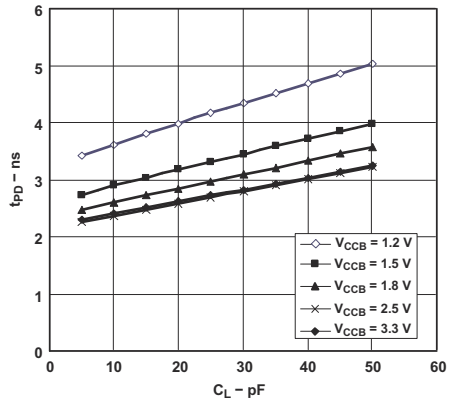
T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA}	TYP	UNIT
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10MHz, t_r = t_f = 1ns	V_{CCA} = V_{CCB} = 1.2V	1	pF
				V_{CCA} = V_{CCB} = 1.5V	1	
				V_{CCA} = V_{CCB} = 1.8V	1	
				V_{CCA} =V_{CCB} = 2.5V	1.5	
				V_{CCA} = V_{CCB} = 3.3V	2	
		Outputs disabled	C_L = 0, f = 10MHz, t_r = t_f = 1ns	V_{CCA} = V_{CCB} = 1.2V	1	
				V_{CCA} = V_{CCB} = 1.5V		
				V_{CCA} = V_{CCB} = 1.8V		
				V_{CCA} =V_{CCB} = 2.5V		
				V_{CCA} = V_{CCB} = 3.3V		
	B to A	Outputs enabled	C_L = 0, f = 10MHz, t_r = t_f = 1ns	V_{CCA} = V_{CCB} = 1.2V	12	
				V_{CCA} = V_{CCB} = 1.5V	12.5	
				V_{CCA} = V_{CCB} = 1.8V	13	
				V_{CCA} =V_{CCB} = 2.5V	14	
				V_{CCA} = V_{CCB} = 3.3V	15	
		Outputs disabled	C_L = 0, f = 10MHz, t_r = t_f = 1ns	V_{CCA} = V_{CCB} = 1.2V	1	
				V_{CCA} = V_{CCB} = 1.5V		
				V_{CCA} = V_{CCB} = 1.8V		
				V_{CCA} =V_{CCB} = 2.5V		
				V_{CCA} = V_{CCB} = 3.3V		
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10MHz, t_r = t_f = 1ns	V_{CCA} = V_{CCB} = 1.2V	12	pF
				V_{CCA} = V_{CCB} = 1.5V	12.5	
				V_{CCA} = V_{CCB} = 1.8V	13	
				V_{CCA} =V_{CCB} = 2.5V	14	
				V_{CCA} = V_{CCB} = 3.3V	15	
		Outputs disabled	C_L = 0, f = 10MHz, t_r = t_f = 1ns	V_{CCA} = V_{CCB} = 1.2V	1	
				V_{CCA} = V_{CCB} = 1.5V		
				V_{CCA} = V_{CCB} = 1.8V		
				V_{CCA} =V_{CCB} = 2.5V		
				V_{CCA} = V_{CCB} = 3.3V		
	B to A	Outputs enabled	C_L = 0, f = 10MHz, t_r = t_f = 1ns	V_{CCA} = V_{CCB} = 1.2V	1	
				V_{CCA} = V_{CCB} = 1.5V	1	
				V_{CCA} = V_{CCB} = 1.8V	1	
				V_{CCA} =V_{CCB} = 2.5V	1	
				V_{CCA} = V_{CCB} = 3.3V	2	
		Outputs disabled	C_L = 0, f = 10MHz, t_r = t_f = 1ns	V_{CCA} = V_{CCB} = 1.2V	1	
				V_{CCA} = V_{CCB} = 1.5V		
				V_{CCA} = V_{CCB} = 1.8V		
				V_{CCA} =V_{CCB} = 2.5V		
				V_{CCA} = V_{CCB} = 3.3V		

(1) Power dissipation capacitance per transceiver

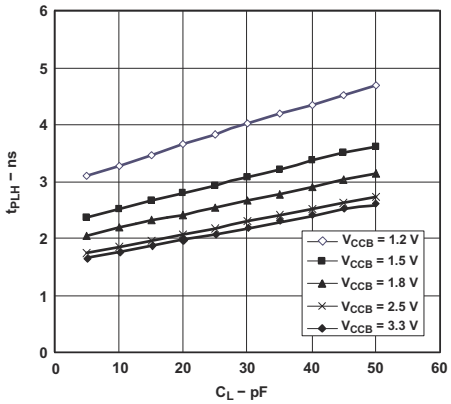
5.12 Typical Characteristics

T_A = 25°C



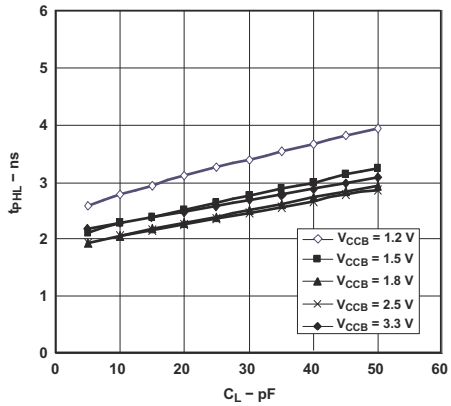
V_{CCA} = 1.2V

図 5-1. Typical Propagation Delay (A to B) vs Load Capacitance



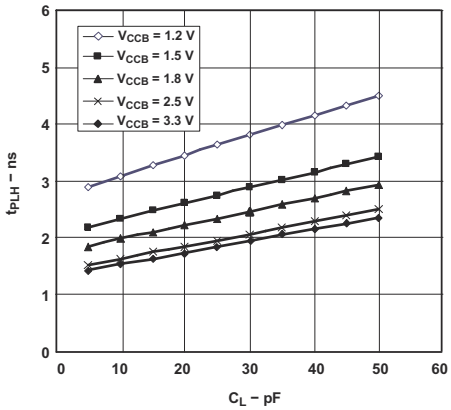
V_{CCA} = 1.5V

図 5-2. Typical Propagation Delay (A to B) vs Load Capacitance



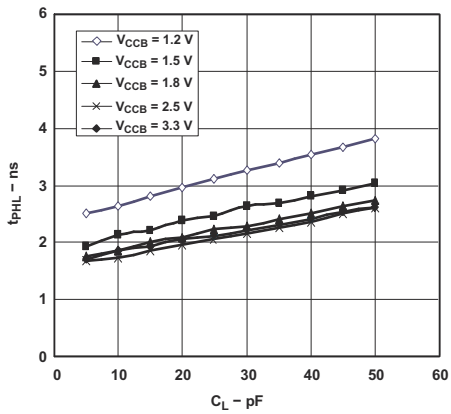
V_{CCA} = 1.5V

図 5-3. Typical Propagation Delay (A to B) vs Load Capacitance



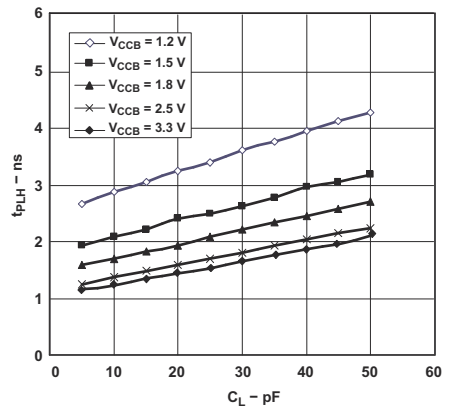
V_{CCA} = 1.8V

図 5-4. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 1.8V

図 5-5. Typical Propagation Delay (A to B) vs Load Capacitance

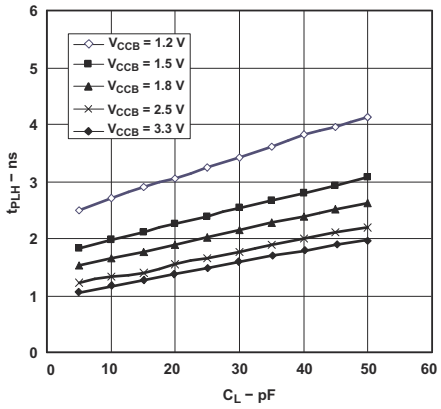


V_{CCA} = 2.5V

図 5-6. Typical Propagation Delay (A to B) vs Load Capacitance

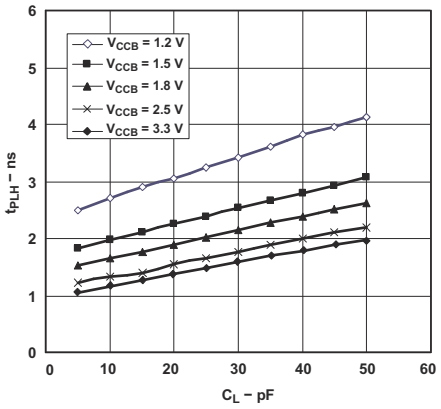
5.12 Typical Characteristics (continued)

T_A = 25°C



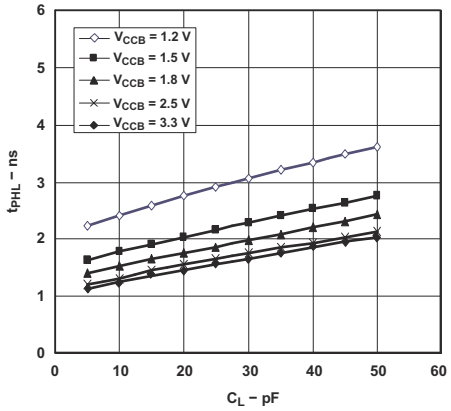
V_{CCA} = 2.5V

図 5-7. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 3.3V

図 5-8. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 3.3V

図 5-9. Typical Propagation Delay (A to B) vs Load Capacitance

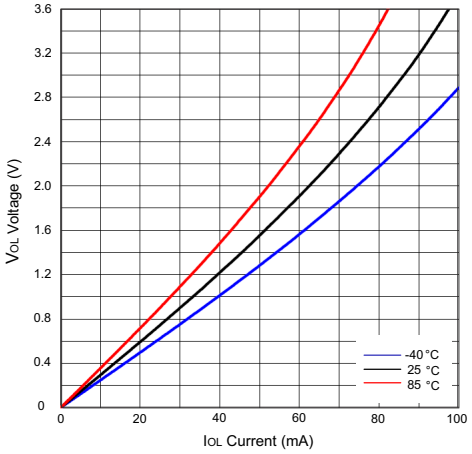


図 5-10. Low-Level Output Voltage (V_{OL}) vs Low-Level Current (I_{OL})

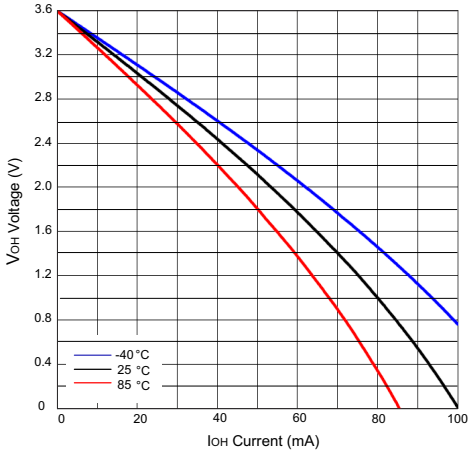
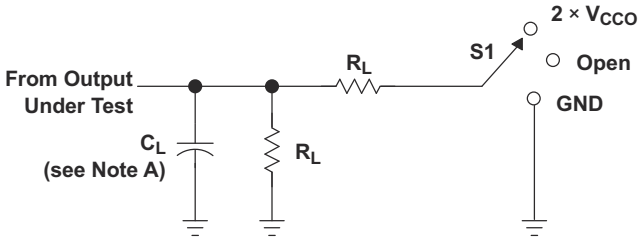


図 5-11. High-Level Output Voltage (V_{OH}) vs High-Level Current (I_{OH})

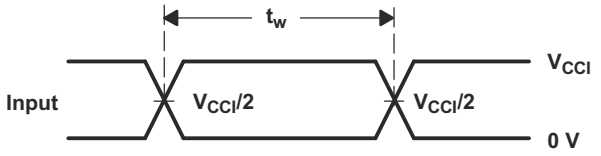
6 Parameter Measurement Information



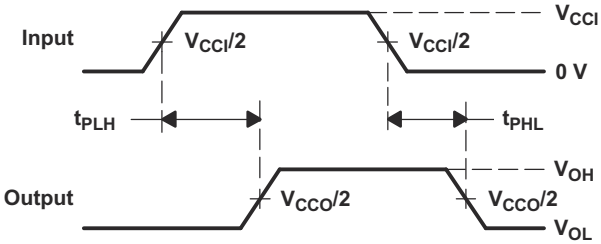
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CCO} GND

LOAD CIRCUIT

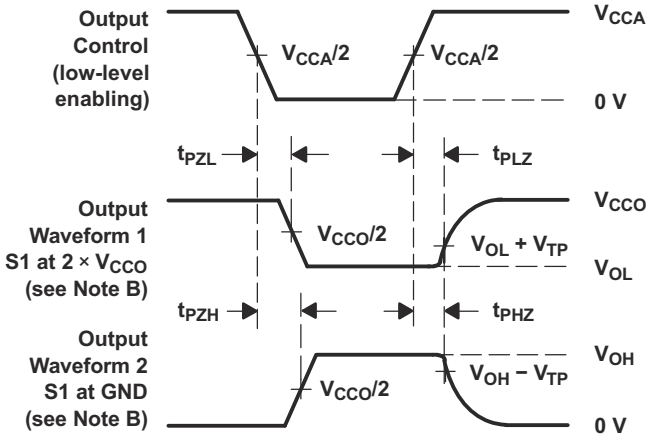
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

図 6-1. Load and Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AVC4T245-Q1 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (1DIR, 2DIR,1 $\overline{OE}$, and 2 $\overline{OE}$) are supported by V_{CCA}, and Bx pins are supported by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.2V to 3.6V, while the B port can accept I/O voltages from 1.2V to 3.6V. A high on DIR allows data transmission from Ax to Bx and a low on DIR allows data transmission from Bx to Ax when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state.

7.2 Functional Block Diagram

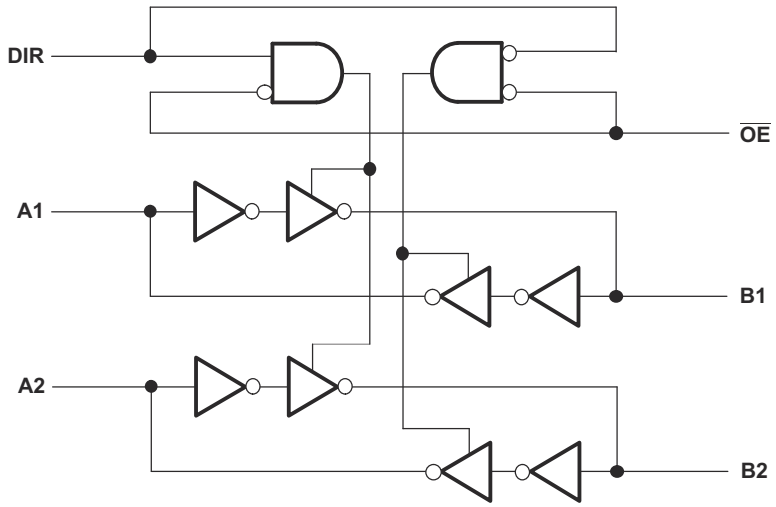


図 7-1. Logic Diagram (Positive Logic) for 1/2 of SN74AVC4T245-Q1

7.3 Feature Description

7.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.2V and 3.6V; thus, making the device suitable for translating between any of the low voltage nodes (1.2V, 1.8V, 2.5V, and 3.3V).

7.3.2 Supports High Speed Translation

The SN74AVC4T245-Q1 device can support high data rate applications. The translated signal data rate can be up to 380Mbps when the signal is translated from 1.8V to 3.3V.

7.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} prevents backflow current by disabling I/O output circuits when the device is in partial-power-down mode.

7.4 Device Functional Modes

表 7-1 lists the functional modes of the SN74AVC4T245-Q1 device.

表 7-1. Function Table
(Each 2-Bit Section)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

8 Application and Implementation

注

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8.1 Application Information

The SN74AVC4T245-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC4T245-Q1 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 380Mbps when the device translates a signal from 1.8V to 3.3V.

8.2 Typical Application

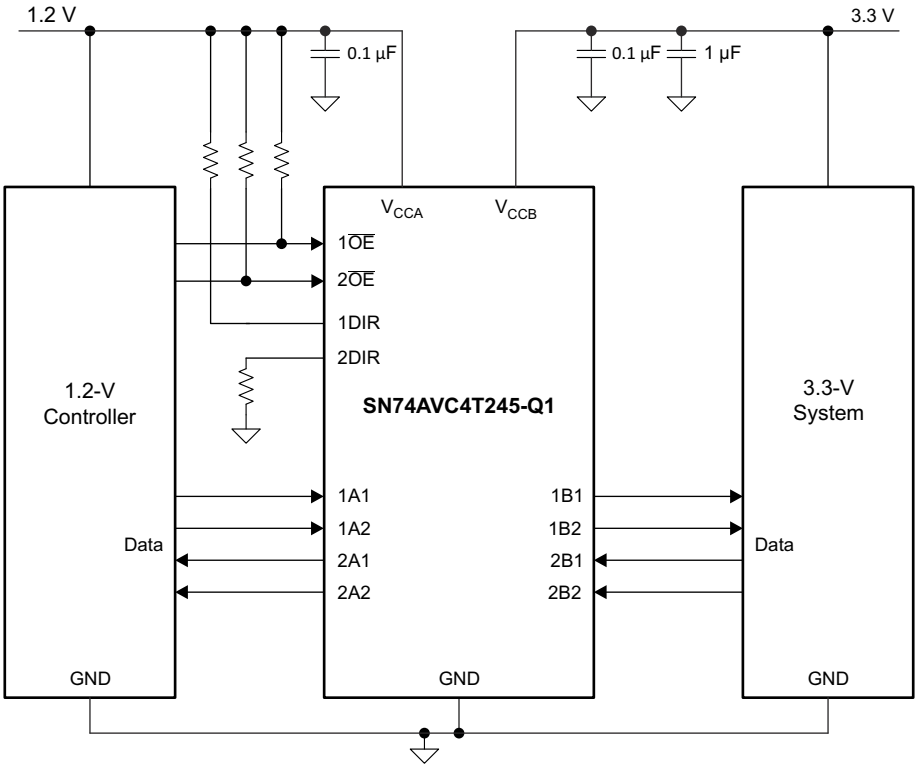

図 8-1. Typical Application Diagram

8.2.1 Design Requirements

表 8-1 lists the parameters for this design example.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2V
Output voltage range	3.3V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T245-Q1 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port. For this example, the input voltage is 1.2V.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T245-Q1 device is driving to determine the output voltage range. For this example, the output voltage is 3.3V.

8.2.3 Application Curve

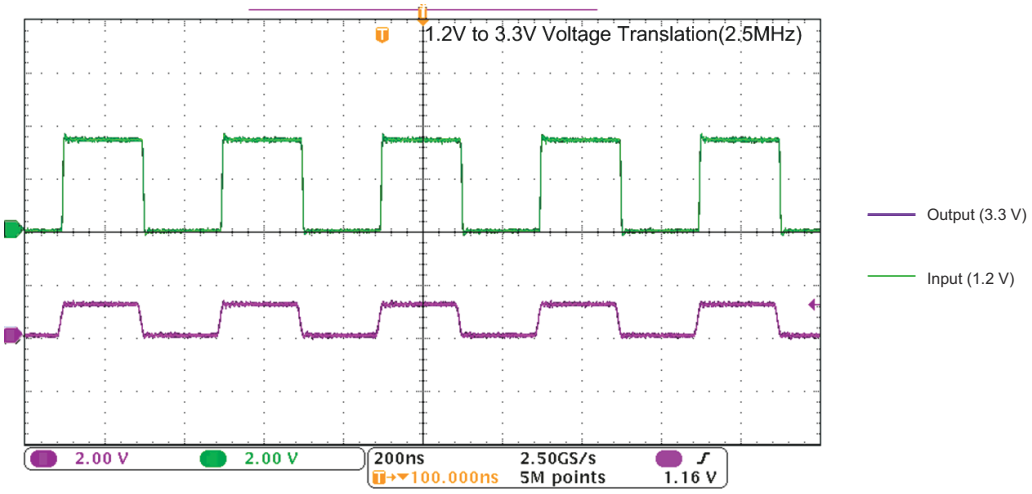

図 8-2. Translation Up (1.2V to 3.3V) at 2.5MHz

8.3 Power Supply Recommendations

The SN74AVC4T245-Q1 device uses two separate configurable power-supply rails: V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.2V to 3.6V, and V_{CCB} accepts any supply voltage from 1.2V to 3.6V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively, allowing for low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The output-enable ($\overline{OE}$) input circuit is designed so that it is supplied by V_{CCA}; when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To place the outputs in the high-impedance state during power up or power down, tie the $\overline{OE}$ input pin to V_{CCA} through a pullup resistor and do not enable it until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

8.4.2 Layout Example

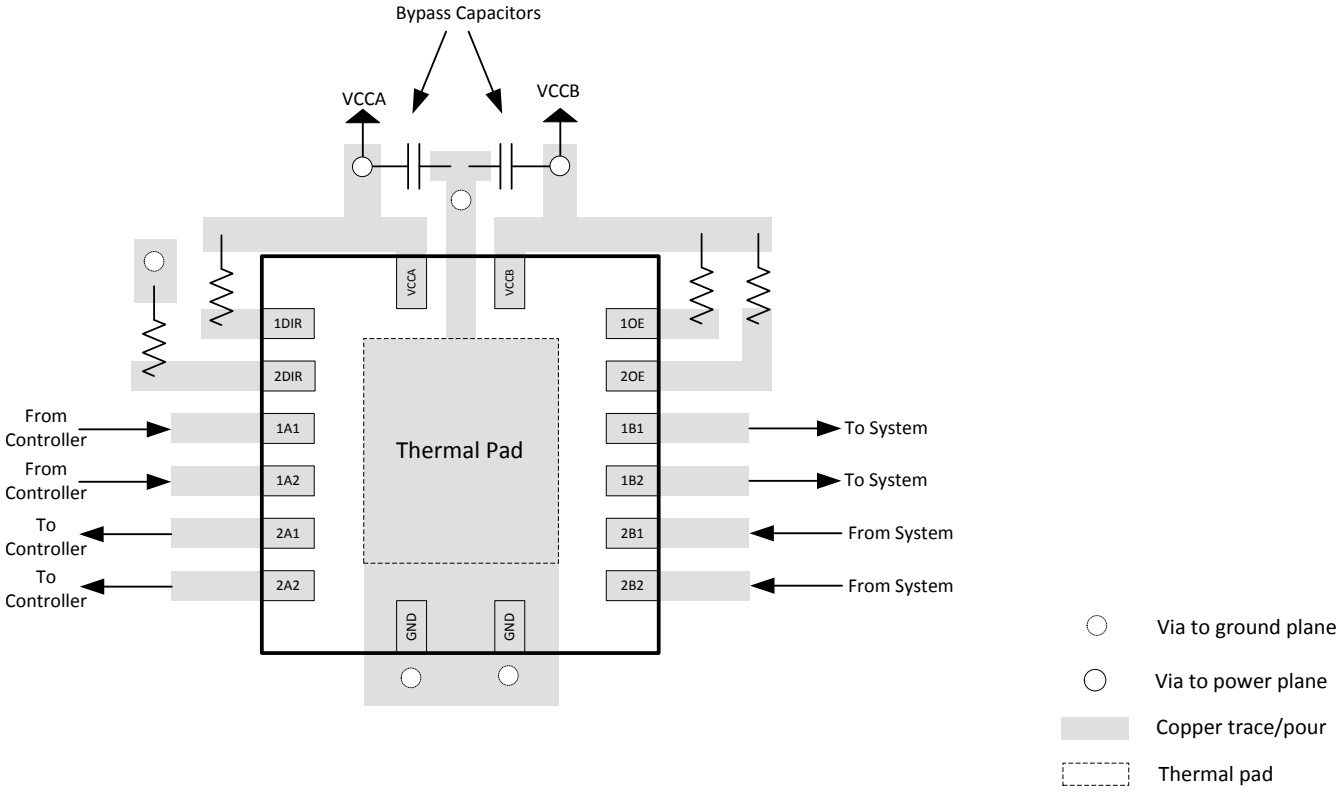

図 8-3. SN74AVC4T245-Q1 RGY Package Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *IC Package Thermal Metrics*
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (March 2016) to Revision C (February 2024)	Page
• 「特長」リストに機能安全のリンクを追加	1
• パッケージ リード サイズを含めるよう「パッケージ情報」表を更新	1
• PW、BQB、DYY パッケージを追加	1

Changes from Revision A (October 2012) to Revision B (October 2015)	Page
• 「アプリケーション」セクションを追加	1
• データシート全体を通して部品番号に -Q1 を追加	1
• データシートに「製品情報」表を追加	1
• データシートから「注文情報」表を削除	1
• Added *Pin Functions* table to the data sheet	3

- Added *ESD Ratings* table to the data sheet 5
- Added *Thermal Information* table to the data sheet..... 6
- Added *Typical Characteristics* section to the data sheet..... 14
- Added 図 5-1 through 図 5-9 to the *セクション 5.12* section 14
- Added all new content from *セクション 8.1* through the end of the data sheet..... 17

Changes from Revision * (November 2009) to Revision A (October 2012) **Page**

- 「特長」に AEC-Q100 の情報を追加..... 1
- 「特長」から、JESD 22、8000V 人体モデル (A114-A)、1000V デバイス帯電モデル (C101) を超える ESD 保護を削除。..... 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AVC4T245QDYYRQ1	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245Q
74AVC4T245QDYYRQ1.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245Q
74AVC4T245QPWRQ1	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245Q
74AVC4T245QPWRQ1.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245Q
74AVC4T245QRGYRQ1	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4T245Q
74AVC4T245QRGYRQ1.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4T245Q
74AVC4T245QRGYRQ1.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4T245Q
74AVC4T245QWBQBRQ1	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245Q
74AVC4T245QWBQBRQ1.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245Q
74AVC4T245RGYRQ1G4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4T245Q
74AVC4T245RGYRQ1G4.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4T245Q
74AVC4T245RGYRQ1G4.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4T245Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74AVC4T245-Q1 :

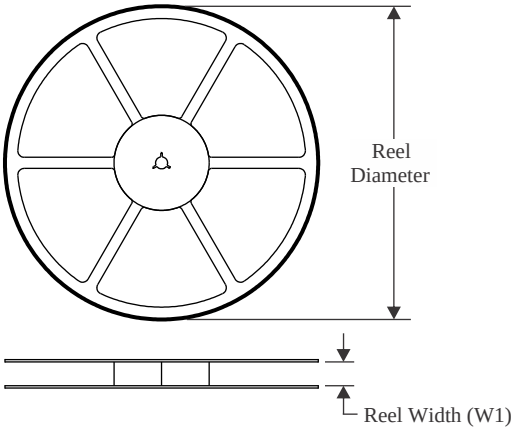
- Catalog : SN74AVC4T245

NOTE: Qualified Version Definitions:

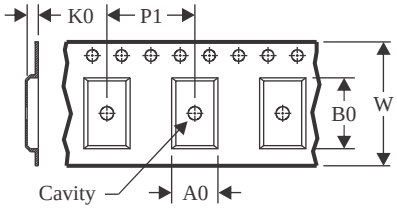
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

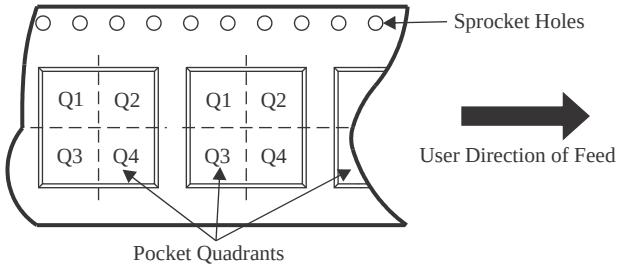


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

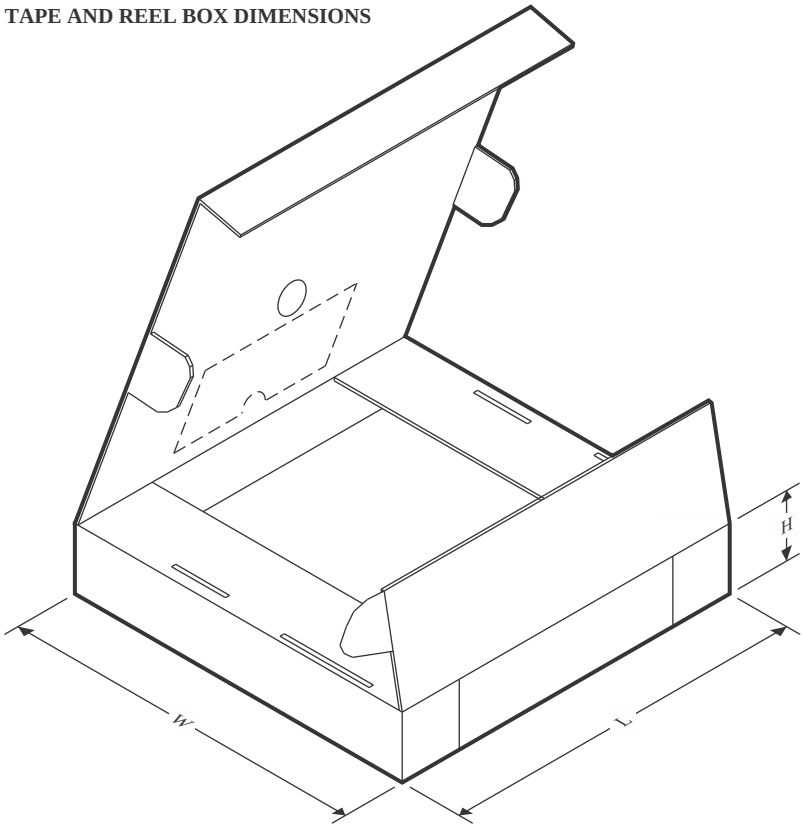
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVC4T245QDYYRQ1	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
74AVC4T245QPWRQ1	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
74AVC4T245QRGYRQ1	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
74AVC4T245QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
74AVC4T245RGYRQ1G4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVC4T245QDYYRQ1	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
74AVC4T245QPWRQ1	TSSOP	PW	16	3000	353.0	353.0	32.0
74AVC4T245QRGYRQ1	VQFN	RGY	16	3000	353.0	353.0	32.0
74AVC4T245QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0
74AVC4T245RGYRQ1G4	VQFN	RGY	16	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

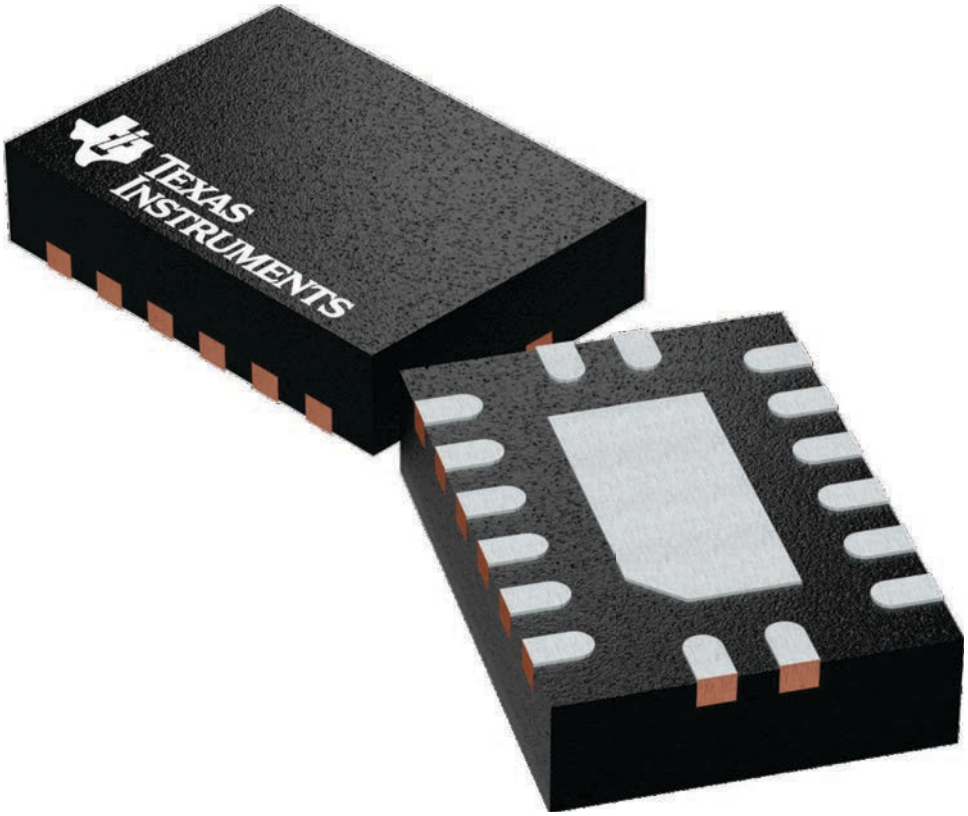
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



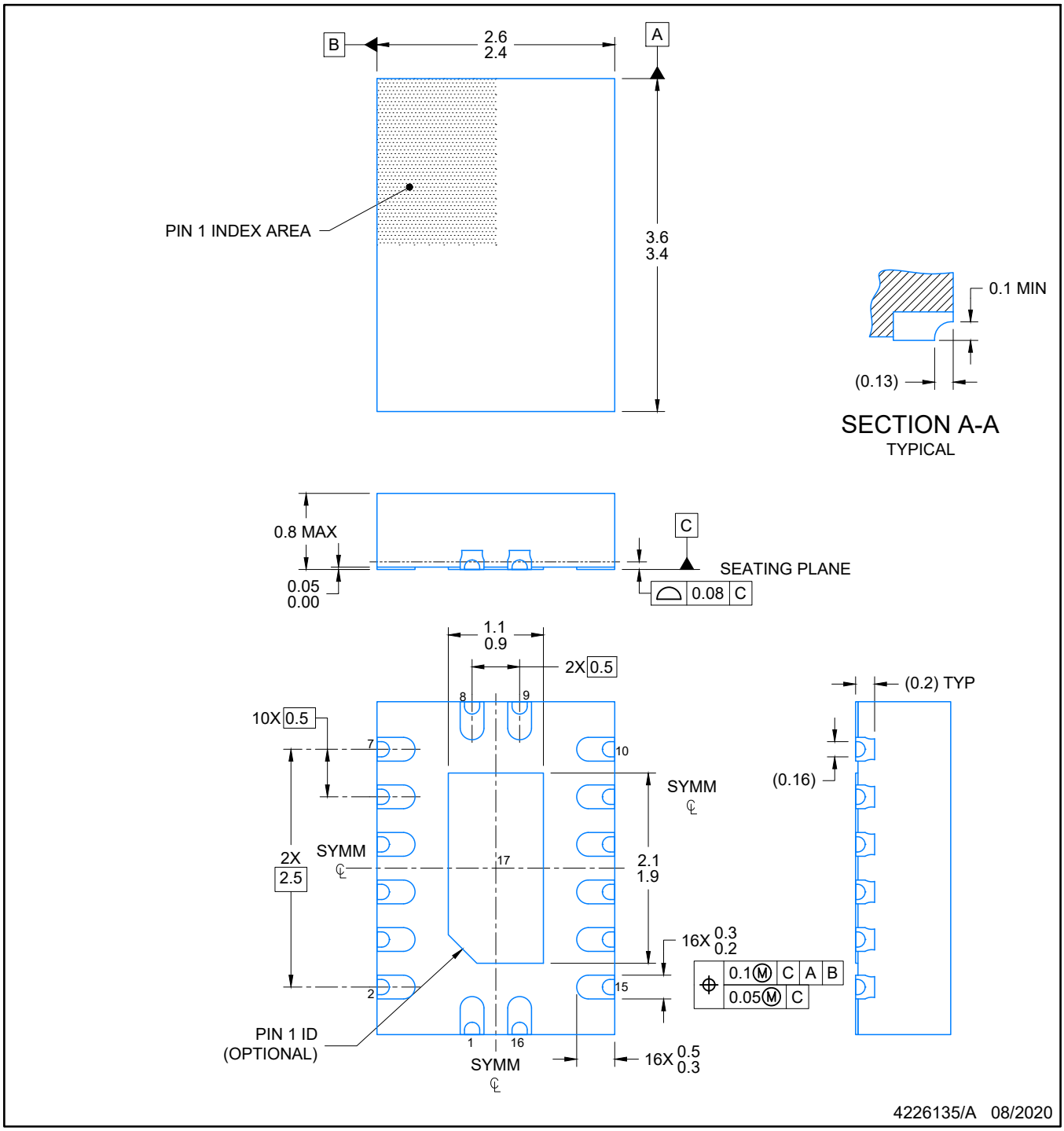
4226161/A

PACKAGE OUTLINE

BQB0016B

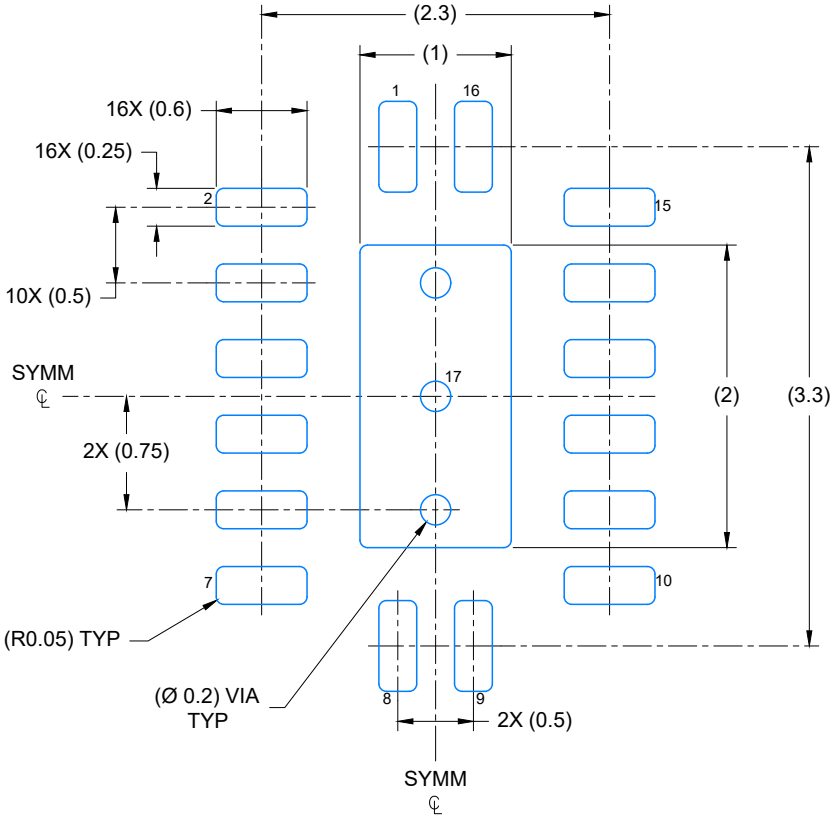
WQFN - 0.8 mm max height

INDSTNAME



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

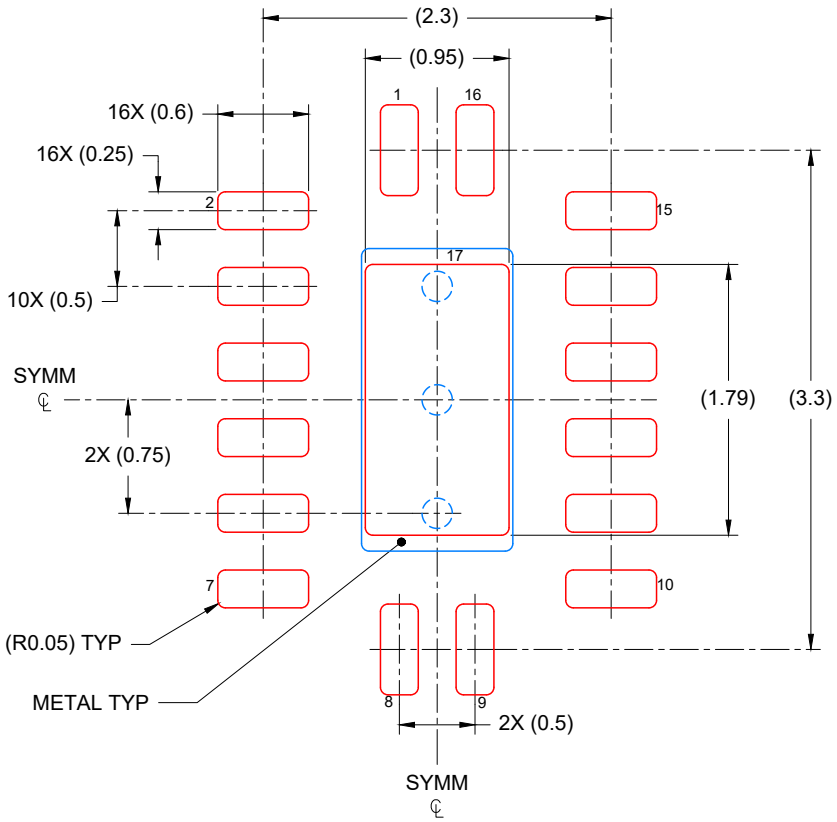


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

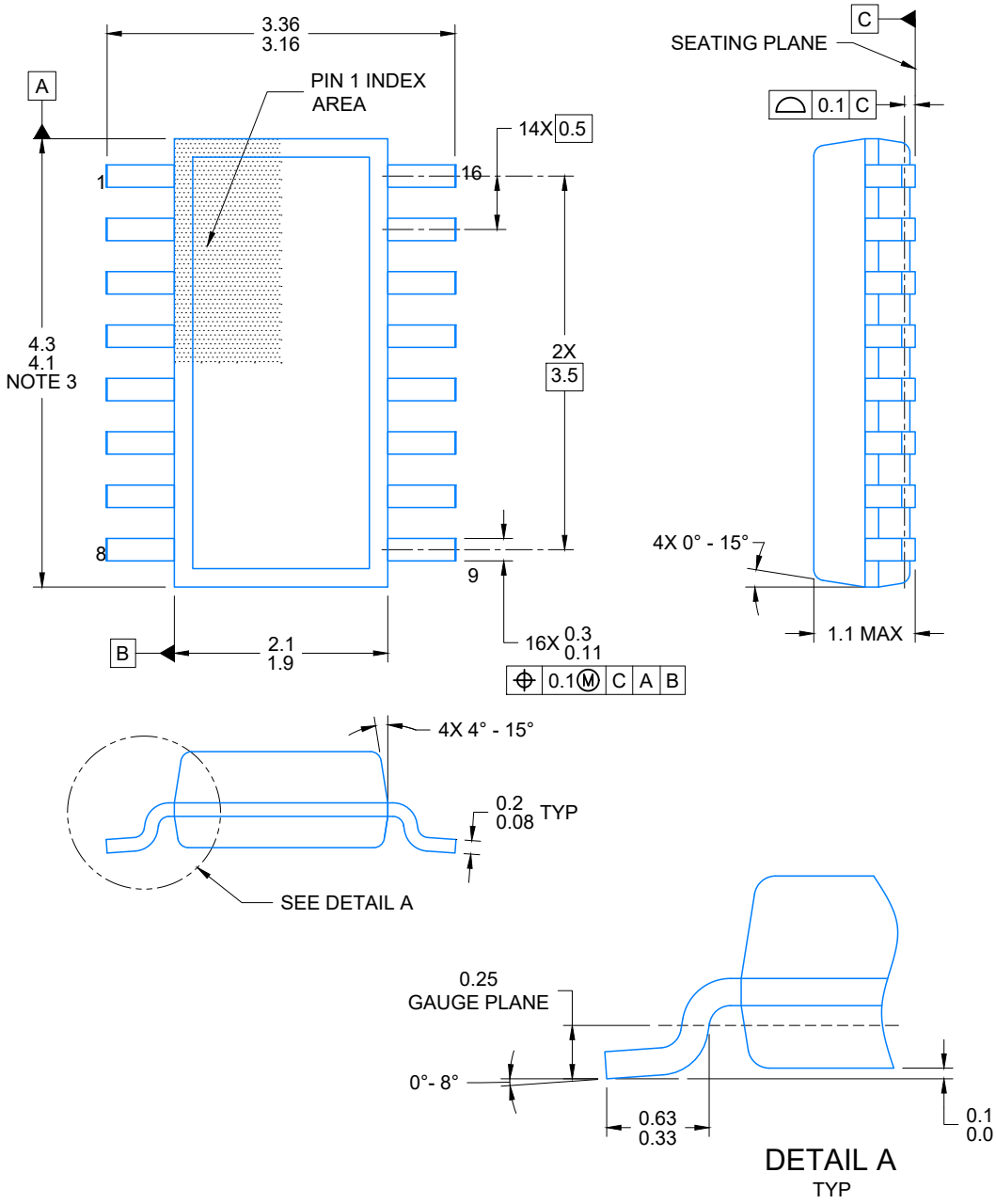
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0016A

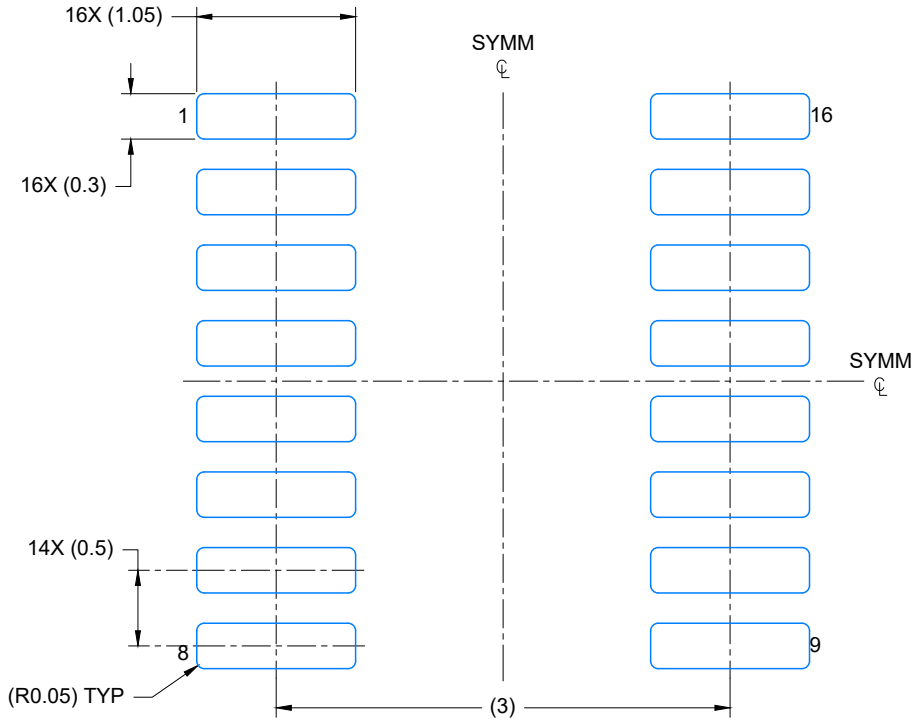
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

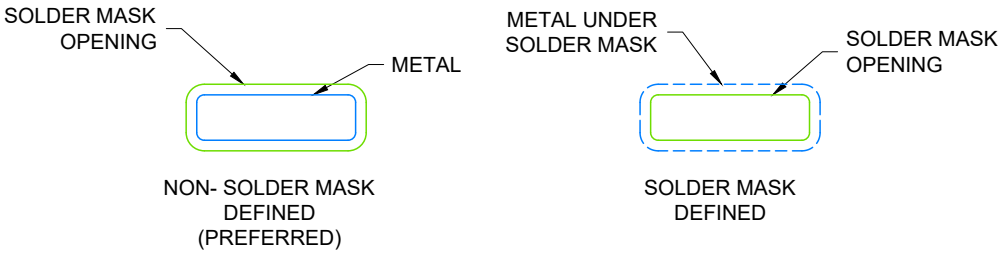


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

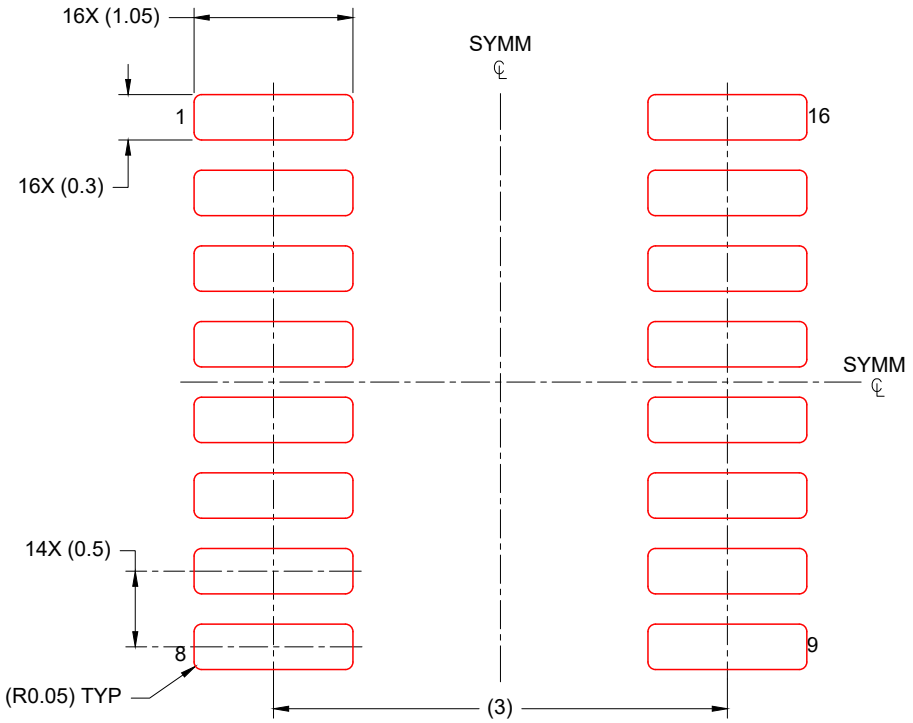
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

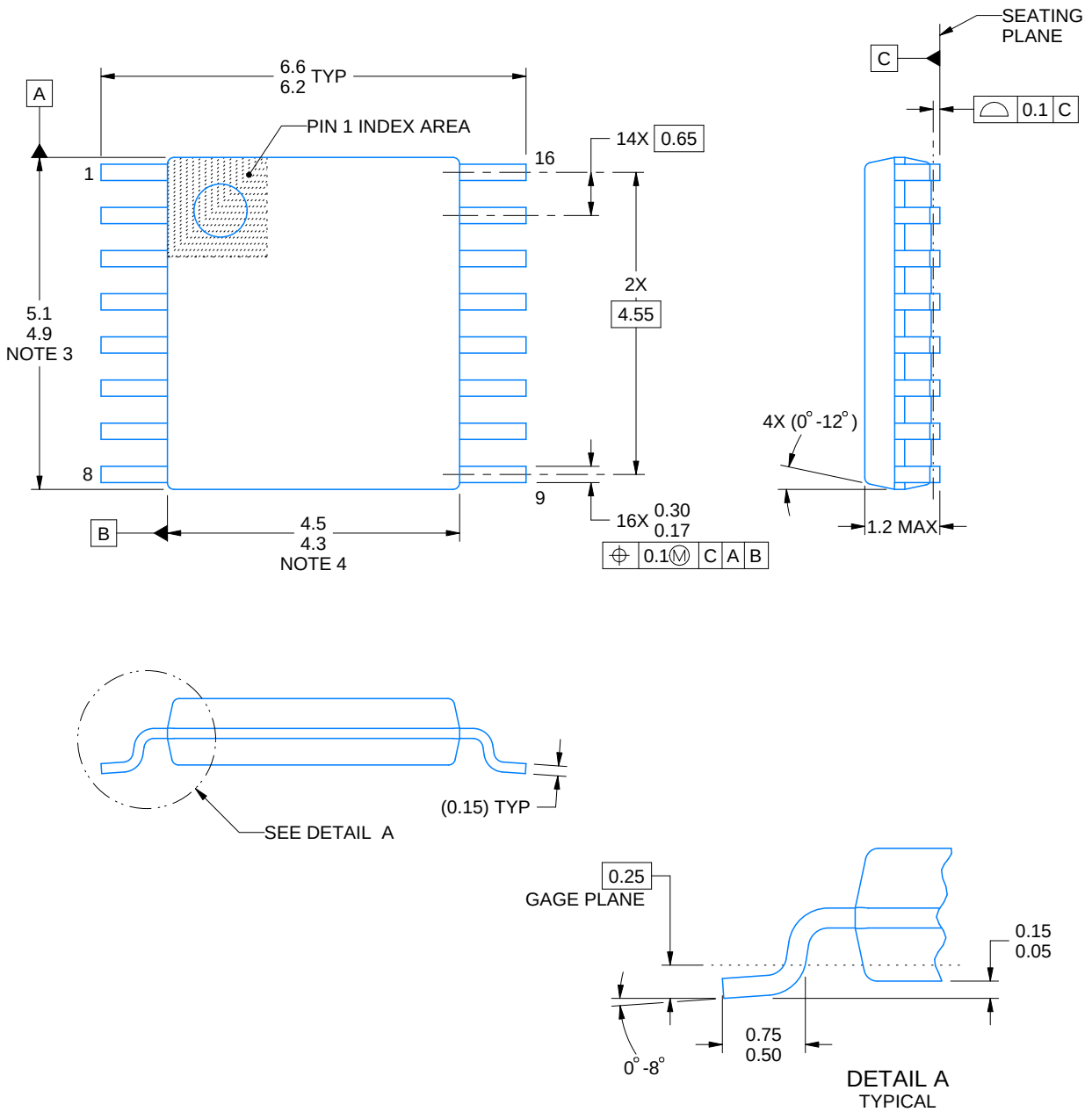
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

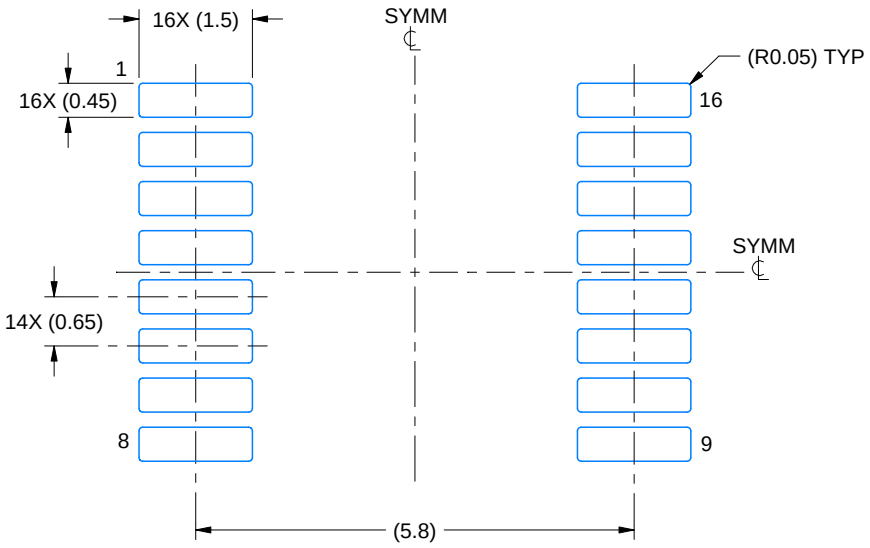
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



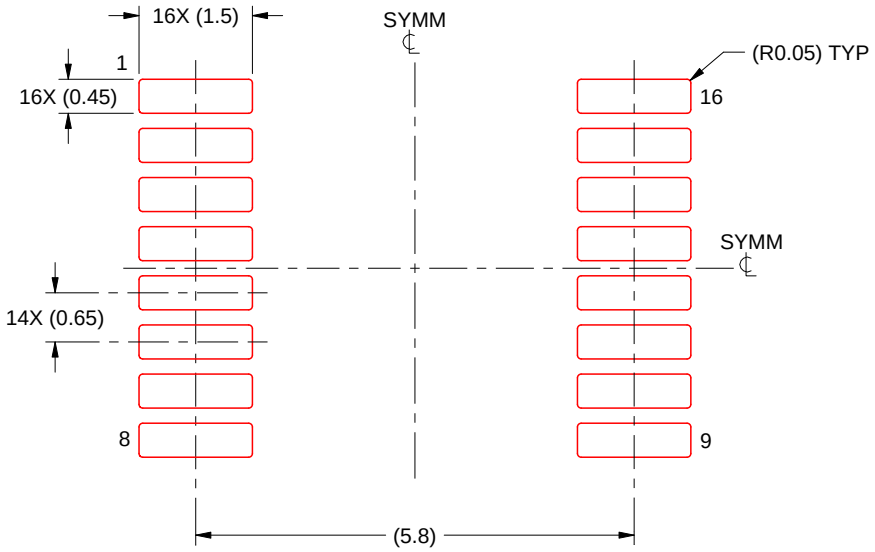
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



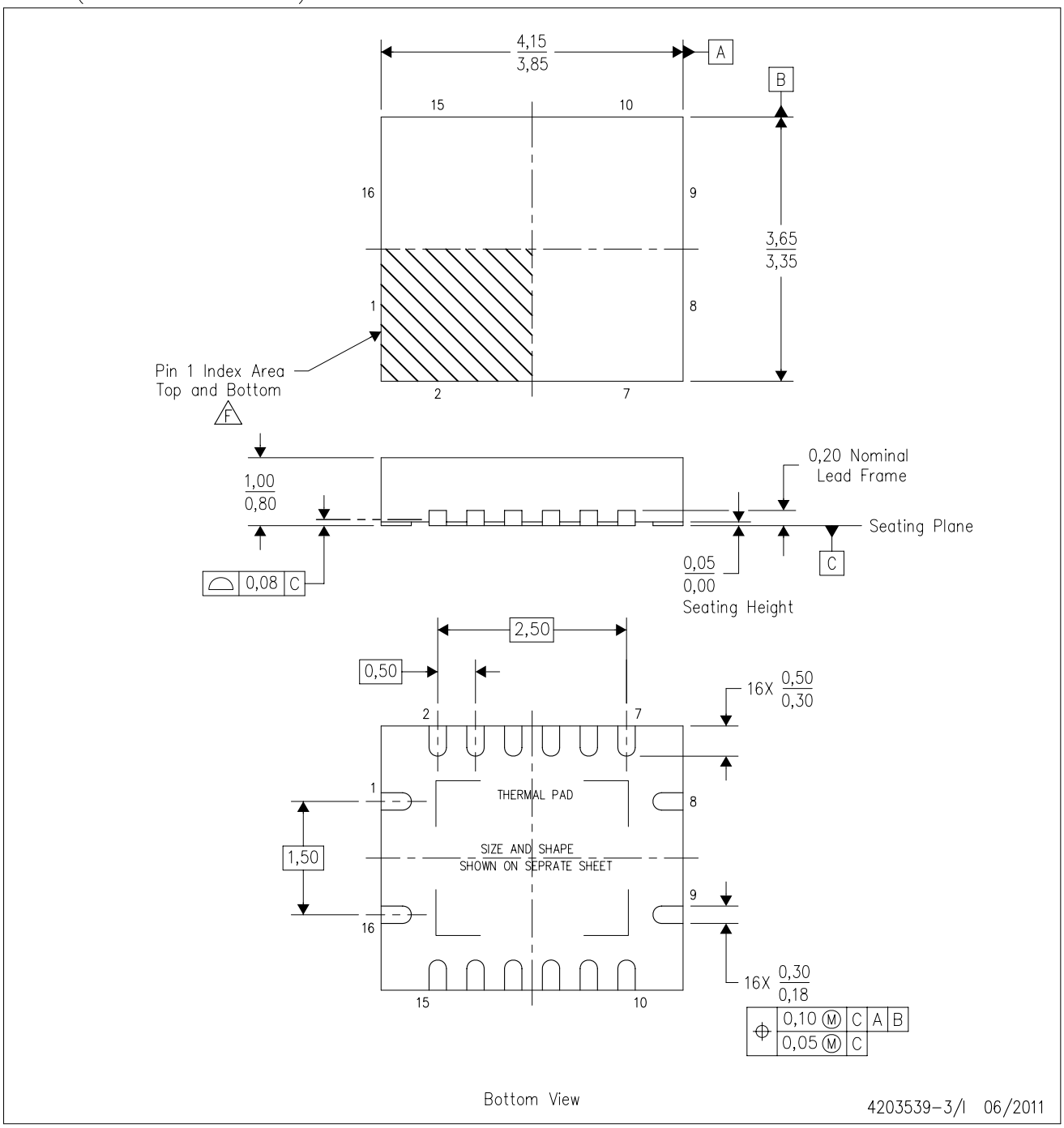
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

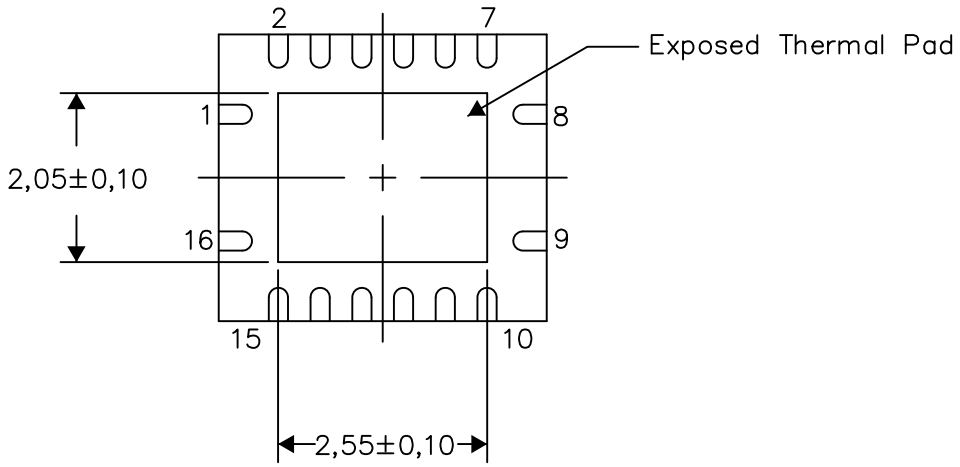
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



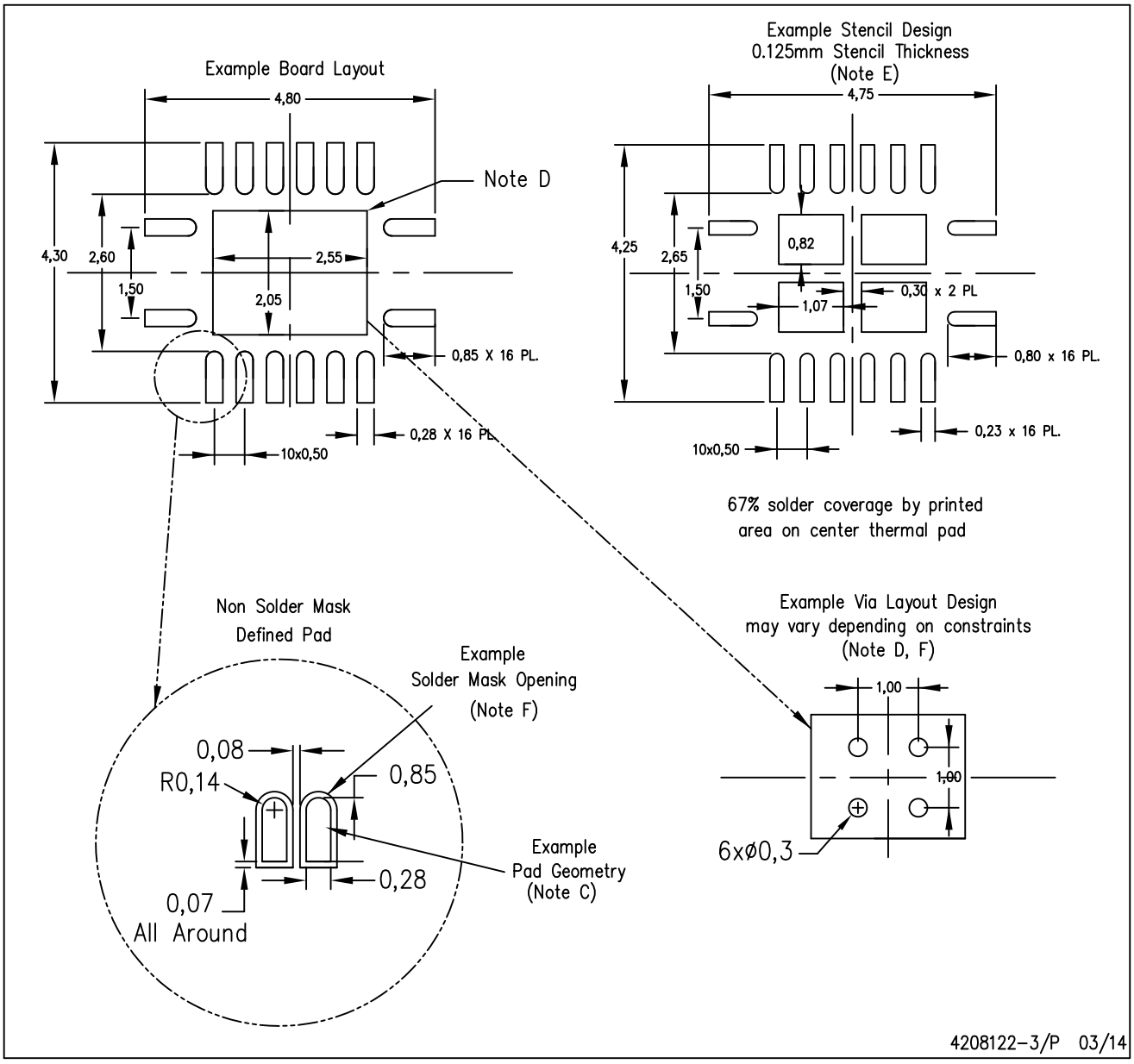
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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最終更新日：2025 年 10 月