

## SN74AXC4T245 4 ビット バストランシーバ、 構成可能電圧変換、3 ステート出力

### 1 特長

- 完全に構成可能なデュアルレール設計により、各ポートは 0.65V~3.6V の範囲の電源電圧で動作可能
- 動作温度範囲: -40°C~+125°C
- 複数の方向制御ピンにより、昇圧と降圧の変換を同時に実行
- グリッチの発生しない電源シーケンシング
- 1.8V から 3.3V への変換時に最高 380Mbps をサポート
- V<sub>CC</sub> 絶縁機能:
  - どちらかの V<sub>CC</sub> 入力が 100mV を下回った場合、すべての I/O 出力がディセーブルされ高インピーダンス状態に移行
- I<sub>off</sub> により部分的パワーダウン モードでの動作をサポート
- AVC ファミリのレベルシフタと互換
- JESD 78, Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護:
  - 8000V 人体モデル
  - 1000V 荷電デバイスモデル

### 2 アプリケーション

- エンタープライズおよび通信
- 産業用
- パーソナル エレクトロニクス
- ワイヤレス インフラ
- ビルオートメーション
- POS システム

### 3 概要

SN74AXC4T245 は、個別に構成可能な 2 つの電源レールを使用した 4 ビット非反転バストランシーバです。本デバイスは、最小 0.65V の V<sub>CCA</sub> と V<sub>CCB</sub> の両方の電源で動作します。A ポートは V<sub>CCA</sub> (0.65V~3.6V の任意の電源電圧を入力できます) に追従するように設計されています。同様に B ポートは V<sub>CCB</sub> (0.65V~3.6V の任意の電源電圧を入力できます) に追従するように設計されています。さらに、SN74AXC4T245 は単一電源システムと互換性があります。

SN74AXC4T245 デバイスは、データバス間の非同期通信用に設計されています。このデバイスは、方向制御入力 (1DIR および 2DIR) のロジックレベルに応じて、A バスから B バスへ、または B バスから A バスへデータを転送します。出力イネーブル入力 (1OE および 2OE) を使用すると、出力をディセーブルにして、バスを実質的に絶縁できます。SN74AXC4T245 デバイスは、制御ピン (xDIR および xOE) が V<sub>CCA</sub> を基準とするように設計されています。

電源オンまたは電源オフ時にレベルシフタ I/O を高インピーダンス状態にするには、プルアップ抵抗を介して OE ピンを V<sub>CCA</sub> に接続します。

このデバイスは、I<sub>off</sub> 電流を使用する部分的パワーダウンアプリケーション用に完全に動作が規定されています。I<sub>off</sub> 保護回路により、電源切断時に入力、出力、複合 I/O は指定の電圧にバイアスされ、それらとの間に過剰な電流が流れることはありません。

V<sub>CC</sub> 絶縁機能により、V<sub>CCA</sub> と V<sub>CCB</sub> のどちらかが 100mV を下回った場合に出力を無効化することで、両方の I/O ポートを高インピーダンス状態にすることができます。

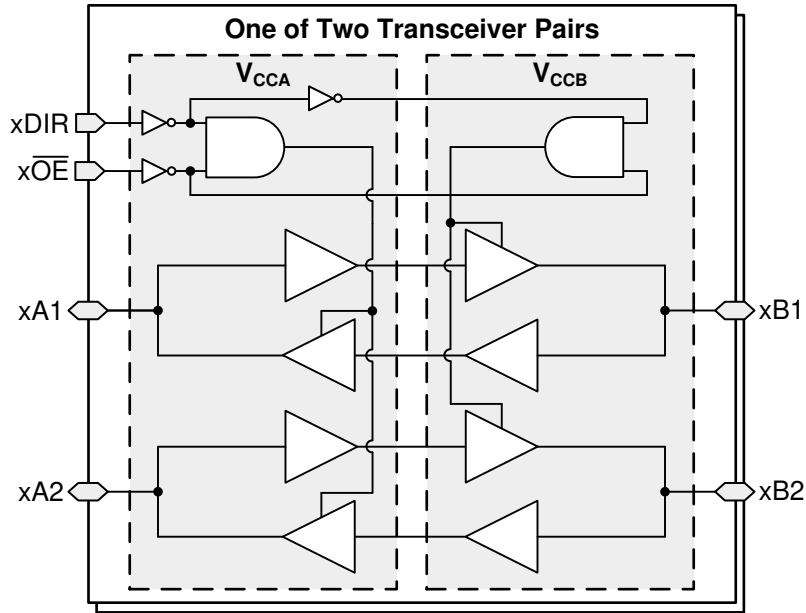
グリッチの発生しない電源シーケンシングにより、堅牢な電源シーケンシング性能が得られると同時に、どちらの電源レールも任意の順序で電源オン/オフできます。

#### パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN74AXC4T245	PW (TSSOP, 16)	5mm × 6.4mm
	BQB (WQFN, 16)	3.5mm × 2.5mm
	RSV (UQFN, 16)	2.6mm × 1.8mm

- 詳細については、[セクション 11](#) を参照してください。
- パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



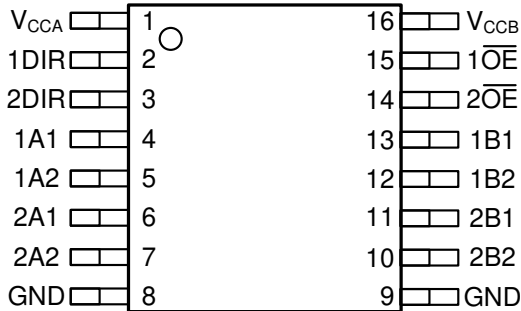


機能ブロック図

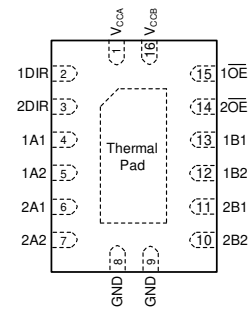
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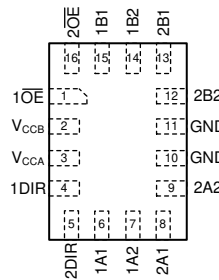
### 4 Pin Configuration and Functions



4-1. PW Package 16-Pin TSSOP (Top View)



4-2. BQB Package 16-Pin WQFN (Transparent Top View)



4-3. RSV Package 16-Pin UQFN (Transparent Top View)

表 4-1. Pin Functions

PIN NAME	NO.			TYPE <sup>(1)</sup>	DESCRIPTION
	PW	RSV	BQB		
1A1	4	6	4	I/O	Input/output 1A1. Referenced to V <sub>CCA</sub> .
1A2	5	7	5	I/O	Input/output 1A2. Referenced to V <sub>CCA</sub> .
1B1	13	15	13	I/O	Input/output 1B1. Referenced to V <sub>CCB</sub> .
1B2	12	14	12	I/O	Input/output 1B2. Referenced to V <sub>CCB</sub> .
1DIR	2	4	2	I	Direction-control input for '1' ports.
1 $\overline{OE}$	15	1	15	I	Tri-state output-mode enable. Pull $\overline{OE}$ high to place '1' outputs in tri-state mode. Referenced to V <sub>CCA</sub> .
2A1	6	8	6	I/O	Input/output 2A1. Referenced to V <sub>CCA</sub> .
2A2	7	9	7	I/O	Input/output 2A2. Referenced to V <sub>CCA</sub> .
2B1	11	13	11	I/O	Input/output 2B1. Referenced to V <sub>CCB</sub> .
2B2	10	12	10	I/O	Input/output 2B2. Referenced to V <sub>CCB</sub> .
2DIR	3	5	3	I	Direction-control input for '2' ports.
2 $\overline{OE}$	14	16	14	I	Tri-state output-mode enable. Pull $\overline{OE}$ high to place '2' outputs in tri-state mode. Referenced to V <sub>CCA</sub> .
GND	8, 9	10, 11	8, 9	—	Ground.
V <sub>CCA</sub>	1	3	1	—	A-port power supply voltage. $0.65V \leq V_{CCA} \leq 3.6V$ .
V <sub>CCB</sub>	16	2	16	—	B-port power supply voltage. $0.65V \leq V_{CCB} \leq 3.6V$ .

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage A		-0.5	4.2	V
V <sub>CCB</sub>	Supply voltage B		-0.5	4.2	V
V <sub>I</sub>	Input Voltage <sup>(2)</sup>	I/O Ports (A Port)	-0.5	4.2	V
		I/O Ports (B Port)	-0.5	4.2	
		Control Inputs	-0.5	4.2	
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A Port	-0.5	4.2	V
		B Port	-0.5	4.2	
V <sub>O</sub>	Voltage applied to any output in the high or low state <sup>(2) (3)</sup>	A Port	-0.5 V <sub>CCA</sub> + 0.2		V
		B Port	-0.5 V <sub>CCB</sub> + 0.2		
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50		mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50		mA
I <sub>O</sub>	Continuous output current		-50	50	mA
	Continuous current through V <sub>CC</sub> or GND		-100	100	mA
T <sub>J</sub>	Junction Temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.2V maximum if the output current rating is observed.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1) 2</sup>

			MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage A		0.65	3.6	V
V <sub>CCB</sub>	Supply voltage B		0.65	3.6	V
V <sub>IH</sub>	High-level input voltage	Data Inputs	V <sub>CCI</sub> = 0.65V - 0.75V	V <sub>CCI</sub> × 0.70	V
			V <sub>CCI</sub> = 0.76V - 1V	V <sub>CCI</sub> × 0.70	
			V <sub>CCI</sub> = 1.1V - 1.95V	V <sub>CCI</sub> × 0.65	
			V <sub>CCI</sub> = 2.3V - 2.7V	1.6	
			V <sub>CCI</sub> = 3V - 3.6V	2	
		Control Inputs(xDIR, xOE) Referenced to V <sub>CCA</sub>	V <sub>CCA</sub> = 0.65V - 0.75V	V <sub>CCA</sub> × 0.70	
			V <sub>CCA</sub> = 0.76V - 1V	V <sub>CCA</sub> × 0.70	
			V <sub>CCA</sub> = 1.1V - 1.95V	V <sub>CCA</sub> × 0.65	
			V <sub>CCA</sub> = 2.3V - 2.7V	1.6	
			V <sub>CCA</sub> = 3V - 3.6V	2	
V <sub>IL</sub>	Low-level input voltage	Data Inputs	V <sub>CCI</sub> = 0.65V - 0.75V	V <sub>CCI</sub> × 0.30	V
			V <sub>CCI</sub> = 0.76V - 1V	V <sub>CCI</sub> × 0.30	
			V <sub>CCI</sub> = 1.1V - 1.95V	V <sub>CCI</sub> × 0.35	
			V <sub>CCI</sub> = 2.3V - 2.7V	0.7	
			V <sub>CCI</sub> = 3V - 3.6V	0.8	
		Control Inputs(xDIR, xOE) Referenced to V <sub>CCA</sub>	V <sub>CCA</sub> = 0.65V - 0.75V	V <sub>CCA</sub> × 0.30	
			V <sub>CCA</sub> = 0.76V - 1V	V <sub>CCA</sub> × 0.30	
			V <sub>CCA</sub> = 1.1V - 1.95V	V <sub>CCA</sub> × 0.35	
			V <sub>CCA</sub> = 2.3V - 2.7V	0.7	
			V <sub>CCA</sub> = 3V - 3.6V	0.8	
V <sub>I</sub>	Input voltage <sup>1</sup>		0	3.6	V
V <sub>O</sub>	Output voltage	Active State	0	V <sub>CCO</sub>	V
		Tri-State	0	3.6	
Δt/Δv <sup>2</sup>	Input transition rate			10	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

(1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(2) All unused inputs of the device must be held at VCC or GND for proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AXC4T245			UNIT
		PW (TSSOP)	RSV (UQFN)	BQB (WQFN)	
		16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	126.9	130.1	73.0	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	49.3	70.3	35.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	74.3	57.4	42.8	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	8.1	4.6	4.6	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	73.4	55.8	42.8	°C/W
R <sub>θJC(bottom)</sub>	Junction-to-case (bottom) thermal resistance	NA	NA	10.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	Operating free-air temperature (T <sub>A</sub> )						UNIT	
				–40°C to 85°C			–40°C to 125°C				
				MIN	TYP <sup>(4)</sup>	MAX	MIN	TYP <sup>(4)</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IH</sub>		0.7V - 3.6V	0.7V - 3.6V	V <sub>CCO</sub> – 0.1		V <sub>CCO</sub> – 0.1		V	
						I <sub>OH</sub> = –100μA	0.65V	0.65V	0.55		0.55
						I <sub>OH</sub> = –50μA	0.76V	0.76V	0.58		0.58
						I <sub>OH</sub> = –200μA	0.85V	0.85V	0.65		0.65
						I <sub>OH</sub> = –3mA	1.1V	1.1V	0.85		0.85
						I <sub>OH</sub> = –6mA	1.4V	1.4V	1.05		1.05
						I <sub>OH</sub> = –8mA	1.65V	1.65V	1.2		1.2
						I <sub>OH</sub> = –9mA	2.3V	2.3V	1.75		1.75
						I <sub>OH</sub> = –12mA	3V	3V	2.3		2.3
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub>		0.7V - 3.6V	0.7V - 3.6V			0.1		V	
						I <sub>OL</sub> = 100μA	0.65V	0.65V	0.1		0.1
						I <sub>OL</sub> = 50μA	0.76V	0.76V	0.18		0.18
						I <sub>OL</sub> = 200μA	0.85V	0.85V	0.2		0.2
						I <sub>OL</sub> = 500μA	1.1V	1.1V	0.25		0.25
						I <sub>OL</sub> = 3mA	1.4V	1.4V	0.35		0.35
						I <sub>OL</sub> = 6mA	1.65V	1.65V	0.45		0.45
						I <sub>OL</sub> = 8mA	2.3V	2.3V	0.55		0.55
						I <sub>OL</sub> = 9mA	3V	3V	0.7		0.7
I <sub>I</sub>	Input leakage current	Control inputs (xDIR, xOE): V <sub>I</sub> = V <sub>CCA</sub> or GND		0.65V- 3.6V	0.65V- 3.6V	–0.5	0.5	–1	1	μA	
		Data Inputs (xAx, xBx): V <sub>I</sub> = V <sub>CCI</sub> or GND		0.65V- 3.6V	0.65V- 3.6V	–4	4	–8	8	μA	
I <sub>off</sub>	Partial power down current	A or B Port		0V	0V - 3.6V	–4	4	–8	8	μA	
		V <sub>I</sub> or V <sub>O</sub> = 0V - 3.6V		0V - 3.6V	0V	–4	4	–8	8		
I <sub>OZ</sub>	Tri-state output current <sup>(3)</sup>	A or B Port V <sub>I</sub> = V <sub>CCI</sub> or GND, V <sub>O</sub> = V <sub>CCO</sub> or GND, OE = V <sub>IH</sub>		3.6V	3.6V	–4	4	–8	8	μA	
I <sub>CCA</sub>	V <sub>CCA</sub> supply current	V <sub>I</sub> = V <sub>CCI</sub> or GND	I <sub>O</sub> = 0	0.65V- 3.6V	0.65V- 3.6V			13		μA	
				0V	3.6V	–2	–12				
				3.6V	0V	8		16			
I <sub>CCB</sub>	V <sub>CCB</sub> supply current	V <sub>I</sub> = V <sub>CCI</sub> or GND	I <sub>O</sub> = 0	0.65V- 3.6V	0.65V- 3.6V			13		μA	
				0V	3.6V	8		16			
				3.6V	0V	–2	–12				
I <sub>CCA</sub> + I <sub>CCB</sub>	Combined supply current	V <sub>I</sub> = V <sub>CCI</sub> or GND	I <sub>O</sub> = 0	0.65V- 3.6V	0.65V- 3.6V			20		40	μA
C <sub>i</sub>	Control input capacitance	V <sub>I</sub> = 3.3V or GND		3.3V	3.3V	4.5		4.5		pF	
C <sub>io</sub>	Data I/O capacitance	OE = V <sub>CCA</sub> , V <sub>O</sub> = 1.65V DC +1MHz -16dBm sine wave		3.3V	3.3V	6.6		6.6		pF	

- (1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
- (2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.
- (3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.
- (4) All typical data is taken at 25°C.

### 5.6 Switching Characteristics, V<sub>CCA</sub> = 0.7V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V <sub>CCB</sub> )														UNIT				
				0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V			3.3 ± 0.3V			
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX		
t <sub>pd</sub>	Propagation delay	A	B	-40°C to 85°C	0.5	155	0.5	108	0.5	76	0.5	40	0.5	37	0.5	40	0.5	67	0.5	185	ns	
				-40°C to 125°C	0.5	155	0.5	108	0.5	76	0.5	40	0.5	37	0.5	40	0.5	67	0.5	185		
		B	A	-40°C to 85°C	0.5	156	0.5	128	0.5	106	0.5	55	0.5	21	0.5	15	0.5	11	0.5	10		ns
				-40°C to 125°C	0.5	156	0.5	128	0.5	106	0.5	55	0.5	21	0.5	15	0.5	11	0.5	10		
t <sub>dis</sub>	Disable time	OE	A	-40°C to 85°C	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	ns	
				-40°C to 125°C	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156	0.5	156		
		OE	B	-40°C to 85°C	0.5	154	0.5	121	0.5	101	0.5	55	0.5	54	0.5	56	0.5	65	0.5	125		ns
				-40°C to 125°C	0.5	154	0.5	121	0.5	101	0.5	55	0.5	54	0.5	56	0.5	65	0.5	125		
t <sub>en</sub>	Enable time	OE	A	-40°C to 85°C	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	ns	
				-40°C to 125°C	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238	0.5	238		
		OE	B	-40°C to 85°C	0.5	286	0.5	194	0.5	146	0.5	94	0.5	76	0.5	70	0.5	69	0.5	146		ns
				-40°C to 125°C	0.5	286	0.5	194	0.5	146	0.5	94	0.5	76	0.5	70	0.5	69	0.5	146		

### 5.7 Switching Characteristics, V<sub>CCA</sub> = 0.8V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V <sub>CCB</sub> )														UNIT				
				0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V			3.3 ± 0.3V			
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX		
t <sub>pd</sub>	Propagation delay	A	B	-40°C to 85°C	0.5	128	0.5	88	0.5	63	0.5	29	0.5	24	0.5	23	0.5	24	0.5	34	ns	
				-40°C to 125°C	0.5	128	0.5	88	0.5	63	0.5	29	0.5	24	0.5	23	0.5	24	0.5	34		
		B	A	-40°C to 85°C	0.5	108	0.5	88	0.5	70	0.5	38	0.5	21	0.5	15	0.5	11	0.5	10		ns
				-40°C to 125°C	0.5	108	0.5	88	0.5	70	0.5	38	0.5	21	0.5	15	0.5	11	0.5	10		
t <sub>dis</sub>	Disable time	OE	A	-40°C to 85°C	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	ns	
				-40°C to 125°C	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103	0.5	103		
		OE	B	-40°C to 85°C	0.5	143	0.5	110	0.5	90	0.5	42	0.5	36	0.5	36	0.5	37	0.5	47		ns
				-40°C to 125°C	0.5	143	0.5	110	0.5	90	0.5	42	0.5	36	0.5	36	0.5	37	0.5	47		



## 5.7 Switching Characteristics, $V_{CCA} = 0.8V$ (続き)

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )														UNIT			
				0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V			3.3 ± 0.3V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	
$t_{en}$	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	ns		
				-40°C to 125°C	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143	0.5	143			
		$\overline{OE}$	B	-40°C to 85°C	0.5	243	0.5	172	0.5	129	0.5	79	0.5	60	0.5	54	0.5	48		0.5	53
				-40°C to 125°C	0.5	243	0.5	172	0.5	129	0.5	79	0.5	60	0.5	54	0.5	48		0.5	53

## 5.8 Switching Characteristics, $V_{CCA} = 0.9V$

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )														UNIT			
				0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V			3.3 ± 0.3V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	106	0.5	70	0.5	53	0.5	24	0.5	18	0.5	17	0.5	16	ns		
				-40°C to 125°C	0.5	106	0.5	70	0.5	53	0.5	24	0.5	18	0.5	17	0.5	16		0.5	19
		B	A	-40°C to 85°C	0.5	76	0.5	63	0.5	53	0.5	27	0.5	18	0.5	13	0.5	10		0.5	9
				-40°C to 125°C	0.5	76	0.5	63	0.5	53	0.5	27	0.5	18	0.5	13	0.5	10		0.5	9
$t_{dis}$	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	ns		
				-40°C to 125°C	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81	0.5	81			
		$\overline{OE}$	B	-40°C to 85°C	0.5	138	0.5	105	0.5	84	0.5	37	0.5	30	0.5	28	0.5	26		0.5	30
				-40°C to 125°C	0.5	138	0.5	105	0.5	84	0.5	37	0.5	30	0.5	28	0.5	26		0.5	30
$t_{en}$	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	ns		
				-40°C to 125°C	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95	0.5	95			
		$\overline{OE}$	B	-40°C to 85°C	0.5	222	0.5	148	0.5	116	0.5	71	0.5	52	0.5	46	0.5	39		0.5	39
				-40°C to 125°C	0.5	222	0.5	148	0.5	116	0.5	71	0.5	52	0.5	46	0.5	39		0.5	39

## 5.9 Switching Characteristics, $V_{CCA} = 1.2V$

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT					
				0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V			2.5 ± 0.2V		3.3 ± 0.3V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	55	0.5	37	0.5	27	0.5	15	0.5	11	0.5	10	0.5	8	0.5	9	ns
				-40°C to 125°C	0.5	55	0.5	37	0.5	27	0.5	15	0.5	11	0.5	10	0.5	8	0.5	9	
		B	A	-40°C to 85°C	0.5	41	0.5	29	0.5	24	0.5	15	0.5	10	0.5	9	0.5	7	0.5	6	
				-40°C to 125°C	0.5	41	0.5	29	0.5	24	0.5	15	0.5	10	0.5	9	0.5	7	0.5	6	
$t_{dis}$	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	ns
				-40°C to 125°C	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	
		$\overline{OE}$	B	-40°C to 85°C	0.5	132	0.5	99	0.5	79	0.5	31	0.5	24	0.5	21	0.5	18	0.5	18	
				-40°C to 125°C	0.5	132	0.5	99	0.5	79	0.5	31	0.5	24	0.5	21	0.5	18	0.5	18	
$t_{en}$	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	ns
				-40°C to 125°C	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	0.5	45	
		$\overline{OE}$	B	-40°C to 85°C	0.5	164	0.5	108	0.5	79	0.5	58	0.5	41	0.5	35	0.5	27	0.5	24	
				-40°C to 125°C	0.5	164	0.5	108	0.5	79	0.5	58	0.5	41	0.5	35	0.5	27	0.5	24	

## 5.10 Switching Characteristics, $V_{CCA} = 1.5V$

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )												UNIT					
				0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V			2.5 ± 0.2V		3.3 ± 0.3V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	21	0.5	21	0.5	18	0.5	11	0.5	9	0.5	8	0.5	7	0.5	6	ns
				-40°C to 125°C	0.5	21	0.5	21	0.5	18	0.5	11	0.5	9	0.5	8	0.5	7	0.5	6	
		B	A	-40°C to 85°C	0.5	37	0.5	24	0.5	18	0.5	11	0.5	9	0.5	8	0.5	5	0.5	5	
				-40°C to 125°C	0.5	37	0.5	24	0.5	18	0.5	11	0.5	9	0.5	8	0.5	5	0.5	5	
$t_{dis}$	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	ns
				-40°C to 125°C	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	0.5	21	
		$\overline{OE}$	B	-40°C to 85°C	0.5	131	0.5	97	0.5	77	0.5	29	0.5	21	0.5	19	0.5	15	0.5	15	
				-40°C to 125°C	0.5	131	0.5	97	0.5	77	0.5	29	0.5	21	0.5	19	0.5	15	0.5	15	

### 5.10 Switching Characteristics, $V_{CCA} = 1.5V$ (続き)

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )														UNIT			
				0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V			3.3 ± 0.3V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	
$t_{en}$	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	ns		
				-40°C to 125°C	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26			
		$\overline{OE}$	B	-40°C to 85°C	0.5	109	0.5	84	0.5	68	0.5	47	0.5	35	0.5	29	0.5	22		0.5	20
				-40°C to 125°C	0.5	109	0.5	84	0.5	68	0.5	47	0.5	35	0.5	29	0.5	22		0.5	20

### 5.11 Switching Characteristics, $V_{CCA} = 1.8V$

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )														UNIT			
				0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V			3.3 ± 0.3V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	
$t_{pd}$	Propagation delay	A	B	-40°C to 85°C	0.5	15	0.5	15	0.5	13	0.5	9	0.5	8	0.5	7	0.5	6	ns		
				-40°C to 125°C	0.5	15	0.5	15	0.5	13	0.5	9	0.5	8	0.5	7	0.5	6		0.5	6
		B	A	-40°C to 85°C	0.5	40	0.5	23	0.5	17	0.5	10	0.5	8	0.5	7	0.5	5		0.5	4
				-40°C to 125°C	0.5	40	0.5	23	0.5	17	0.5	10	0.5	8	0.5	7	0.5	5		0.5	4
$t_{dis}$	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	ns		
				-40°C to 125°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18			
		$\overline{OE}$	B	-40°C to 85°C	0.5	130	0.5	96	0.5	76	0.5	28	0.5	21	0.5	18	0.5	15		0.5	14
				-40°C to 125°C	0.5	130	0.5	96	0.5	76	0.5	28	0.5	21	0.5	18	0.5	15		0.5	14
$t_{en}$	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	ns		
				-40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20			
		$\overline{OE}$	B	-40°C to 85°C	0.5	102	0.5	75	0.5	62	0.5	41	0.5	32	0.5	27	0.5	20		0.5	18
				-40°C to 125°C	0.5	102	0.5	75	0.5	62	0.5	41	0.5	32	0.5	27	0.5	20		0.5	18

### 5.12 Switching Characteristics, V<sub>CCA</sub> = 2.5V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V <sub>CCB</sub> )														UNIT				
				0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V			3.3 ± 0.3V			
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX		
t <sub>pd</sub>	Propagation delay	A	B	-40°C to 85°C	0.5	11	0.5	11	0.5	10	0.5	7	0.5	5	0.5	5	0.5	5	0.5	5	ns	
				-40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	7	0.5	5	0.5	5	0.5	5	0.5	5		
		B	A	-40°C to 85°C	0.5	67	0.5	24	0.5	16	0.5	8	0.5	7	0.5	6	0.5	5	0.5	4		ns
				-40°C to 125°C	0.5	67	0.5	24	0.5	16	0.5	8	0.5	7	0.5	6	0.5	5	0.5	4		
t <sub>dis</sub>	Disable time	OE	A	-40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	ns	
				-40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13		
		OE	B	-40°C to 85°C	0.5	128	0.5	95	0.5	76	0.5	27	0.5	20	0.5	17	0.5	13	0.5	13		ns
				-40°C to 125°C	0.5	128	0.5	95	0.5	76	0.5	27	0.5	20	0.5	17	0.5	13	0.5	13		
t <sub>en</sub>	Enable time	OE	A	-40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	ns	
				-40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13		
		OE	B	-40°C to 85°C	0.5	120	0.5	70	0.5	56	0.5	36	0.5	26	0.5	22	0.5	18	0.5	16		ns
				-40°C to 125°C	0.5	120	0.5	70	0.5	56	0.5	36	0.5	26	0.5	22	0.5	18	0.5	16		

### 5.13 Switching Characteristics, V<sub>CCA</sub> = 3.3V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER	FROM	TO	Test Conditions	B-Port Supply Voltage (V <sub>CCB</sub> )														UNIT				
				0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V			3.3 ± 0.3V			
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX		
t <sub>pd</sub>	Propagation delay	A	B	-40°C to 85°C	0.5	10	0.5	10	0.5	9	0.5	6	0.5	5	0.5	4	0.5	4	0.5	4	ns	
				-40°C to 125°C	0.5	10	0.5	10	0.5	9	0.5	6	0.5	5	0.5	4	0.5	4	0.5	4		
		B	A	-40°C to 85°C	0.5	185	0.5	34	0.5	19	0.5	9	0.5	6	0.5	6	0.5	5	0.5	4		ns
				-40°C to 125°C	0.5	185	0.5	34	0.5	19	0.5	9	0.5	6	0.5	6	0.5	5	0.5	4		
t <sub>dis</sub>	Disable time	OE	A	-40°C to 85°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	ns	
				-40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12		
		OE	B	-40°C to 85°C	0.5	141	0.5	95	0.5	75	0.5	27	0.5	19	0.5	17	0.5	13	0.5	12		ns
				-40°C to 125°C	0.5	141	0.5	95	0.5	75	0.5	27	0.5	19	0.5	17	0.5	13	0.5	12		

### 5.13 Switching Characteristics, $V_{CCA} = 3.3V$ (続き)

See [Figure 1](#) and [Table 1](#) for test circuit and loading. See [Figure 2](#), [Figure 3](#), and [Figure 4](#) for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage ( $V_{CCB}$ )														UNIT		
					0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V			3.3 ± 0.3V	
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX
$t_{en}$	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	ns		
				-40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11			
		$\overline{OE}$	B	-40°C to 85°C	0.5	189	0.5	82	0.5	59	0.5	35	0.5	24	0.5	20	0.5	16		0.5	14
				-40°C to 125°C	0.5	189	0.5	82	0.5	59	0.5	35	0.5	24	0.5	20	0.5	16		0.5	14

5.14 Operating Characteristics: T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	UNIT
C <sub>pdA</sub>	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1MHz, tr = tf = 1ns	0.7V	0.7V		2.2		pF
			0.8V	0.8V		2.1		
			0.9V	0.9V		2.1		
			1.2V	1.2V		2.1		
			1.5V	1.5V		2.0		
			1.8V	1.8V		2.0		
			2.5V	2.5V		2.1		
			3.3V	3.3V		2.3		
	Power Dissipation Capacitance per transceiver (A to B: outputs disabled)	CL = 0, RL = Open f = 1MHz, tr = tf = 1ns	0.7V	0.7V		1.5		pF
			0.8V	0.8V		1.5		
			0.9V	0.9V		1.5		
			1.2V	1.2V		1.4		
			1.5V	1.5V		1.4		
			1.8V	1.8V		1.4		
			2.5V	2.5V		1.4		
			3.3V	3.3V		1.6		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1MHz, tr = tf = 1ns	0.7V	0.7V		12.1		pF
			0.8V	0.8V		12.1		
			0.9V	0.9V		12.1		
			1.2V	1.2V		12.4		
			1.5V	1.5V		13.0		
			1.8V	1.8V		14.2		
			2.5V	2.5V		17.4		
			3.3V	3.3V		20.1		
	Power Dissipation Capacitance per transceiver (B to A: outputs disabled)	CL = 0, RL = Open f = 1MHz, tr = tf = 1ns	0.7V	0.7V		1.1		pF
			0.8V	0.8V		1.1		
			0.9V	0.9V		1.1		
			1.2V	1.2V		1.1		
1.5V			1.5V		1.1			
1.8V			1.8V		1.1			
2.5V			2.5V		1.1			
3.3V			3.3V		1.1			

5.14 Operating Characteristics: T<sub>A</sub> = 25°C (続き)

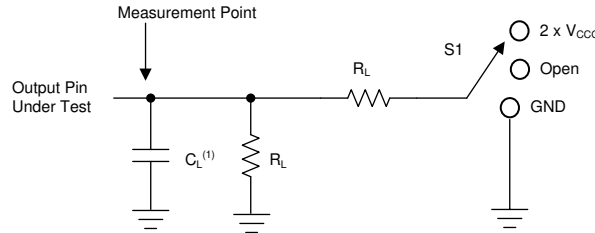
PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	UNIT
C <sub>pdB</sub>	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1MHz, tr = tf = 1ns	0.7V	0.7V		12.1		pF
			0.8V	0.8V		12.1		
			0.9V	0.9V		12.1		
			1.2V	1.2V		12.4		
			1.5V	1.5V		12.9		
			1.8V	1.8V		14.1		
			2.5V	2.5V		17.2		
			3.3V	3.3V		20.1		
	Power Dissipation Capacitance per transceiver (A to B: outputs disabled)	CL = 0, RL = Open f = 1MHz, tr = tf = 1ns	0.7V	0.7V		1.1		pF
			0.8V	0.8V		1.1		
			0.9V	0.9V		1.1		
			1.2V	1.2V		1.1		
			1.5V	1.5V		1.1		
			1.8V	1.8V		1.1		
			2.5V	2.5V		1.1		
			3.3V	3.3V		1.1		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1MHz, tr = tf = 1ns	0.7V	0.7V		1.2		pF
			0.8V	0.8V		1.8		
			0.9V	0.9V		1.8		
			1.2V	1.2V		1.7		
			1.5V	1.5V		1.7		
			1.8V	1.8V		1.7		
			2.5V	2.5V		2		
			3.3V	3.3V		2.5		
	Power Dissipation Capacitance per transceiver (B to A: outputs disabled)	CL = 0, RL = Open f = 1MHz, tr = tf = 1ns	0.7V	0.7V		1.1		pF
			0.8V	0.8V		1.8		
			0.9V	0.9V		1.8		
			1.2V	1.2V		1.7		
1.5V			1.5V		1.7			
1.8V			1.8V		1.7			
2.5V			2.5V		2			
3.3V			3.3V		2.1			

## 6 Parameter Measurement Information

### 6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- $f = 1\text{MHz}$
- $Z_O = 50\Omega$
- $dv/dt \leq 1\text{ns/V}$

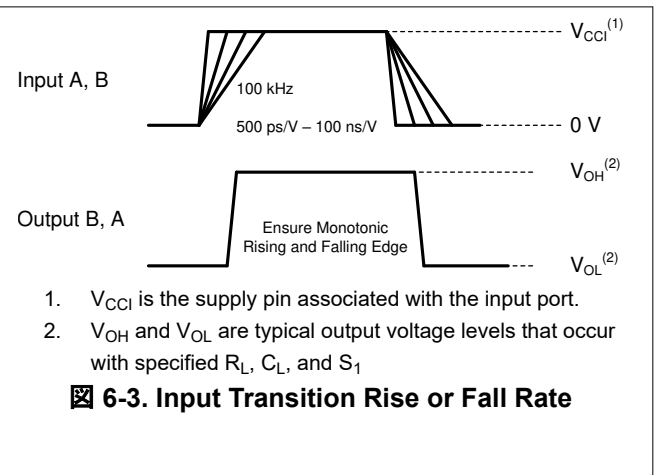
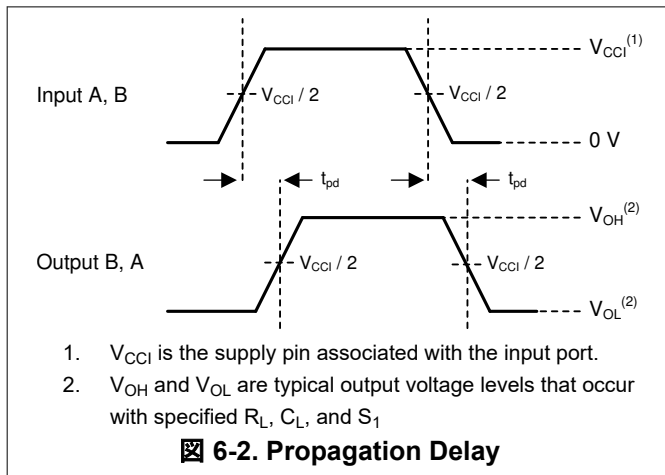


A.  $C_L$  includes probe and jig capacitance.

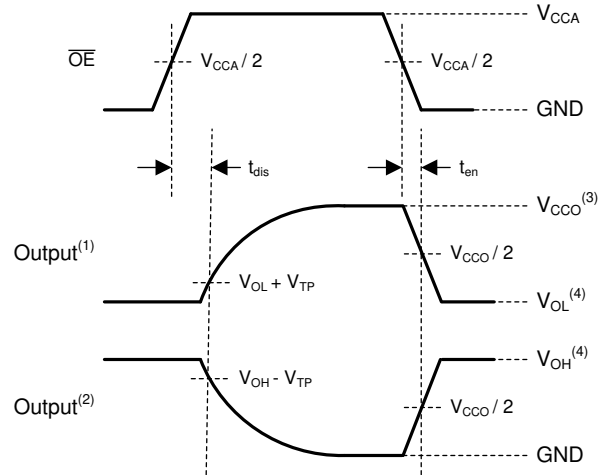
图 6-1. Load Circuit

表 6-1. Load Circuit Conditions

Parameter	$V_{CCO}$	$R_L$	$C_L$	$S_1$	$V_{TP}$
$\Delta t/\Delta v$ Input transition rise or fall rate	0.65V – 3.6V	1M $\Omega$	15pF	Open	N/A
$t_{pd}$ Propagation (delay) time	1.1V – 3.6V	2k $\Omega$	15pF	Open	N/A
	0.65V – 0.95V	20k $\Omega$	15pF	Open	N/A
$t_{en}, t_{dis}$ Enable time, disable time	3V – 3.6V	2k $\Omega$	15pF	$2 \times V_{CCO}$	0.3V
	1.65V – 2.7V	2k $\Omega$	15pF	$2 \times V_{CCO}$	0.15V
	1.1V – 1.6V	2k $\Omega$	15pF	$2 \times V_{CCO}$	0.1V
	0.65V – 0.95V	20k $\Omega$	15pF	$2 \times V_{CCO}$	0.1V
$t_{en}, t_{dis}$ Enable time, disable time	3V – 3.6V	2k $\Omega$	15pF	GND	0.3V
	1.65V – 2.7V	2k $\Omega$	15pF	GND	0.15V
	1.1V – 1.6V	2k $\Omega$	15pF	GND	0.1V
	0.65V – 0.95V	20k $\Omega$	15pF	GND	0.1V







- A. Output waveform on the condition that input is driven to a valid Logic Low.
- B. Output waveform on the condition that input is driven to a valid Logic High.
- C.  $V_{CCO}$  is the supply pin associated with the output port.
- D.  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels with specified  $R_L$ ,  $C_L$ , and  $S_1$ .

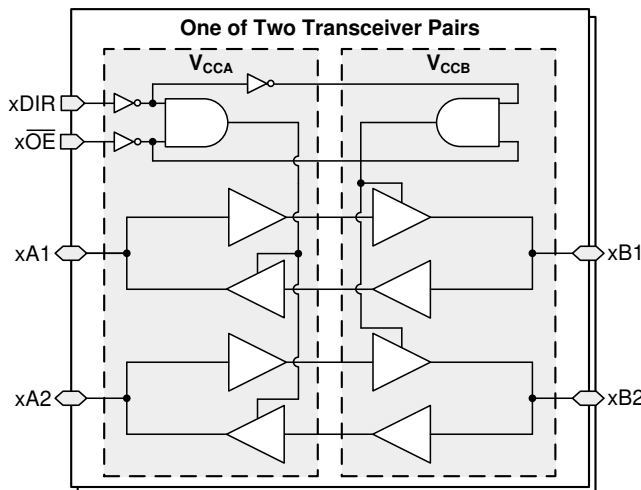
**图 6-4. Enable Time And Disable Time**

## 7 Detailed Description

### 7.1 Overview

The SN74AXC4T245 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (1DIR, 2DIR, 1  $\overline{\text{OE}}$ , and 2  $\overline{\text{OE}}$ ) are referenced to  $V_{\text{CCA}}$  logic levels, and Bx pins are referenced to  $V_{\text{CCB}}$  logic levels. The A port is able to accept I/O voltages ranging from 0.65V to 3.6V, while the B port can accept I/O voltages from 0.65V to 3.6V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when  $\overline{\text{OE}}$  is set to low. When  $\overline{\text{OE}}$  is set to high, both Ax and Bx pins are in the high-impedance state. See [Device Functional Modes](#) for a summary of the operation of the control logic.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t/\Delta v$  in [Recommended Operating Conditions](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

#### 7.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

#### 7.3.3 Partial Power Down ( $I_{\text{off}}$ )

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by  $I_{\text{off}}$  in the [Electrical Characteristics](#).

#### 7.3.4 $V_{\text{CC}}$ Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is  $<100\text{mV}$ .

### 7.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Recommended Operating Conditions](#).

### 7.3.6 Glitch-free Power Supply Sequencing

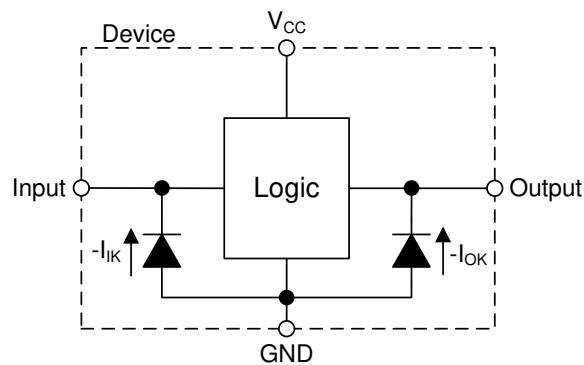
Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral. For more information regarding the power up glitch performance of the AXC family of level translators, see the [Glitch Free Power Sequencing With AXC Level Translators](#) application report

### 7.3.7 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in [Figure 7-1](#).

注意

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output**

### 7.3.8 Fully Configurable Dual-Rail Design

Both the  $V_{CCA}$  and  $V_{CCB}$  pins can be supplied at any voltage from 0.65V to 3.6V, making the device suitable for translating between any of the voltage nodes (0.7V, 0.8V, 0.9V, 1.2V, 1.8V, 2.5V and 3.3V).

### 7.3.9 I/Os with Integrated Static Pull-Down Resistors

To avoid floating inputs on the I/Os, this device has 71k $\Omega$  typical integrated weak pull-downs on all data I/Os. This feature allows all inputs to be left floating without the concern for unstable outputs or increased current consumption. This also reduces external component count for applications where not all channels are used or need to be fixed low. If an external pull-up is required, then it should be no larger than 7k $\Omega$  to avoid contention with the 71k $\Omega$  internal pull-down.

### 7.3.10 Supports High-Speed Translation

The SN74AXC4T245 device can support high data-rate applications. The translated signal data rate can be up to 380Mbps when the signal is translated from 1.8V to 3.3V.

## 7.4 Device Functional Modes

**表 7-1. Function Table  
(Each 2-Bit Section)**

CONTROL INPUTS <sup>(1)</sup>		PORT STATUS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.

## 8 Application and Implementation

### 注

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### 8.1 Application Information

The SN74AXC4T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AXC4T245 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380Mbps when device translates a signal from 1.8V to 3.3V.

One example application is shown in 図 8-1, where the SN74AXC4T245 device is used to translate a low voltage UART signal from an SoC to a higher voltage signal which properly drive the inputs of the bluetooth module, and vice versa.

### 8.2 Typical Application

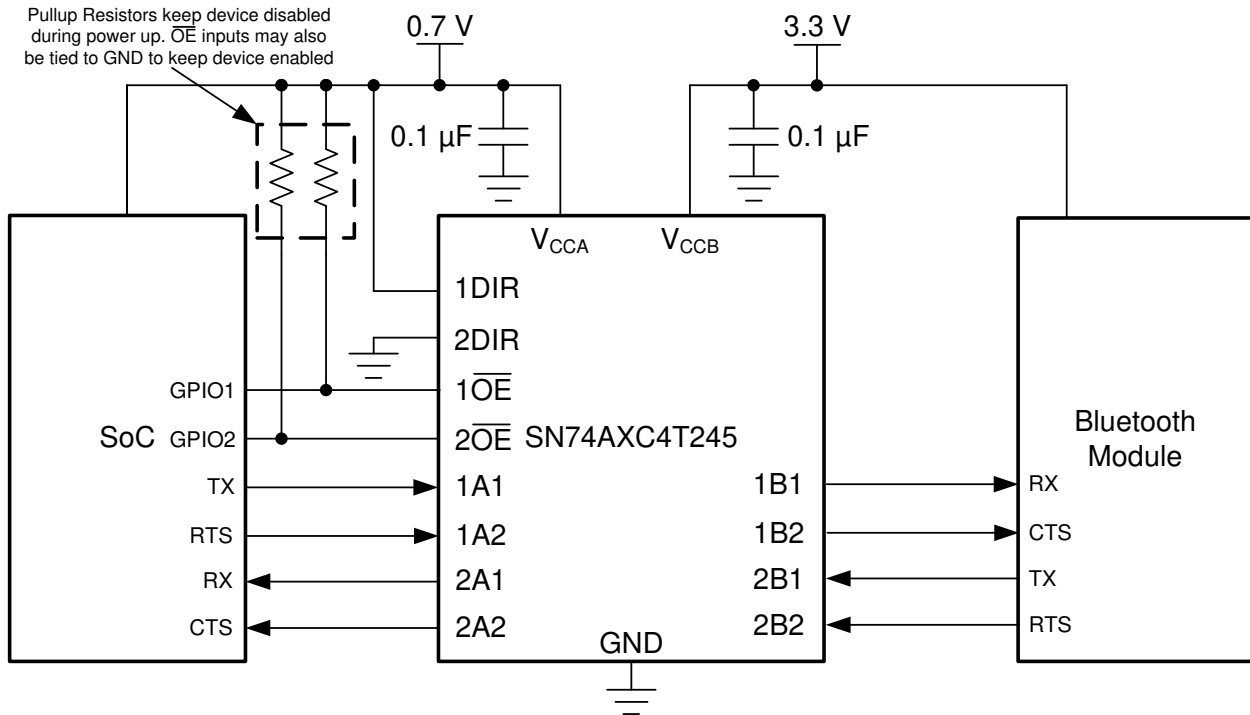


図 8-1. UART Interface Application

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65V to 3.6V
Output voltage range	0.65V to 3.6V

## 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXC4T245 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage ( $V_{IH}$ ) of the input port. For a valid logic low the value must be less than the low-level input voltage ( $V_{IL}$ ) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXC4T245 device is driving to determine the output voltage range.

## 8.2.3 Application Curve

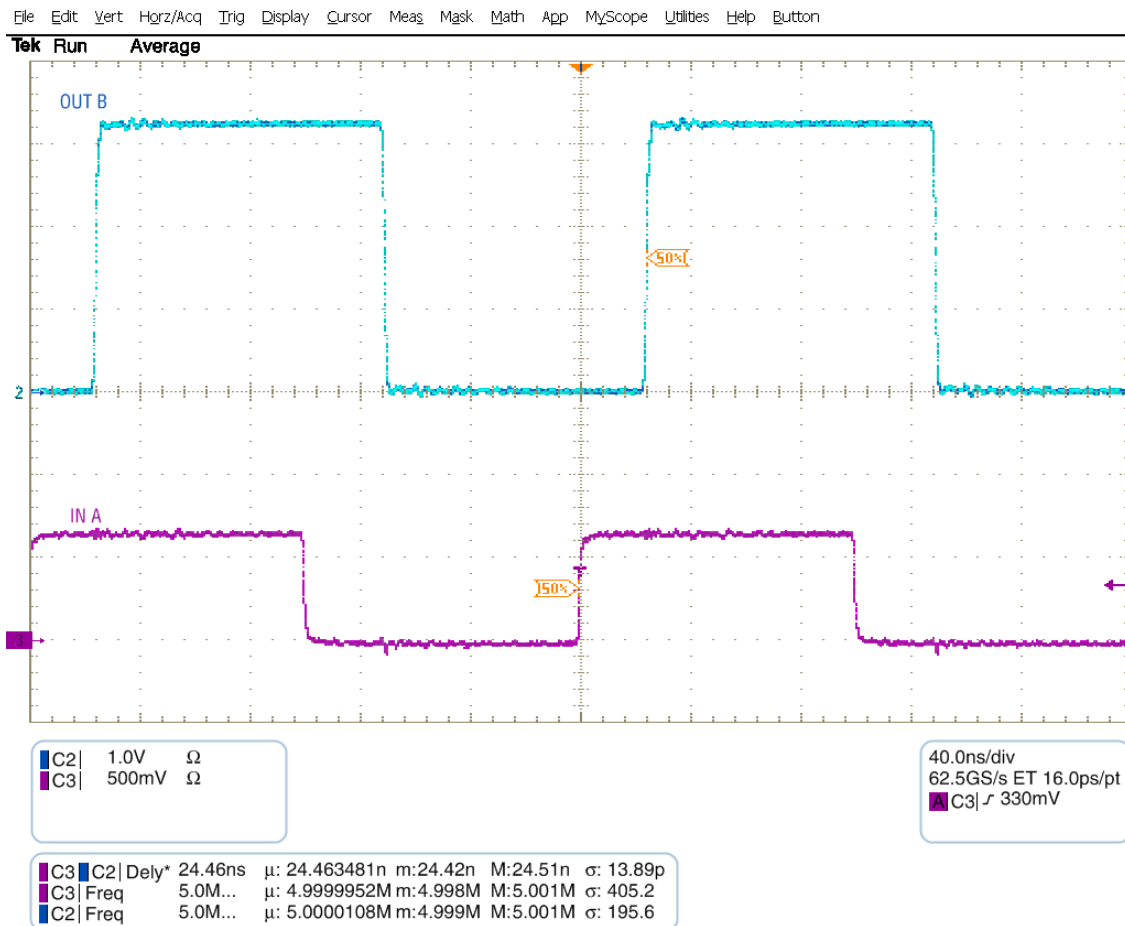


図 8-2. Up Translation at 2.5MHz (0.7V to 3.3V)

## 8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the [Glitch Free Power Sequencing With AXC Level Translators](#) application report

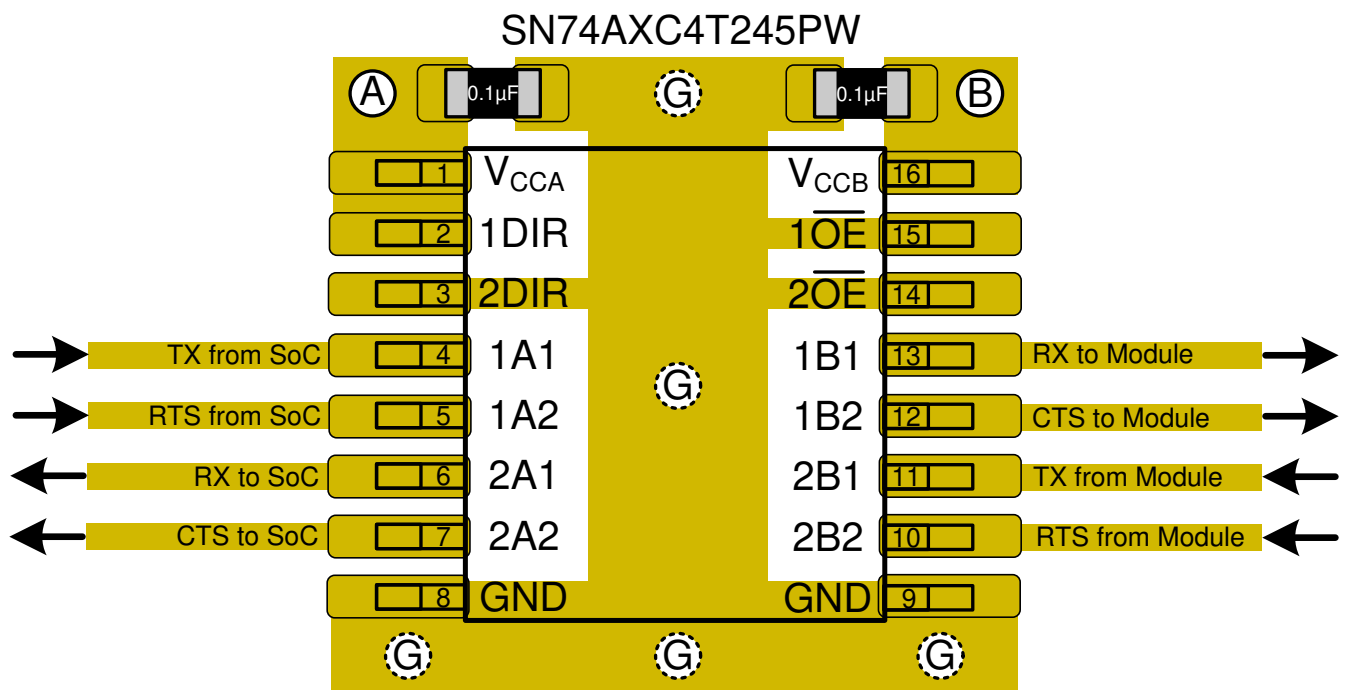
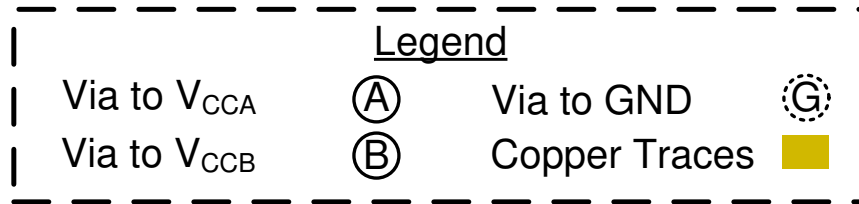
## 8.4 Layout

### 8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as follows:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible.
- Use short trace lengths to avoid excessive loading.

### 8.4.2 Layout Example



☒ 8-3. Layout Example

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application report](#)
- Texas Instruments, [Power Sequencing for AXC Family of Devices application report](#)

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (July 2020) to Revision B (April 2024)	Page
• Added the <i>I/Os with Integrated Static Pull-Down Resistors</i> section.....	19

Changes from Revision * (December 2018) to Revision A (July 2020)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新。.....	1
• 「製品情報」表に BQB (WQFN) パッケージ オプションを追加.....	1



## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AXC4T245BQBR	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4T245	<a href="#">Samples</a>
SN74AXC4T245PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	SN4T245	<a href="#">Samples</a>
SN74AXC4T245RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1TIR	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74AXC4T245 :**

- Automotive : [SN74AXC4T245-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AXC4T245BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74AXC4T245PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AXC4T245RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AXC4T245BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74AXC4T245PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AXC4T245RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

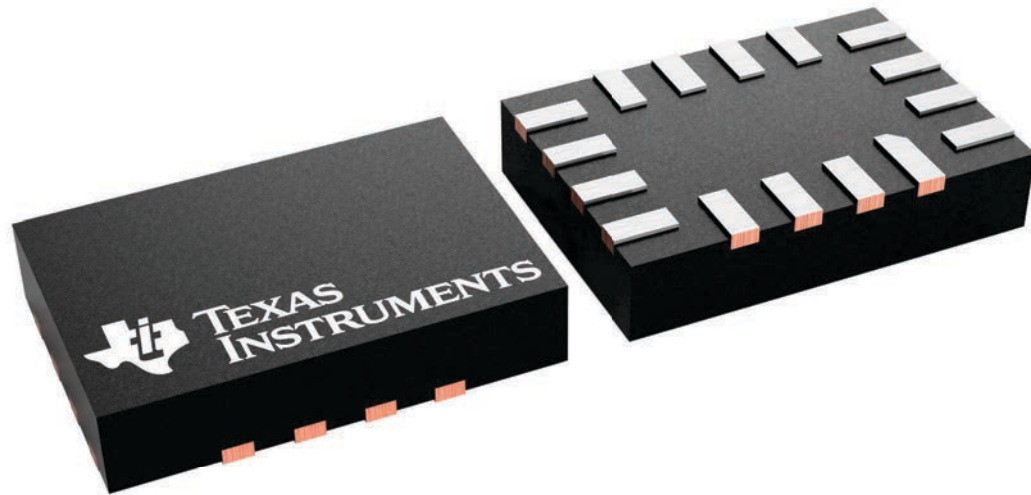
**RSV 16**

**UQFN - 0.55 mm max height**

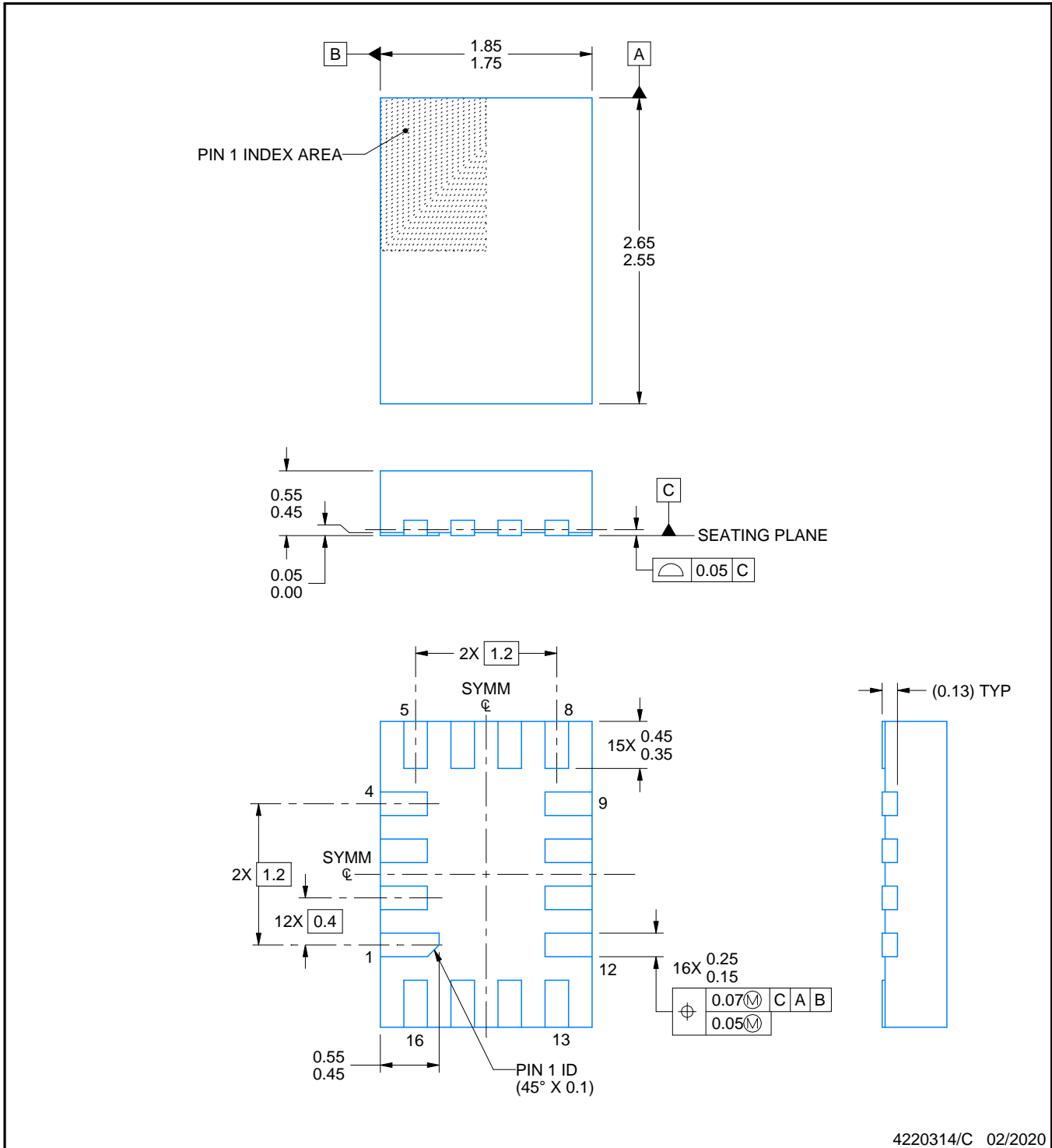
1.8 x 2.6, 0.4 mm pitch

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231225/A



4220314/C 02/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

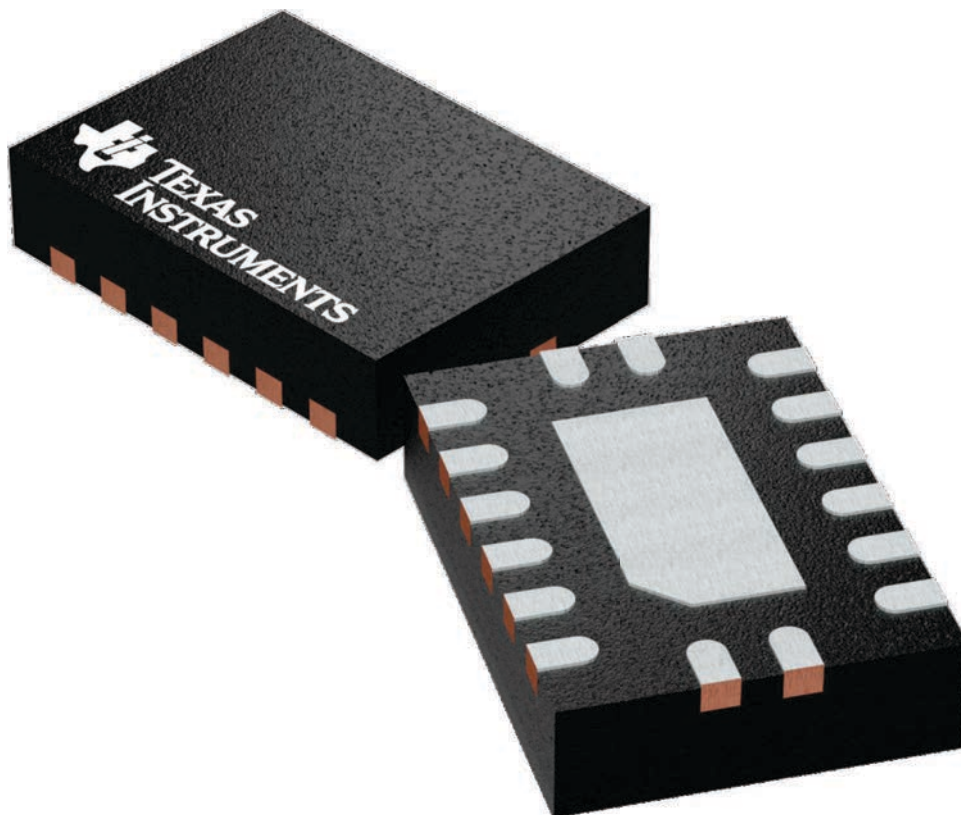
**BQB 16**

**WQFN - 0.8 mm max height**

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226161/A



4224640/A 11/2018

**NOTES:**

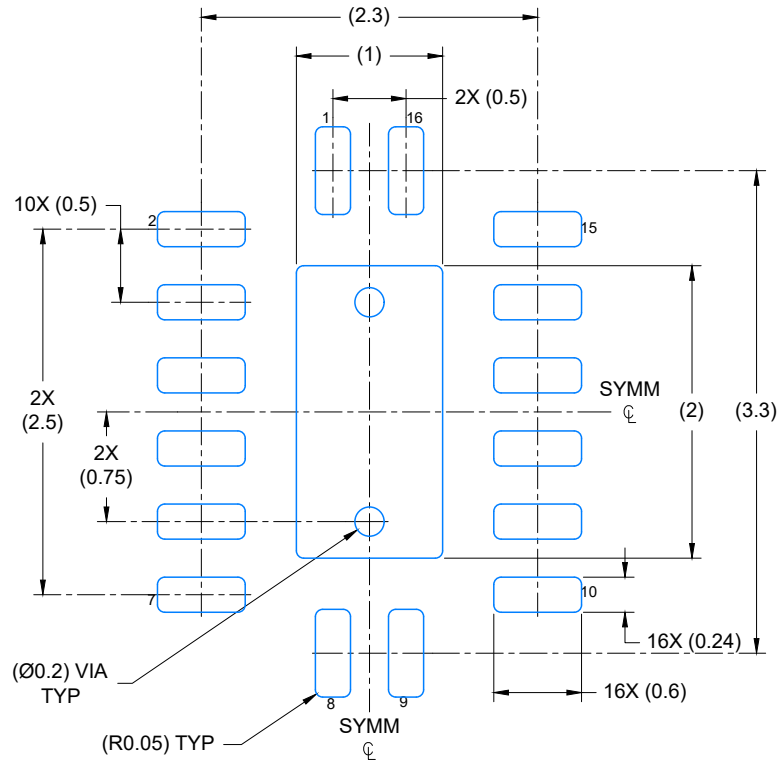
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

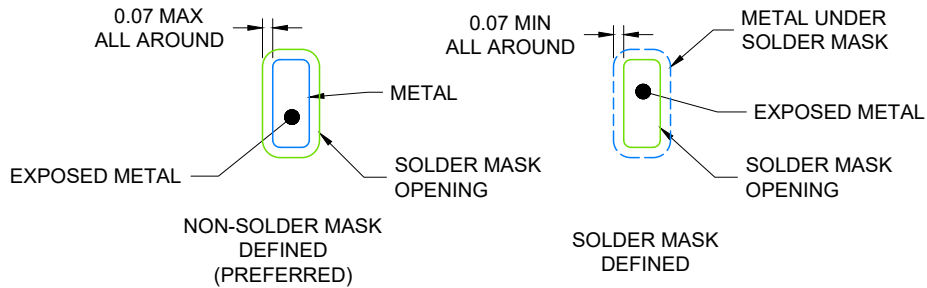
**BQB0016A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



# EXAMPLE STENCIL DESIGN

**BQB0016A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 85% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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