参考資料

SN74AXCH1T45 シングル・ビット、デュアル電源バス・トランシーバ、構成可能な電圧変換、3 ステート出力、バス・ホールド入力

1 特長

- 完全に構成可能なデュアル・レール設計により、各ポートは 0.65V～3.6V の範囲の電源電圧で動作可能
- 動作温度：–40℃～+125℃
- グリッチの発生しない電源シーケンシング
- データ入力時のバス・ホールドにより、外部のプルアップまたはプルダウン抵抗が不要
- 最大静止電流 (I_{CCA} + I_{CCB})：10μA (最高 85℃) および 16μA (最高 125℃)
- 1.8V から 3.3V への変換時に最高 500Mbps をサポート
- V_{CC} 絶縁機能
  - どちらかの V_{CC} 入力が 100mV を下回った場合、すべての I/O 出力がディスエーブルされ高インピーダンス状態に移行
- I_{off} により部分的パワーダウン・モード動作をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を超える ESD 保護
  - 8000V、人体モデル
  - 1000V、デバイス帯電モデル

2 アプリケーション

- パーソナル・エレクトロニクス
- エンタープライズおよび通信
- ワイヤレス・インフラ
- ビル・オートメーション
- POS システム
- エンタープライズ向けソリッド・ステート・ドライブ

3 概要

SN74AXCH1T45 は、別々に構成可能な 2 本の電源レールを採用したシングル・ビットの非反転バス・トランシーバです。このデバイスは、V_{CCA} 電源と V_{CCB} 電源の両方が最低 0.65V で動作します。A ポートは V_{CCA} (0.65V～3.6V の任意の電圧を入力できます) に追従するように設計されています。同様に B ポートは V_{CCB} (0.65V～3.6V の任意の電圧を入力できます) に追従するように設計されています。さらに、SN74AXCH1T45 は単一電源システムにも対応しています。

信号伝搬の方向は DIR ピンを使用して制御します。DIR ピンを HIGH に設定するとポート A からポート B への変換になり、DIR ピンを LOW に設定するとポート B からポート A への変換になります。DIR ピンは V_{CCA} を基準とすることから、そのロジック HIGH とロジック LOW のスレッショルドは V_{CCA} に追従します。

アクティブなバス・ホールド回路により、使用されていない、または駆動されていない入力を有効なロジック状態に保持します。プルアップまたはプルダウン抵抗とバス・ホールド回路との併用は推奨しません。V_{CCA} または V_{CCB} に電源が存在する場合、方向制御ピンの状態とは関係なく、バス・ホールド回路はそれぞれ A または B 入力でアクティブ状態を維持します。

このデバイスは、I_{off} 電流を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。I_{off} 保護回路により、電源切断時に入力、出力、複合 I/O は指定の電圧にバイアスされ、それらとの間に過剰な電流が流れることはありません。

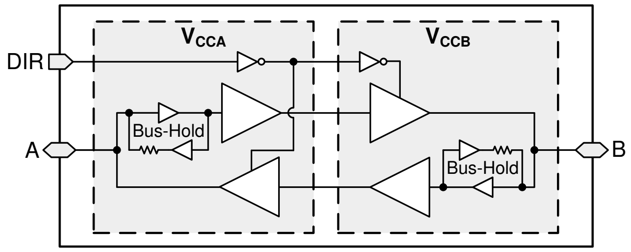
V_{CC} 絶縁機能により、V_{CCA} と V_{CCB} のどちらかが 100mV を下回ると、両方の出力がディスエーブルになり、両方の I/O ポートが高インピーダンス状態になります。

グリッチの発生しない電源シーケンシングにより、堅牢な電源シーケンシング性能が得られると同時に、どちらの電源レールも任意の順序で電源オン / オフできます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN74AXCH1T45DBV	SOT-23 (6)	2.90mm × 1.60mm
SN74AXCH1T45DCK	SC70 (6)	2.00mm × 1.25mm
SN74AXCH1T45DTQ	X2SON (6)	1.00mm × 0.80mm
SN74AXCH1T45DRY	SON (6)	1.40mm × 1.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (June 2020) to Revision C (September 2020)	Page
• Updated I_{CCA}, I_{CCB}, and I_{CCA} + I_{CCB} to reflect updated performance of device	6

Changes from Revision A (January 2019) to Revision B (June 2020)	Page
• 「製品情報」表に DRY パッケージ・オプションを追加	1
• Added pinout drawing for DRY package	3

Changes from Revision * (December 2018) to Revision A (January 2019)	Page
• 「製品情報」表に DBV および DTQ パッケージ・オプションを追加	1
• 「改訂履歴」セクションを更新	1
• Added pinout drawings for DBV and DTQ packages	3
• Added DRY package to Pin Configurations	3

5 Pin Configuration and Functions

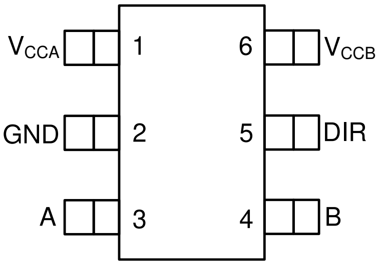

VCCA
1
6
VCCB
GND
2
5
DIR
A
3
4
B

図 5-1. DBV Package 6-Pin SOT-23 Top View

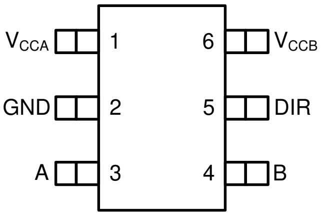

VCCA
1
6
VCCB
GND
2
5
DIR
A
3
4
B

図 5-2. DCK Package 6-Pin SC70 Top View

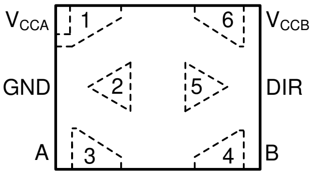

VCCA
1
6
VCCB
GND
2
5
DIR
A
3
4
B

図 5-3. DTQ Package 6-Pin X2SON Transparent Top View

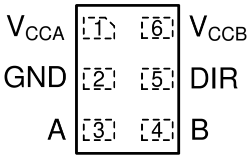

VCCA
1
6
VCCB
GND
2
5
DIR
A
3
4
B

図 5-4. DRY Package 6-Pin SON Transparent Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V_{CCA}	—	A-port supply voltage. 0.65 V ≤ V_{CCA} ≤ 3.6 V.
2	GND	—	Ground
3	A	I/O	Input/output A. This pin is referenced to V_{CCA}.
4	B	I/O	Input/output B. This pin is referenced to V_{CCB}.
5	DIR	I	Direction control signal. See for functionality.
6	V_{CCB}	—	B-port supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.2	V
V_{CCB}	Supply voltage B		–0.5	4.2	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.2	V
		I/O Ports (B Port)	–0.5	4.2	
		Control Inputs	–0.5	4.2	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.2	V
		B Port	–0.5	4.2	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.2	V
		B Port	–0.5	V_{CCB} + 0.2	
I_{IK}	Input clamp current	$V_I < 0$	–50		mA
I_{OK}	Output clamp current	$V_O < 0$	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			0.65	3.6	V
V_{CCB}	Supply voltage B			0.65	3.6	V
V_{IH}	High-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V	V_{CCI} x 0.70		V
			V_{CCI} = 0.76 V - 1 V	V_{CCI} x 0.70		
			V_{CCI} = 1.1 V - 1.95 V	V_{CCI} x 0.65		
			V_{CCI} = 2.3 V - 2.7 V	1.6		
			V_{CCI} = 3 V - 3.6 V	2		
		Control Input (DIR) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V	V_{CCA} x 0.70		
			V_{CCA} = 0.76 V - 1 V	V_{CCA} x 0.70		
			V_{CCA} = 1.1 V - 1.95 V	V_{CCA} x 0.65		
			V_{CCA} = 2.3 V - 2.7 V	1.6		
			V_{CCA} = 3 V - 3.6 V	2		
V_{IL}	Low-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V		V_{CCI} x 0.30	V
			V_{CCI} = 0.76 V - 1 V		V_{CCI} x 0.30	
			V_{CCI} = 1.1 V - 1.95 V		V_{CCI} x 0.35	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3 V - 3.6 V		0.8	
		Control Input (DIR) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V		V_{CCA} x 0.30	
			V_{CCA} = 0.76 V - 1 V		V_{CCA} x 0.30	
			V_{CCA} = 1.1 V - 1.95 V		V_{CCA} x 0.35	
			V_{CCA} = 2.3 V - 2.7 V		0.7	
			V_{CCA} = 3 V - 3.6 V		0.8	
V_I	Input voltage (3)			0	3.6	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	3.6	
Δt/Δv	Input transition rate				100	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) VCCI is the VCC associated with the input port.
(2) VCCO is the VCC associated with the output port.
(3) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AXCH1T45				UNIT
		DBV (SOT-23)	DCK (SC70)	DTQ (X2SON)	DRY (SON)	
		6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214.0	223.9	327.8	308.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.8	150.9	194.9	206.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	93.6	75.3	248.4	181.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	78.1	58.2	24.1	42.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	93.4	75.0	247.6	180.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
						–40°C to 85°C			–40°C to 125°C			
						MIN	TYP[3]	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = –100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = –50 µA	0.65 V	0.65 V	0.55			0.55			
			I_{OH} = –200 µA	0.76 V	0.76 V	0.58			0.58			
			I_{OH} = –500 µA	0.85 V	0.85 V	0.65			0.65			
			I_{OH} = –3 mA	1.1 V	1.1 V	0.85			0.85			
			I_{OH} = –6 mA	1.4 V	1.4 V	1.05			1.05			
			I_{OH} = –8 mA	1.65 V	1.65 V	1.2			1.2			
			I_{OH} = –9 mA	2.3 V	2.3 V	1.75			1.75			
			I_{OH} = –12 mA	3 V	3 V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V			0.1			0.1	V
			I_{OL} = 50 µA	0.65 V	0.65 V			0.1			0.1	
			I_{OL} = 200 µA	0.76 V	0.76 V			0.18			0.18	
			I_{OL} = 500 µA	0.85 V	0.85 V			0.2			0.2	
			I_{OL} = 3 mA	1.1 V	1.1 V			0.25			0.25	
			I_{OL} = 6 mA	1.4 V	1.4 V			0.35			0.35	
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7			0.7	
I_{BHL}	Bus-hold low sustaining current (4)	V_I = 0.20 V		0.65 V	0.65 V	4			4			µA
		V_I = 0.23 V		0.76 V	0.76 V	8			7			
		V_I = 0.26 V		0.85 V	0.85 V	10			10			
		V_I = 0.39 V		1.1 V	1.1 V	20			20			
		V_I = 0.49 V		1.4 V	1.4 V	40			30			
		V_I = 0.58 V		1.65 V	1.65 V	55			45			
		V_I = 0.7 V		2.3 V	2.3 V	90			80			
		V_I = 0.8 V		3 V	3 V	145			135			
I_{BHH}	Bus-hold high sustaining current (5)	V_I = 0.45 V		0.65 V	0.65 V	–4			–4			µA
		V_I = 0.53 V		0.76 V	0.76 V	–8			–7			
		V_I = 0.59 V		0.85 V	0.85 V	–10			–10			
		V_I = 0.71 V		1.1 V	1.1 V	–20			–20			
		V_I = 0.91 V		1.4 V	1.4 V	–40			–30			
		V_I = 1.07 V		1.65 V	1.65 V	–55			–45			
		V_I = 1.6 V		2.3 V	2.3 V	–90			–80			
		V_I = 2.0 V		3 V	3 V	–145			–135			

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
						–40°C to 85°C			–40°C to 125°C			
						MIN	TYP[3]	MAX	MIN	TYP	MAX	
I_{BHLO}	Bus-hold low overdrive current (6)	V_I = 0 to V_{CC}		0.75 V	0.75 V	40			40			µA
				0.84 V	0.84 V	50			50			
				0.95 V	0.95 V	65			65			
				1.3 V	1.3 V	105			105			
				1.6 V	1.6 V	150			150			
				1.95 V	1.95 V	205			205			
				2.7 V	2.7 V	335			335			
				3.6 V	3.6 V	480			480			
I_{BHHO}	Bus-hold high overdrive current (7)	V_I = 0 to V_{CC}		0.75 V	0.75 V	–40			–40			µA
				0.84 V	0.84 V	–50			–50			
				0.95 V	0.95 V	–65			–65			
				1.3 V	1.3 V	–105			–105			
				1.6 V	1.6 V	–150			–150			
				1.95 V	1.95 V	–205			–205			
				2.7 V	2.7 V	–335			–335			
				3.6 V	3.6 V	–480			–480			
I_I	Input leakage current	Control input (DIR): V_I = V_{CCA} or GND		0.65 V - 3.6 V	0.65 V - 3.6 V	–0.5		0.5	–1		1	µA
		A or B Port: Vi = V_{CCI} or GND		0.65 V - 3.6 V	0.65 V - 3.6 V	–4		4	–8		8	
I_{off}	Partial power down current	A or B Port: Vi or Vo = 0 V - 3.6 V		0 V	0 V - 3.6 V	–8		8	–12		12	µA
				0 V - 3.6 V	0 V	–8		8	–12		12	
I_{CCA}	V_{CCA} supply current	V_I = V_{CCI} or GND	I_O = 0	0.65 V - 3.6 V	0.65 V - 3.6 V			8			12	µA
				0 V	3.6 V	–2			–8			
				3.6 V	0 V			2			8	
I_{CCB}	V_{CCB} supply current	V_I = V_{CCI} or GND	I_O = 0	0.65 V - 3.6 V	0.65 V - 3.6 V			8			12	µA
				0 V	3.6 V			2			8	
				3.6 V	0 V	–2			–8			
I_{CCA} + I_{CCB}	Combined supply current	V_I = V_{CCI} or GND	I_O = 0	0.65 V - 3.6 V	0.65 V - 3.6 V			10			16	µA
C_i	Control input capacitance	V_I = 3.3 V or GND		3.3 V	3.3 V		4.3			4.3		pF
C_{io}	Data I/O capacitance, A Port	V_O = 1.65 V DC +1 MHz -16 dBm sine wave		3.3 V	0 V		7.4			7.4		pF
C_{io}	Data I/O capacitance, B Port	V_O = 1.65 V DC +1 MHz -16 dBm sine wave		0 V	3.3 V		7.4			7.4		pF

(1) VCCI is the VCC associated with the input port.
(2) VCCO is the VCC associated with the output port.
(3) All typical data is taken at 25°C.
(4) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}(MAX). I_{BHL} should be measured after lowering V_I to GND and then raising it to V_{IL}(MAX).
(5) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}(MIN). I_{BHH} should be measured after raising V_I to V_{CC} and then lowering it to V_{IH}(MIN).
(6) An external driver must source at least I_{BHLO} to switch this node from low to high.
(7) An external driver must sink at least I_{BHHO} to switch this node from high to low.

表 6-1. Switching Characteristics, V_{CCA} = 0.7 V

t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	181	0.5	119	0.5	85	0.5	51	0.5	49	0.5	52	0.5	65	0.5	152	ns
				–40°C to 125°C	0.5	181	0.5	119	0.5	85	0.5	51	0.5	49	0.5	52	0.5	65	0.5	152	
		B	A	–40°C to 85°C	0.5	181	0.5	162	0.5	136	0.5	96	0.5	91	0.5	89	0.5	88	0.5	88	
				–40°C to 125°C	0.5	181	0.5	162	0.5	136	0.5	96	0.5	91	0.5	89	0.5	88	0.5	88	
t_{dis}	Disable time	DIR	A	–40°C to 85°C	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	ns
				–40°C to 125°C	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	0.5	152	
		DIR	B	–40°C to 85°C	0.5	170	0.5	127	0.5	102	0.5	48	0.5	42	0.5	46	0.5	58	0.5	108	
				–40°C to 125°C	0.5	170	0.5	127	0.5	102	0.5	48	0.5	42	0.5	46	0.5	58	0.5	108	
t_{en}	Enable time	DIR	A	–40°C to 85°C	0.5	343	0.5	278	0.5	231	0.5	141	0.5	132	0.5	134	0.5	144	0.5	193	ns
				–40°C to 125°C	0.5	343	0.5	278	0.5	231	0.5	141	0.5	132	0.5	134	0.5	144	0.5	193	
		DIR	B	–40°C to 85°C	0.5	326	0.5	257	0.5	222	0.5	194	0.5	191	0.5	191	0.5	197	0.5	277	
				–40°C to 125°C	0.5	326	0.5	257	0.5	222	0.5	194	0.5	191	0.5	191	0.5	197	0.5	277	

表 6-2. Switching Characteristics, V_{CCA} = 0.8 V

t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	162	0.5	98	0.5	65	0.5	33	0.5	28	0.5	26	0.5	27	0.5	37	ns
				–40°C to 125°C	0.5	162	0.5	98	0.5	65	0.5	33	0.5	28	0.5	26	0.5	27	0.5	37	
		B	A	–40°C to 85°C	0.5	119	0.5	98	0.5	81	0.5	54	0.5	45	0.5	44	0.5	43	0.5	42	
				–40°C to 125°C	0.5	119	0.5	98	0.5	81	0.5	54	0.5	45	0.5	44	0.5	43	0.5	42	
t_{dis}	Disable time	DIR	A	–40°C to 85°C	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	ns
				–40°C to 125°C	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	0.5	107	
		DIR	B	–40°C to 85°C	0.5	160	0.5	117	0.5	90	0.5	39	0.5	31	0.5	29	0.5	29	0.5	37	
				–40°C to 125°C	0.5	160	0.5	117	0.5	90	0.5	39	0.5	31	0.5	29	0.5	29	0.5	37	
t_{en}	Enable time	DIR	A	–40°C to 85°C	0.5	268	0.5	205	0.5	165	0.5	90	0.5	74	0.5	71	0.5	70	0.5	77	ns
				–40°C to 125°C	0.5	268	0.5	205	0.5	165	0.5	90	0.5	74	0.5	71	0.5	70	0.5	77	
		DIR	B	–40°C to 85°C	0.5	257	0.5	194	0.5	161	0.5	130	0.5	125	0.5	126	0.5	125	0.5	132	
				–40°C to 125°C	0.5	257	0.5	194	0.5	161	0.5	130	0.5	125	0.5	126	0.5	125	0.5	132	

表 6-3. Switching Characteristics, V_{CCA} = 0.9 V

t_{pd} Propagation delay	A	B	–40°C to 85°C	0.5	135	0.5	81	0.5	54	0.5	24	0.5	18	0.5	17	0.5	15	0.5	18	ns
			–40°C to 125°C	0.5	135	0.5	81	0.5	54	0.5	24	0.5	18	0.5	17	0.5	15	0.5	18	
	B	A	–40°C to 85°C	0.5	86	0.5	65	0.5	54	0.5	41	0.5	30	0.5	26	0.5	23	0.5	23	
			–40°C to 125°C	0.5	86	0.5	65	0.5	54	0.5	41	0.5	30	0.5	26	0.5	23	0.5	23	
t_{dis} Disable time	DIR	A	–40°C to 85°C	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	ns
			–40°C to 125°C	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	0.5	79	
	DIR	B	–40°C to 85°C	0.5	154	0.5	111	0.5	85	0.5	34	0.5	27	0.5	25	0.5	21	0.5	23	
			–40°C to 125°C	0.5	154	0.5	111	0.5	85	0.5	34	0.5	27	0.5	25	0.5	21	0.5	23	
t_{en} Enable time	DIR	A	–40°C to 85°C	0.5	227	0.5	166	0.5	131	0.5	71	0.5	53	0.5	48	0.5	42	0.5	44	ns
			–40°C to 125°C	0.5	227	0.5	166	0.5	131	0.5	71	0.5	53	0.5	48	0.5	42	0.5	44	
	DIR	B	–40°C to 85°C	0.5	206	0.5	152	0.5	125	0.5	96	0.5	91	0.5	89	0.5	89	0.5	92	
			–40°C to 125°C	0.5	206	0.5	152	0.5	125	0.5	96	0.5	91	0.5	89	0.5	89	0.5	92	

表 6-4. Switching Characteristics, V_{CCA} = 1.2 V

t_{pd} Propagation delay	A	B	–40°C to 85°C	0.5	95	0.5	54	0.5	41	0.5	16	0.5	11	0.5	9	0.5	8	0.5	8	ns
			–40°C to 125°C	0.5	95	0.5	54	0.5	41	0.5	16	0.5	11	0.5	9	0.5	8	0.5	8	
	B	A	–40°C to 85°C	0.5	51	0.5	33	0.5	24	0.5	16	0.5	13	0.5	11	0.5	8	0.5	8	
			–40°C to 125°C	0.5	51	0.5	33	0.5	24	0.5	16	0.5	13	0.5	11	0.5	8	0.5	8	
t_{dis} Disable time	DIR	A	–40°C to 85°C	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	ns
			–40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	
	DIR	B	–40°C to 85°C	0.5	148	0.5	105	0.5	78	0.5	30	0.5	23	0.5	20	0.5	16	0.5	16	
			–40°C to 125°C	0.5	148	0.5	105	0.5	78	0.5	30	0.5	23	0.5	20	0.5	16	0.5	16	
t_{en} Enable time	DIR	A	–40°C to 85°C	0.5	191	0.5	129	0.5	96	0.5	43	0.5	34	0.5	30	0.5	23	0.5	22	ns
			–40°C to 125°C	0.5	191	0.5	129	0.5	96	0.5	43	0.5	34	0.5	30	0.5	23	0.5	22	
	DIR	B	–40°C to 85°C	0.5	116	0.5	75	0.5	61	0.5	41	0.5	37	0.5	36	0.5	35	0.5	35	
			–40°C to 125°C	0.5	116	0.5	75	0.5	61	0.5	41	0.5	37	0.5	36	0.5	35	0.5	35	

表 6-5. Switching Characteristics, V_{CCA} = 1.5 V

t_{pd} Propagation delay	A	B	–40°C to 85°C	0.5	91	0.5	45	0.5	30	0.5	13	0.5	9	0.5	8	0.5	6	0.5	6	ns
			–40°C to 125°C	0.5	91	0.5	45	0.5	30	0.5	13	0.5	9	0.5	8	0.5	6	0.5	6	
	B	A	–40°C to 85°C	0.5	49	0.5	28	0.5	18	0.5	11	0.5	9	0.5	8	0.5	6	0.5	5	
			–40°C to 125°C	0.5	49	0.5	28	0.5	18	0.5	11	0.5	9	0.5	8	0.5	6	0.5	5	
t_{dis} Disable time	DIR	A	–40°C to 85°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	ns
			–40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	
	DIR	B	–40°C to 85°C	0.5	146	0.5	103	0.5	76	0.5	28	0.5	21	0.5	19	0.5	15	0.5	14	
			–40°C to 125°C	0.5	146	0.5	103	0.5	76	0.5	28	0.5	21	0.5	19	0.5	15	0.5	14	
t_{en} Enable time	DIR	A	–40°C to 85°C	0.5	186	0.5	124	0.5	89	0.5	38	0.5	29	0.5	26	0.5	20	0.5	18	ns
			–40°C to 125°C	0.5	186	0.5	124	0.5	89	0.5	38	0.5	29	0.5	26	0.5	20	0.5	18	
	DIR	B	–40°C to 85°C	0.5	104	0.5	58	0.5	43	0.5	31	0.5	28	0.5	27	0.5	25	0.5	25	
			–40°C to 125°C	0.5	104	0.5	58	0.5	43	0.5	31	0.5	28	0.5	27	0.5	25	0.5	25	

表 6-6. Switching Characteristics, V_{CCA} = 1.8 V

t_{pd} Propagation delay	A	B	–40°C to 85°C	0.5	89	0.5	44	0.5	26	0.5	11	0.5	8	0.5	7	0.5	6	0.5	5	ns
			–40°C to 125°C	0.5	89	0.5	44	0.5	26	0.5	11	0.5	8	0.5	7	0.5	6	0.5	5	
	B	A	–40°C to 85°C	0.5	52	0.5	26	0.5	17	0.5	9	0.5	8	0.5	7	0.5	6	0.5	5	
			–40°C to 125°C	0.5	52	0.5	26	0.5	17	0.5	9	0.5	8	0.5	7	0.5	6	0.5	5	
t_{dis} Disable time	DIR	A	–40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	ns
			–40°C to 125°C	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	
	DIR	B	–40°C to 85°C	0.5	147	0.5	103	0.5	76	0.5	27	0.5	20	0.5	18	0.5	14	0.5	13	
			–40°C to 125°C	0.5	147	0.5	103	0.5	76	0.5	27	0.5	20	0.5	18	0.5	14	0.5	13	
t_{en} Enable time	DIR	A	–40°C to 85°C	0.5	185	0.5	122	0.5	86	0.5	35	0.5	27	0.5	24	0.5	19	0.5	17	ns
			–40°C to 125°C	0.5	185	0.5	122	0.5	86	0.5	35	0.5	27	0.5	24	0.5	19	0.5	17	
	DIR	B	–40°C to 85°C	0.5	100	0.5	54	0.5	37	0.5	27	0.5	25	0.5	24	0.5	22	0.5	22	
			–40°C to 125°C	0.5	100	0.5	54	0.5	37	0.5	27	0.5	25	0.5	24	0.5	22	0.5	22	

表 6-7. Switching Characteristics, V_{CCA} = 2.5 V

t_{pd} Propagation delay	A	B	–40°C to 85°C	0.5	88	0.5	42	0.5	23	0.5	8	0.5	6	0.5	6	0.5	5	0.5	5	ns
			–40°C to 125°C	0.5	88	0.5	42	0.5	23	0.5	8	0.5	6	0.5	6	0.5	5	0.5	5	
	B	A	–40°C to 85°C	0.5	65	0.5	27	0.5	15	0.5	8	0.5	6	0.5	6	0.5	5	0.5	4	
			–40°C to 125°C	0.5	65	0.5	27	0.5	15	0.5	8	0.5	6	0.5	6	0.5	5	0.5	4	
t_{dis} Disable time	DIR	A	–40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	ns
			–40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	
	DIR	B	–40°C to 85°C	0.5	146	0.5	102	0.5	75	0.5	27	0.5	19	0.5	17	0.5	13	0.5	12	
			–40°C to 125°C	0.5	146	0.5	102	0.5	75	0.5	27	0.5	19	0.5	17	0.5	13	0.5	12	
t_{en} Enable time	DIR	A	–40°C to 85°C	0.5	191	0.5	122	0.5	85	0.5	33	0.5	25	0.5	22	0.5	17	0.5	16	ns
			–40°C to 125°C	0.5	191	0.5	122	0.5	85	0.5	33	0.5	25	0.5	22	0.5	17	0.5	16	
	DIR	B	–40°C to 85°C	0.5	95	0.5	50	0.5	31	0.5	20	0.5	18	0.5	17	0.5	17	0.5	17	
			–40°C to 125°C	0.5	95	0.5	50	0.5	31	0.5	20	0.5	18	0.5	17	0.5	17	0.5	17	

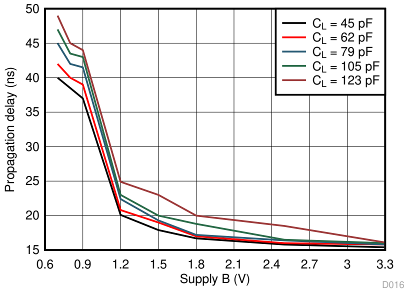
表 6-8. Switching Characteristics, V_{CCA} = 3.3 V

t_{pd} Propagation delay	A	B	–40°C to 85°C	0.5	87	0.5	42	0.5	23	0.5	8	0.5	5	0.5	5	0.5	4	0.5	4	ns
			–40°C to 125°C	0.5	87	0.5	42	0.5	23	0.5	8	0.5	5	0.5	5	0.5	4	0.5	4	
	B	A	–40°C to 85°C	0.5	154	0.5	37	0.5	18	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4	
			–40°C to 125°C	0.5	154	0.5	37	0.5	18	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4	
t_{dis} Disable time	DIR	A	–40°C to 85°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	ns
			–40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	
	DIR	B	–40°C to 85°C	0.5	147	0.5	102	0.5	75	0.5	26	0.5	19	0.5	17	0.5	13	0.5	12	
			–40°C to 125°C	0.5	147	0.5	102	0.5	75	0.5	26	0.5	19	0.5	17	0.5	13	0.5	12	
t_{en} Enable time	DIR	A	–40°C to 85°C	0.5	275	0.5	129	0.5	88	0.5	34	0.5	24	0.5	21	0.5	17	0.5	16	ns
			–40°C to 125°C	0.5	275	0.5	129	0.5	88	0.5	34	0.5	24	0.5	21	0.5	17	0.5	16	
	DIR	B	–40°C to 85°C	0.5	94	0.5	49	0.5	30	0.5	18	0.5	16	0.5	16	0.5	15	0.5	15	
			–40°C to 125°C	0.5	94	0.5	49	0.5	30	0.5	18	0.5	16	0.5	16	0.5	15	0.5	15	

6.6 Operating Characteristics: T_A = 25°C

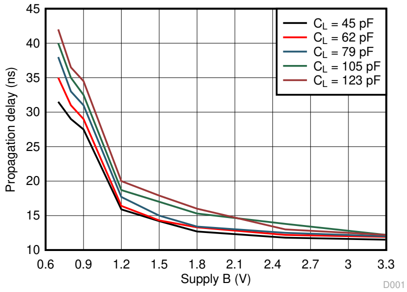
PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.0		pF
			0.8 V	0.8 V		2.0		
			0.9 V	0.9 V		2.0		
			1.2 V	1.2 V		2.0		
			1.5 V	1.5 V		1.9		
			1.8 V	1.8 V		2.0		
			2.5 V	2.5 V		2.4		
			3.3 V	3.3 V		3.0		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		12		pF
			0.8 V	0.8 V		12		
			0.9 V	0.9 V		12		
			1.2 V	1.2 V		12		
			1.5 V	1.5 V		13		
			1.8 V	1.8 V		13		
			2.5 V	2.5 V		17		
			3.3 V	3.3 V		21		
C_{pdB}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		12		pF
			0.8 V	0.8 V		12		
			0.9 V	0.9 V		12		
			1.2 V	1.2 V		12		
			1.5 V	1.5 V		13		
			1.8 V	1.8 V		13		
			2.5 V	2.5 V		17		
			3.3 V	3.3 V		21		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.1		pF
			0.8 V	0.8 V		2.2		
			0.9 V	0.9 V		2.2		
			1.2 V	1.2 V		2.2		
			1.5 V	1.5 V		2.3		
			1.8 V	1.8 V		2.3		
			2.5 V	2.5 V		2.6		
			3.3 V	3.3 V		3.3		

6.7 Typical Characteristics



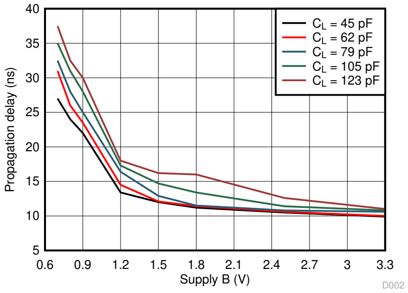
T_A = 25°C V_{CCA} = 0.7 V

図 6-1. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



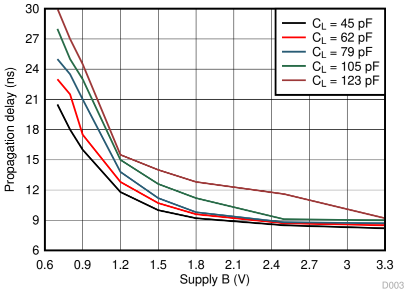
T_A = 25°C V_{CCA} = 0.8 V

図 6-2. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



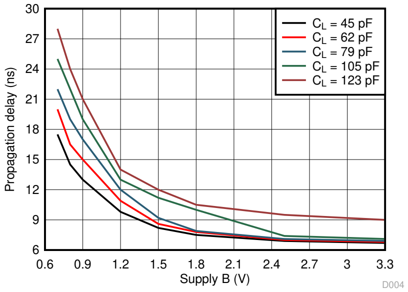
T_A = 25°C V_{CCA} = 0.9 V

図 6-3. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



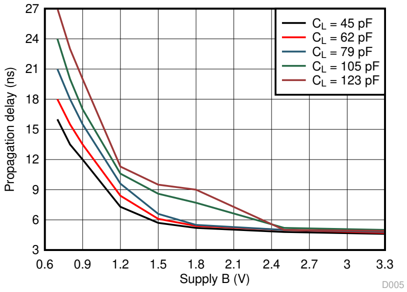
T_A = 25°C V_{CCA} = 1.2 V

図 6-4. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



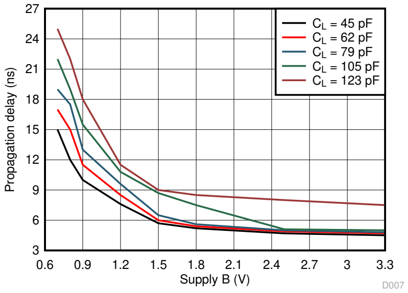
T_A = 25°C V_{CCA} = 1.5 V

図 6-5. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



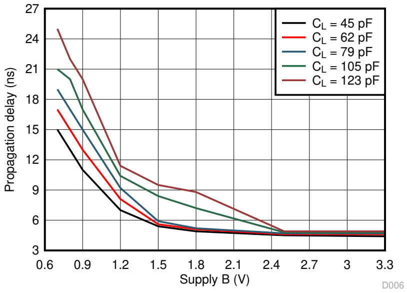
T_A = 25°C V_{CCA} = 1.8 V

図 6-6. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



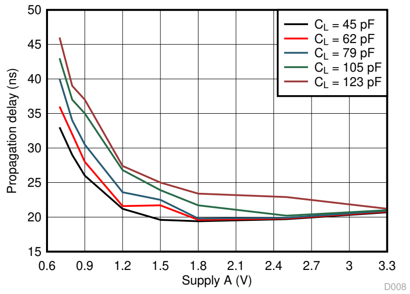
T_A = 25°C V_{CCA} = 3.3 V

図 6-7. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



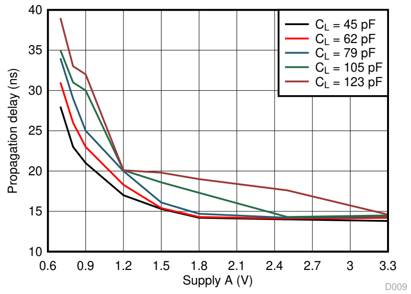
T_A = 25°C V_{CCA} = 2.5 V

図 6-8. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



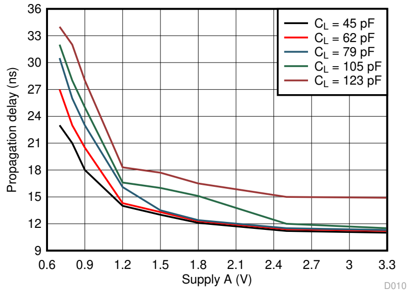
T_A = 25°C V_{CCA} = 0.7 V

図 6-9. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



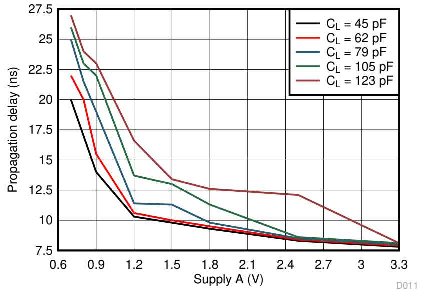
T_A = 25°C V_{CCA} = 0.8 V

図 6-10. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



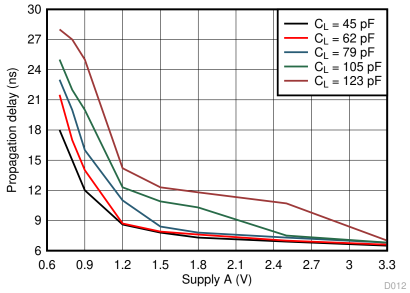
T_A = 25°C V_{CCA} = 0.9 V

図 6-11. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



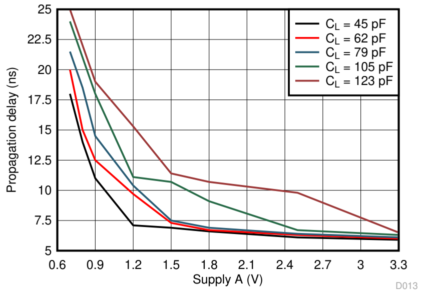
T_A = 25°C V_{CCA} = 1.2 V

図 6-12. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



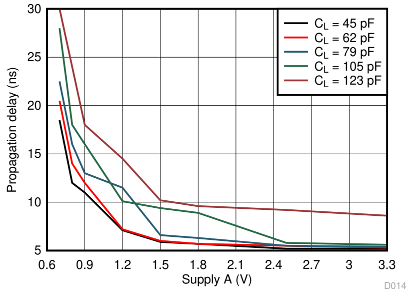
T_A = 25°C V_{CCA} = 1.5 V

図 6-13. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



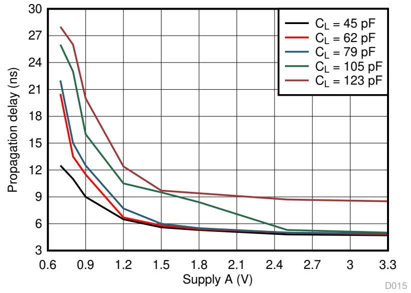
T_A = 25°C V_{CCA} = 1.8 V

図 6-14. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



T_A = 25°C V_{CCA} = 2.5 V

図 6-15. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



T_A = 25°C V_{CCA} = 3.3 V

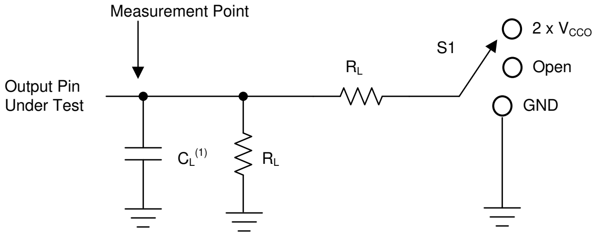
図 6-16. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- dv/dt ≤ 1 ns/V

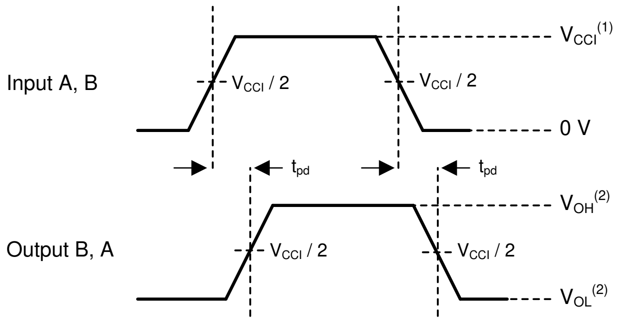

Measurement Point
Output Pin Under Test
R_L
S1
2 x V_{CCO}
Open
GND
$C_L^{(1)}$
R_L

A. C_L includes probe and jig capacitance.

図 7-1. Load Circuit

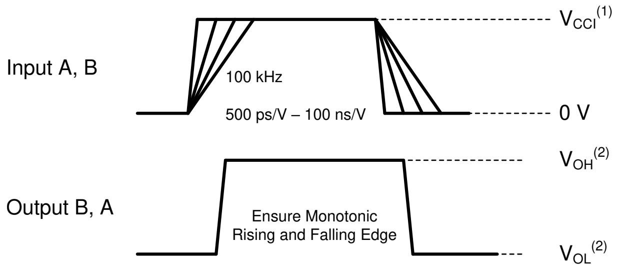
表 7-1. Load Circuit Conditions

Parameter	V_{CCO}	R_L	C_L	S_1	V_{TP}
Δt/Δv Input transition rise or fall rate	0.65 V – 3.6 V	1 MΩ	15 pF	Open	N/A
t_{pd} Propagation (delay) time	1.1 V – 3.6 V	2 kΩ	15 pF	Open	N/A
	0.65 V – 0.95 V	20 kΩ	15 pF	Open	N/A
t_{en}, t_{dis} Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.3 V
	1.65 V – 2.7 V	2 kΩ	15 pF	2 × V_{CCO}	0.15 V
	1.1 V – 1.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.1 V
	0.65 V – 0.95 V	20 kΩ	15 pF	2 × V_{CCO}	0.1 V
t_{en}, t_{dis} Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	GND	0.3 V
	1.65 V – 2.7 V	2 kΩ	15 pF	GND	0.15 V
	1.1 V – 1.6 V	2 kΩ	15 pF	GND	0.1 V
	0.65 V – 0.95 V	20 kΩ	15 pF	GND	0.1 V


Input A, B
$V_{CCI}^{(1)}$
V_{CCI} / 2
V_{CCI} / 2
0 V
t_{pd}
t_{pd}
$V_{OH}^{(2)}$
Output B, A
V_{CCI} / 2
V_{CCI} / 2
$V_{OL}^{(2)}$

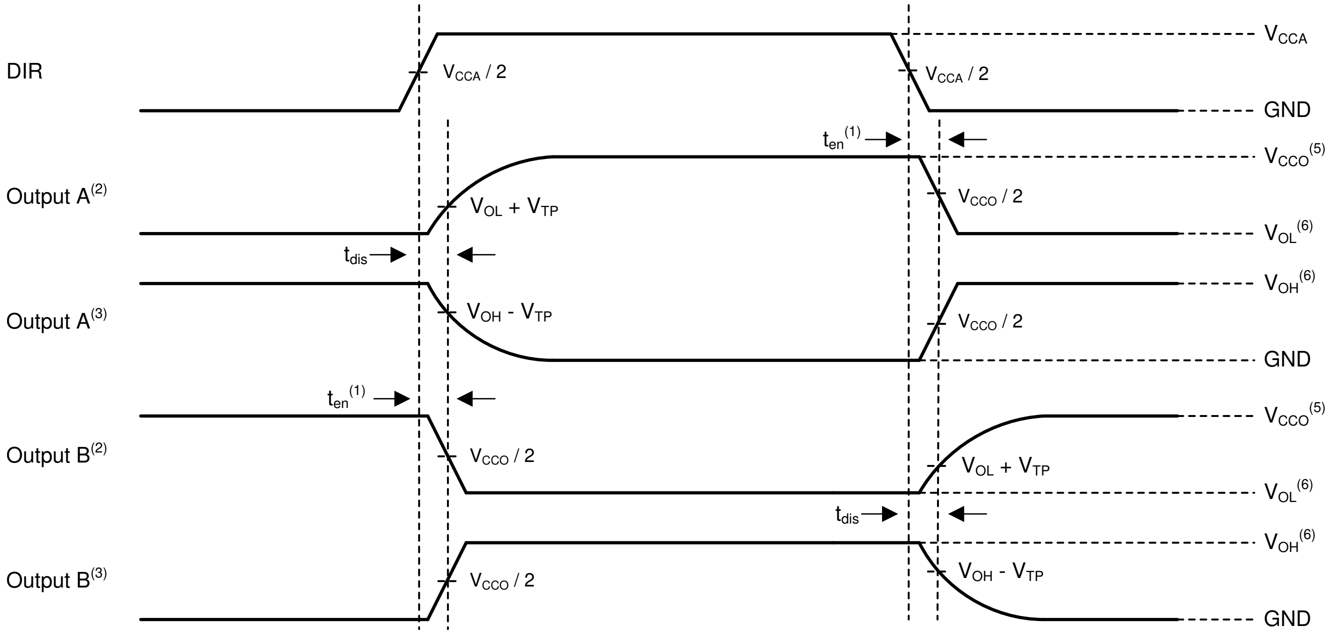
1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

図 7-2. Propagation Delay


Input A, B
$V_{CCI}^{(1)}$
100 kHz
500 ps/V – 100 ns/V
0 V
$V_{OH}^{(2)}$
Output B, A
Ensure Monotonic Rising and Falling Edge
$V_{OL}^{(2)}$

1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

図 7-3. Input Transition Rise or Fall Rate


DIR
Output A(2)
Output A(3)
Output B(2)
Output B(3)
VCCA
GND
VCCA / 2
VCCA / 2
ten(1)
tdis
VCCO(5)
VOL + VTP
VCCO / 2
VOL(6)
VOH(6)
VOH - VTP
VCCO / 2
GND
ten(1)
VCCO(5)
VCCO / 2
VOL + VTP
VOL(6)
tdis
VOH(6)
VCCO / 2
VOH - VTP
GND

1. Illustrative purposes only. Enable Time is a calculation as described in the data sheet.
2. Output waveform on the condition that input is driven to a valid Logic Low.
3. Output waveform on the condition that input is driven to a valid Logic High.
4. V_{CCI} is the supply pin associated with the input port
5. V_{CCO} is the supply pin associated with the output port.
6. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

図 7-4. Disable and Enable Time

8 Detailed Description

8.1 Overview

The SN74AXCH1T45 is single-bit, dual-supply, noninverting voltage level translator. Pin A and the direction control pin are referenced to V_{CCA} logic levels and pin B is referenced to V_{CCB} logic levels, as depicted in . The A port can accept I/O voltages ranging from 0.65 V to 3.6 V, and the B port can accept I/O voltages from 0.65 V to 3.6 V. A logic high on the DIR pin enables data transmission from A to B and a logic low on the DIR pin enables data transmission from B to A.

8.2 Functional Block Diagram

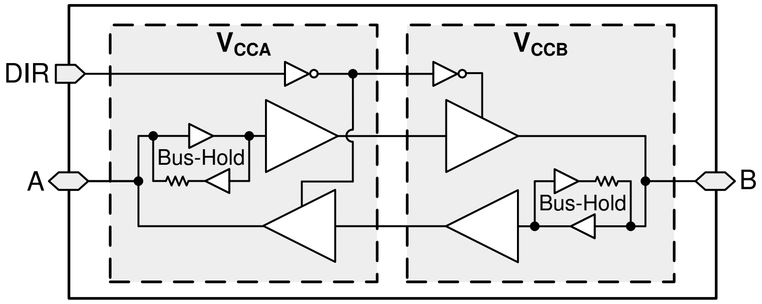


図 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

8.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.4 V_{CC} Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is <100mV.

8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

8.3.6 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in 図 8-2.

CAUTION

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

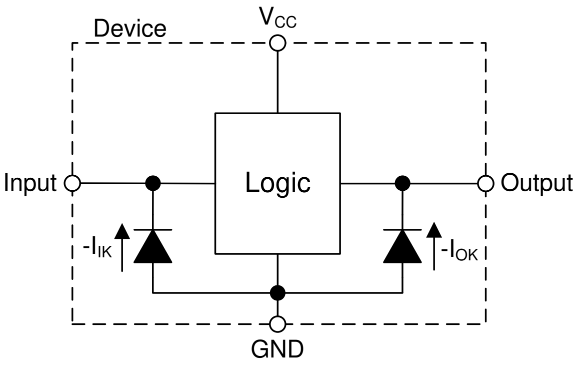


図 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.7 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 0.65 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V and 3.3 V).

8.3.8 Supports High-Speed Translation

The SN74AXCH1T45 device can support high data-rate applications. The translated signal data rate can be up to 500 Mbps when the signal is translated from 1.8 V to 3.3 V.

8.3.9 Bus-Hold Data Inputs

Each data input on this device includes a weak latch that maintains a valid logic level on the input. The state of these latches is unknown at startup and remains unknown until the input has been forced to a valid high or low state. After data has been sent through a channel, the latch then maintains the previous state on the input if the line is left floating. It is not recommended to use pull-up or pull-down resistors together with a bus-hold input, as it may cause undefined inputs to occur which leads to excessive current consumption.

Bus-hold data inputs prevent floating inputs on this device. The *Implications of Slow or Floating CMOS Inputs* application report explains the problems associated with leaving CMOS inputs floating.

These latches remain active at all times, independent of all control signals such as direction control or output enable.

The *Bus-Hold Circuit* application report has additional details regarding bus-hold inputs.

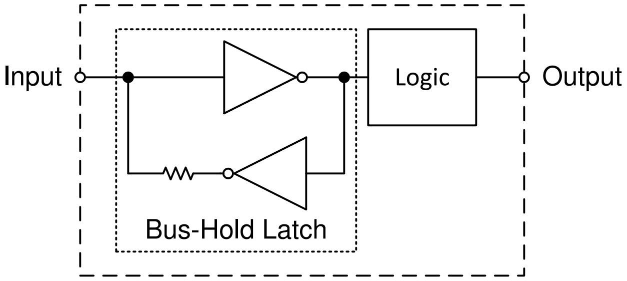


図 8-3. Simplified Schematic For Device With Bus-Hold Data Inputs

8.4 Device Functional Modes

表 8-1 lists the device functions for the DIR input.

表 8-1. Function Table

INPUT[1] DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SN74AXCH1T45 device can be used in level-translation applications for interfacing devices or systems with one another when they are operating at different interface voltages. The maximum data rate can be up to 500 Mbps when the device translate signals from 1.8 V to 3.3 V.

9.1.1 Enable Times

Calculate the enable times for the SN74AXC1T45 using the following formulas:

$$t_{A\_en} \text{ (DIR to A)} = t_{dis} \text{ (DIR to B)} + t_{pd} \text{ (B to A)} \tag{1}$$

$$t_{B\_en} \text{ (DIR to B)} = t_{dis} \text{ (DIR to A)} + t_{pd} \text{ (A to B)} \tag{2}$$

In a bidirectional application, these enable times provide the maximum delay time from the time the DIR bit is switched until an output is expected. For example, if the SN74AXCH1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled (t_{dis}) before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay (t_{pd}). To avoid bus contention care should be taken to not apply an input signal prior to the output port being disabled (t_{dis} max).

9.2 Typical Applications

9.2.1 Interrupt Request Application

図 9-1 shows an example of the SN74AXCH1T45 being used in an application where a system controller flags an interrupt request (IRQ) to the CPU. The system controller determines the direction of the IRQ line to either flag an interrupt to the CPU or allow the CPU to drive data on the line. In this application the controller is operating at 3.3 V while the CPU can be operating as low as 0.65 V.

The SN74AXCH1T45 device is used to ensure that these devices can communicate at the appropriate voltage levels. Because the SN74AXCH1T45 does not have an output-enable ($\overline{\text{OE}}$) pin, the system designer should take precautions to avoid bus contention between the CPU and controller when changing directions.

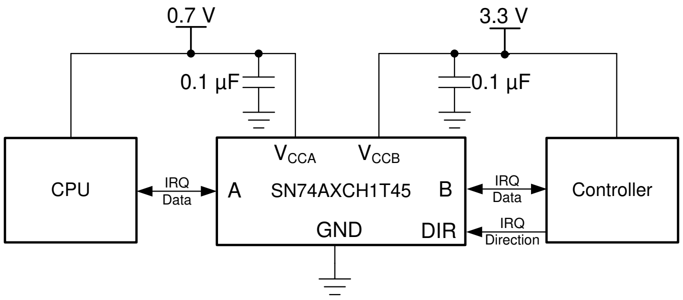


図 9-1. Interrupt Request Application

9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

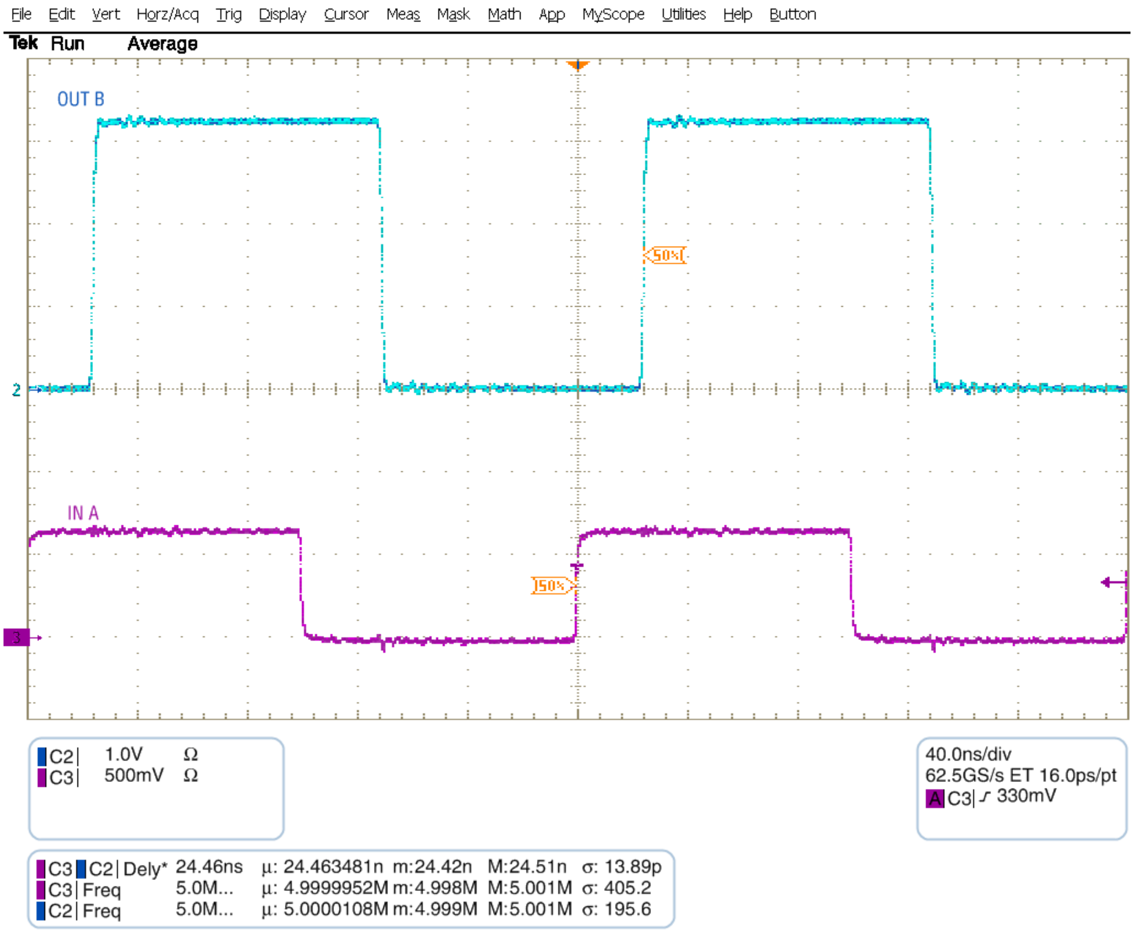
DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXCH1T45 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXCH1T45 device is driving to determine the output voltage range.

9.2.1.3 Application Curve


File Edit Vert Horz/Acq Trig Display Cursor Meas Mask Math App MyScope Utilities Help Button
Tek Run Average
OUT B
50%
2
IN A
50%
3

```
C2|  1.0V    Ω
C3|  500mV   Ω
```

```
40.0ns/div
62.5GS/s ET 16.0ps/pt
A C3| ⎍ 330mV
```

```
C3 C2| Dely* 24.46ns  µ: 24.463481n m:24.42n  M:24.51n  σ: 13.89p
C3| Freq     5.0M...  µ: 4.9999952M m:4.998M  M:5.001M  σ: 405.2
C2| Freq     5.0M...  µ: 5.0000108M m:4.999M  M:5.001M  σ: 195.6
```

図 9-2. Up Translation at 2.5 MHz (0.7 V to 3.3 V)

9.2.2 Universal Asynchronous Receiver-Transmitter (UART) Interface Application

図 9-3 shows the SN74AXCH1T45 being used for the two-bit UART interface application. One SN74AXCH1T45 device is used to level shift the voltage and drive the TX from the processor to the GPS Module while a second SN74AXCH1T45 device is used to drive the TX Data line from the GPS Module to the Processor. Devices with bus-hold inputs remove the requirement for external pullup resistors to maintain a valid logic level at the input.

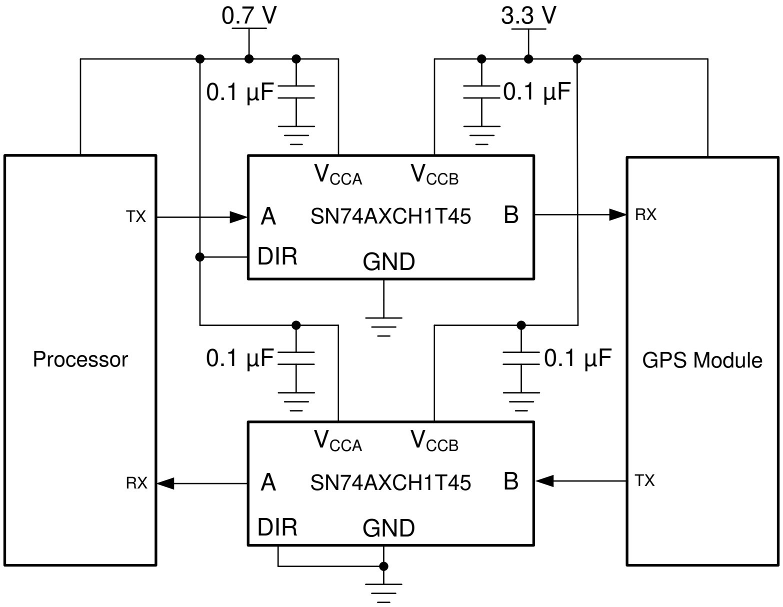

0.7 V
3.3 V
0.1 µF
0.1 µF
Processor
TX
RX
V_{CCA}
V_{CCB}
A
SN74AXCH1T45
B
DIR
GND
0.1 µF
0.1 µF
V_{CCA}
V_{CCB}
A
SN74AXCH1T45
B
DIR
GND
RX
TX
GPS Module

図 9-3. UART Interface Application

9.2.2.1 Design Requirements

Refer to *Design Requirements*.

9.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Power Sequencing for AXC Family of Devices* application report

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible.
- Use short trace lengths to avoid excessive loading.

11.2 Layout Example

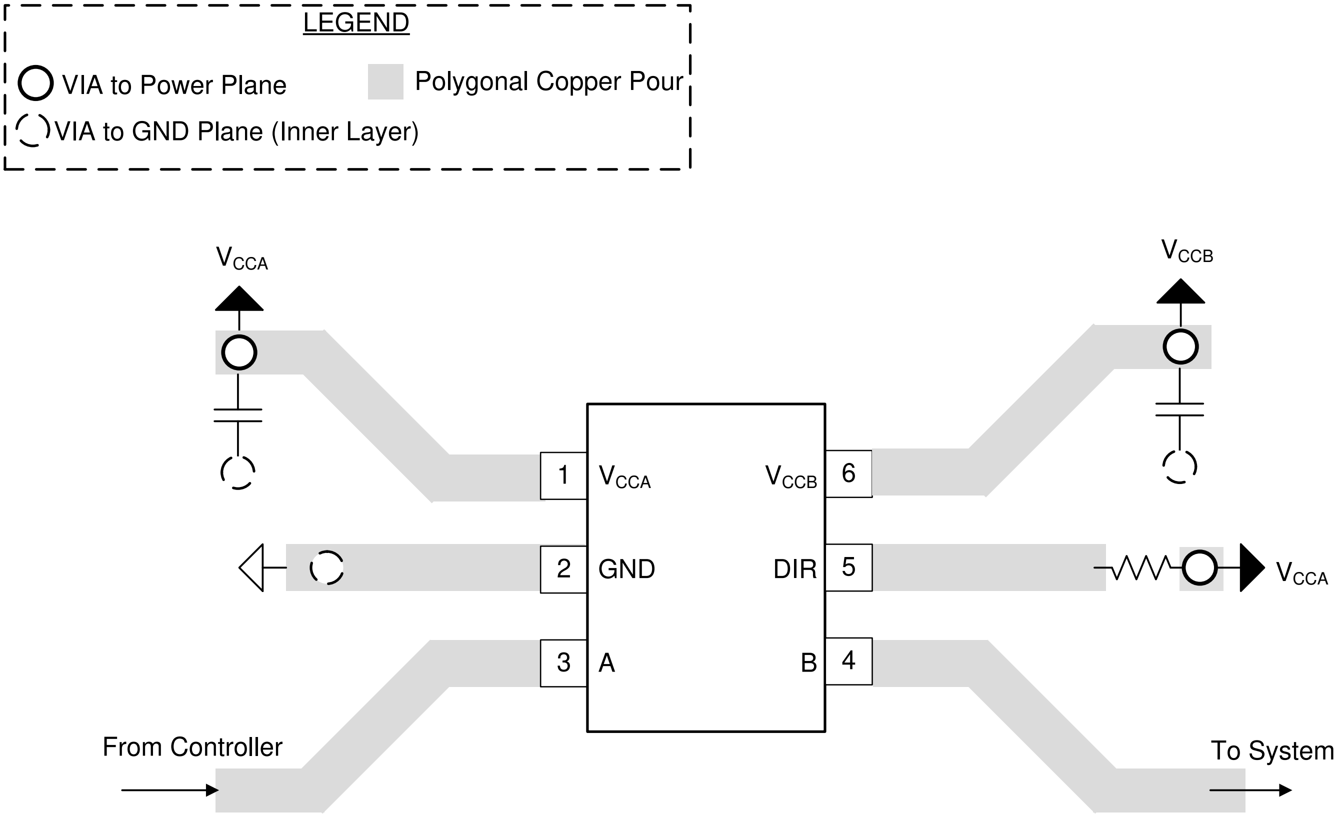

LEGEND
○ VIA to Power Plane
▨ Polygonal Copper Pour
◌ VIA to GND Plane (Inner Layer)
V_{CCA}
V_{CCB}
1
V_{CCA}
V_{CCB}
6
2
GND
DIR
5
V_{CCA}
3
A
B
4
From Controller
To System

図 11-1. PCB Layout Example

12 Device and Documentation Support

12.1 Documentation Support

For related documentation see the following:

- Texas Instruments, *Evaluate SN74AXC1T45DRL Using a Generic EVM* application report
- Texas Instruments, *System Considerations For Using Bus-hold Circuits To Avoid Floating Inputs*application report
- Texas Instruments, *Power Sequencing for the AXC Family of Devices* application report
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AXCH1T45DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1PNL
SN74AXCH1T45DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1PNL
SN74AXCH1T45DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1PNL
SN74AXCH1T45DBVRG4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1PNL
SN74AXCH1T45DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1CC
SN74AXCH1T45DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1CC
SN74AXCH1T45DRY2	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IR
SN74AXCH1T45DRY2.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IR
SN74AXCH1T45DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	II
SN74AXCH1T45DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	II
SN74AXCH1T45DTQR	Active	Production	X2SON (DTQ) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DM
SN74AXCH1T45DTQR.B	Active	Production	X2SON (DTQ) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

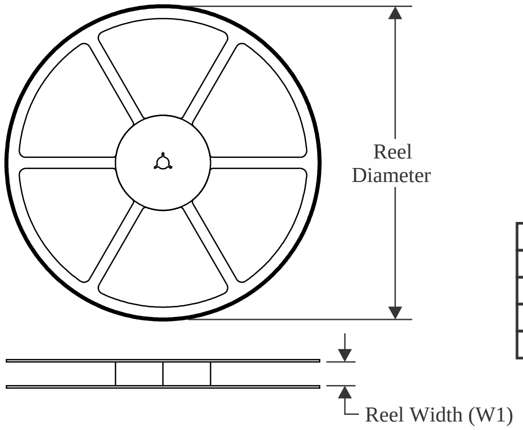
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

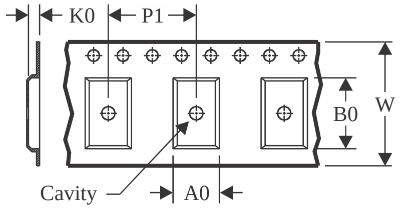
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

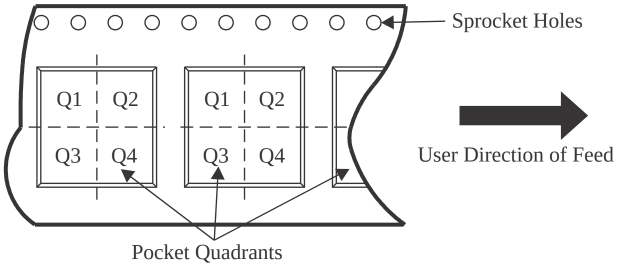

Reel
Diameter
Reel Width (W1)

TAPE DIMENSIONS


K0
P1
B0
W
Cavity
A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

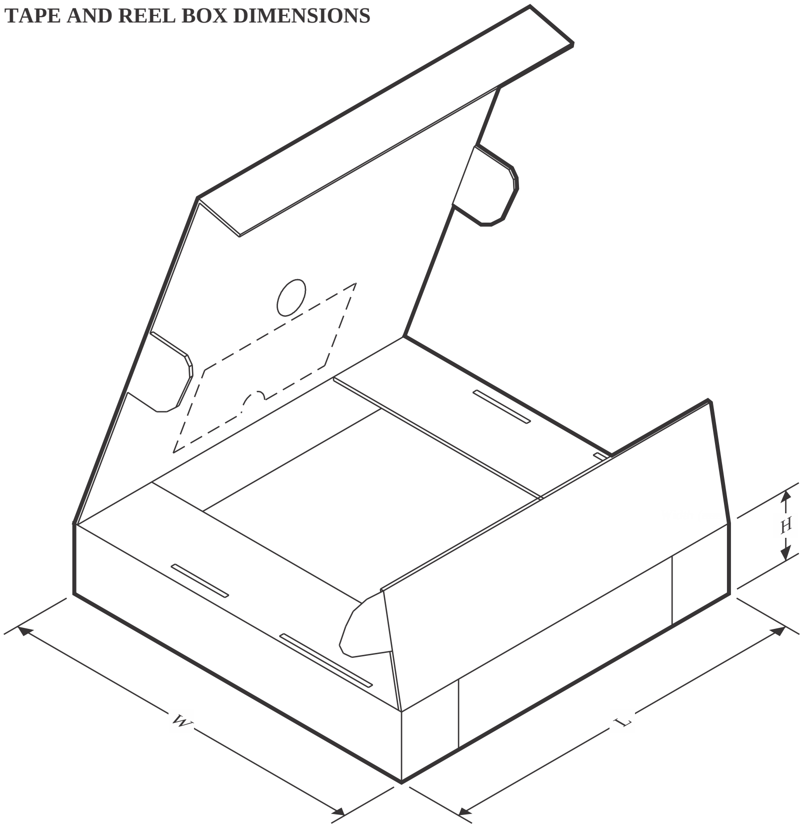
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
Sprocket Holes
User Direction of Feed
Pocket Quadrants

*All dimensions are nominal

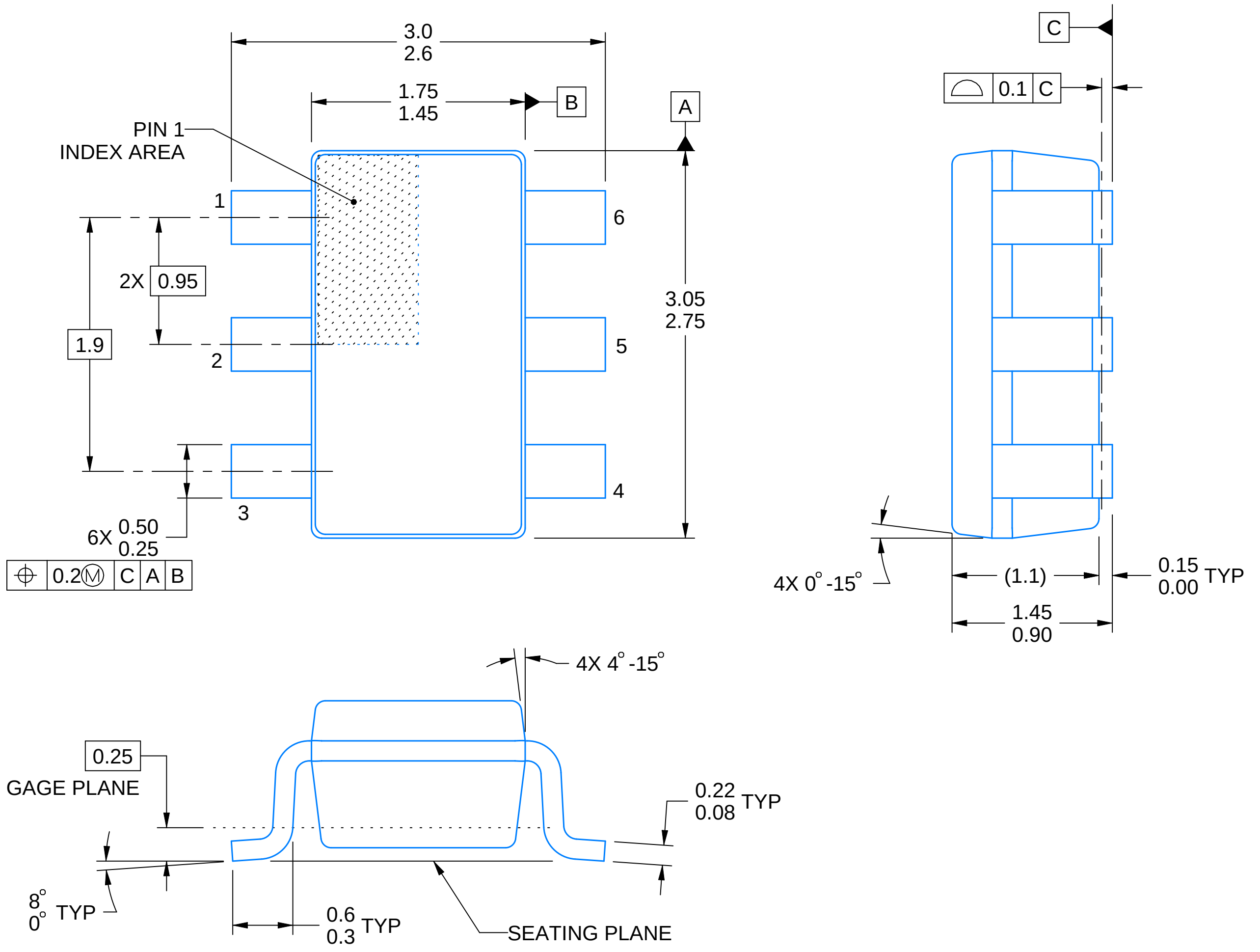
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AXCH1T45DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AXCH1T45DBVRG4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AXCH1T45DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AXCH1T45DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AXCH1T45DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.68	4.0	8.0	Q3
SN74AXCH1T45DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74AXCH1T45DTQR	X2SON	DTQ	6	3000	180.0	9.5	0.94	1.13	0.5	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

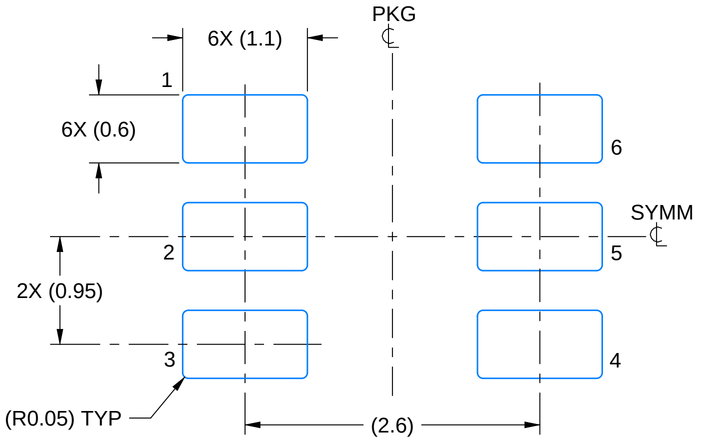
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AXCH1T45DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74AXCH1T45DBVRG4	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74AXCH1T45DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74AXCH1T45DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AXCH1T45DRY2	SON	DRY	6	5000	189.0	185.0	36.0
SN74AXCH1T45DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74AXCH1T45DTQR	X2SON	DTQ	6	3000	189.0	185.0	36.0


3.0
2.6
1.75
1.45
B
A
C
0.1 C
PIN 1
INDEX AREA
1
6
2X 0.95
1.9
3.05
2.75
2
5
3
4
6X 0.50
0.25
0.2Ⓜ C A B
4X 0°-15°
(1.1)
0.15
0.00 TYP
1.45
0.90
4X 4°-15°
0.25
GAGE PLANE
0.22
0.08 TYP
8°
0° TYP
0.6
0.3 TYP
SEATING PLANE

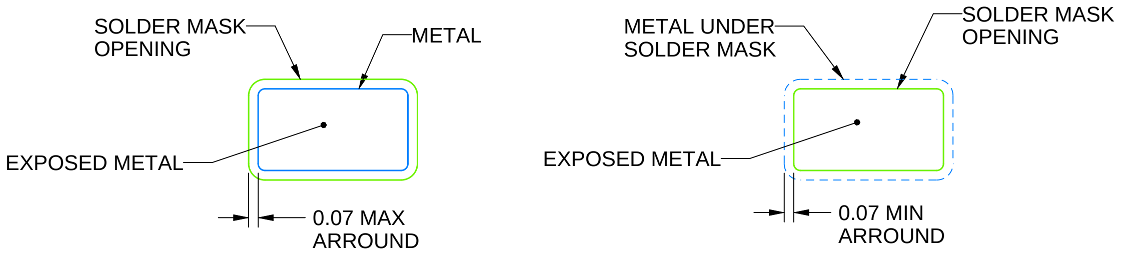
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.


PKG
℄
6X (1.1)
1
6X (0.6)
6
SYMM
℄
2
5
2X (0.95)
3
4
(R0.05) TYP
(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X


SOLDER MASK
OPENING
METAL
EXPOSED METAL
0.07 MAX
ARROUND
METAL UNDER
SOLDER MASK
SOLDER MASK
OPENING
EXPOSED METAL
0.07 MIN
ARROUND

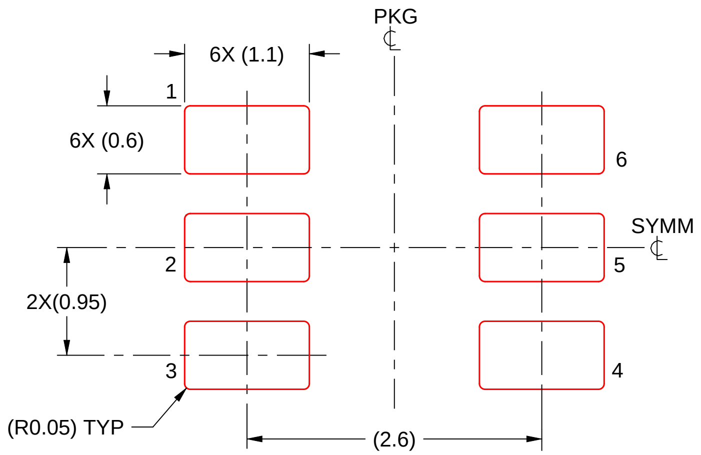
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

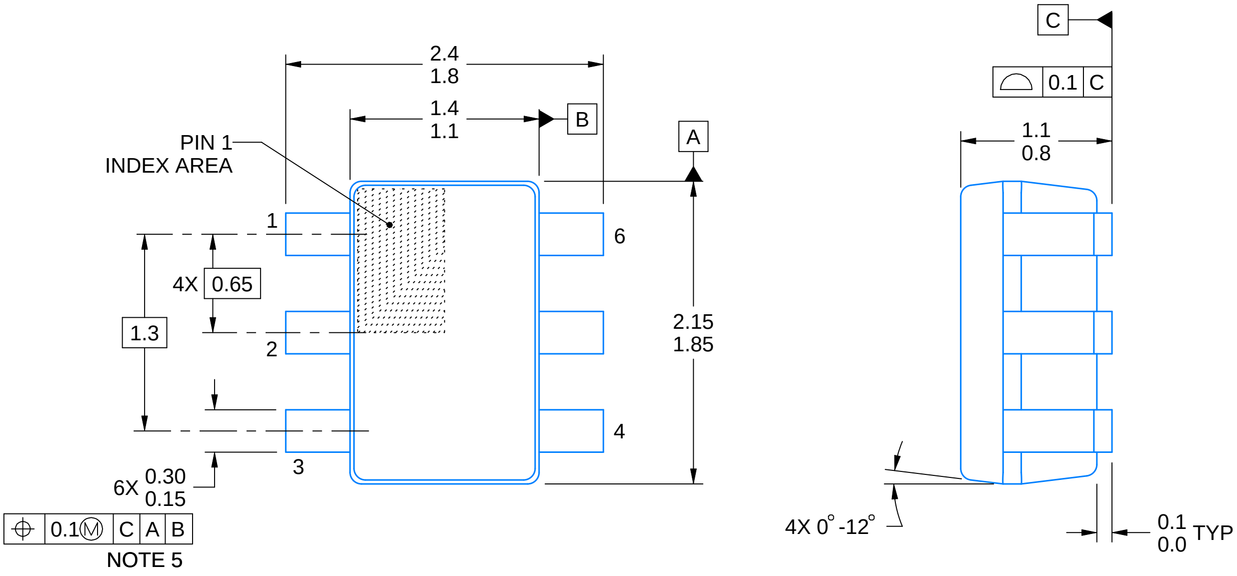
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

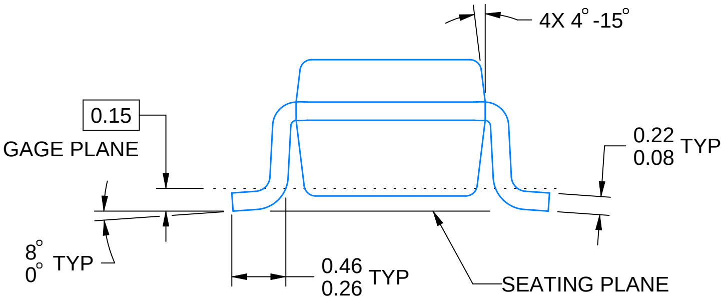


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

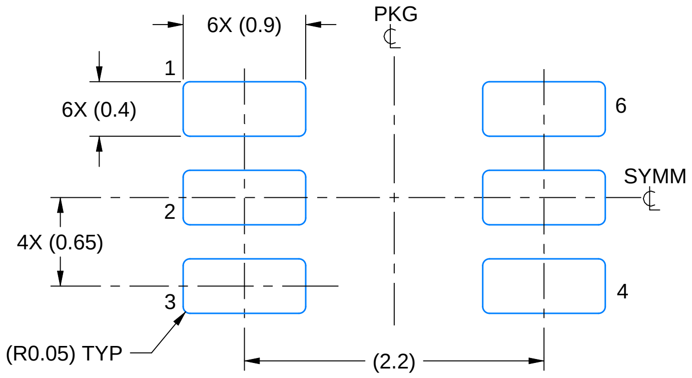

2.4
1.8
1.4
1.1
B
A
C
PIN 1
INDEX AREA
1
2
3
4
6
4X 0.65
1.3
2.15
1.85
6X 0.30
0.15
⌖ 0.1Ⓜ C A B
NOTE 5
0.1 C
1.1
0.8
4X 0° -12°
0.1
0.0 TYP


4X 4° -15°
0.15
GAGE PLANE
0.22
0.08 TYP
8°
0° TYP
0.46
0.26 TYP
SEATING PLANE

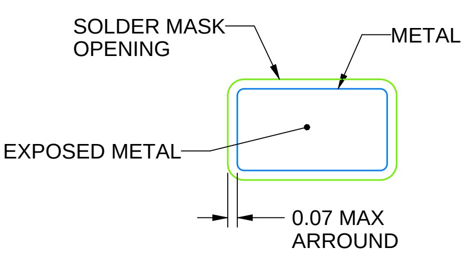
4214835/D 11/2024

NOTES:

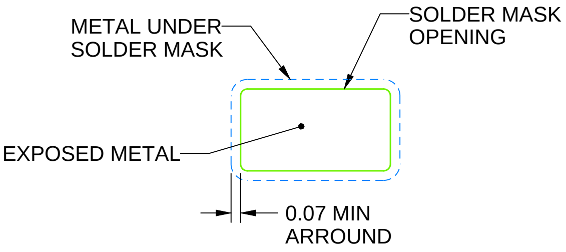
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.


6X (0.9)
PKG
℄
1
6X (0.4)
6
SYMM
℄
2
4X (0.65)
3
4
(R0.05) TYP
(2.2)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X


SOLDER MASK
OPENING
METAL
EXPOSED METAL
0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

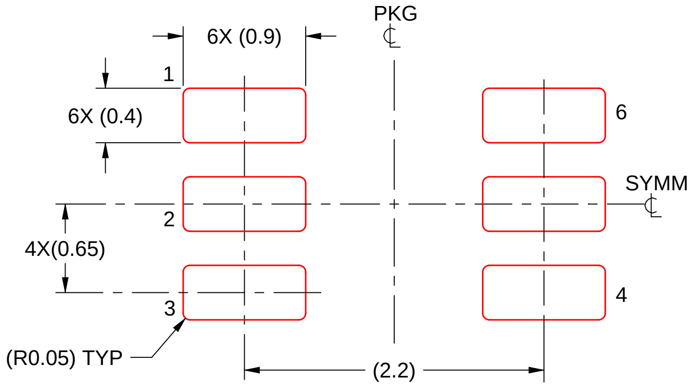

METAL UNDER
SOLDER MASK
SOLDER MASK
OPENING
EXPOSED METAL
0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

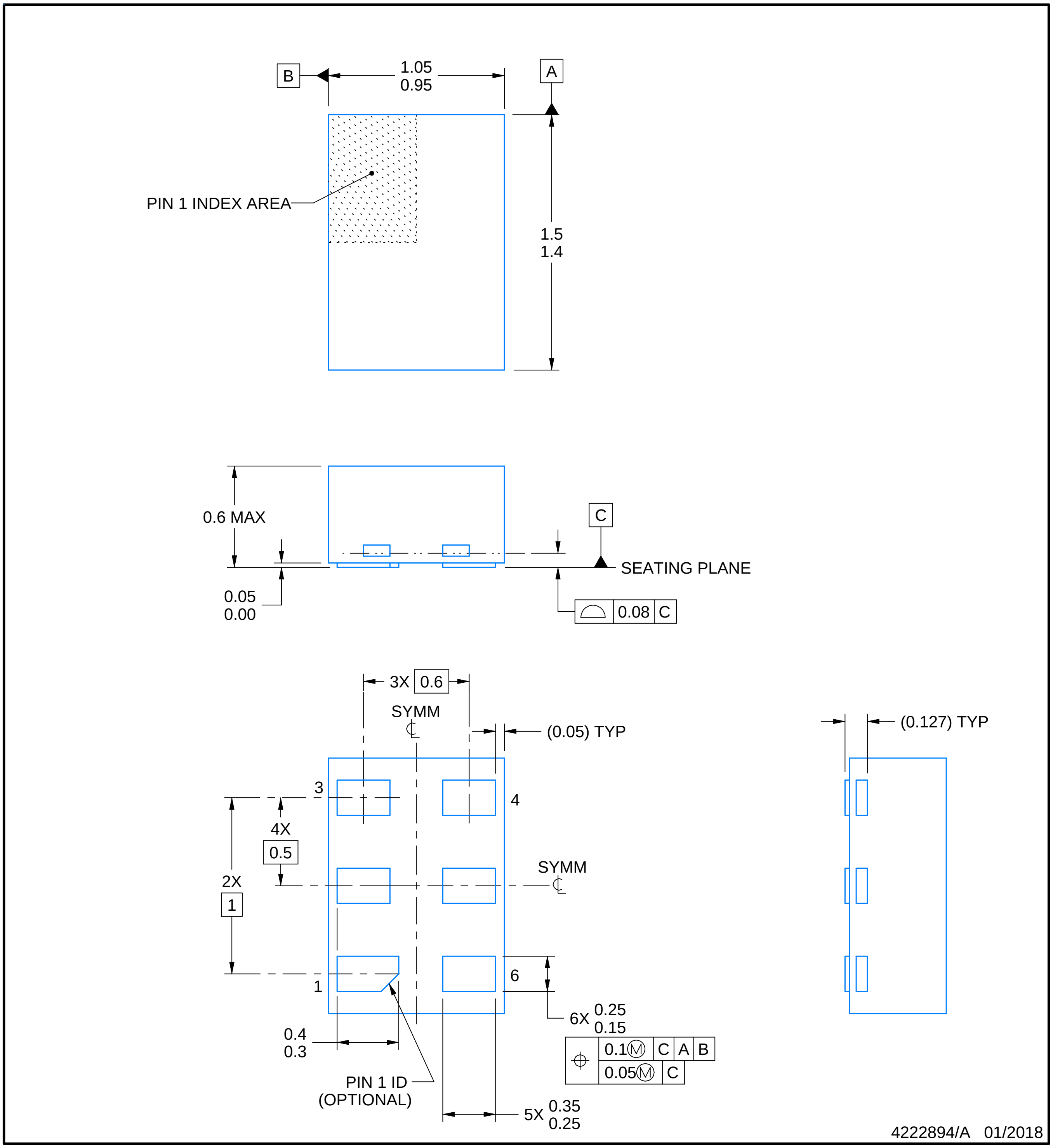
GENERIC PACKAGE VIEW

DRY 6 **USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

TEXAS INSTRUMENTS

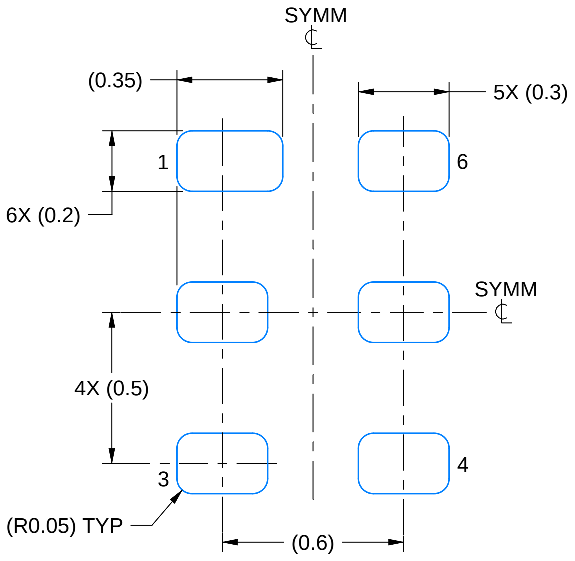
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.


B
1.05
0.95
A
PIN 1 INDEX AREA
1.5
1.4
0.6 MAX
C
SEATING PLANE
0.05
0.00
0.08 C
3X 0.6
SYMM
(0.05) TYP
(0.127) TYP
3
4
4X 0.5
2X 1
SYMM
1
6
0.4
0.3
6X 0.25 0.15
0.1Ⓜ C A B
0.05Ⓜ C
PIN 1 ID (OPTIONAL)
5X 0.35 0.25

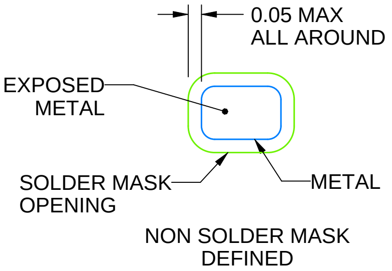
4222894/A 01/2018

NOTES:

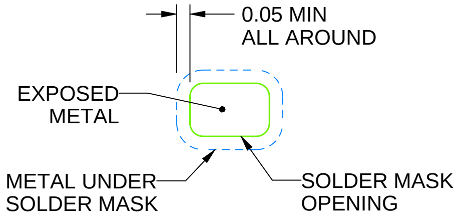
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.


SYMM
℄
(0.35)
5X (0.3)
1
6
6X (0.2)
SYMM
℄
4X (0.5)
3
4
(R0.05) TYP
(0.6)

LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X


0.05 MAX
ALL AROUND
EXPOSED
METAL
SOLDER MASK
OPENING
METAL

NON SOLDER MASK
DEFINED


0.05 MIN
ALL AROUND
EXPOSED
METAL
METAL UNDER
SOLDER MASK
SOLDER MASK
OPENING

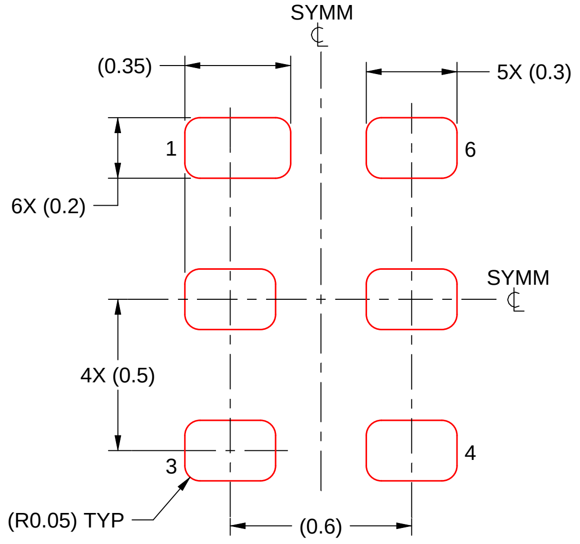
SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

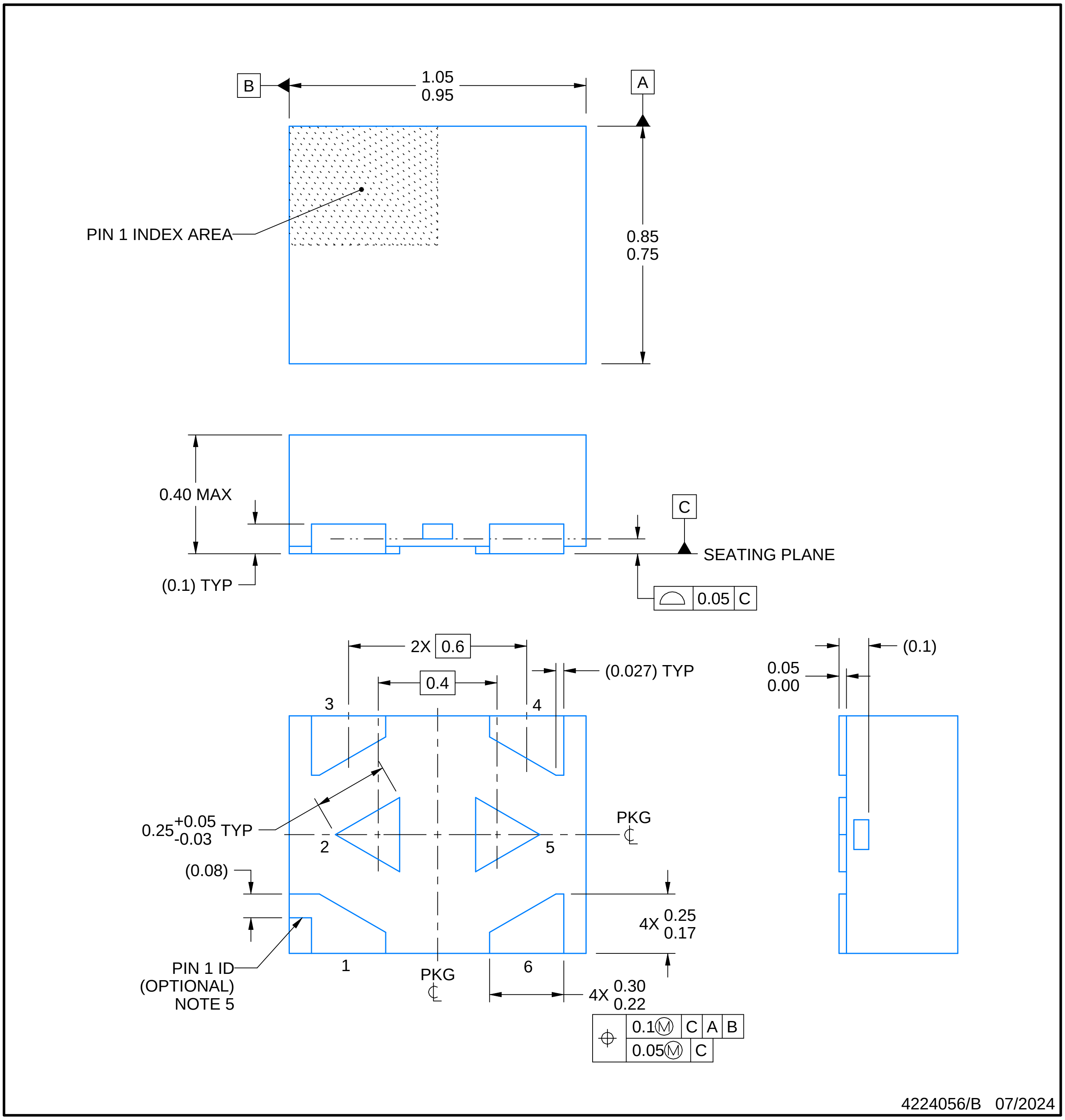
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).


SYMM
℄
(0.35)
5X (0.3)
1
6
6X (0.2)
SYMM
℄
4X (0.5)
3
4
(R0.05) TYP
(0.6)

SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

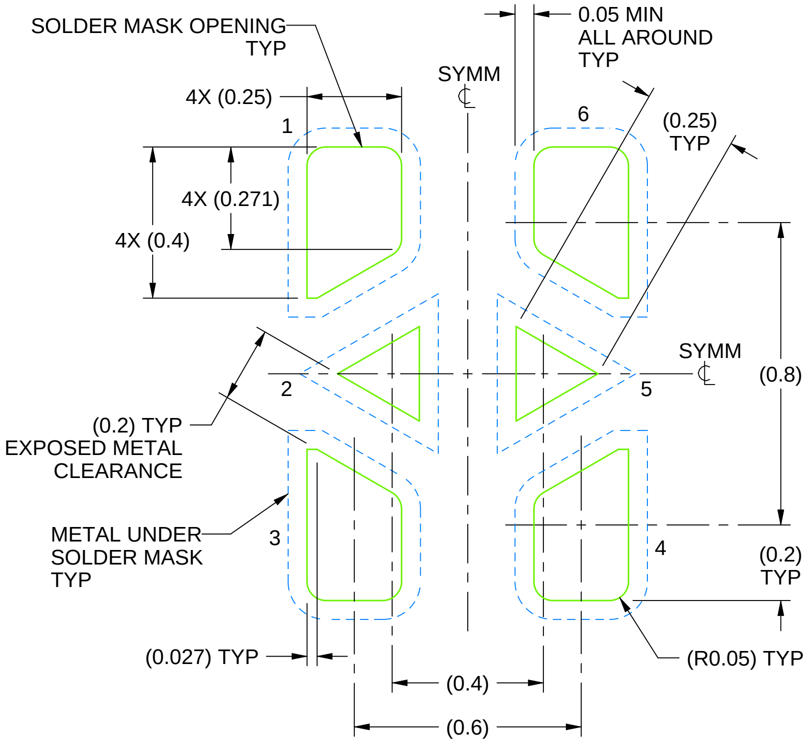
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.


B
1.05
0.95
A
PIN 1 INDEX AREA
0.85
0.75
0.40 MAX
C
SEATING PLANE
(0.1) TYP
0.05 C
2X 0.6
0.4
(0.027) TYP
0.05
0.00
(0.1)
3
4
0.25 +0.05 -0.03 TYP
2
5
PKG ℄
(0.08)
4X 0.25
0.17
PIN 1 ID
(OPTIONAL)
NOTE 5
1
PKG ℄
6
4X 0.30
0.22
0.1Ⓜ C A B
0.05Ⓜ C
4224056/B 07/2024

NOTES:

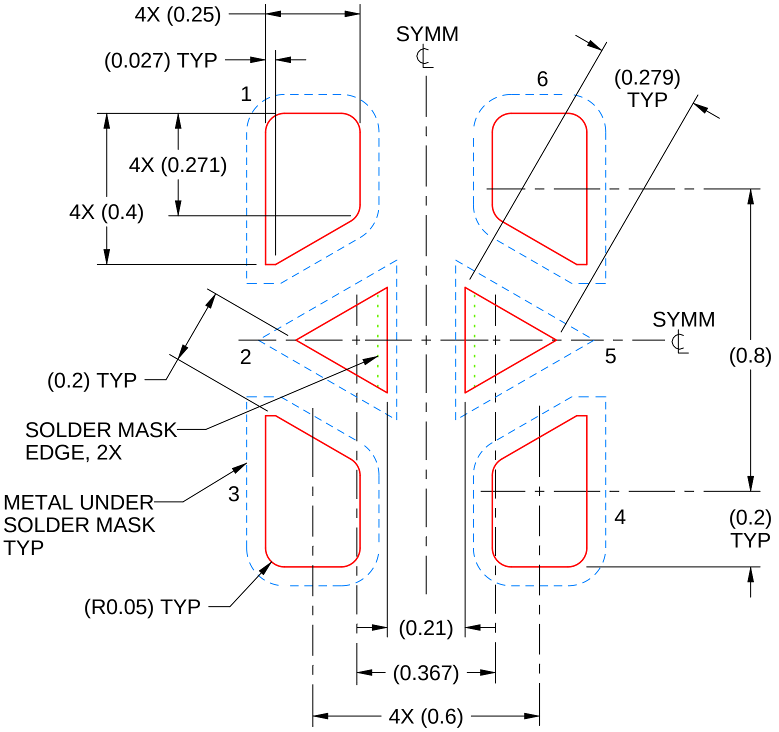
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.


SOLDER MASK OPENING
TYP
0.05 MIN
ALL AROUND
TYP
SYMM
℄
4X (0.25)
1
6
(0.25)
TYP
4X (0.271)
4X (0.4)
SYMM
℄
2
5
(0.8)
(0.2) TYP
EXPOSED METAL
CLEARANCE
METAL UNDER
SOLDER MASK
TYP
3
4
(0.2)
TYP
(0.027) TYP
(R0.05) TYP
(0.4)
(0.6)

LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

NOTES: (continued)

6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.


4X (0.25)
(0.027) TYP
SYMM
℄
6
(0.279)
TYP
1
4X (0.271)
4X (0.4)
SYMM
℄
2
5
(0.8)
(0.2) TYP
SOLDER MASK
EDGE, 2X
METAL UNDER
SOLDER MASK
TYP
3
4
(0.2)
TYP
(R0.05) TYP
(0.21)
(0.367)
4X (0.6)

SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月