SN74AXCH8T245 構成可能な電圧変換、TRI-STATE出力、バス・ホールド回路を搭載した8ビット・デュアル電源バス・トランシーバ

1 特長

- 認定済みの完全に構成可能なデュアル・レール設計により、各ポートは0.65V～3.6Vの範囲の電源電圧で動作可能
- 動作温度範囲: -40℃～+125℃
- データ入力時のバス・ホールドにより、外部のプルアップまたはプルダウン抵抗が不要
- 複数の方向制御ピンにより、昇圧と降圧の変換を同時に実行
- 最高380Mbpsをサポート（1.8Vから3.3Vへの変換時）
- V_{CC}絶縁機能により、電源オフ時に両方のバスを実質的に絶縁
- 部分的パワーダウン・モードにより、電源オフ時にバックフロー電流を制限
- SN74AVCH8T245および74AVCH8T245レベル・シフタと互換
- JESD 78、Class II準拠で100mA超のラッチアップ性能
- JESD 22を超えるESD保護
  - 人体モデルで8000V
  - 荷電デバイス・モデルで1000V

2 アプリケーション

- エンタープライズおよび通信
- ワイヤレス・インフラ
- ビルディング・オートメーション
- データ・センター向けスイッチ
- エンタープライズ用ソリッド・ステート・ドライブ
- ラック・サーバー
- EPOS

3 概要

SN74AXCH8T245デバイスは、8ビットの非反転バス・トランシーバで、最新の電圧ノード(0.7V、0.8V、0.9V)で動作しているデバイスと、業界標準の電圧ノード(1.8V、2.5V、3.3V)で動作しているデバイスとの間で、電圧レベル不一致の問題を双方向に解決できます。

このデバイスは、2つの独立した電源レール（V_{CCA}とV_{CCB}）を使用して動作します。データ・ピンA1～A8はV_{CCA}に追従し、データ・ピンB1～B8はV_{CCB}に追従するよう設計されています。どちらの電源レールも0.65V～3.6Vの任意の電圧で動作します。また、SN74AXCH8T245は単一電源システムとも互換性があります。

SN74AXCH8T245デバイスは、データ・バス間の非同期通信用に設計されています。このデバイスは、方向制御(DIR1およびDIR2)入力の論理レベルに応じて、AバスからBバス、またはBバスからAバスにデータを転送します。出力イネーブル($\overline{OE}$)入力を使用すると、出力をディセーブルにして、バスを実質的に絶縁できます。

SN74AXCH8T245デバイスは、制御ピン(DIRおよび$\overline{OE}$)がV_{CCA}を基準とするよう設計されています。

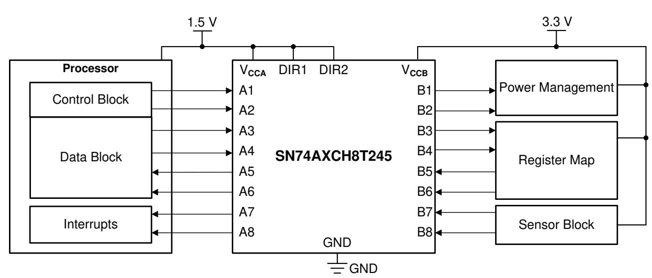
アクティブなバス・ホールド回路により、使用されていない、または駆動されていないピンは、有効なロジック状態に保持されます。バス・ホールド回路と、プルアップまたはプルダウン抵抗との併用は推奨しません。V_{CCA}またはV_{CCB}に電源が存在する場合、バス・ホールド回路は対応するすべてのAおよびBポートについて、方向制御や出力イネーブルとは独立に、常時アクティブに維持されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
SN74AXCH8T245PW	TSSOP (24)	7.80mm×4.40mm
SN74AXCH8T245RHL	VQFN (24)	5.50mm×3.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



目次

4 改訂履歴

から変更 **Original (August 2018) to Revision A** **Page**

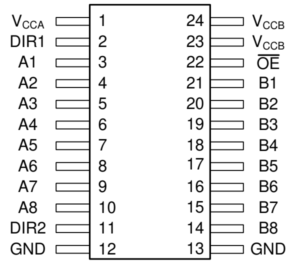
5 概要(続き)

このデバイスは、I_{off}を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。I_{off}回路は、デバイスの電源がオフになったとき、出力をディセーブルにします。これによってデバイスへの電流の逆流が抑止され、デバイスが損傷から保護されます。

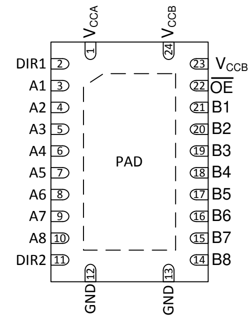
V_{CC}絶縁機能により、いずれかのV_{CC}入力電圧が100mV未満になると、すべてのレベル・シフタ出力がディセーブルされ、高インピーダンス状態になります。電源投入時または切断時にレベル・シフタI/Oが高インピーダンス状態であることを保証するため、$\overline{OE}$はプルアップ抵抗を経由してV_{CCA}に接続する必要があります。この抵抗の最小値は、ドライバの電流シンク能力によって決まります。

6 Pin Configuration and Functions

PW Package
24-Pin TSSOP
Top View



RHL Package(1)
24-Pin VQFN
Top View



(1) PAD - may be grounded (recommended) or left floating.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	PW, RHL		
A1	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	I/O	Input/output A4. Referenced to V_{CCA}.
A5	7	I/O	Input/output A5. Referenced to V_{CCA}.
A6	8	I/O	Input/output A6. Referenced to V_{CCA}.
A7	9	I/O	Input/output A7. Referenced to V_{CCA}.
A8	10	I/O	Input/output A8. Referenced to V_{CCA}.
B1	21	I/O	Input/output B1. Referenced to V_{CCB}.
B2	20	I/O	Input/output B2. Referenced to V_{CCB}.
B3	19	I/O	Input/output B3. Referenced to V_{CCB}.
B4	18	I/O	Input/output B4. Referenced to V_{CCB}.
B5	17	I/O	Input/output B5. Referenced to V_{CCB}.
B6	16	I/O	Input/output B6. Referenced to V_{CCB}.
B7	15	I/O	Input/output B7. Referenced to V_{CCB}.
B8	14	I/O	Input/output B8. Referenced to V_{CCB}.
DIR1	2	I	Direction-control signal. Referenced to V_{CCA}.
DIR2	11	I	Direction-control signal. Referenced to V_{CCA}. See *Multiple Direction Control Pins* for additional details. Tie to GND to maintain backwards compatibility with the SN74AVCH8T245 device.
GND	12	—	Ground
	13	—	Ground
$\overline{OE}$	22	I	Output Enable. Pull to GND to enable all outputs. Pull to V_{CCA} to place all outputs in high-impedance mode. Referenced to V_{CCA}.
V_{CCA}	1	—	A-port supply voltage. 0.65 V ≤ V_{CCA} ≤ 3.6 V
V_{CCB}	23	—	B-port supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V
	24	—	B-port supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CCA}		–0.5	4.2	V
Supply voltage, V_{CCB}		–0.5	4.2	V
Input voltage, V_I (2)	I/O ports (A port)	–0.5	4.2	V
	I/O ports (B port)	–0.5	4.2	
	Control inputs	–0.5	4.2	
Voltage applied to any output in the high-impedance or power-off state, V_O (2)	A port	–0.5	4.2	V
	B port	–0.5	4.2	
Voltage applied to any output in the high or low state, V_O (2) (3)	A port	–0.5	V_{CCA} + 0.2	V
	B port	–0.5	V_{CCB} + 0.2	
Input clamp current, I_{IK}	$V_I < 0$	–50		mA
Output clamp current, I_{OK}	$V_O < 0$	–50		mA
Continuous output current, I_O		–50	50	mA
Continuous current through V_{CCA}, V_{CCB}, or GND		–100	100	mA
Junction Temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage			0.65	3.6	V
V_{CCB}	Supply voltage			0.65	3.6	V
V_{IH}	High-level input voltage	Data inputs	V_{CCI} = 0.65 V - 0.75 V	V_{CCI} × 0.70		V
			V_{CCI} = 0.76 V - 1 V	V_{CCI} × 0.70		
			V_{CCI} = 1.1 V - 1.95 V	V_{CCI} × 0.65		
			V_{CCI} = 2.3 V - 2.7 V	1.6		
			V_{CCI} = 3 V - 3.6 V	2		
		Control inputs (DIR, $\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V	V_{CCA} × 0.70		
			V_{CCA} = 0.76 V - 1 V	V_{CCA} × 0.70		
			V_{CCA} = 1.1 V - 1.95 V	V_{CCA} × 0.65		
			V_{CCA} = 2.3 V - 2.7 V	1.6		
			V_{CCA} = 3 V - 3.6 V	2		
V_{IL}	Low-level input voltage	Data inputs	V_{CCI} = 0.65 V - 0.75 V		V_{CCI} × 0.30	V
			V_{CCI} = 0.76 V - 1 V		V_{CCI} × 0.30	
			V_{CCI} = 1.1 V - 1.95 V		V_{CCI} × 0.35	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3 V - 3.6 V		0.8	
		Control inputs (DIR, $\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V		V_{CCA} × 0.30	
			V_{CCA} = 0.76 V - 1 V		V_{CCA} × 0.30	
			V_{CCA} = 1.1 V - 1.95 V		V_{CCA} × 0.35	
			V_{CCA} = 2.3 V - 2.7 V		0.7	
			V_{CCA} = 3 V - 3.6 V		0.8	
V_I	Input voltage(3)			0	3.6	V
V_O	Output voltage	Active state		0	V_{CCO} (2)	V
		Tri-state		0	3.6	
Δt/Δv	Input transition rise or fall rate				10	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

7.4 Thermal Information

THERMAL METRIC(1)		SN74AXCH8T245		UNIT
		PW (TSSOP)	RHL (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.7	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.4	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.9	13.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.0	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.4	13.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	–40°C to 85°C MIN	–40°C to 85°C TYP(2)	–40°C to 85°C MAX	–40°C to 125°C MIN	–40°C to 125°C TYP(2)	–40°C to 125°C MAX	UNIT
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = –100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = –50 µA	0.65 V	0.65 V	0.55			0.55			
			I_{OH} = –200 µA	0.76 V	0.76 V	0.58			0.58			
			I_{OH} = –500 µA	0.85 V	0.85 V	0.65			0.65			
			I_{OH} = -3 mA	1.1 V	1.1 V	0.85			0.85			
			I_{OH} = -6 mA	1.4 V	1.4 V	1.05			1.05			
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			1.2			
			I_{OH} = -9 mA	2.3 V	2.3 V	1.75			1.75			
			I_{OH} = -12 mA	3 V	3 V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V			0.1			0.1	V
			I_{OL} = 50 µA	0.65 V	0.65 V			0.1			0.1	
			I_{OL} = 200 µA	0.76 V	0.76 V			0.18			0.18	
			I_{OL} = 500 µA	0.85 V	0.85 V			0.2			0.2	
			I_{OL} = 3 mA	1.1 V	1.1 V			0.25			0.25	
			I_{OL} = 6 mA	1.4 V	1.4 V			0.35			0.35	
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7			0.7	
I_{BHL}	Bus-hold low sustaining current (3)	V_I= 0.20 V		0.65 V	0.65 V	4			4			µA
		V_I= 0.23 V		0.76 V	0.76 V	8			7			
		V_I= 0.26 V		0.85 V	0.85 V	10			10			
		V_I= 0.39 V		1.1 V	1.1 V	20			20			
		V_I= 0.49 V		1.4 V	1.4 V	40			30			
		V_I= 0.58 V		1.65 V	1.65 V	55			45			
		V_I= 0.7 V		2.3 V	2.3 V	90			80			
		V_I= 0.8 V		3 V	3 V	145			135			
I_{BHH}	Bus-hold high sustaining current (4)	V_I= 0.45 V		0.65 V	0.65 V	–4			–4			µA
		V_I= 0.53 V		0.76 V	0.76 V	–8			–7			
		V_I= 0.59 V		0.85 V	0.85 V	–10			–10			
		V_I= 0.71 V		1.1 V	1.1 V	–20			–20			
		V_I= 0.91 V		1.4 V	1.4 V	–40			–30			
		V_I= 1.07 V		1.65 V	1.65 V	–55			–45			
		V_I= 1.6 V		2.3 V	2.3 V	–90			–80			
		V_I= 2.0 V		3 V	3 V	–145			–135			
I_{BHLO}	Bus-hold low overdrive current (5)	V_I= 0 to V_{CC}		0.75 V	0.75 V	40			40			µA
				0.84 V	0.84 V	50			50			
				0.95 V	0.95 V	65			65			
				1.3 V	1.3 V	105			105			
				1.6 V	1.6 V	150			150			
				1.95 V	1.95 V	205			205			
				2.7 V	2.7 V	335			335			
				3.6V	3.6V	480			480			

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) All typical values are for T_A = 25°C.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}(MAX). I_{BHL} should be measured after lowering V_I to GND and then raising it to V_{IL}(MAX).
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}(MIN). I_{BHH} should be measured after raising V_I to V_{CC} and then lowering it to V_{IH}(MIN).
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.

Electrical Characteristics (continued)

Over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	–40°C to 85°C			–40°C to 125°C			UNIT
					MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
I_{BHHO}	Bus-hold high overdrive current (6)	V_I= 0 to V_{CC}	0.75 V	0.75 V	–40			–40			µA
			0.84 V	0.84 V	–50			–50			
			0.95 V	0.95 V	–65			–65			
			1.3 V	1.3 V	–105			–105			
			1.6 V	1.6 V	–150			–150			
			1.95 V	1.95 V	–205			–205			
			2.7 V	2.7 V	–335			–335			
			3.6V	3.6V	–480			–480			
I_I	Input leakage current	Control Inputs (DIR, $\overline{OE}$): V_I = V_{CCA} or GND	0.65 V - 3.6 V	0.65 V - 3.6 V	–0.5		0.5	–1		1	µA
I_{off}	Partial power down current	A Port: V_I or V_O = 0 V - 3.6 V	0 V	0 V - 3.6 V	–8		8	–12		12	µA
		B Port: V_I or V_O = 0 V - 3.6 V	0 V - 3.6 V	0 V	–8		8	–12		12	
I_{OZ}	High-impedance state output current	A Port: V_O = V_{CCO} or GND, V_I = V_{CCI} or GND, $\overline{OE}$ = V_{IH}	3.6 V	3.6 V	–8		8	–12		12	µA
		B Port: V_O = V_{CCO} or GND, V_I = V_{CCI} or GND, $\overline{OE}$ = V_{IH}	3.6 V	3.6 V	–8		8	–12		12	
I_{CCA}	V_{CCA} supply current	V_I = V_{CCI} or GND, I_O = 0 mA	0.65 V - 3.6 V	0.65 V - 3.6 V			20			42	µA
			0 V	3.6 V	–2			–12			
			3.6 V	0 V			13			27	
I_{CCB}	V_{CCB} supply current	V_I = V_{CCI} or GND, I_O = 0 mA	0.65 V - 3.6 V	0.65 V - 3.6 V			20			40	µA
			0 V	3.6 V			13			27	
			3.6 V	0 V	–2			–12			
I_{CCA} + I_{CCB}	Combined supply current	V_I = V_{CCI} or GND, I_O = 0 mA	0.65 V - 3.6 V	0.65 V - 3.6 V			30			60	µA
C_i	Input capacitance	Control Inputs (DIR, $\overline{OE}$): V_I = 3.3 V or GND	3.3 V	3.3 V		4.5			4.5		pF
C_{io}	Data I/O capacitance	Ports A and B: $\overline{OE}$ = V_{CCA}, V_O = 1.65V DC + 1 MHz -16 dBm sine wave	3.3 V	3.3 V		7.3			7.3		pF

(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

7.6 Switching Characteristics, V_{CCA} = 0.7 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB}) 0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	178	0.5	115	0.5	83	0.5	49	ns
			–40°C to 125°C	0.5	178	0.5	115	0.5	83	0.5	49	
		B input to A output	–40°C to 85°C	0.5	178	0.5	159	0.5	132	0.5	94	
			–40°C to 125°C	0.5	178	0.5	159	0.5	132	0.5	94	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	194	0.5	194	0.5	194	0.5	194	ns
			–40°C to 125°C	0.5	194	0.5	194	0.5	194	0.5	194	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	216	0.5	179	0.5	158	0.5	78	
			–40°C to 125°C	0.5	216	0.5	179	0.5	158	0.5	78	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	240	0.5	240	0.5	240	0.5	240	ns
			–40°C to 125°C	0.5	240	0.5	240	0.5	240	0.5	240	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	292	0.5	180	0.5	125	0.5	76	
			–40°C to 125°C	0.5	292	0.5	180	0.5	125	0.5	76	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB}) 1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	47	0.5	50	0.5	62	0.5	151	ns
			–40°C to 125°C	0.5	47	0.5	50	0.5	62	0.5	151	
		B input to A output	–40°C to 85°C	0.5	89	0.5	88	0.5	87	0.5	86	
			–40°C to 125°C	0.5	89	0.5	88	0.5	87	0.5	86	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	194	0.5	194	0.5	194	0.5	194	ns
			–40°C to 125°C	0.5	194	0.5	194	0.5	194	0.5	194	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	70	0.5	69	0.5	67	0.5	101	
			–40°C to 125°C	0.5	70	0.5	69	0.5	67	0.5	101	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	240	0.5	240	0.5	240	0.5	240	ns
			–40°C to 125°C	0.5	240	0.5	240	0.5	240	0.5	240	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	69	0.5	69	0.5	84	0.5	552	
			–40°C to 125°C	0.5	69	0.5	69	0.5	84	0.5	552	

7.7 Switching Characteristics, V_{CCA} = 0.8 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	159	0.5	96	0.5	64	0.5	33	ns
			–40°C to 125°C	0.5	159	0.5	96	0.5	64	0.5	33	
		B input to A output	–40°C to 85°C	0.5	117	0.5	97	0.5	79	0.5	54	
			–40°C to 125°C	0.5	117	0.5	97	0.5	79	0.5	54	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	154	0.5	154	0.5	154	0.5	154	ns
			–40°C to 125°C	0.5	154	0.5	154	0.5	154	0.5	154	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	202	0.5	165	0.5	144	0.5	65	
			–40°C to 125°C	0.5	202	0.5	165	0.5	144	0.5	65	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	137	0.5	137	0.5	137	0.5	137	ns
			–40°C to 125°C	0.5	137	0.5	137	0.5	137	0.5	137	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	270	0.5	160	0.5	104	0.5	55	
			–40°C to 125°C	0.5	270	0.5	160	0.5	104	0.5	55	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	27	0.5	26	0.5	26	0.5	35	ns
			–40°C to 125°C	0.5	27	0.5	26	0.5	26	0.5	35	
		B input to A output	–40°C to 85°C	0.5	44	0.5	43	0.5	42	0.5	41	
			–40°C to 125°C	0.5	44	0.5	43	0.5	42	0.5	41	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	154	0.5	154	0.5	154	0.5	154	ns
			–40°C to 125°C	0.5	154	0.5	154	0.5	154	0.5	154	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	57	0.5	55	0.5	50	0.5	52	
			–40°C to 125°C	0.5	57	0.5	55	0.5	50	0.5	52	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	137	0.5	137	0.5	137	0.5	137	ns
			–40°C to 125°C	0.5	137	0.5	137	0.5	137	0.5	137	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	46	0.5	44	0.5	46	0.5	59	
			–40°C to 125°C	0.5	46	0.5	44	0.5	46	0.5	59	

7.8 Switching Characteristics, V_{CCA} = 0.9 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to output	–40°C to 85°C	0.5	133	0.5	79	0.5	53	0.5	23	ns
			–40°C to 125°C	0.5	133	0.5	79	0.5	53	0.5	23	
		B input to A output	–40°C to 85°C	0.5	84	0.5	64	0.5	53	0.5	41	
			–40°C to 125°C	0.5	84	0.5	64	0.5	53	0.5	41	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	130	0.5	130	0.5	130	0.5	130	ns
			–40°C to 125°C	0.5	130	0.5	130	0.5	130	0.5	130	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	193	0.5	157	0.5	137	0.5	57	
			–40°C to 125°C	0.5	193	0.5	157	0.5	137	0.5	57	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	128	0.5	128	0.5	128	0.5	128	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	257	0.5	149	0.5	94	0.5	45	
			–40°C to 125°C	0.5	257	0.5	149	0.5	94	0.5	45	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	18	0.5	16	0.5	15	0.5	18	ns
			–40°C to 125°C	0.5	18	0.5	16	0.5	15	0.5	18	
		B input to A output	–40°C to 85°C	0.5	29	0.5	25	0.5	23	0.5	22	
			–40°C to 125°C	0.5	29	0.5	25	0.5	23	0.5	22	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	130	0.5	130	0.5	130	0.5	130	ns
			–40°C to 125°C	0.5	130	0.5	130	0.5	130	0.5	130	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	50	0.5	48	0.5	42	0.5	43	
			–40°C to 125°C	0.5	50	0.5	48	0.5	42	0.5	43	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	128	0.5	128	0.5	128	0.5	128	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	37	0.5	34	0.5	32	0.5	36	
			–40°C to 125°C	0.5	37	0.5	34	0.5	32	0.5	36	

7.9 Switching Characteristics, V_{CCA} = 1.2 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB}) 0.7 V ± 0.05 V MIN	0.7 V ± 0.05 V MAX	0.8 V ± 0.04 V MIN	0.8 V ± 0.04 V MAX	0.9 V ± 0.045 V MIN	0.9 V ± 0.045 V MAX	1.2 V ± 0.1 V MIN	1.2 V ± 0.1 V MAX	UNIT
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	95	0.5	54	0.5	40	0.5	15	ns
			–40°C to 125°C	0.5	95	0.5	54	0.5	40	0.5	15	
		B input to A output	–40°C to 85°C	0.5	49	0.5	33	0.5	23	0.5	15	
			–40°C to 125°C	0.5	49	0.5	33	0.5	23	0.5	15	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	47	0.5	47	0.5	47	0.5	47	ns
			–40°C to 125°C	0.5	47	0.5	47	0.5	47	0.5	47	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	181	0.5	147	0.5	127	0.5	49	
			–40°C to 125°C	0.5	181	0.5	147	0.5	127	0.5	49	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	40	0.5	40	0.5	40	0.5	40	ns
			–40°C to 125°C	0.5	40	0.5	40	0.5	40	0.5	40	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	221	0.5	132	0.5	81	0.5	34	
			–40°C to 125°C	0.5	221	0.5	132	0.5	81	0.5	34	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB}) 1.5 V ± 0.1 V MIN	1.5 V ± 0.1 V MAX	1.8 V ± 0.15 V MIN	1.8 V ± 0.15 V MAX	2.5 V ± 0.2 V MIN	2.5 V ± 0.2 V MAX	3.3 V ± 0.3 V MIN	3.3 V ± 0.3 V MAX	UNIT
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	11	0.5	9	0.5	8	0.5	8	ns
			–40°C to 125°C	0.5	11	0.5	9	0.5	8	0.5	8	
		B input to A output	–40°C to 85°C	0.5	12	0.5	10	0.5	8	0.5	8	
			–40°C to 125°C	0.5	12	0.5	10	0.5	8	0.5	8	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	47	0.5	47	0.5	47	0.5	47	ns
			–40°C to 125°C	0.5	47	0.5	47	0.5	47	0.5	47	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	42	0.5	40	0.5	34	0.5	34	
			–40°C to 125°C	0.5	42	0.5	40	0.5	34	0.5	34	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	39	0.5	40	0.5	40	0.5	40	ns
			–40°C to 125°C	0.5	39	0.5	40	0.5	40	0.5	40	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	25	0.5	22	0.5	20	0.5	19	
			–40°C to 125°C	0.5	25	0.5	22	0.5	20	0.5	19	

7.10 Switching Characteristics, V_{CCA} = 1.5 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	90	0.5	44	0.5	29	0.5	12	ns
			–40°C to 125°C	0.5	90	0.5	44	0.5	29	0.5	12	
		B input to A output	–40°C to 85°C	0.5	47	0.5	27	0.5	18	0.5	11	
			–40°C to 125°C	0.5	47	0.5	27	0.5	18	0.5	11	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	ns
			–40°C to 125°C	0.5	37	0.5	37	0.5	37	0.5	37	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	176	0.5	142	0.5	122	0.5	44	
			–40°C to 125°C	0.5	176	0.5	142	0.5	122	0.5	44	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	ns
			–40°C to 125°C	0.5	25	0.5	25	0.5	25	0.5	25	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	214	0.5	114	0.5	71	0.5	29	
			–40°C to 125°C	0.5	214	0.5	114	0.5	71	0.5	29	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	9	0.5	8	0.5	6	0.5	6	ns
			–40°C to 125°C	0.5	9	0.5	8	0.5	6	0.5	6	
		B input to A output	–40°C to 85°C	0.5	9	0.5	8	0.5	6	0.5	5	
			–40°C to 125°C	0.5	9	0.5	8	0.5	6	0.5	5	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	ns
			–40°C to 125°C	0.5	37	0.5	37	0.5	37	0.5	37	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	38	0.5	37	0.5	31	0.5	31	
			–40°C to 125°C	0.5	38	0.5	37	0.5	31	0.5	31	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	ns
			–40°C to 125°C	0.5	25	0.5	25	0.5	25	0.5	25	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	21	0.5	18	0.5	15	0.5	13	
			–40°C to 125°C	0.5	21	0.5	18	0.5	15	0.5	13	

7.11 Switching Characteristics, V_{CCA} = 1.8 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	88	0.5	43	0.5	25	0.5	10	ns
			–40°C to 125°C	0.5	88	0.5	43	0.5	25	0.5	10	
		B input to A output	–40°C to 85°C	0.5	50	0.5	26	0.5	16	0.5	9	
			–40°C to 125°C	0.5	50	0.5	26	0.5	16	0.5	9	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	35	0.5	35	0.5	35	0.5	35	ns
			–40°C to 125°C	0.5	35	0.5	35	0.5	35	0.5	35	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	174	0.5	139	0.5	119	0.5	42	
			–40°C to 125°C	0.5	174	0.5	139	0.5	119	0.5	42	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	20	0.5	20	0.5	20	0.5	20	ns
			–40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	213	0.5	111	0.5	67	0.5	27	
			–40°C to 125°C	0.5	213	0.5	111	0.5	67	0.5	27	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	8	0.5	7	0.5	6	0.5	5	ns
			–40°C to 125°C	0.5	8	0.5	7	0.5	6	0.5	5	
		B input to A output	–40°C to 85°C	0.5	7	0.5	6	0.5	5	0.5	4	
			–40°C to 125°C	0.5	7	0.5	7	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	35	0.5	35	0.5	35	0.5	35	ns
			–40°C to 125°C	0.5	35	0.5	35	0.5	35	0.5	35	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	36	0.5	35	0.5	30	0.5	29	
			–40°C to 125°C	0.5	36	0.5	35	0.5	30	0.5	29	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	20	0.5	20	0.5	20	0.5	20	ns
			–40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	19	0.5	16	0.5	13	0.5	11	
			–40°C to 125°C	0.5	19	0.5	16	0.5	13	0.5	11	

7.12 Switching Characteristics, V_{CCA} = 2.5 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	87	0.5	42	0.5	23	0.5	8	ns
			–40°C to 125°C	0.5	87	0.5	42	0.5	23	0.5	8	
		B input to A output	–40°C to 85°C	0.5	62	0.5	26	0.5	15	0.5	8	
			–40°C to 125°C	0.5	62	0.5	26	0.5	15	0.5	8	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	28	0.5	28	0.5	28	0.5	28	ns
			–40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	173	0.5	137	0.5	117	0.5	40	
			–40°C to 125°C	0.5	173	0.5	137	0.5	117	0.5	40	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	ns
			–40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	211	0.5	107	0.5	63	0.5	24	
			–40°C to 125°C	0.5	211	0.5	107	0.5	63	0.5	24	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	6	0.5	6	0.5	5	0.5	5	ns
			–40°C to 125°C	0.5	6	0.5	6	0.5	5	0.5	5	
		B input to A output	–40°C to 85°C	0.5	6	0.5	6	0.5	5	0.5	4	
			–40°C to 125°C	0.5	6	0.5	6	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	28	0.5	28	0.5	28	0.5	28	ns
			–40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	34	0.5	33	0.5	28	0.5	28	
			–40°C to 125°C	0.5	34	0.5	33	0.5	28	0.5	28	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	ns
			–40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	16	0.5	14	0.5	10	0.5	9	
			–40°C to 125°C	0.5	16	0.5	14	0.5	10	0.5	9	

7.13 Switching Characteristics, V_{CCA} = 3.3 V

See Figure 1 and Figure 2 for test circuit and loading conditions. See Figure 3 and Figure 4 for measurement waveforms.

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	87	0.5	41	0.5	22	0.5	8	ns
			–40°C to 125°C	0.5	87	0.5	41	0.5	22	0.5	8	
		B input to A output	–40°C to 85°C	0.5	151	0.5	36	0.5	18	0.5	8	
			–40°C to 125°C	0.5	151	0.5	36	0.5	18	0.5	8	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	27	0.5	27	0.5	27	0.5	27	ns
			–40°C to 125°C	0.5	27	0.5	27	0.5	27	0.5	27	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	172	0.5	136	0.5	116	0.5	39	
			–40°C to 125°C	0.5	172	0.5	136	0.5	116	0.5	39	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	ns
			–40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	210	0.5	106	0.5	62	0.5	23	
			–40°C to 125°C	0.5	210	0.5	106	0.5	62	0.5	23	

PARAMETER			TEST CONDITION	B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A input to B output	–40°C to 85°C	0.5	5	0.5	5	0.5	4	0.5	4	ns
			–40°C to 125°C	0.5	5	0.5	5	0.5	4	0.5	4	
		B input to A output	–40°C to 85°C	0.5	6	0.5	5	0.5	5	0.5	4	
			–40°C to 125°C	0.5	6	0.5	5	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	27	0.5	27	0.5	27	0.5	27	ns
			–40°C to 125°C	0.5	27	0.5	27	0.5	27	0.5	27	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	33	0.5	32	0.5	27	0.5	27	
			–40°C to 125°C	0.5	33	0.5	32	0.5	27	0.5	27	
t_{en}	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	ns
			–40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	
		$\overline{OE}$ input to B output	–40°C to 85°C	0.5	15	0.5	13	0.5	10	0.5	8	
			–40°C to 125°C	0.5	15	0.5	13	0.5	10	0.5	8	

7.14 Operating Characteristics: T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdA}	Power dissipation capacitance per transceiver (A to B: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		3.0		pF
			V_{CCA} = V_{CCB} = 0.8 V		3.0		
			V_{CCA} = V_{CCB} = 0.9 V		3.0		
			V_{CCA} = V_{CCB} = 1.2 V		3.1		
			V_{CCA} = V_{CCB} = 1.5 V		3.0		
			V_{CCA} = V_{CCB} = 1.8 V		3.2		
			V_{CCA} = V_{CCB} = 2.5 V		3.7		
			V_{CCA} = V_{CCB} = 3.3 V		4.4		
C_{pdA}	Power dissipation capacitance per transceiver (A to B: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		2.5		pF
			V_{CCA} = V_{CCB} = 0.8 V		2.5		
			V_{CCA} = V_{CCB} = 0.9 V		2.6		
			V_{CCA} = V_{CCB} = 1.2 V		2.6		
			V_{CCA} = V_{CCB} = 1.5 V		2.6		
			V_{CCA} = V_{CCB} = 1.8 V		2.7		
			V_{CCA} = V_{CCB} = 2.5 V		3.2		
			V_{CCA} = V_{CCB} = 3.3 V		3.9		
C_{pdA}	Power dissipation capacitance per transceiver (B to A: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		12.6		pF
			V_{CCA} = V_{CCB} = 0.8 V		12.3		
			V_{CCA} = V_{CCB} = 0.9 V		12.4		
			V_{CCA} = V_{CCB} = 1.2 V		12.4		
			V_{CCA} = V_{CCB} = 1.5 V		12.7		
			V_{CCA} = V_{CCB} = 1.8 V		13.6		
			V_{CCA} = V_{CCB} = 2.5 V		17.4		
			V_{CCA} = V_{CCB} = 3.3 V		20.9		
C_{pdA}	Power dissipation capacitance per transceiver (B to A: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.2		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.1		
			V_{CCA} = V_{CCB} = 0.9 V		1.1		
			V_{CCA} = V_{CCB} = 1.2 V		1.0		
			V_{CCA} = V_{CCB} = 1.5 V		1.0		
			V_{CCA} = V_{CCB} = 1.8 V		0.9		
			V_{CCA} = V_{CCB} = 2.5 V		0.9		
			V_{CCA} = V_{CCB} = 3.3 V		0.9		

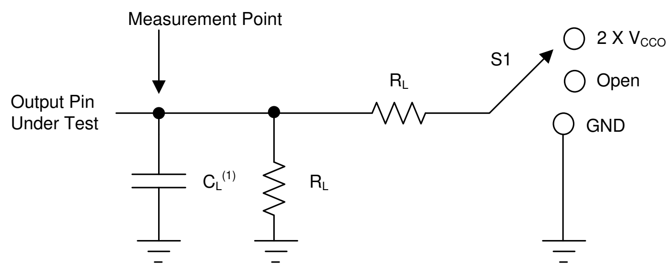
Operating Characteristics: T_A = 25°C (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdB}	Power dissipation capacitance per transceiver (A to B: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		12.6		pF
			V_{CCA} = V_{CCB} = 0.8 V		12.4		
			V_{CCA} = V_{CCB} = 0.9 V		12.4		
			V_{CCA} = V_{CCB} = 1.2 V		12.4		
			V_{CCA} = V_{CCB} = 1.5 V		12.6		
			V_{CCA} = V_{CCB} = 1.8 V		13.6		
			V_{CCA} = V_{CCB} = 2.5 V		17.2		
			V_{CCA} = V_{CCB} = 3.3 V		20.8		
C_{pdB}	Power dissipation capacitance per transceiver (A to B: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.4		
			V_{CCA} = V_{CCB} = 0.8 V		1.3		pF
			V_{CCA} = V_{CCB} = 0.9 V		1.3		
			V_{CCA} = V_{CCB} = 1.2 V		1.2		
			V_{CCA} = V_{CCB} = 1.5 V		1.1		
			V_{CCA} = V_{CCB} = 1.8 V		1.1		
			V_{CCA} = V_{CCB} = 2.5 V		1.1		
			V_{CCA} = V_{CCB} = 3.3 V		1.0		
C_{pdB}	Power dissipation capacitance per transceiver (B to A: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		3.3		pF
			V_{CCA} = V_{CCB} = 0.8 V		3.3		
			V_{CCA} = V_{CCB} = 0.9 V		3.3		
			V_{CCA} = V_{CCB} = 1.2 V		3.2		
			V_{CCA} = V_{CCB} = 1.5 V		3.2		
			V_{CCA} = V_{CCB} = 1.8 V		3.3		
			V_{CCA} = V_{CCB} = 2.5 V		3.6		
			V_{CCA} = V_{CCB} = 3.3 V		4.4		
C_{pdB}	Power dissipation capacitance per transceiver (B to A: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		2.8		
			V_{CCA} = V_{CCB} = 0.8 V		2.8		pF
			V_{CCA} = V_{CCB} = 0.9 V		2.8		
			V_{CCA} = V_{CCB} = 1.2 V		2.8		
			V_{CCA} = V_{CCB} = 1.5 V		2.7		
			V_{CCA} = V_{CCB} = 1.8 V		2.8		
			V_{CCA} = V_{CCB} = 2.5 V		3.1		
			V_{CCA} = V_{CCB} = 3.3 V		3.9		

8 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f =1 MHz
- Z_0 = 50 Ω
- dv / dt ≤ 1 ns/V



(1) C_L includes probe and jig capacitance.

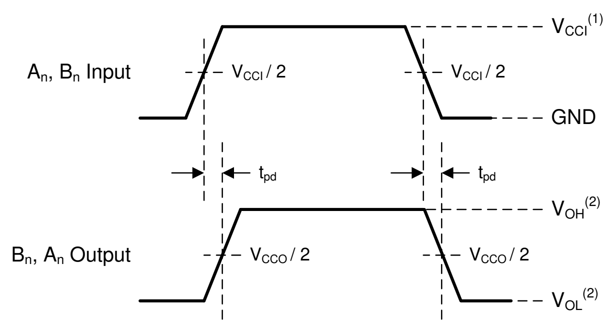
図 1. Load Circuit

Parameter	V_{CCO}	R_L	C_L	S1	V_{TP}
t_{pd}	1.1 V - 3.6 V	2 kΩ	15 pF	Open	N/A
	0.65 V - 0.95 V	20 kΩ	15 pF	Open	N/A
t_{en}(1), t_{dis}(1)	3 V - 3.6 V	2 kΩ	15 pF	2 X V_{CCO}	0.3 V
	1.65 V - 2.7 V	2 kΩ	15 pF	2 X V_{CCO}	0.15 V
	1.1 V - 1.6 V	2 kΩ	15 pF	2 X V_{CCO}	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	2 X V_{CCO}	0.1 V
t_{en}(2), t_{dis}(2)	3 V - 3.6 V	2 kΩ	15 pF	GND	0.3 V
	1.65V - 2.7 V	2 kΩ	15 pF	GND	0.15 V
	1.1 V - 1.6 V	2 kΩ	15 pF	GND	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	GND	0.1 V

(1) Output waveform on the conditions that input is driven to a valid Logic Low.

(2) Output waveform on the condition that input is driven to a valid Logic High.

図 2. Load Circuit Conditions

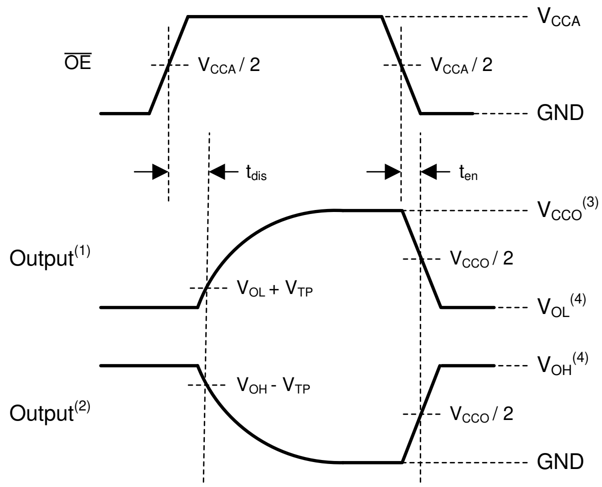


(1) V_{CCI} is the supply pin associated with the input port.

(2) V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

図 3. Propagation Delay

Parameter Measurement Information (continued)



(1) Output waveform on the condition that input is driven to a valid Logic Low.
(2) Output waveform on the condition that input is driven to a valid Logic High.
(3) V_{CCO} is the supply pin associated with the output port.
(4) V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

図 4. Enable Time And Disable Time

9 Detailed Description

9.1 Overview

The SN74AXCH8T245 device is an 8-bit, dual-supply non-inverting transceiver with bidirectional voltage level translation. The I/O pins labeled with A and the control pins (DIR1, DIR2, and $\overline{OE}$) are supported by V_{CCA}, and the I/O pins labeled with B are supported by V_{CCB}. Both the A port and the B port are able to accept I/O voltages ranging from 0.65 V to 3.6 V.

9.2 Functional Block Diagram

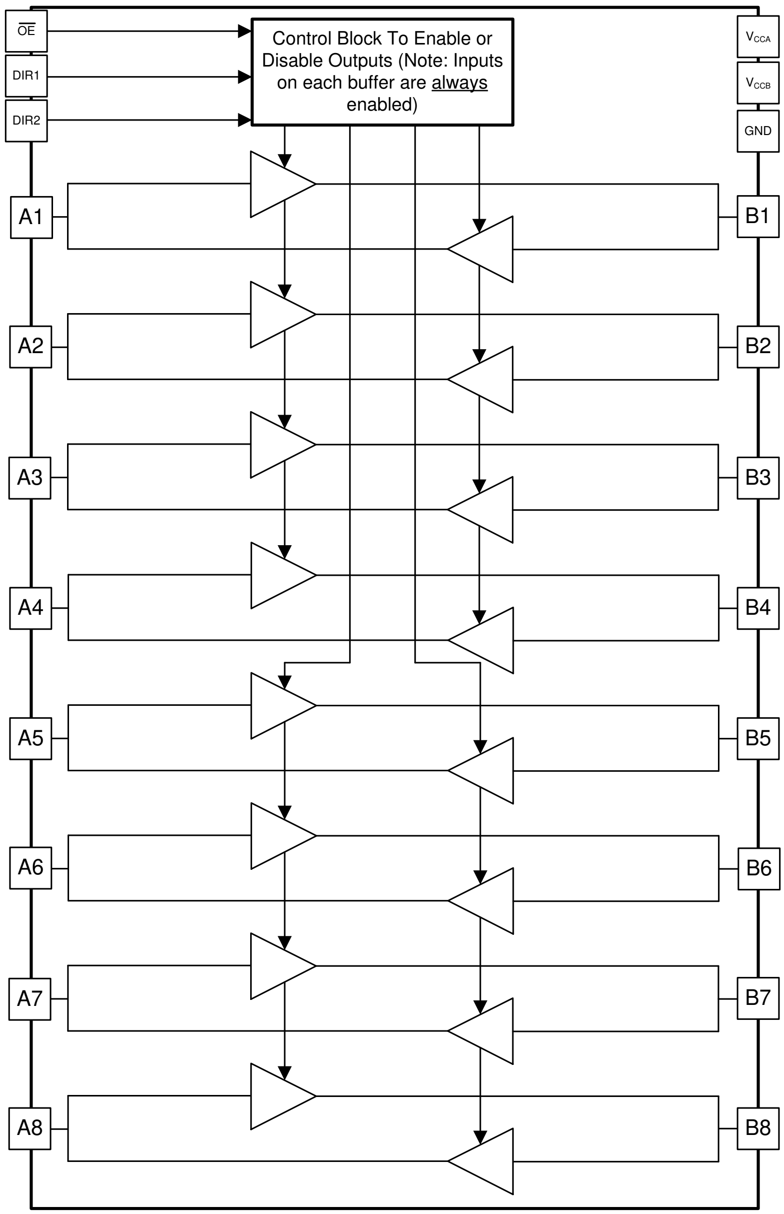


図 5. Functional Block Diagram

9.3 Feature Description

9.3.1 Up-Translation and Down-Translation From 0.65 V to 3.6 V

Both supply pins are configurable over the full 0.65 V to 3.6 V voltage range, which makes the device suitable for translating between any of the low voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

9.3.2 Multiple Direction Control Pins

Two control pins are used to configure the 8 data I/Os. I/O channels 1 through 4 are grouped together and I/O channels 5 through 8 are banked together. The benefit of this is to permit simultaneous up-translation and down-translation within one device. This eliminates the need for multiple devices, where each device can only provide up-translation or down-translation sequentially. Simultaneous up and down translation is supported when both V_{CCA} and V_{CCB} are at least 1.40 V.

9.3.3 Bus-Hold Circuitry

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state, which helps with board space savings and reduced component costs. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. See the Bus-Hold Circuit application note for more details. (SCLA015).

Note that the bus-hold circuitry always remains active when the corresponding supply is present (i.e. B port bus-hold circuits are active when V_{CCB} is present, and A port bus-hold circuits are active when V_{CCA} is present). The bus hold circuitry is also active even when the device is in a partial power down state or when the output enable pin is used to place all outputs into high impedance.

9.3.4 I_{off} Supports Partial-Power-Down Mode Operation

This feature is to limit the leakage current of an I/O pin being driven to a voltage as large as 3.6 V while having its corresponding power supply rail powered down. This is represented by the I_{off} parameter in the *Electrical Characteristics* table.

9.4 Device Functional Modes

All control inputs are referenced to V_{CCA} and must be driven to a valid Logic High or Logic Low (that is, not floating) to assure proper device operation and to prevent excessive power consumption. 表 1 summarizes the possible modes of device operation based on the configuration of the control inputs.

表 1. Function Table(1)

CONTROL INPUTS			Signal Direction	
$\overline{OE}$	DIR1	DIR2	Bits 1:4	Bits 5:8
H	X	X	Disabled (Hi-Z)	
L	L	L	B to A	
L	L	H	B to A	A to B
L	H	L	A to B	
L	H	H	A to B	B to A

(1) Input circuits of the data I/Os are always active and must be driven to a valid logic level.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AXCH8T245 device can be used in level-translation applications for interfacing devices or systems operating at different voltage nodes. 図 6 depicts an application in which the SN74AXCH8T245 device is up-translating a 0.7 V input to a 3.3 V output to interface between a system controller and a peripheral device.

10.2 Typical Application

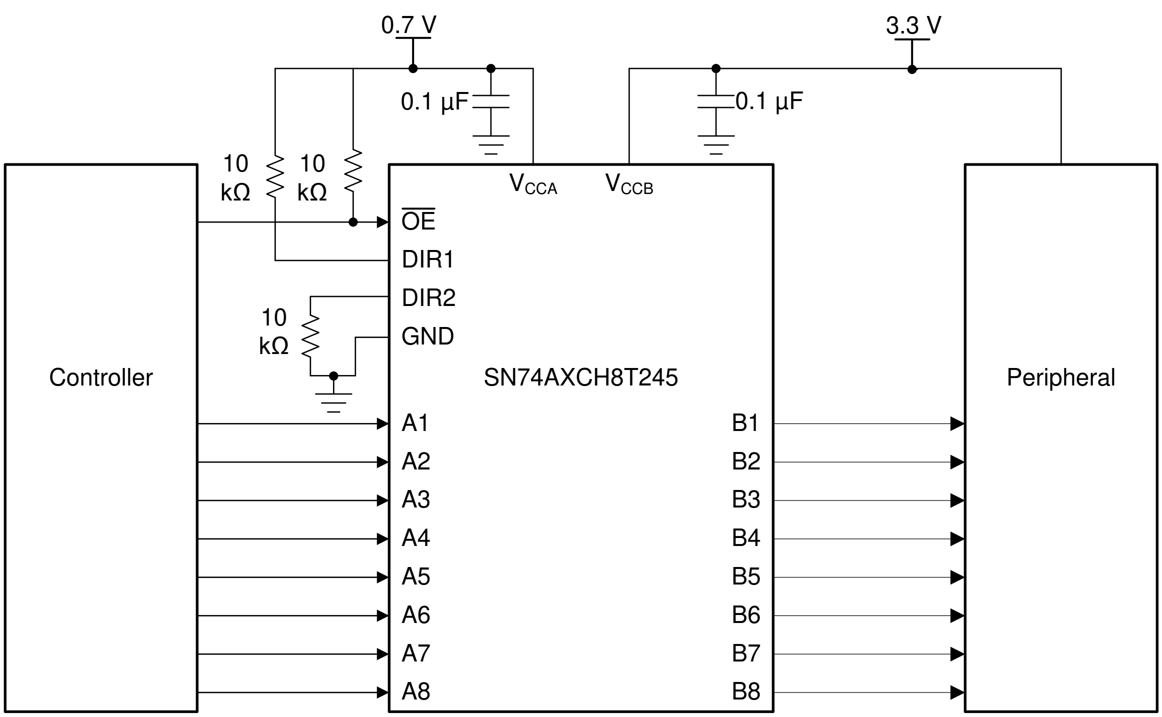


図 6. Typical Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in 表 2.

表 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXCH8T245 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXCH8T245 device is driving to determine the output voltage range.

10.2.3 Application Curve

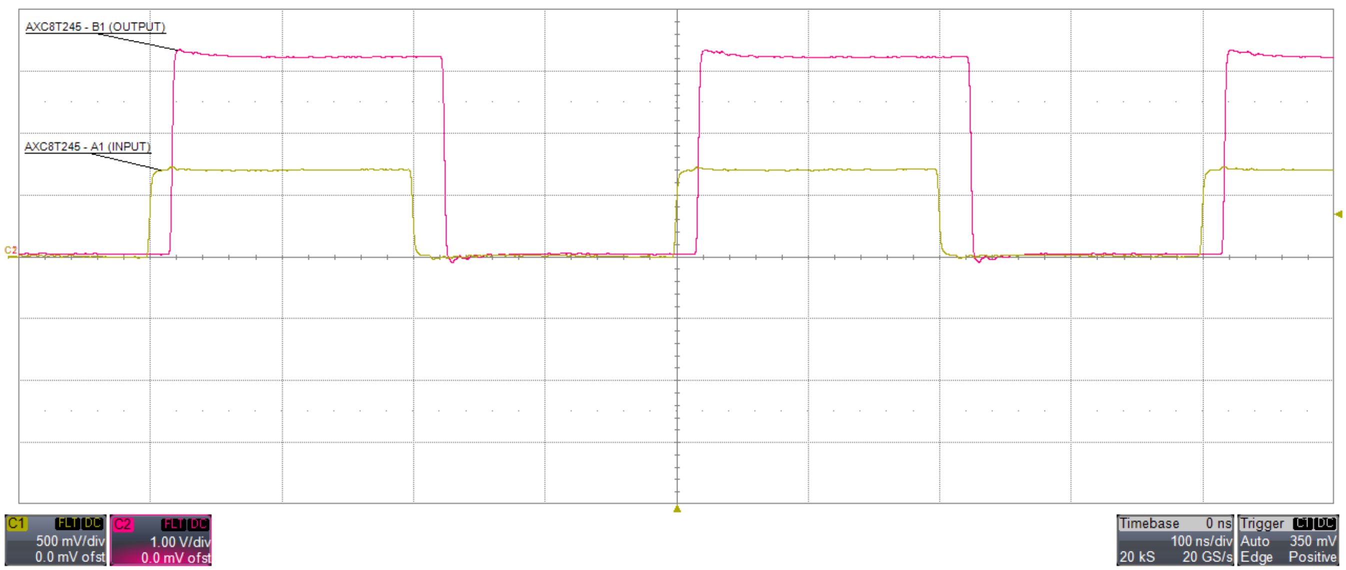


図 7. Translation Up (0.7 V to 3.3 V) at 2.5 MHz

11 Power Supply Recommendations

Always apply a ground reference to the GND pins first. However, there are no additional requirements for power supply sequencing.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Power Sequencing for AXC Family of Devices* application report.

12 Layout

12.1 Layout Guidelines

To assure reliability of the device, follow common printed-circuit board layout guidelines.

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

12.2 Layout Example

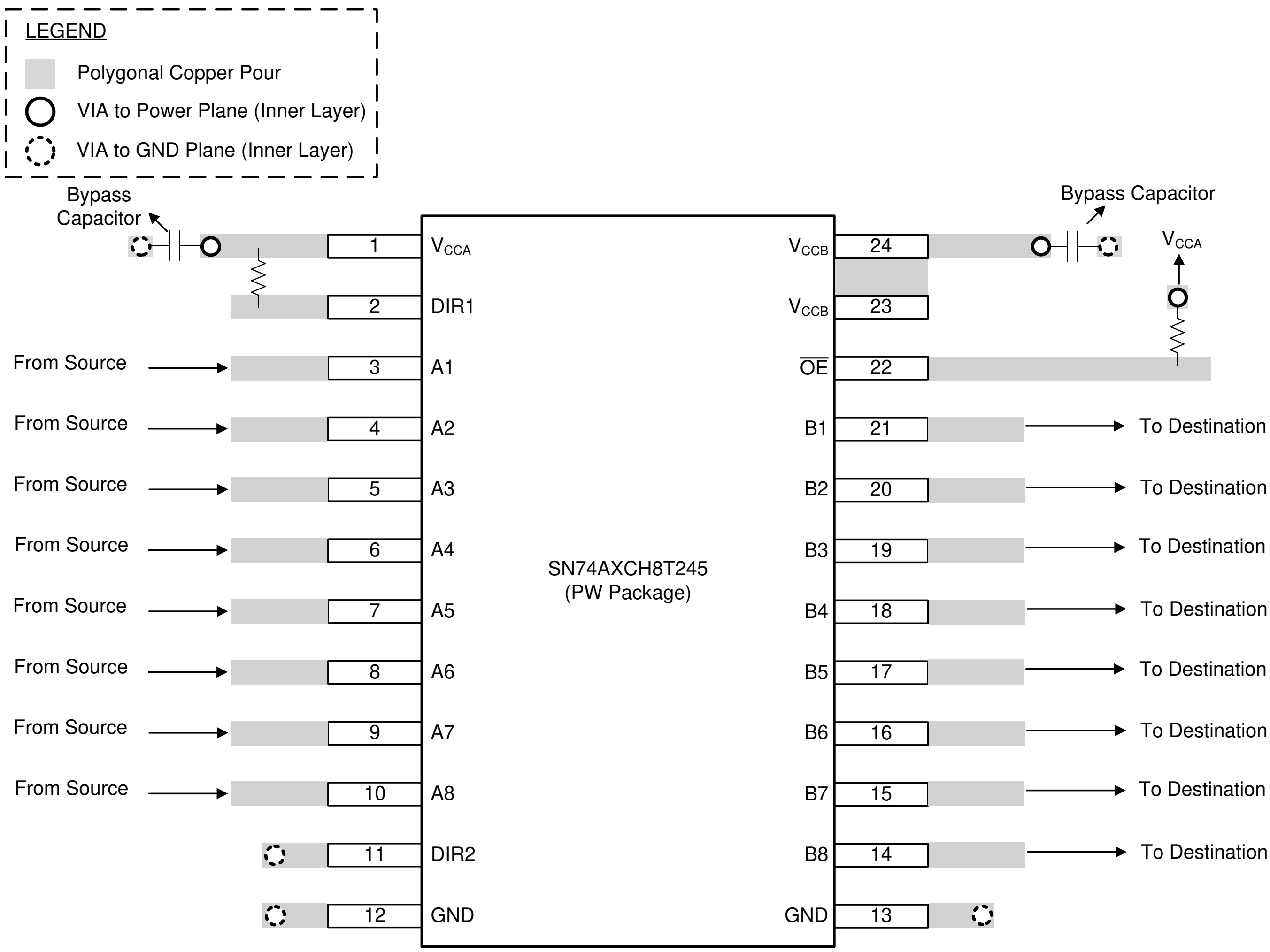


図 8. SN74AXCH8T245 Device Layout Example

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

13.1.1 関連資料

関連資料については、以下を参照してください。

テキサス・インスツルメンツ、*『低速またはフローティングCMOS入力の影響』*アプリケーション・レポート
テキサス・インスツルメンツ、*『AXCデバイス・ファミリの電源シーケンス』*アプリケーション・レポート

13.2 ドキュメントの更新通知を受け取る方法

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13.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

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13.4 商標

E2E is a trademark of Texas Instruments.

13.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AXCH8T245PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245	Samples
SN74AXCH8T245RHLR	ACTIVE	VQFN	RHL	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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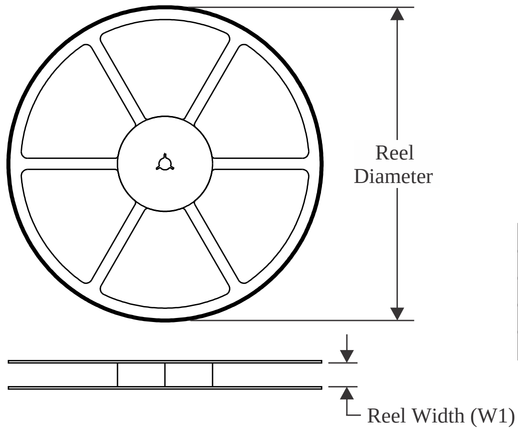
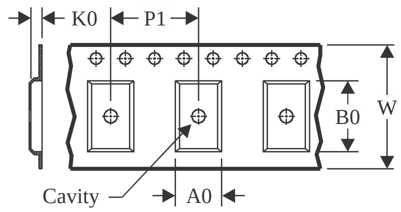
TAPE AND REEL INFORMATION

REEL DIMENSIONS

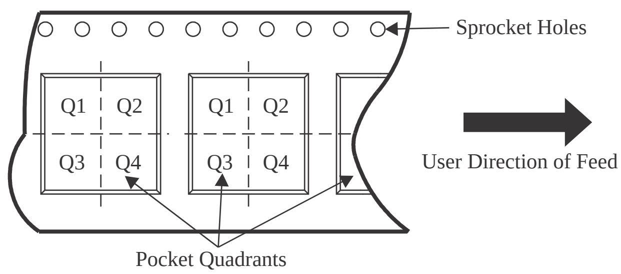


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

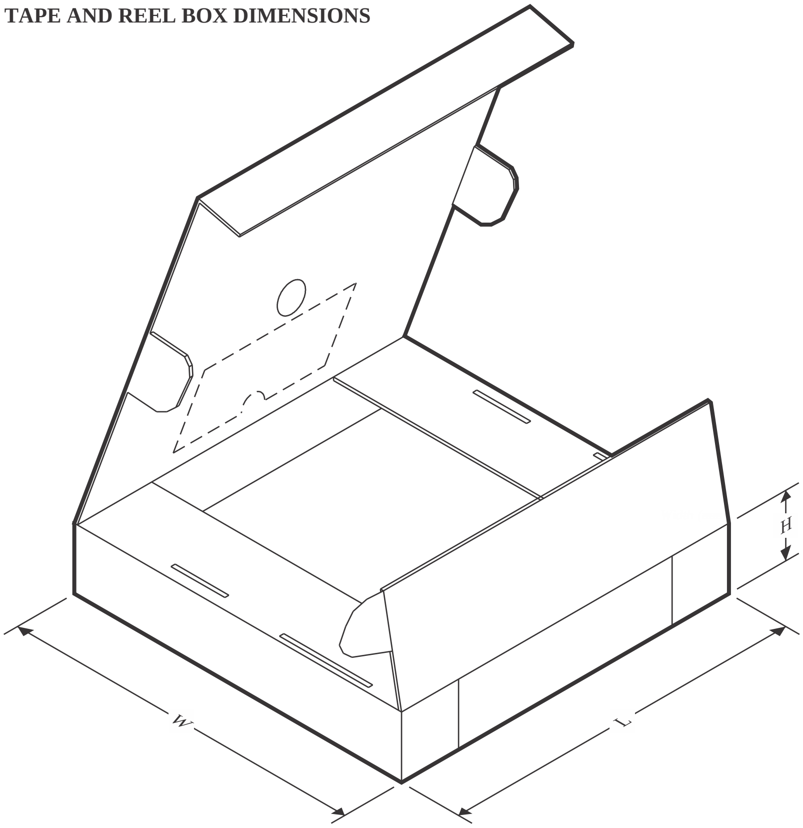
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

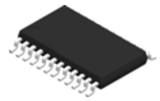
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AXCH8T245PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74AXCH8T245RHLR	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

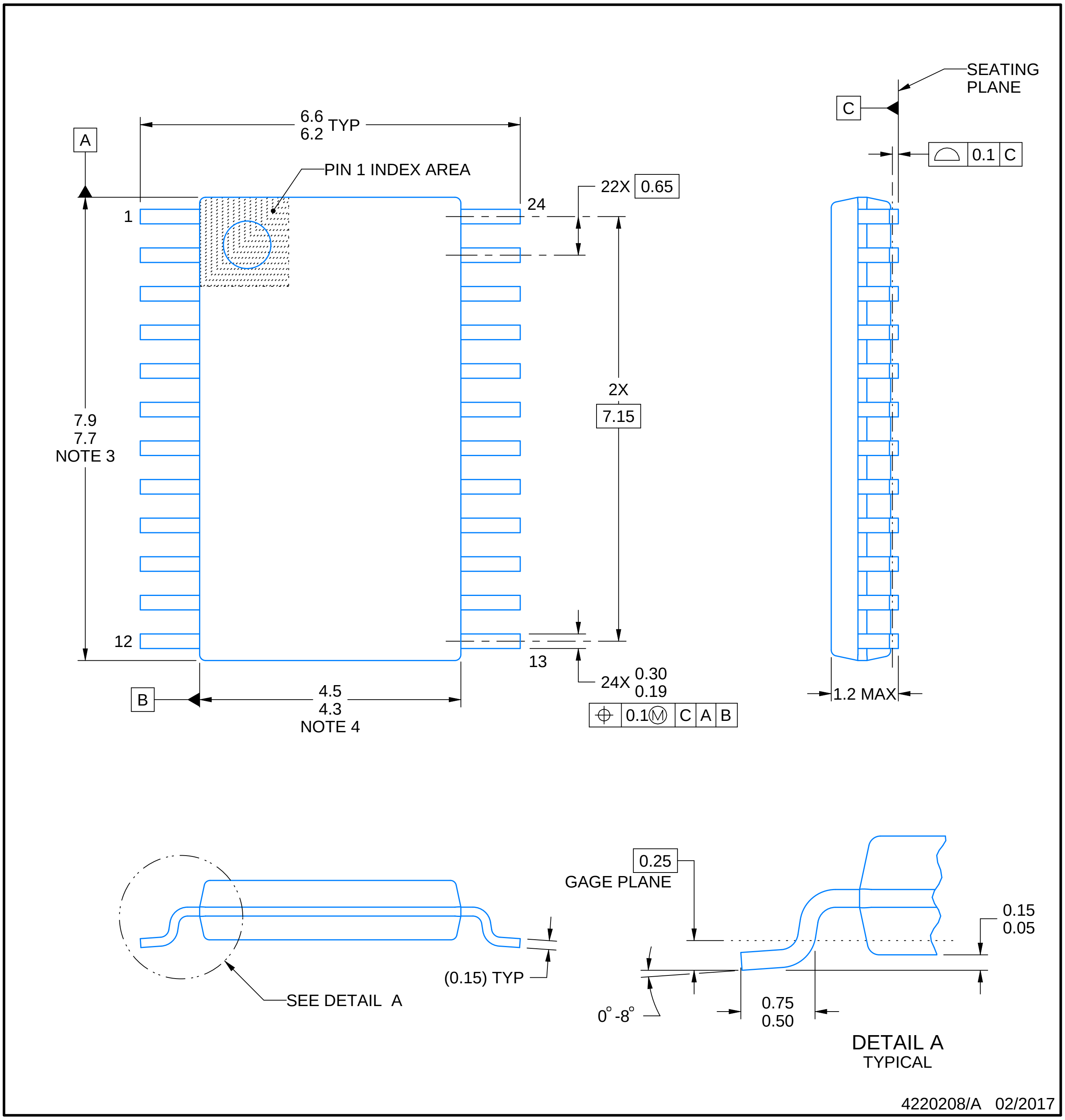
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

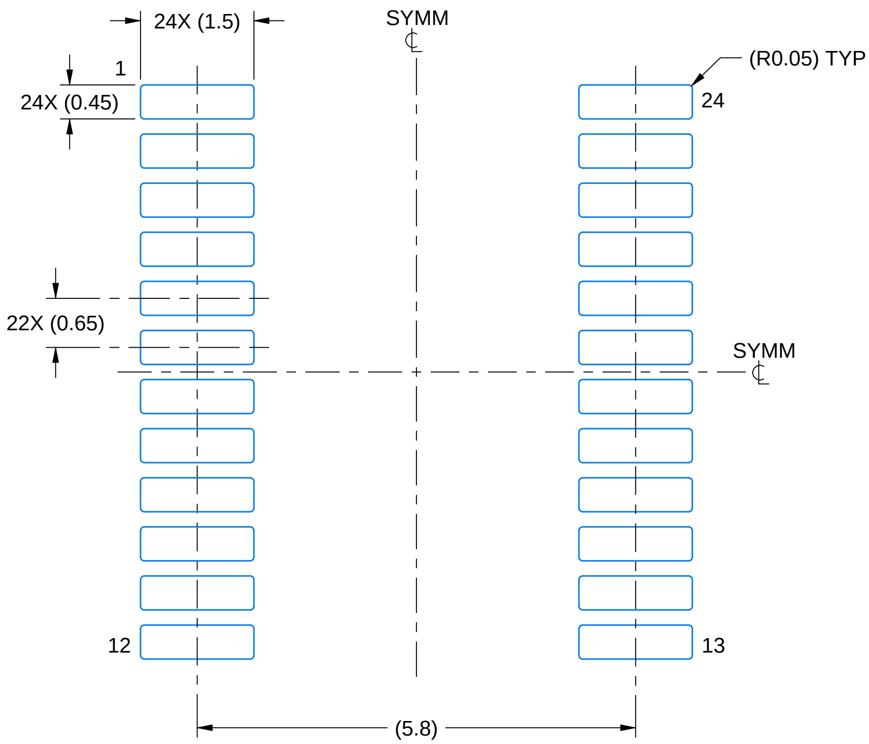
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AXCH8T245PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74AXCH8T245RHLR	VQFN	RHL	24	3000	367.0	367.0	35.0



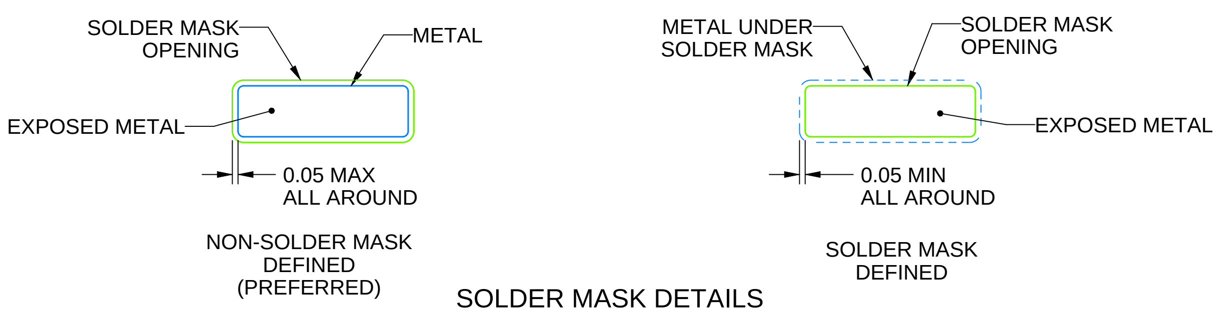


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

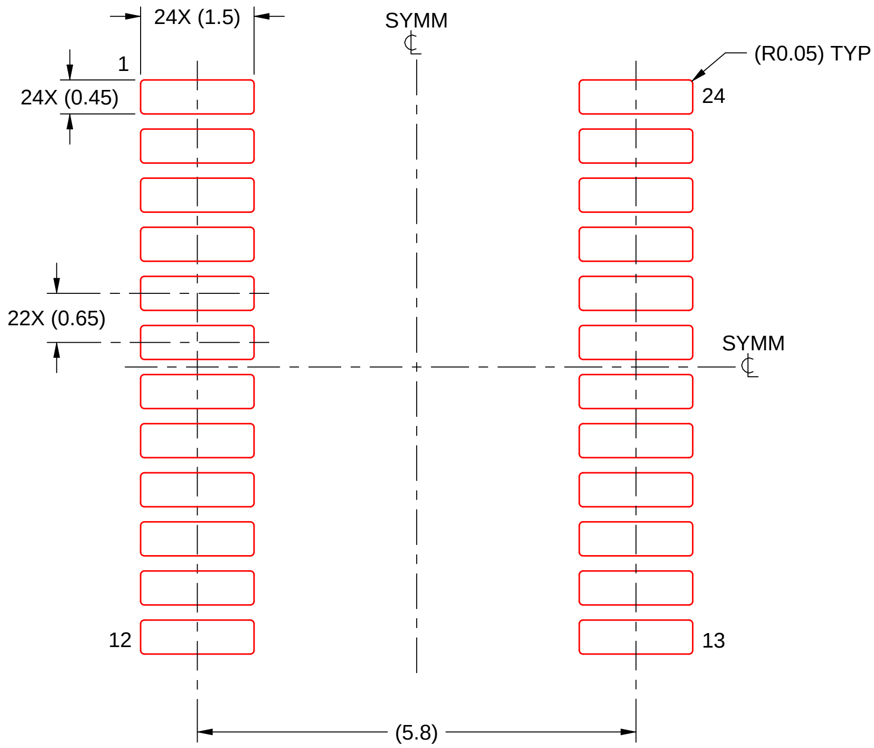


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

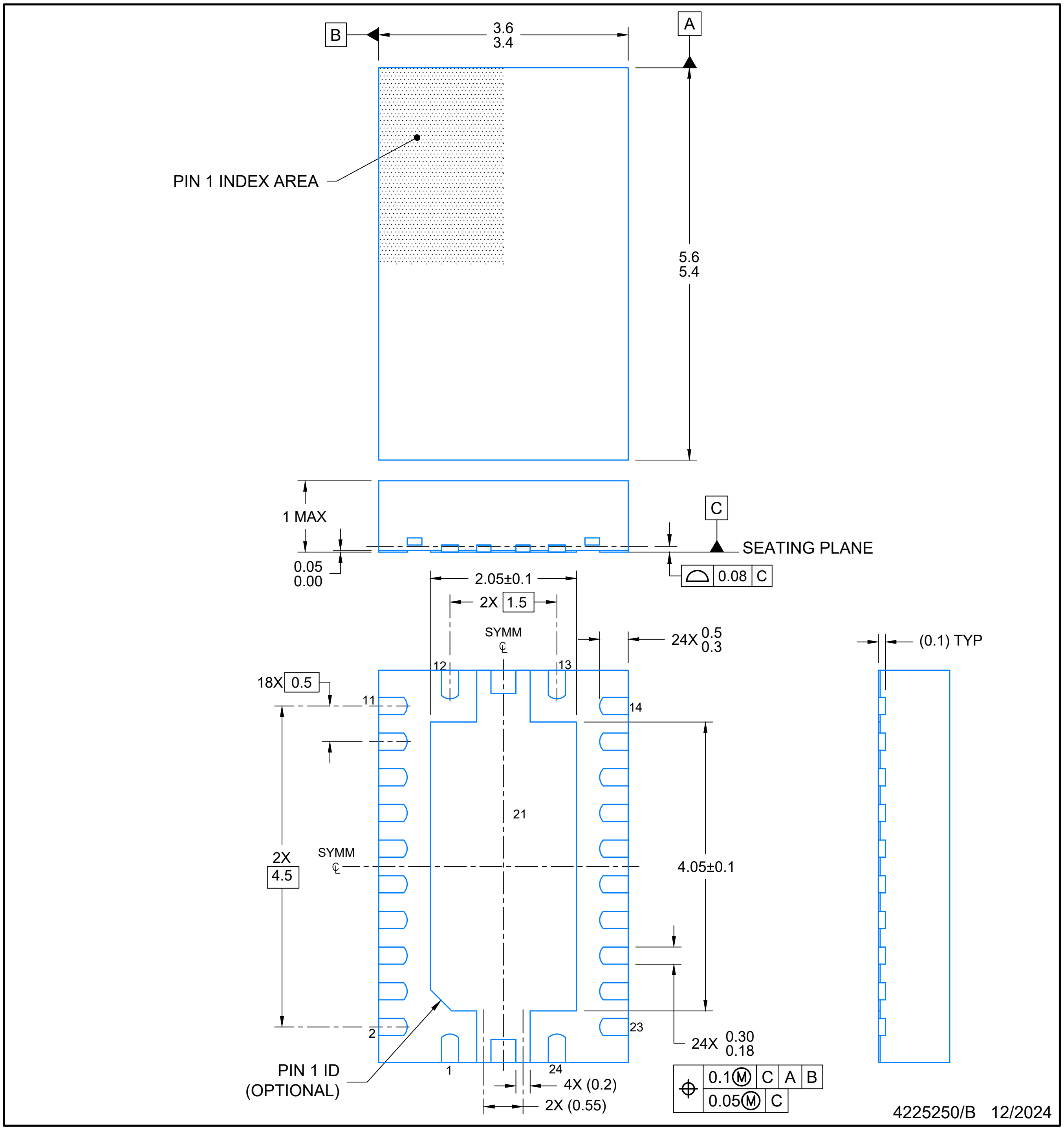


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

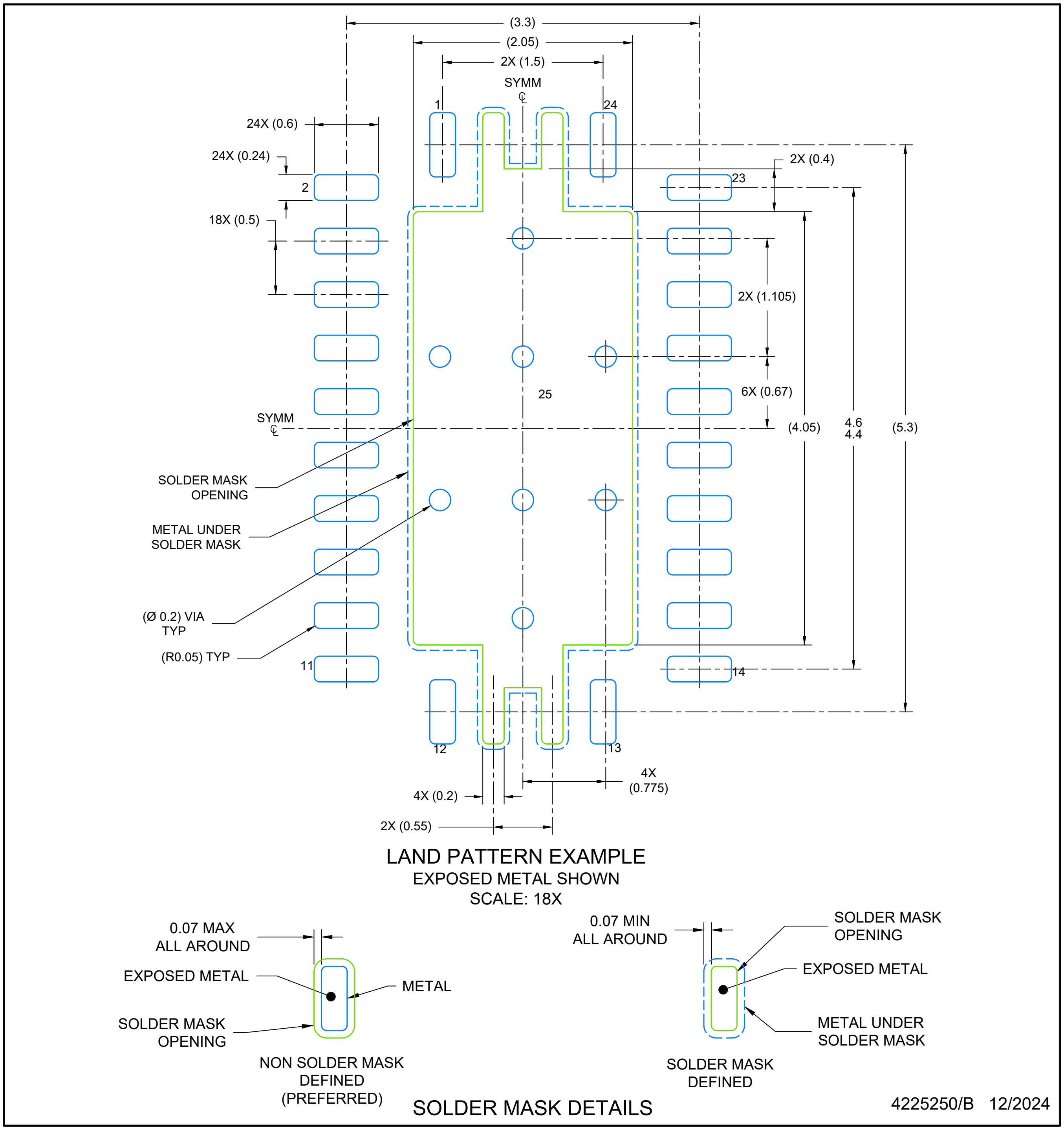
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



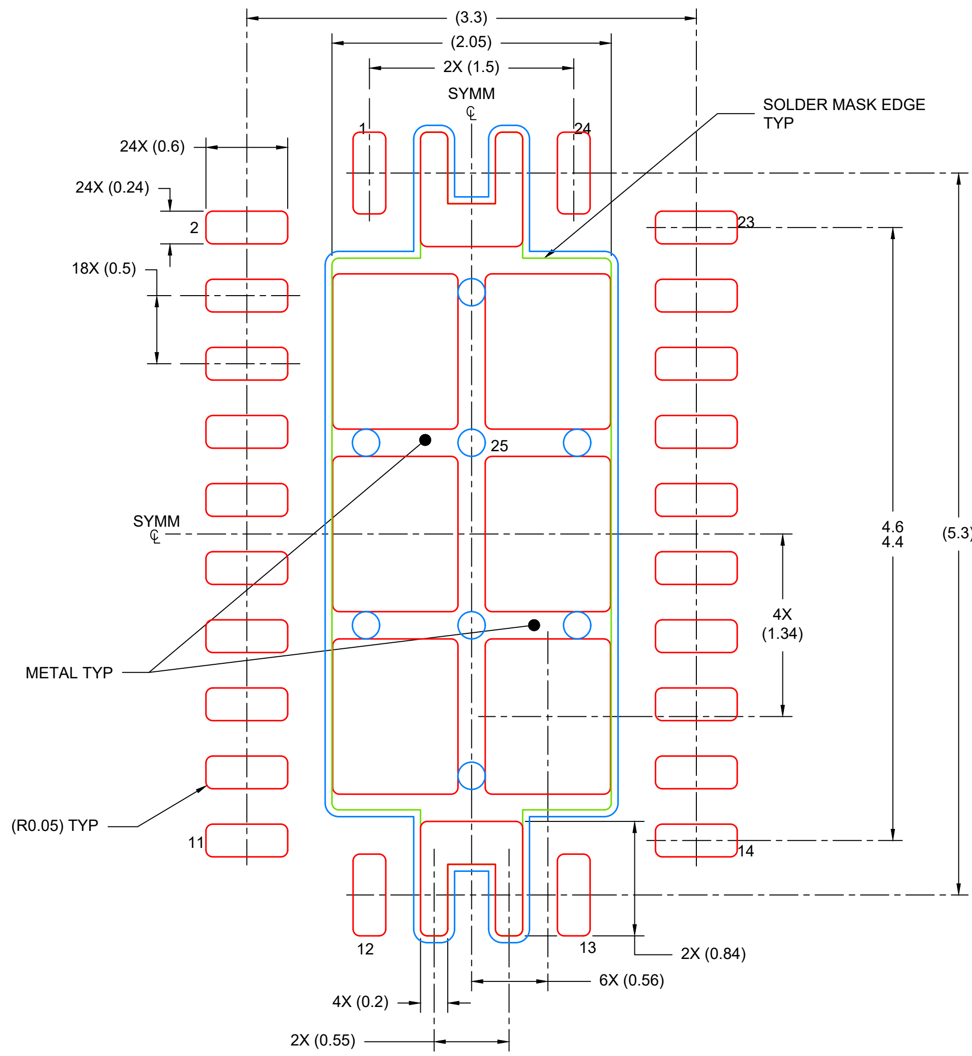
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

4225250/B 12/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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