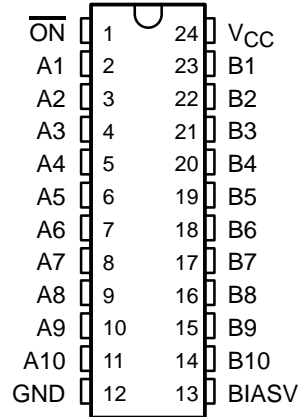


SN74CBT6800A
10-BIT FET BUS SWITCH
WITH PRECHARGED OUTPUTS
 SCDS005N – MARCH 1993 – REVISED MARCH 2001

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**

DB, DBQ, DGV, DW, OR PW PACKAGE
 (TOP VIEW)



description

The SN74CBT6800A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The SN74CBT6800A is organized as one 10-bit switch with a single enable (\overline{ON}) input. When \overline{ON} is low, the switch is on, and port A is connected to port B. When \overline{ON} is high, the switch between port A and port B is open. When \overline{ON} is high or V_{CC} is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube	SN74CBT6800ADW	CBT6800A
		Tape and reel	SN74CBT6800ADWR	
	SSOP – DB	Tape and reel	SN74CBT6800ADBR	CT6800A
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT6800ADBQR	CBT6800A
	TSSOP – PW	Tape and reel	SN74CBT6800APWR	CT6800A
	TVSOP – DGV	Tape and reel	SN74CBT6800ADGVR	CT6800A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT ON	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



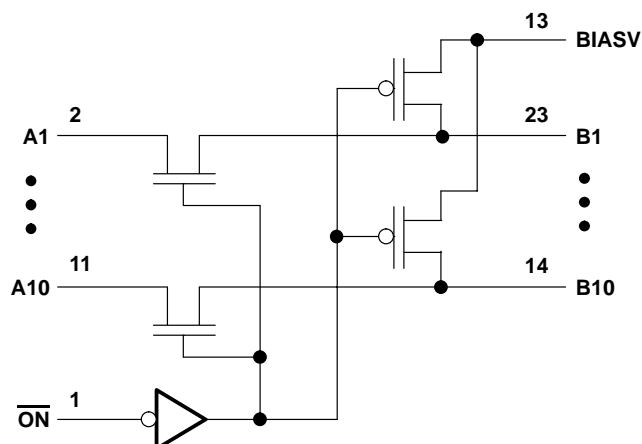
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated

SN74CBT6800A 10-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS

SCDS005N – MARCH 1993 – REVISED MARCH 2001

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Bias voltage range, BIASV	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2):		
DB package	63°C/W
DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	V_{CC}	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
I_I		$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$ or GND			±5	μA
I_O		$V_{CC} = 4.5\text{ V}$,	BIASV = 2.4 V, $V_O = 0$	0.25			mA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_O = 0$, $V_I = V_{CC}$ or GND			50	μA
ΔI_{CC}^\ddagger	Control inputs	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V, Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	$V_I = 3\text{ V}$ or 0			3.5		pF
$C_{O(OFF)}$		$V_O = 3\text{ V}$ or 0,	Switch off		4.5		pF
r_{on}^\S		$V_{CC} = 4\text{ V}$, TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$		11	20	Ω
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	3	7	
				$I_I = 30\text{ mA}$	3	7	
			$V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$	6	15		

† All typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

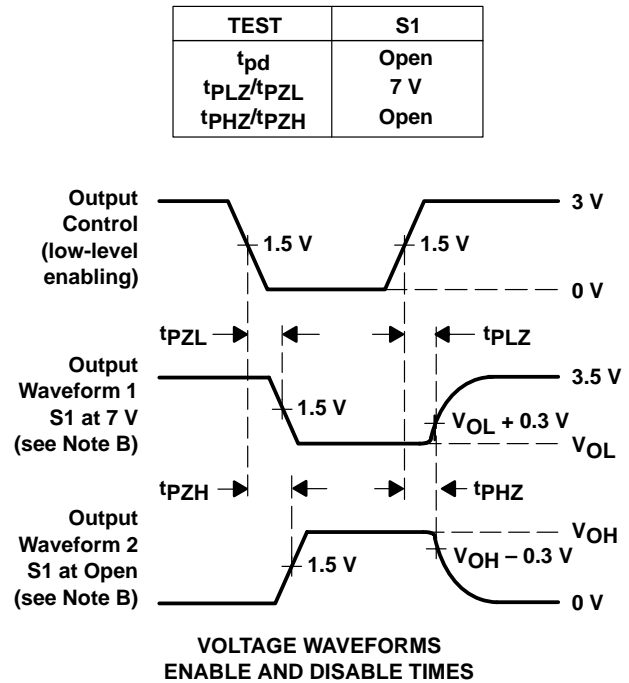
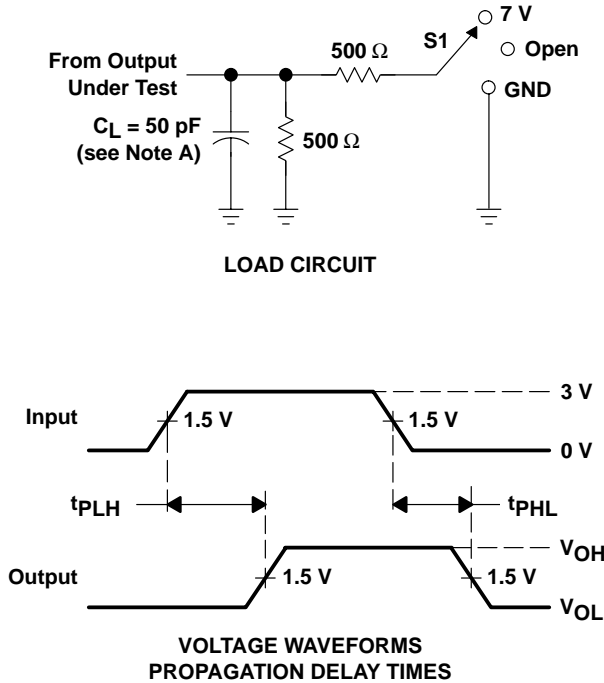
PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}^\parallel		A or B	B or A	0.35		0.25		ns
t_{PZH}	BIASV = GND	$\overline{\text{ON}}$	A or B	6	2	5.1	ns	
t_{PZL}	BIASV = 3 V			6	2	5.6		
t_{PHZ}	BIASV = GND	$\overline{\text{ON}}$	A or B	5.5	1	5	ns	
t_{PLZ}	BIASV = 3 V			5.5	2	5.9		

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

SN74CBT6800A
10-BIT FET BUS SWITCH
WITH PRECHARGED OUTPUTS

SCDS005N – MARCH 1993 – REVISED MARCH 2001

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.
 G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBT6800APWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6800A
SN74CBT6800APWR.A	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT6800A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

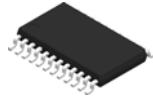
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT6800APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT6800APWR	TSSOP	PW	24	2000	353.0	353.0	32.0

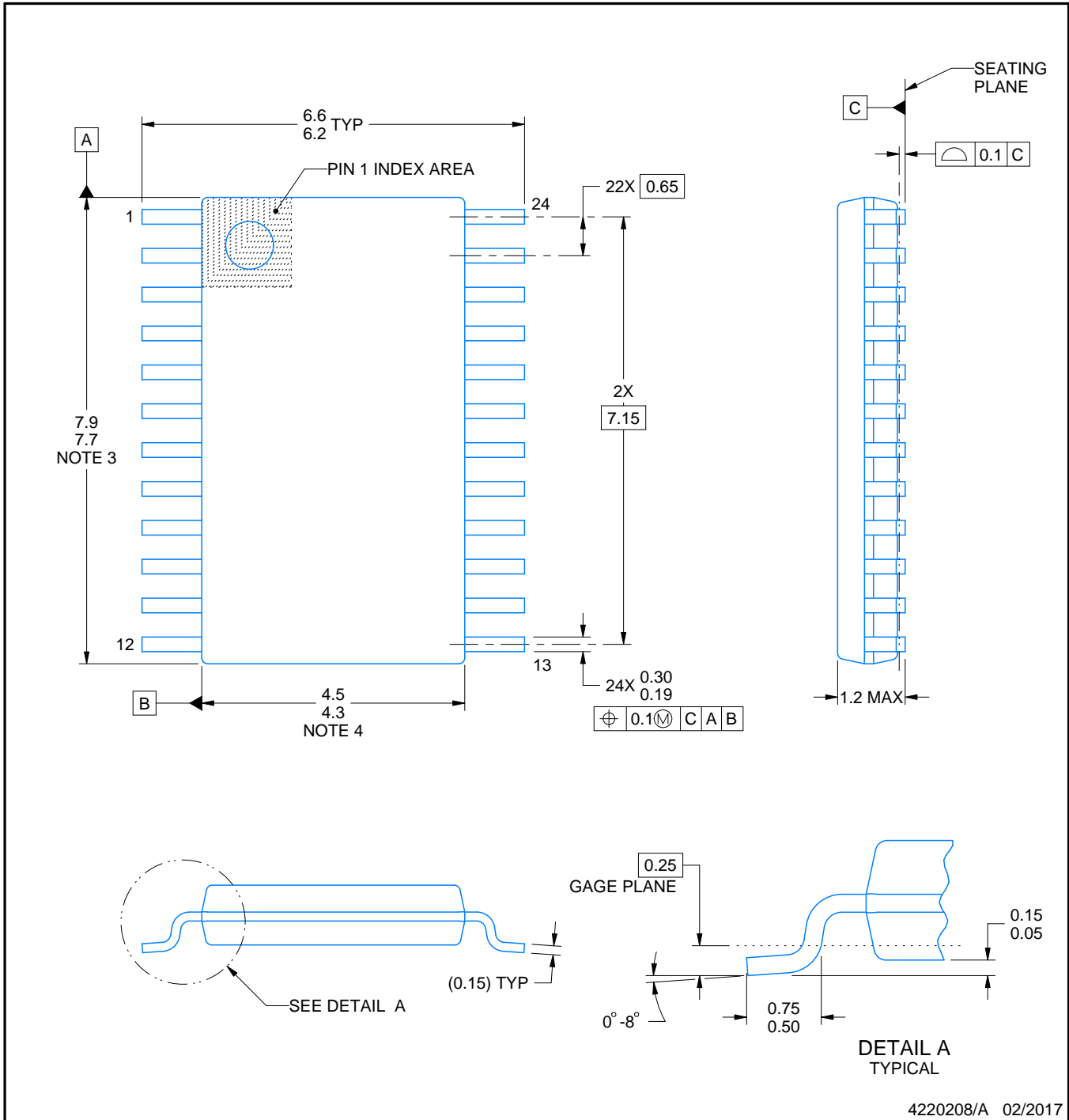
PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

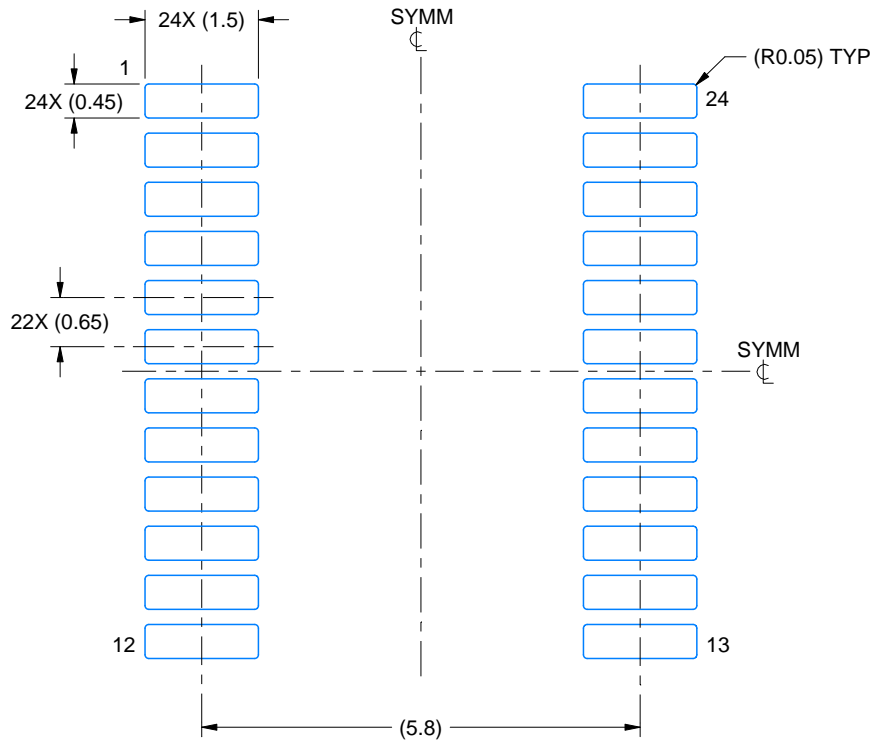
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

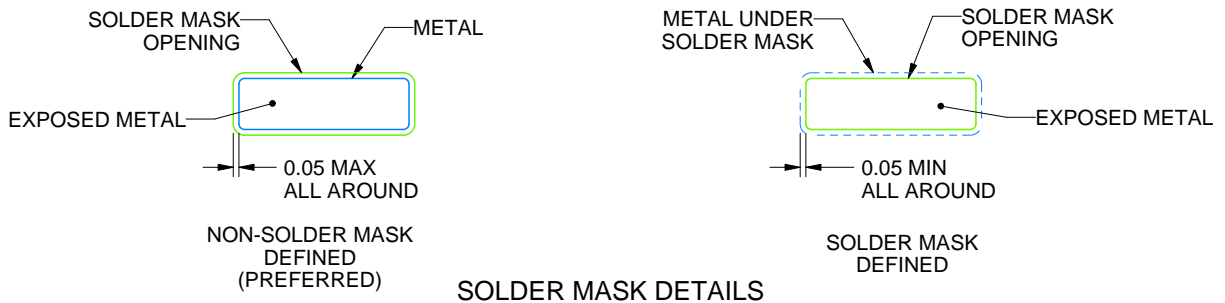
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

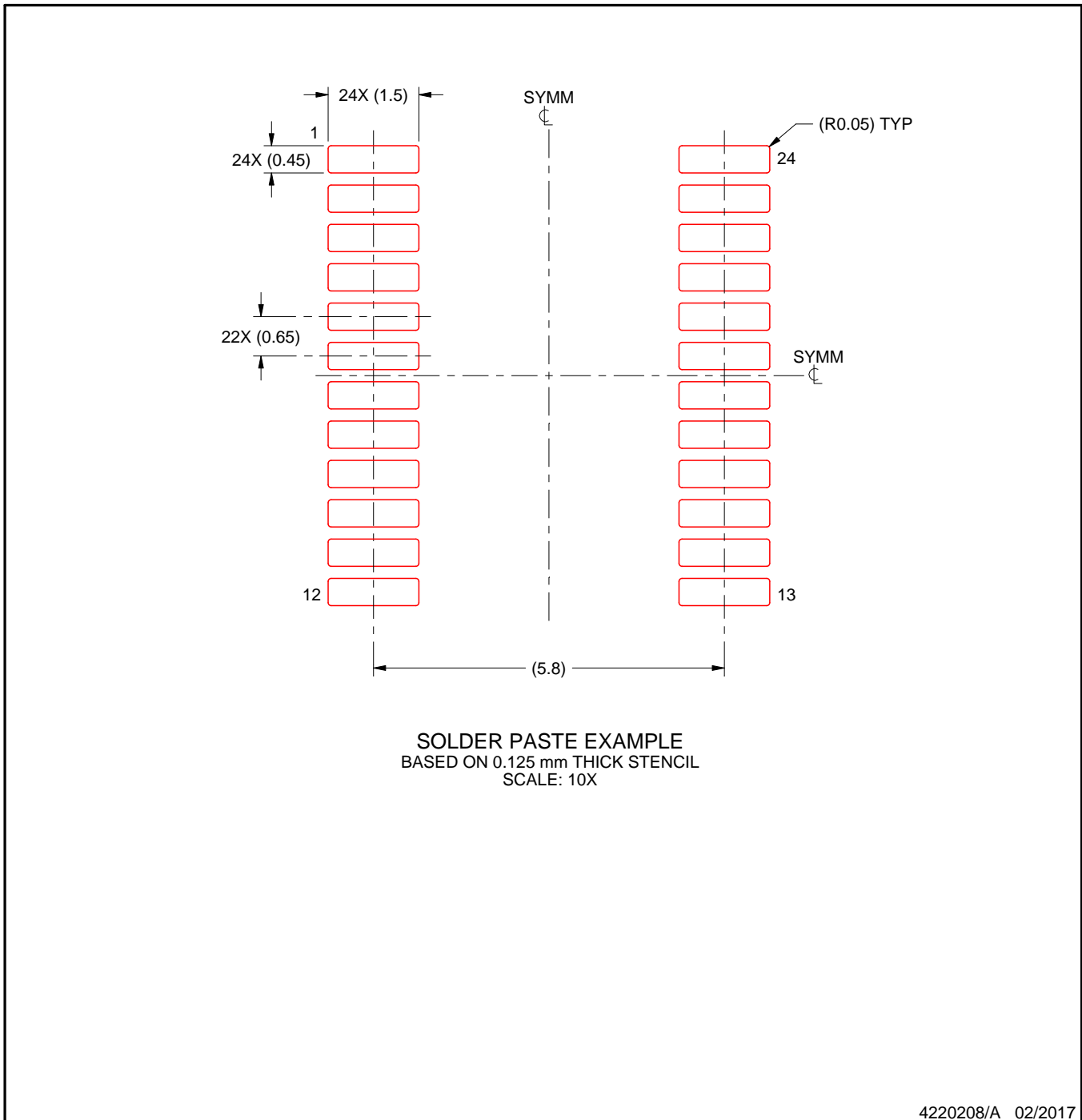
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025