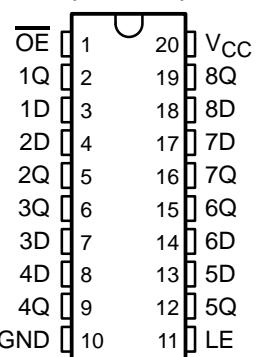


- Eight High-Current Latches in a Single Package
- High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads
- Full Parallel Access for Loading

description

This 8-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

DB, N, OR PW PACKAGE (TOP VIEW)



The eight latches of the SN74HC373A are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

An output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

ORDERING INFORMATION

TA	PACKAGE ^T		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74HC373AN	SN74HC373AN
	SSOP – DB	Tape and reel	SN74HC373ADBR	HC373A
	TSSOP – PW	Tape and reel	SN74HC373APWR	HC373A

^T Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each latch)

INPUTS			OUTPUT Q
\overline{OE}	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

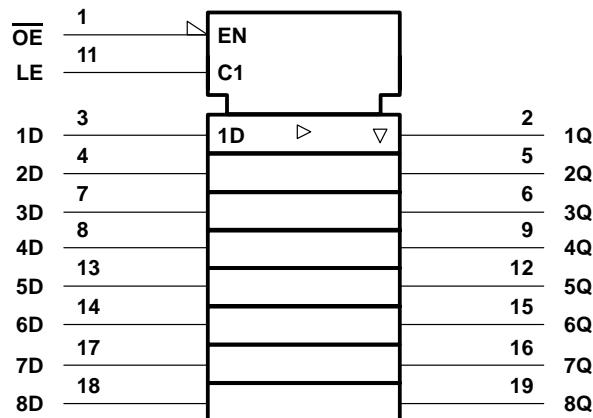


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SN74HC373A OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

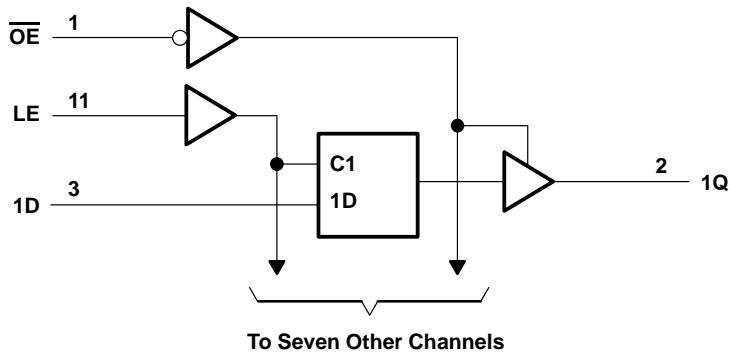
SCLS458 – MARCH 2001

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
N package	69°C/W
PW package	83°C/W
Storage temperature range, T_{STG}	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5			V
		V _{CC} = 4.5 V	3.15			
		V _{CC} = 6 V	4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0	0.5		V
		V _{CC} = 4.5 V	0	1.35		
		V _{CC} = 6 V	0	1.8		
V _I	Input voltage		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V	0	1000		ns
		V _{CC} = 4.5 V	0	500		
		V _{CC} = 6 V	0	400		
T _A	Operating free-air temperature		-40	85	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998	1.9		V
			4.5 V	4.4	4.499	4.4		
			6 V	5.9	5.999	5.9		
		I _{OH} = -6 mA	4.5 V	3.98	4.3	3.84		
		I _{OH} = -7.8 mA	6 V	5.48	5.8	5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.1	0.1		V
			4.5 V		0.1	0.1		
			6 V		0.1	0.1		
		I _{OL} = 6 mA	4.5 V		0.26	0.33		
		I _{OL} = 7.8 mA	6 V		0.26	0.33		
I _I	V _I = V _{CC} or 0	6 V		±0.1	±100	±1000	nA	
I _{OZ}	V _O = V _{CC} or 0	6 V			±0.5	±5	μA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V			8	80	μA	
C _i		2 V to 6 V		3	10	10	pF	

SN74HC373A
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t _w	Pulse duration, LE high	2 V	75	95	ns	ns	ns
		4.5 V	15	19			
		6 V	13	16			
t _{su}	Setup time, data before LE↓	2 V	50	63	ns	ns	ns
		4.5 V	10	13			
		6 V	9	11			
t _h	Hold time, data after LE↓	2 V	20	24	ns	ns	ns
		4.5 V	10	12			
		6 V	10	12			

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{pd}	D	Q	2 V	55	125	155	ns	ns	ns
			4.5 V	15	25	31			
			6 V	12	21	26			
	LE	Any Q	2 V	71	125	155	ns	ns	ns
			4.5 V	20	25	31			
			6 V	16	21	26			
t _{en}	OE	Any Q	2 V	60	125	155	ns	ns	ns
			4.5 V	17	25	31			
			6 V	13	21	26			
t _{dis}	OE	Any Q	2 V	44	125	155	ns	ns	ns
			4.5 V	19	25	31			
			6 V	17	21	26			
t _t		Any Q	2 V	22	60	75	ns	ns	ns
			4.5 V	7	12	15			
			6 V	5	10	13			

SN74HC373A
OCTAL TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

SCLS458 – MARCH 2001

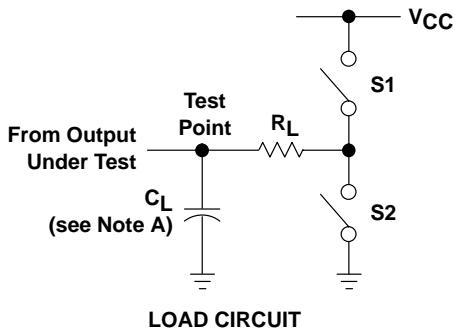
switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	D	Q	2 V	73	175	220	ns	ns	ns
			4.5 V	20	35	44			
			6 V	16	30	37			
	LE	Any Q	2 V	90	175	220			
			4.5 V	25	35	44			
			6 V	20	30	37			
t_{en}	\overline{OE}	Any Q	2 V	78	175	220	ns	ns	ns
			4.5 V	21	35	44			
			6 V	17	30	37			

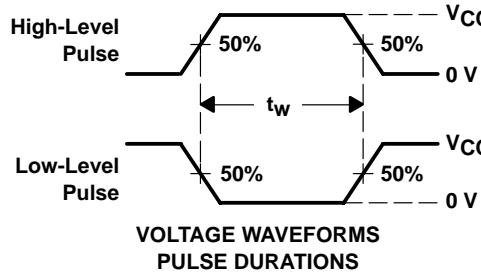
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	100	pF

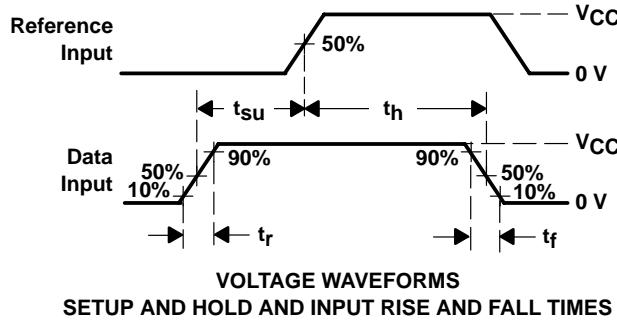
PARAMETER MEASUREMENT INFORMATION



PARAMETER		R _L	C _L	S1	S2
t _{en}	t _{PZH}	1 k Ω	50 pF or 150 pF	Open	Closed
	t _{PZL}			Closed	Open
t _{dis}	t _{PHZ}	1 k Ω	50 pF	Open	Closed
	t _{PLZ}			Closed	Open
t _{pd} or t _t		—	50 pF or 150 pF	Open	Open

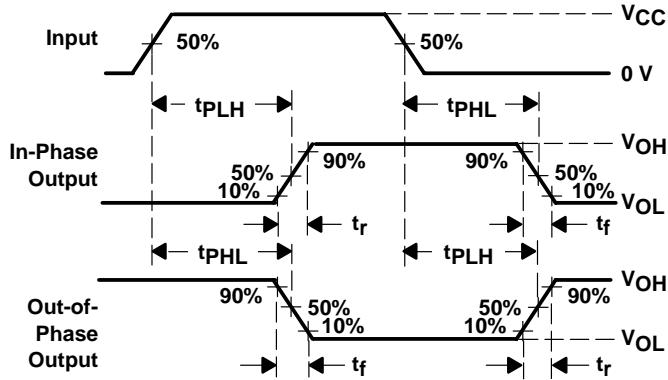


VOLTAGE WAVEFORMS PULSE DURATIONS

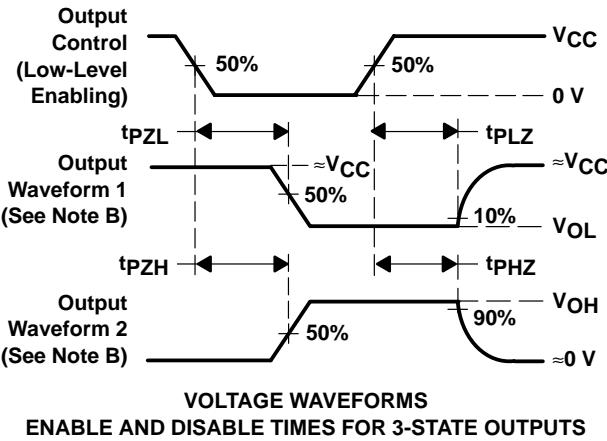


VOLTAGE WAVEFORMS

SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES:

- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_r = 6 ns, t_f = 6 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC373AN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC373AN
SN74HC373ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	HC373A
SN74HC373ANSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See SN74HC373ANSR	HC373A
SN74HC373APWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

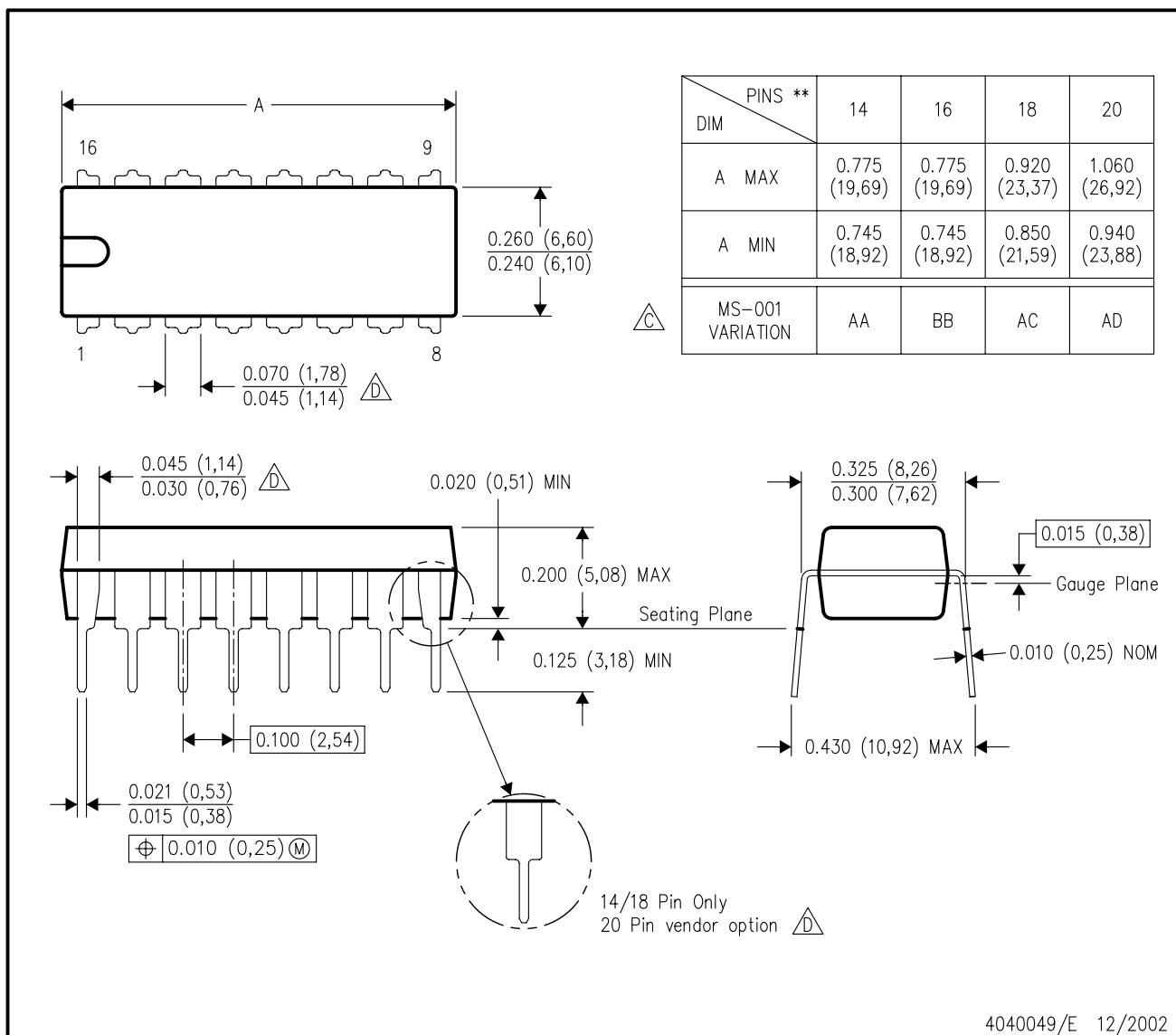
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N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

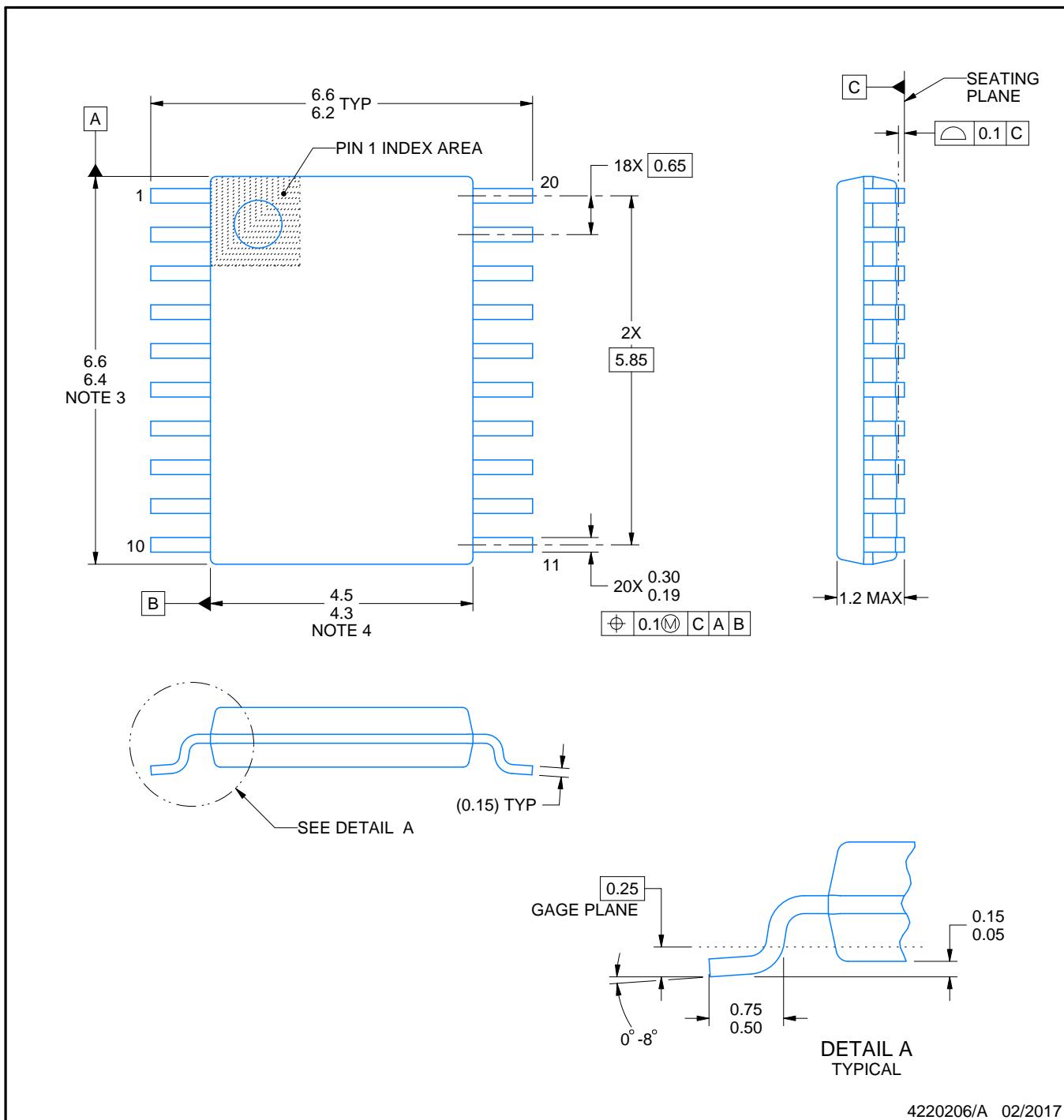
PACKAGE OUTLINE

PW0020A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

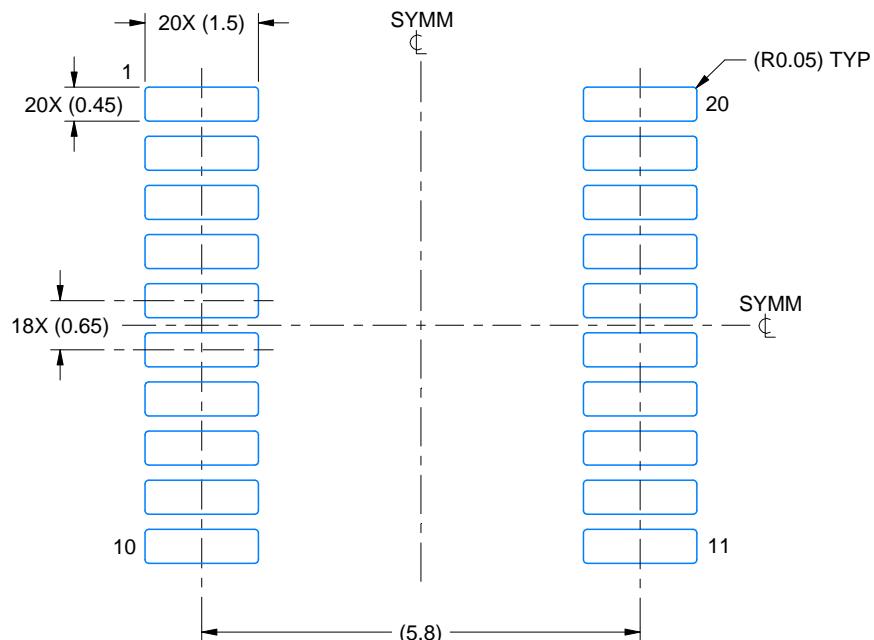
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

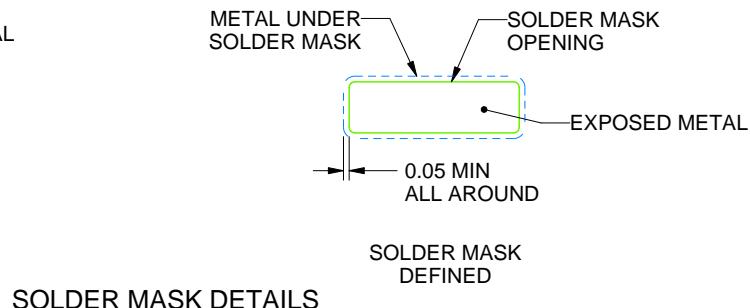
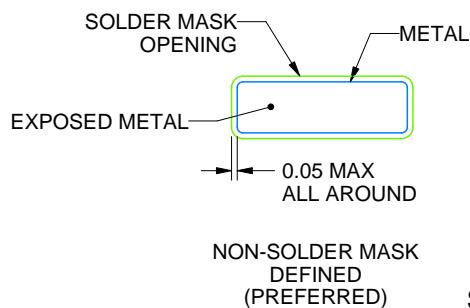
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

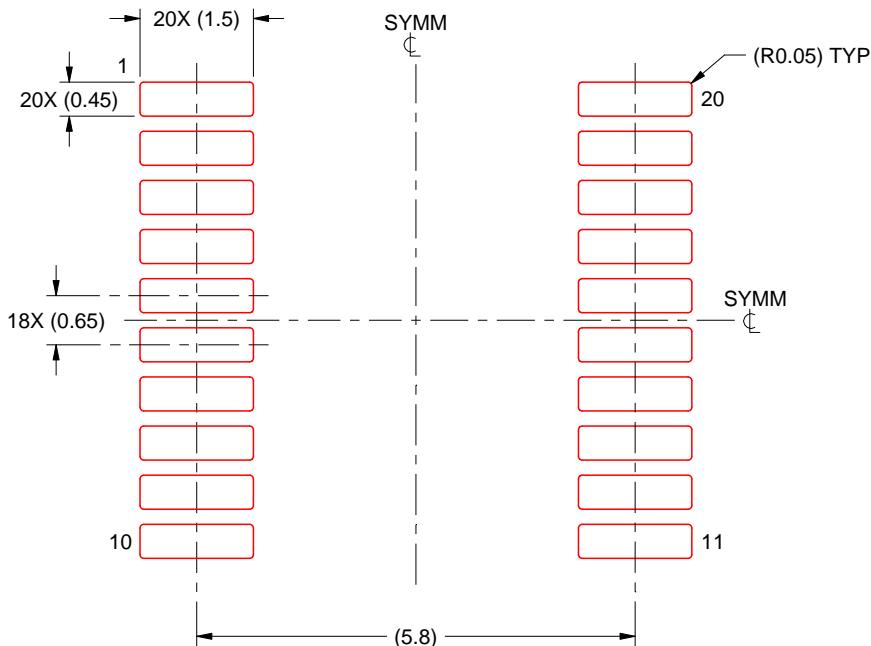
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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