TEXAS INSTRUMENTS

**SN54HC377, SN74HC377**
JAJSNU5D – JANUARY 1996 – REVISED MAY 2022

# SNx4HC377 クロック・イネーブル搭載、オクタル D タイプ・フリップ・フロップ

## 1 特長

- 幅広い動作電圧範囲：2V～6V
- 出力は最大 10 個の LSTTL 負荷を駆動可能
- 低い消費電力、最大 $I_{CC}$ 80µA
- $t_{pd}$ = 12ns (標準値)
- 5V で ±4mA の出力駆動能力
- 低い入力電流：最大 1µA
- シングル・レール出力を備えた 8 つのフリップ・フロップ
- ラッチ付きクロック・イネーブルにより誤クロックを防止

## 2 アプリケーション

- バッファ / ストレージ・レジスタ
- シフト・レジスタ
- パターン・ジェネレータ

## 3 概要

これらのデバイスはイネーブル入力付きポジティブ・エッジ・トリガ・オクタル D タイプ・フリップ・フロップです。'HC377 デバイスは 'HC273 デバイスと似ていますが、共通クリアの代わりにラッチ付きクロック・イネーブル (CLKEN) 入力を備えています。

**製品情報**

| 部品番号 | パッケージ [1] | 本体サイズ (公称) |
|---|---|---|
| SN74HC377DW | SOIC (20) | 12.80mm × 7.50mm |
| SN74HC377N | PDIP (20) | 25.40mm × 6.35mm |
| SN74HC377NS | SO (20) | 15.00mm × 5.30mm |
| SN54HC377J | CDIP (20) | 26.92mm × 6.92mm |
| SNJ54HC377FK | LCCC (20) | 8.89mm × 8.45mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

English Data Sheet: SCLS307

# Table of Contents

# 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision C (January 2022) to Revision D (May 2022) | Page |
|---|---|
| • Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, N was 69 is now 84.6, NS was 60 is now 113.4......................................................................................................................4 | |

| Changes from Revision B (January 2003) to Revision C (January 2022) | Page |
|---|---|
| • 最新のデータシート規格を反映するように、文書全体にわたって表、図、相互参照の採番方法を更新......................1 | |

# 5 Pin Configuration and Functions
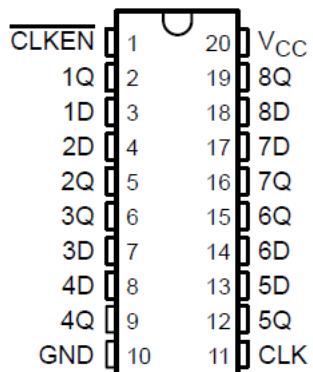


**J, DW, N, or NS package**
**20-Pin CDIP, SOIC, PDIP, SO**
**Top View**
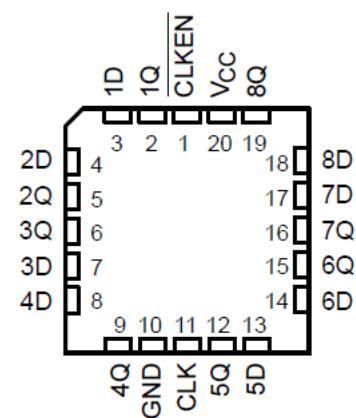


**FK package**
**20-Pin LCCC**
**Top View**

Product Folder Links: *SN54HC377 SN74HC377*

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

|  |  |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range |  | -0.5 | 7 | V |
| $I_{IK}$ | Input clamp current[2] | ($V_I$ < 0 or $V_I$ > $V_{CC}$) |  | ±20 | mA |
| $I_{OK}$ | Output clamp current[2] | ($V_O$ < 0 or $V_O$ > $V_{CC}$) |  | ±20 | mA |
| $I_O$ | Continuous output current | ($V_O$ = 0 to $V_{CC}$) |  | ±25 | mA |
|  | Continuous current through $V_{CC}$ or GND |  |  | ±50 | mA |
| $T_J$ | Junction temperature |  |  | 150 | °C |
| $T_{stg}$ | Storage temperature |  | -65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 Recommended Operating Conditions[1]

|  |  |  | SN54HC377 | | | SN74HC377 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
|  |  |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $V_{CC}$ | Supply voltage |  | 2 | 5 | 6 | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 |  |  | 1.5 |  |  | V |
|  |  | $V_{CC}$ = 4.5 V | 3.15 |  |  | 3.15 |  |  |  |
|  |  | $V_{CC}$ = 6 V | 4.2 |  |  | 4.2 |  |  |  |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V |  |  | 0.5 |  |  | 0.5 | V |
|  |  | $V_{CC}$ = 4.5 V |  |  | 1.35 |  |  | 1.35 |  |
|  |  | $V_{CC}$ = 6 V |  |  | 1.8 |  |  | 1.8 |  |
| $V_I$ | Input voltage |  | 0 |  | $V_{CC}$ | 0 |  | $V_{CC}$ | V |
| $V_O$ | Output voltage |  | 0 |  | $V_{CC}$ | 0 |  | $V_{CC}$ | V |
| $t_t$ | Input transition rise/fall time | $V_{CC}$ = 2 V |  |  | 1000 |  |  | 1000 | ns |
|  |  | $V_{CC}$ = 4.5 V |  |  | 500 |  |  | 500 |  |
|  |  | $V_{CC}$ = 6 V |  |  | 400 |  |  | 400 |  |
| $T_A$ | Operating free-air temperature |  | − 55 |  | 125 | − 40 |  | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

## 6.3 Thermal Information

|  | THERMAL METRIC | DW (SOIC) | N (PDIP) | NS (SO) | UNIT |
|---|---|---|---|---|---|
|  |  | 20 PINS | 20 PINS | 20 PINS |  |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance[1] | 109.1 | 84.6 | 113.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 76 | 72.5 | 78.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 77.6 | 65.3 | 78.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 51.5 | 55.3 | 47.1 | °C/W |
| $\psi_{JB}$ | Junction-to-top characterization parameter | 77.1 | 65.2 | 78.1 | °C/W |

Product Folder Links: *SN54HC377 SN74HC377*

## 6.3 Thermal Information (continued)

| THERMAL METRIC | | DW (SOIC) | N (PDIP) | NS (SO) | UNIT |
|---|---|---|---|---|---|
| | | 20 PINS | 20 PINS | 20 PINS | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1)    For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

## 6.4 Electrical Characteristics

| PARAMETER | TEST CONDITIONS[1] | $V_{CC}$ (V) | $T_A$ = 25°C | | | SN74HC377 | | SN74HC377 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = −20 µA | 2 | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | 4.5 | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | 6 | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | $I_{OH}$ = −4 mA | 4.5 | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | $I_{OH}$ = − 5.2 mA | 6 | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| $V_{OL}$ | $I_{OL}$ = 20 µA | 2 | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | 4.5 | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | 6 | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 4.5 | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | $I_{OL}$ = 5.2 mA | 6 | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | 6 | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0. $I_O$ = 0 | 6 | | | 8 | | 160 | | 80 | µA |
| $C_i$ | | 2 to 6 | | 3 | 10 | | 10 | | 10 | pF |

(1)    $V_I$ = $V_{IH}$ or $V_{IL}$, unless otherwise noted.

## 6.5 Timing Requirements

| | | $V_{CC}$ | $T_A$ = 25°C | | SN54HC377 | | SN74HC377 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | 2 | | 5 | | 3 | | 4 | MHz |
| | | 4.5 | | 25 | | 16 | | 20 | |
| | | 6 | | 29 | | 19 | | 23 | |
| $t_W$ | Pulse duration, CLK high or low | 2 | 100 | | 150 | | 125 | | ns |
| | | 4.5 | 20 | | 30 | | 25 | | |
| | | 6 | 17 | | 25 | | 21 | | |
| $t_{su}$ | Setup time, data before CLK ↑ | D | 2 | 100 | | 150 | | 125 | | ns |
| | | | 4.5 | 20 | | 30 | | 25 | | |
| | | | 6 | 17 | | 25 | | 21 | | |
| | | $\overline{CLKEN}$ high or low | 2 | 100 | | 150 | | 125 | |
| | | | 4.5 | 20 | | 30 | | 25 | |
| | | | 6 | 17 | | 25 | | 21 | |
| $t_h$ | Hold time, data after LE ↑ | $\overline{CLKEN}$ inactive or active, data | 2 | 5 | | 5 | | 5 | | ns |
| | | | 4.5 | 5 | | 5 | | 5 | |
| | | | 6 | 5 | | 5 | | 5 | |

*Submit Document Feedback*      5

Product Folder Links: *SN54HC377 SN74HC377*

## 6.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) See Parameter Measurement Information

| PARAM ETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ (V) | $T_A$ = 25°C | | | SN54HC377 | | SN74HC377 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 2 | 5 | 11 | | 3 | | 4 | | MHz |
| | | | 4.5 | 25 | 54 | | 16 | | 20 | | |
| | | | 6 | 29 | 64 | | 19 | | 23 | | |
| $t_{pd}$ | $\overline{CLK}$ | Any | 2 | | 56 | 160 | | 240 | | 200 | ns |
| | | | 4.5 | | 15 | 32 | | 48 | | 40 | |
| | | | 6 | | 12 | 27 | | 41 | | 34 | |
| $t_t$ | | Any | 2 | | 38 | 75 | | 110 | | 95 | ns |
| | | | 4.5 | | 8 | 15 | | 22 | | 19 | |
| | | | 6 | | 6 | 13 | | 19 | | 16 | |

## 6.7 Operating Characteristics

$T_A$ = 25°C

| | | Test Conditions | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per flip-flop | No load | 30 | pF |

# 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 2.5 ns.

For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.
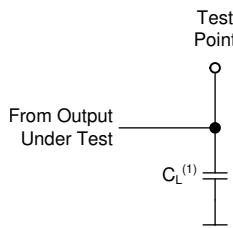


(1) $C_L$ includes probe and test-fixture capacitance.

**図 7-1. Load Circuit for Push-Pull Outputs**
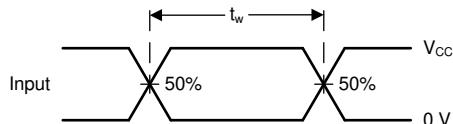


**図 7-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration**
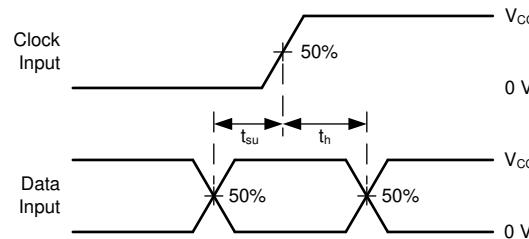


**図 7-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times**
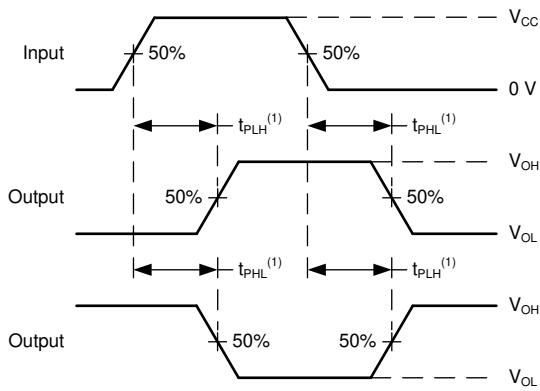


(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**図 7-4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**
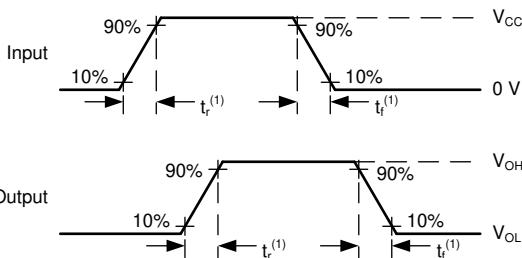


(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

**図 7-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**

Product Folder Links: SN54HC377 SN74HC377

# 8 Detailed Description

## 8.1 Overview

These devices are positive-edge-triggered octal D-type flip-flops with an enable input. The 'HC377 devices are similar to the 'HC273 devices, but feature a latched clock-enable ($\overline{\text{CLKEN}}$) input instead of a common clear.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse, if $\overline{\text{CLKEN}}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. These devices are designed to prevent false clocking by transitions at $\overline{\text{CLKEN}}$.

## 8.2 Functional Block Diagram

Product Folder Links: *SN54HC377 SN74HC377*
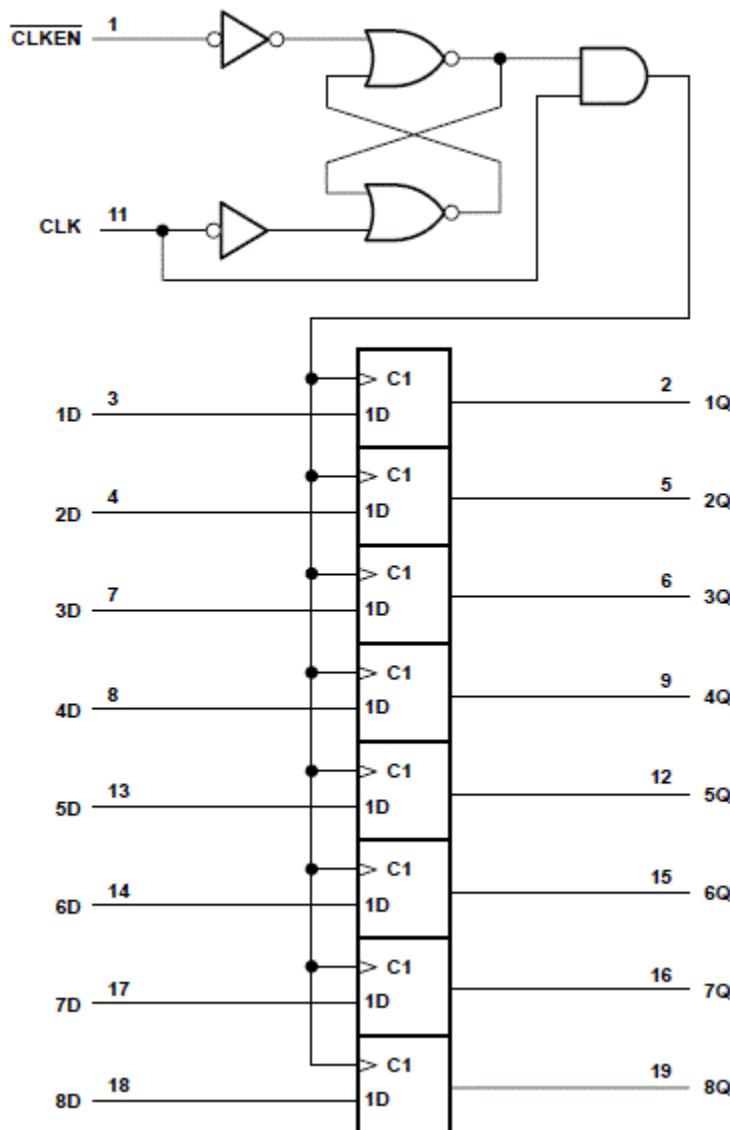
## 8.3 Device Functional Modes

**Function Table**
**(Each Flip-Flop)**

| INPUTS | | | OUTPUT |
| --- | --- | --- | --- |
| $\overline{\text{CLKEN}}$ | CLK | D | Q |
| H | X | X | $Q_0$ |
| L | ↑ | H | H |
| L | ↑ | L | L |
| X | L | X | $Q_0$ |

Product Folder Links: SN54HC377 SN74HC377

## 9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 10 Layout

### 10.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

# 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 11.1 Documentation Support

### 11.1.1 Related Documentation

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

## 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

TI Glossary           This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-87807012A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-87807012A SNJ54HC 377FK |
| 5962-8780701RA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8780701RA SNJ54HC377J |
| SN54HC377J | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC377J |
| SN54HC377J.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC377J |
| SN74HC377DW | Obsolete | Production | SOIC (DW) \| 20 | - | - | Call TI | Call TI | -40 to 85 | HC377 |
| SN74HC377DWR | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC377 |
| SN74HC377DWR.A | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC377 |
| SN74HC377N | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC377N |
| SN74HC377N.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC377N |
| SN74HC377NE4 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC377N |
| SN74HC377NSR | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC377 |
| SN74HC377NSR.A | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC377 |
| SNJ54HC377FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-87807012A SNJ54HC 377FK |
| SNJ54HC377FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-87807012A SNJ54HC 377FK |
| SNJ54HC377J | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8780701RA SNJ54HC377J |
| SNJ54HC377J.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8780701RA SNJ54HC377J |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC377, SN74HC377 :**

- Catalog : SN74HC377

- Military : SN54HC377

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**
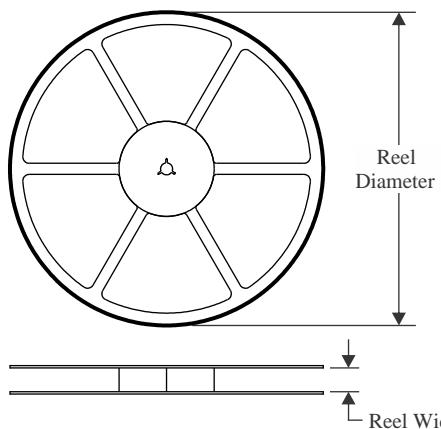


**TAPE DIMENSIONS**
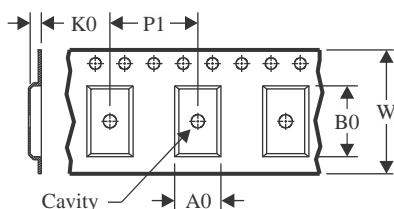


| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
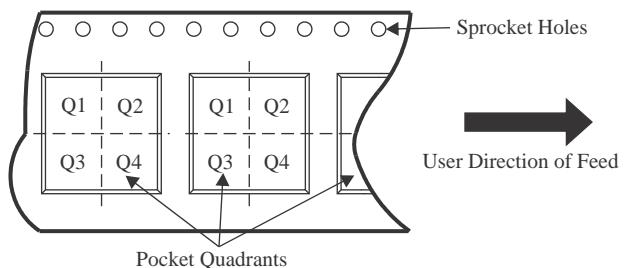


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC377DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74HC377NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

**PACKAGE MATERIALS INFORMATION**

**TAPE AND REEL BOX DIMENSIONS**
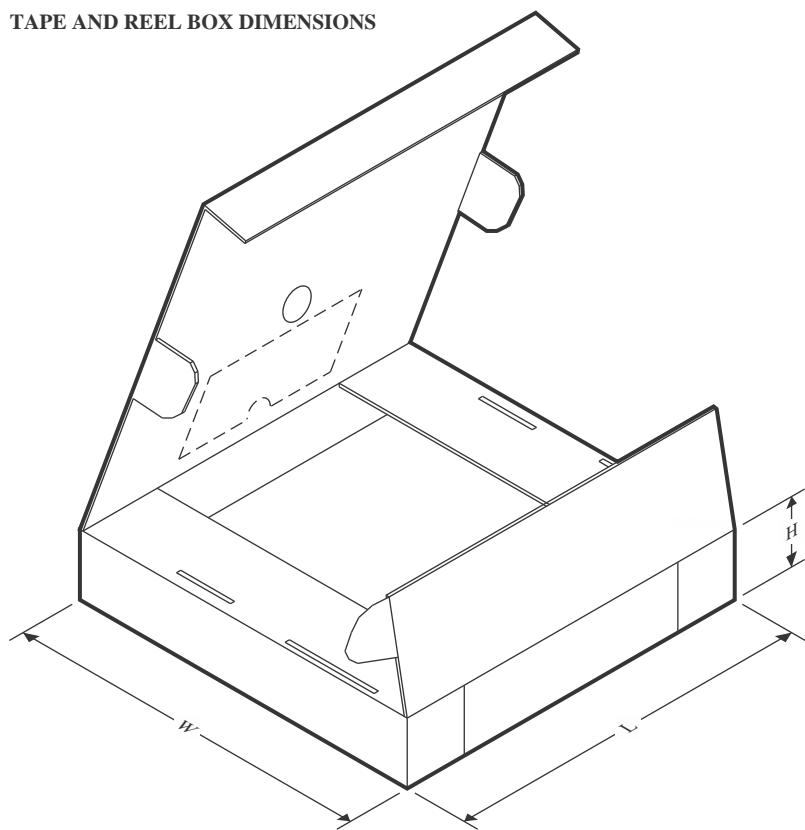


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|-----------|-------------|
| SN74HC377DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74HC377NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |

## TUBE



T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
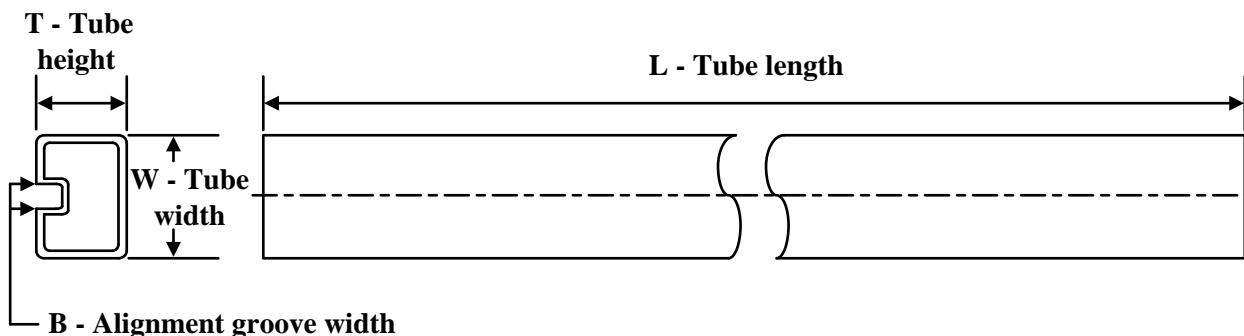
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-87807012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SN74HC377N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC377N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC377NE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC377FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC377FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

**NS (R-PDSO-G**)**                                    PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**

| PINS ** DIM | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A    MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A    MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03
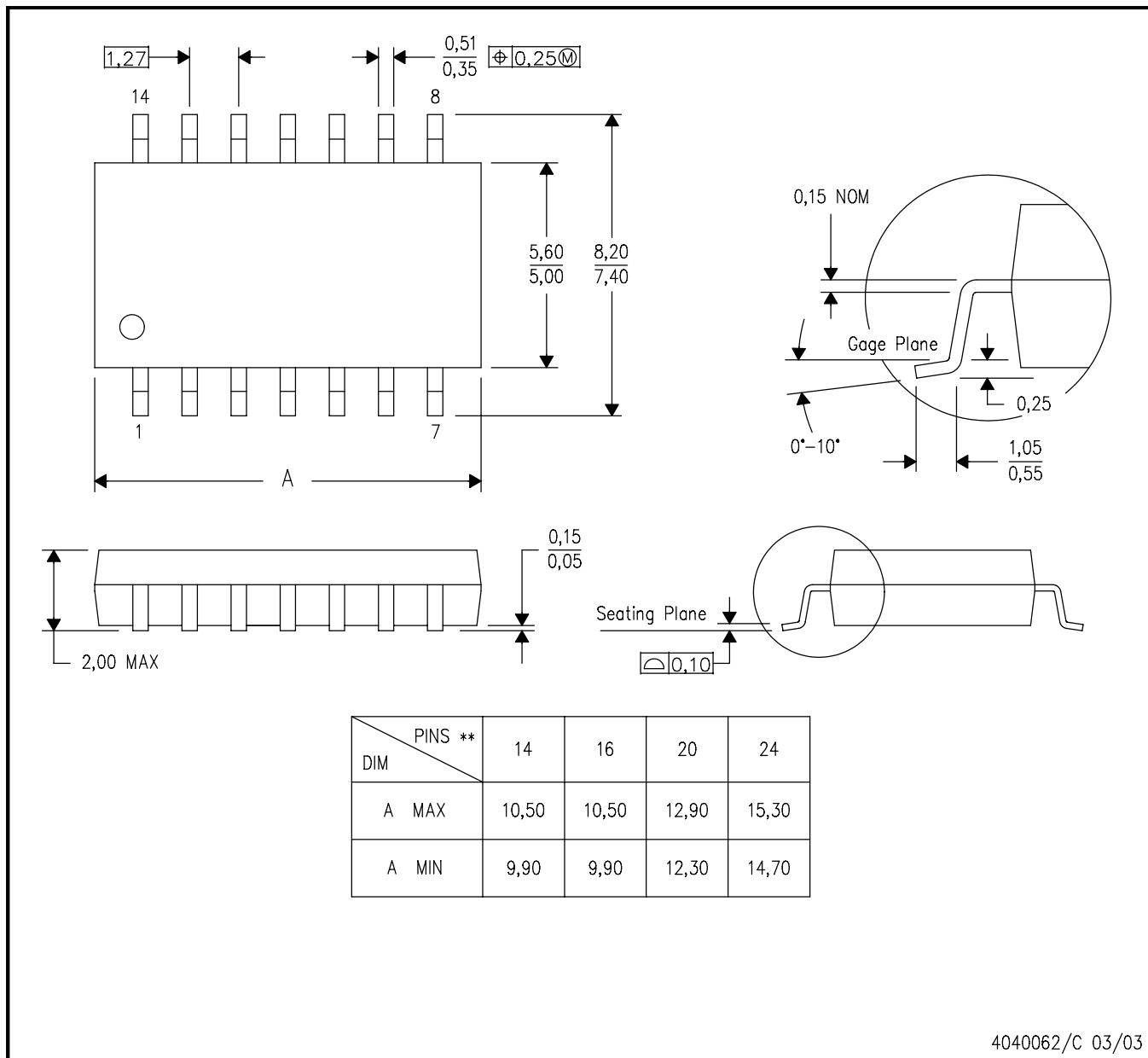
NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.
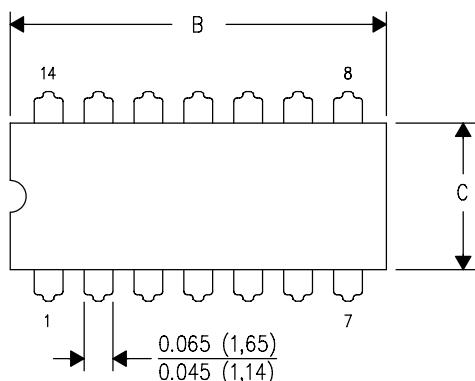
| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14    8

C

1    7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)
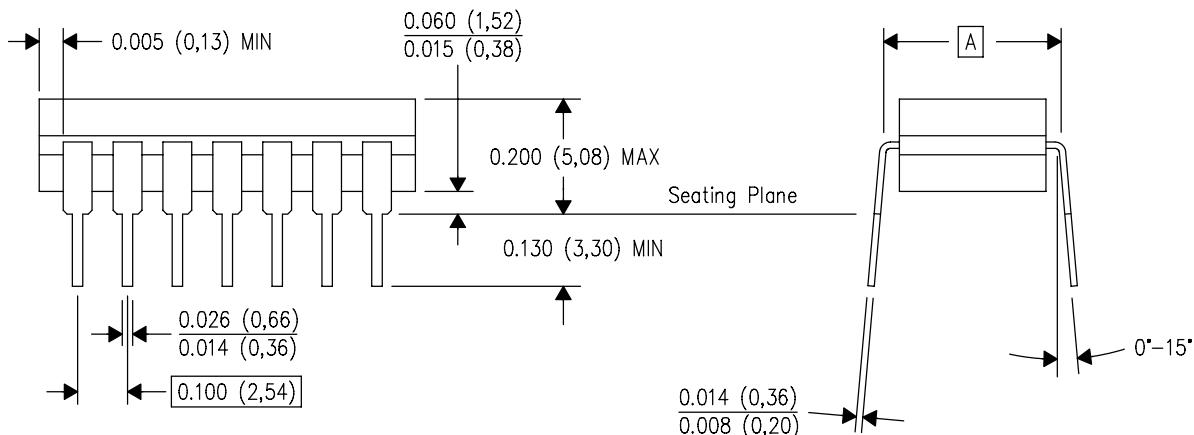
4040083/F 03/03

NOTES:    A.  All linear dimensions are in inches (millimeters).
          B.  This drawing is subject to change without notice.
          C.  This package is hermetically sealed with a ceramic lid using glass frit.
          D.  Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E.  Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
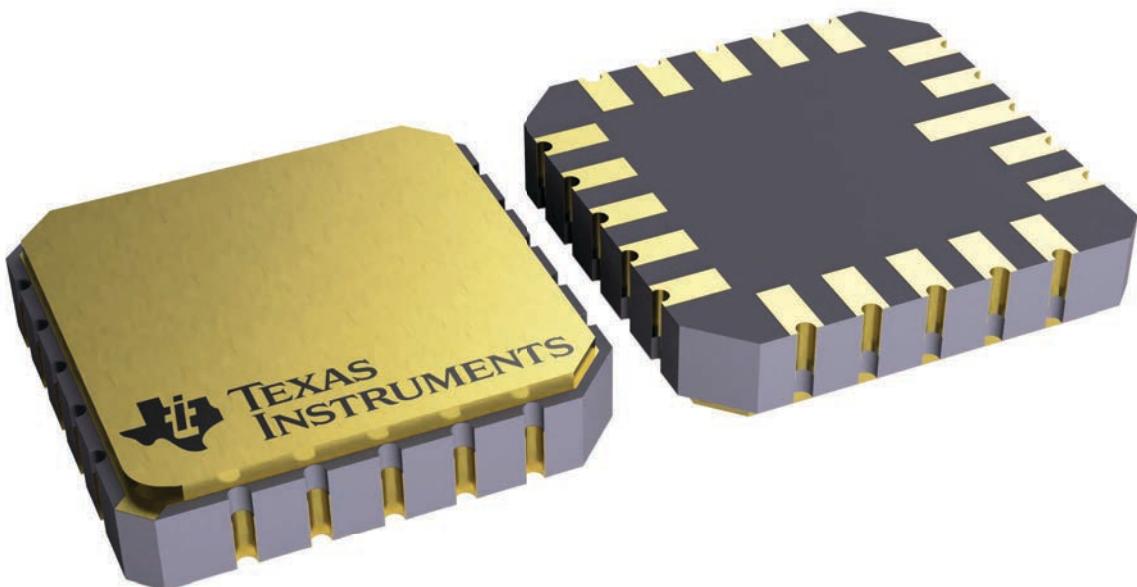


4229370VA\

**MECHANICAL DATA**

## N (R−PDIP−T**)
16 PINS SHOWN

## PLASTIC DUAL−IN−LINE PACKAGE

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS−001 VARIATION | AA | BB | AC | AD |

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) ⚠D

0.045 (1,14) / 0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option ⚠D

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
⚠D The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS INSTRUMENTS
www.ti.com

C

SEATING PLANE

◯ 0.1 C

10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

20

18X 1.27

13.0 / 12.6 NOTE 3

2X 11.43

10

11

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

2.65 MAX

B

7.6 / 7.4 NOTE 4

SEE DETAIL A

0.33 / 0.10 TYP

0.25 GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20X (0.6)

20

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)
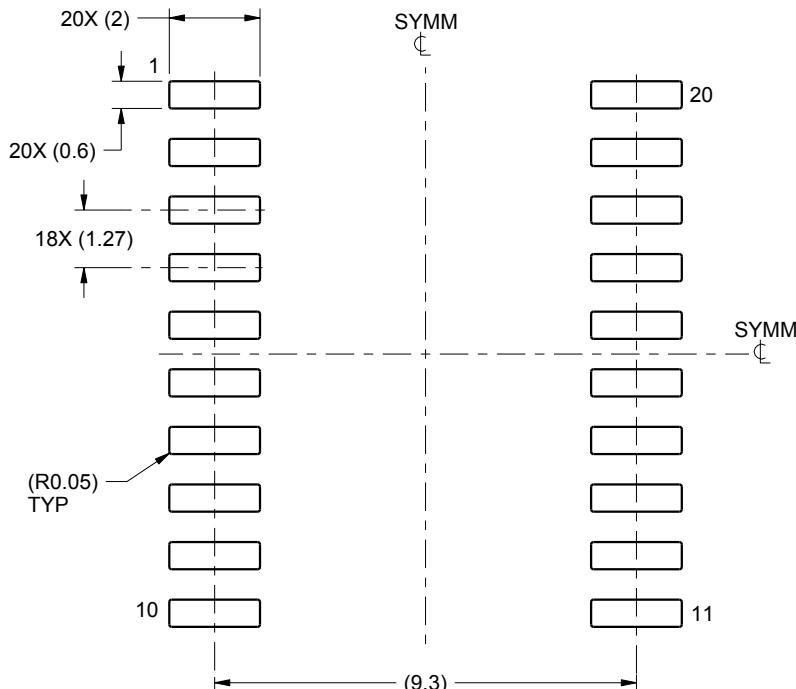
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
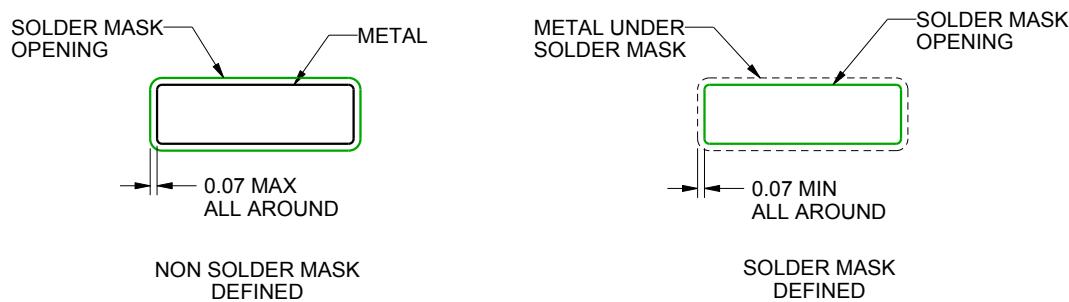
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

TEXAS
INSTRUMENTS
www.ti.com
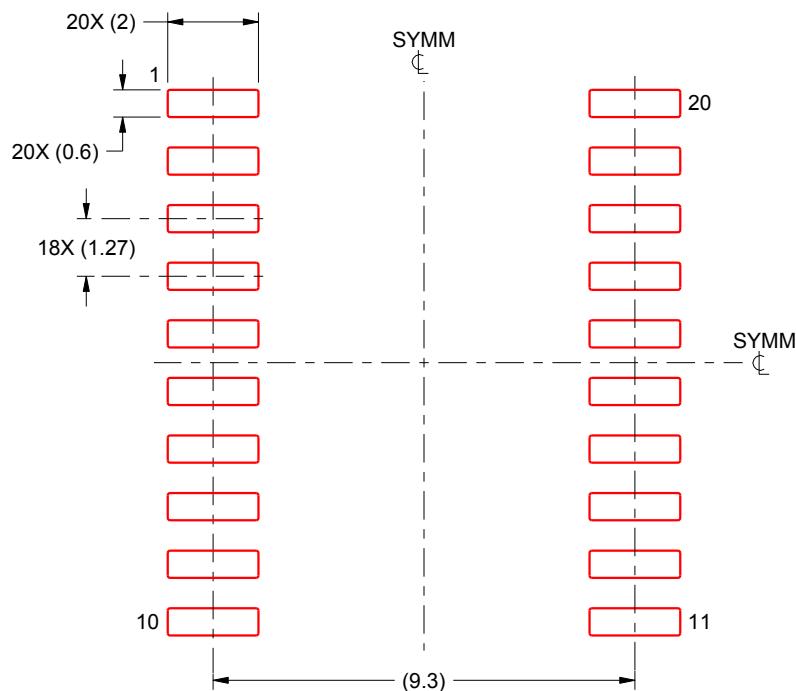
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.