

SNx4HC640 3 ステート出力、オクタル・バス・トランシーバ

1 特長

- 幅広い動作電圧範囲: 2V~6V
- 大電流 3 ステート出力により最大 10 個の LSTTL 負荷を駆動可能
- 低消費電力、最大 I_{CC} 80 μ A
- $t_{pd} = 8ns$ (標準値)
- 5V で $\pm 4mA$ の出力駆動能力
- 低い入力電流: 最大 1 μ A
- 反転ロジック

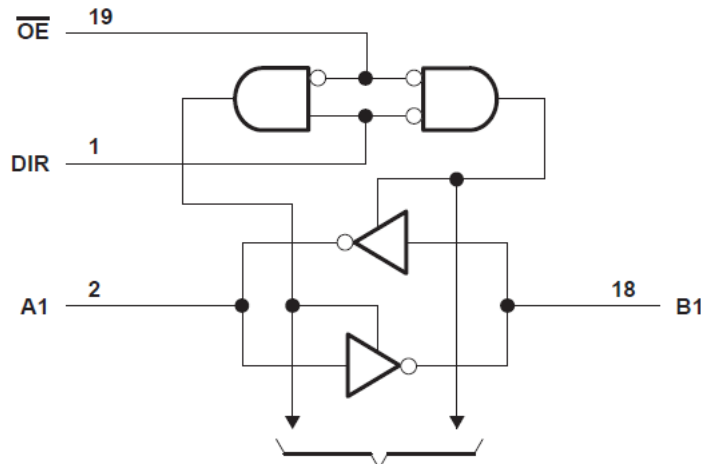
2 概要

SNx4HC640 は、3 ステート出力を備えたオクタル・バス・トランシーバです。8 つのチャンネルはすべて、方向 (DIR) ピンと出力イネーブル (\overline{OE}) ピンにより制御されます。

製品情報 ⁽¹⁾

部品番号	パッケージ	本体サイズ (公称)
SN54HC640	J (CDIP, 20)	26.92mm × 6.92mm
SN74HC640	DW (SOIC, 20)	12.80mm × 7.50mm
	N (PDIP, 20)	25.40mm × 6.35mm
	NS (SO, 20)	15.00mm × 5.30mm
	PW (TSSOP, 20)	4.40mm × 6.50mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



ピン配置
上面図



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3 Revision History

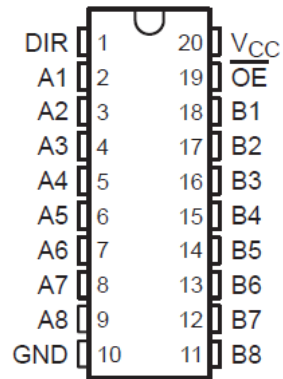
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (August 2003) to Revision E (September 2022)

Page

- | | |
|---|---|
| • 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新..... | 1 |
|---|---|

4 Pin Configuration and Functions



J, DW, N, NS, or PW Package
20-Pin CDIP, SOIC, PDIP, SO, TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	(V _I < 0 or V _I > V _{CC})		±20 mA
I _{OK}	Output clamp current ⁽²⁾	(V _O < 0 or V _O > V _{CC})		±20 mA
I _O	Continuous output current	(V _O = 0 to V _{CC})		±35 mA
V _{CC} or GND	Continuous current through			±70 mA
T _J	Junction temperature			150 °C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

		SN54HC640			SN74HC640			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 6 V		4.2	4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V	
		V _{CC} = 4.5 V		1.35		1.35		
		V _{CC} = 6 V		1.8		1.8		
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise/fall time	V _{CC} = 2 V		1000		1000		ns
		V _{CC} = 4.5 V		500		500		
		V _{CC} = 6 V		400		400		
T _A	Operating free-air temperature	- 55		125	- 40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating SMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	
R _{θJA}	Package thermal impedance	58	69	60	83	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	T _A = 25°C			SN54HC640		SN74HC640		UNIT			
				MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V _{OH}	High-level output voltage	I _{OH} = -20 μA	2	1.9	1.998		1.9		1.9	V				
			4.5	4.4	4.400		4.4		4.4					
			6	5.9	5.999		5.9		5.9					
		I _{OH} = -6 mA	4.5	3.98	4.3		3.7		3.84					
		I _{OH} = -7.8 mA	6	5.48	5.8		5.2		5.34					
V _{OL}	Low-level output voltage	I _{OL} = 20 μA	2		0.002	0.1		0.1		0.1	V			
			4.5		0.001	0.1		0.1		0.1				
			6		0.001	0.1		0.1		0.1				
		I _{OL} = 6 mA	4.5		0.17	0.26		0.4		0.33				
		I _{OL} = 7.8 mA	6		0.15	0.26		0.4		0.33				
I _I	Input hold current	DIR or \overline{OE}	V _I = V _{CC} or 0	6		±0.1	±100		±1000		±1000	nA		
I _{OZ}	Off-state output current	A or B	V _I = V _{CC} or 0. I _O = 0	6		±0.01	±0.5		±10		±5	μA		
ΔI _{CC}	Supply-current change		One input at 0.5V or 2.4 V, Other inputs at 0 or V _{CC}	6					8		160		80	μA
C _i	Input capacitance	DIR or \overline{OE}		2 to 6		3	10		10		10		10	pF

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Switching Characteristics

C_L = 50 pF. See Figure 6

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V _{CC} (V)	T _A = 25°C			SN54HC640		SN74HC640		
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Propagation delay	A or B	Y	2		29	105		160		130	ns
				4.5		10	21		32		26	
				6		8	18		27		22	
t _{en}	Enable time	\overline{OE}	A or B	2		109	230		340		290	ns
				4.5		27	46		68		58	
				6		20	39		58		49	
t _{dis}	Disable time	\overline{OE}	A or B	2		40	150		225		190	ns
				4.5		18	30		45		38	
				6		16	26		38		32	
t _t	Transition time		A or B	2		20	60		90		75	ns
				4.5		8	12		18		15	
				6		6	10		15		13	

5.5 Switching Characteristics

$C_L = 150$ pF. See [Figure 6](#)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	$T_A = 25^\circ\text{C}$			SN54HC640		SN75HC640		
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A or B	B or A	2	44	190	290		235		ns	
				4.5	14	38	58		47			
				6	11	33	49		41			
t_{en}	Enable time	OE	A or B	2	124	315	470		395		ns	
				4.5	31	63	94		79			
				6	23	54	80		68			
t_t	Transition time		A or B	2	45	210	315		265		ns	
				4.5	17	42	63		53			
				6	13	36	53		45			

5.6 Operating Characteristics

$T_A = 25^\circ\text{C}$

		Test Conditions	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	40	pF

6 Parameter Measurement Information

t_{pd} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

t_{dis} is the maximum between t_{PLZ} and t_{PHZ}

t_{en} is the maximum between t_{PZL} and t_{PZH}

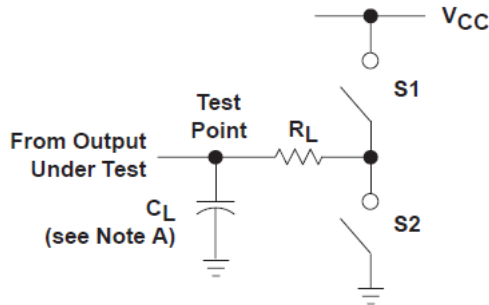


图 6-1. Load Circuit

PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 k Ω	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 k Ω	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open

图 6-2.

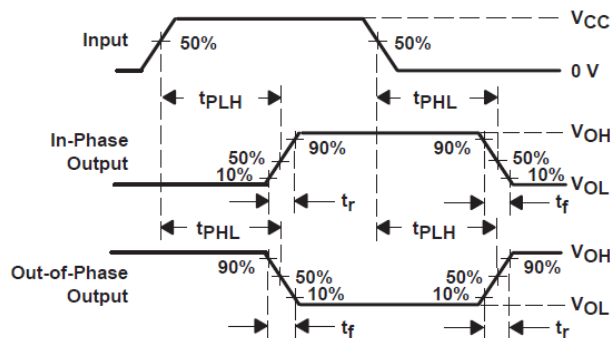


图 6-3. Voltage Waveforms
Propagation Delay and Output Transition Times

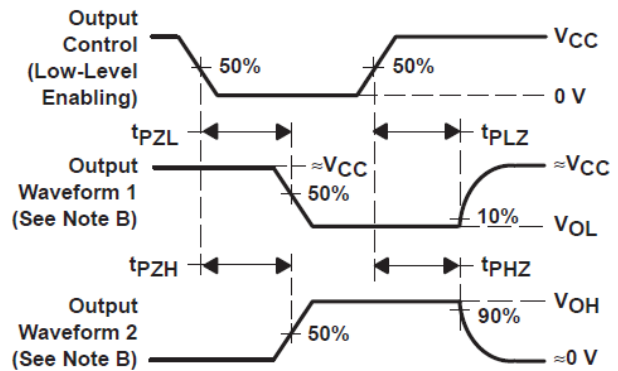


图 6-4. Voltage Waveforms
Enable and Disable Times for 3-State Outputs

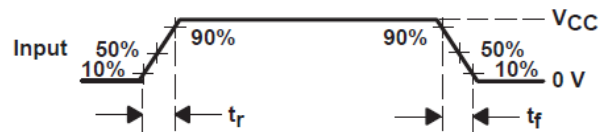


图 6-5. Voltage Waveforms
Propagation Delay and Output Transition Times

A. C_L includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.

D. The outputs are measured one at a time with one input transition per measurement.

7 Detailed Description

7.1 Overview

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

7.2 Functional Block Diagram

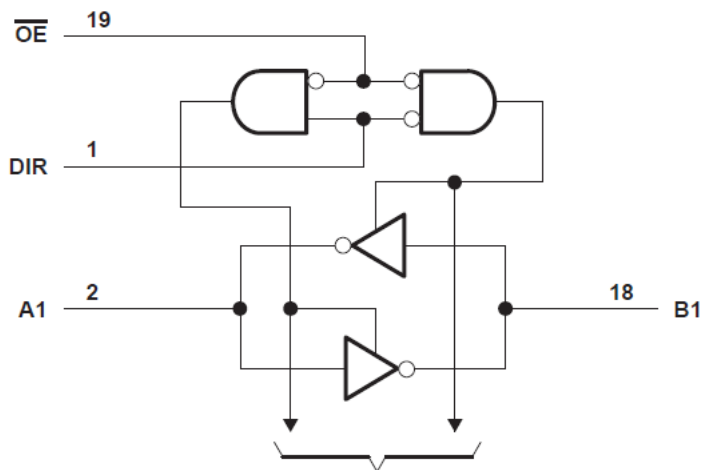


图 7-1. Functional Block Diagram

7.3 Device Functional Modes

表 7-1. Function Table
(each transceiver)

INPUTS ⁽¹⁾		Operation
OE	DIR	
L	L	\overline{B} data to A bus
L	H	\overline{A} data to B bus
H	X	Isolation

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8780901RA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8780901RA SNJ54HC640J	Samples
SN54HC640J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC640J	Samples
SN74HC640DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	HC640	
SN74HC640DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SN74HC640N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC640N	Samples
SN74HC640NSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SN74HC640PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	HC640	
SN74HC640PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC640	Samples
SNJ54HC640J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8780901RA SNJ54HC640J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF SN54HC640, SN74HC640 :

- Catalog : [SN74HC640](#)
- Military : [SN54HC640](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC640DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HC640DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC640NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC640PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

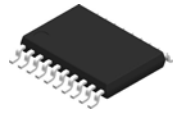
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC640DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC640DWR	SOIC	DW	20	2000	356.0	356.0	41.0
SN74HC640NSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74HC640PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HC640N	N	PDIP	20	20	506	13.97	11230	4.32

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

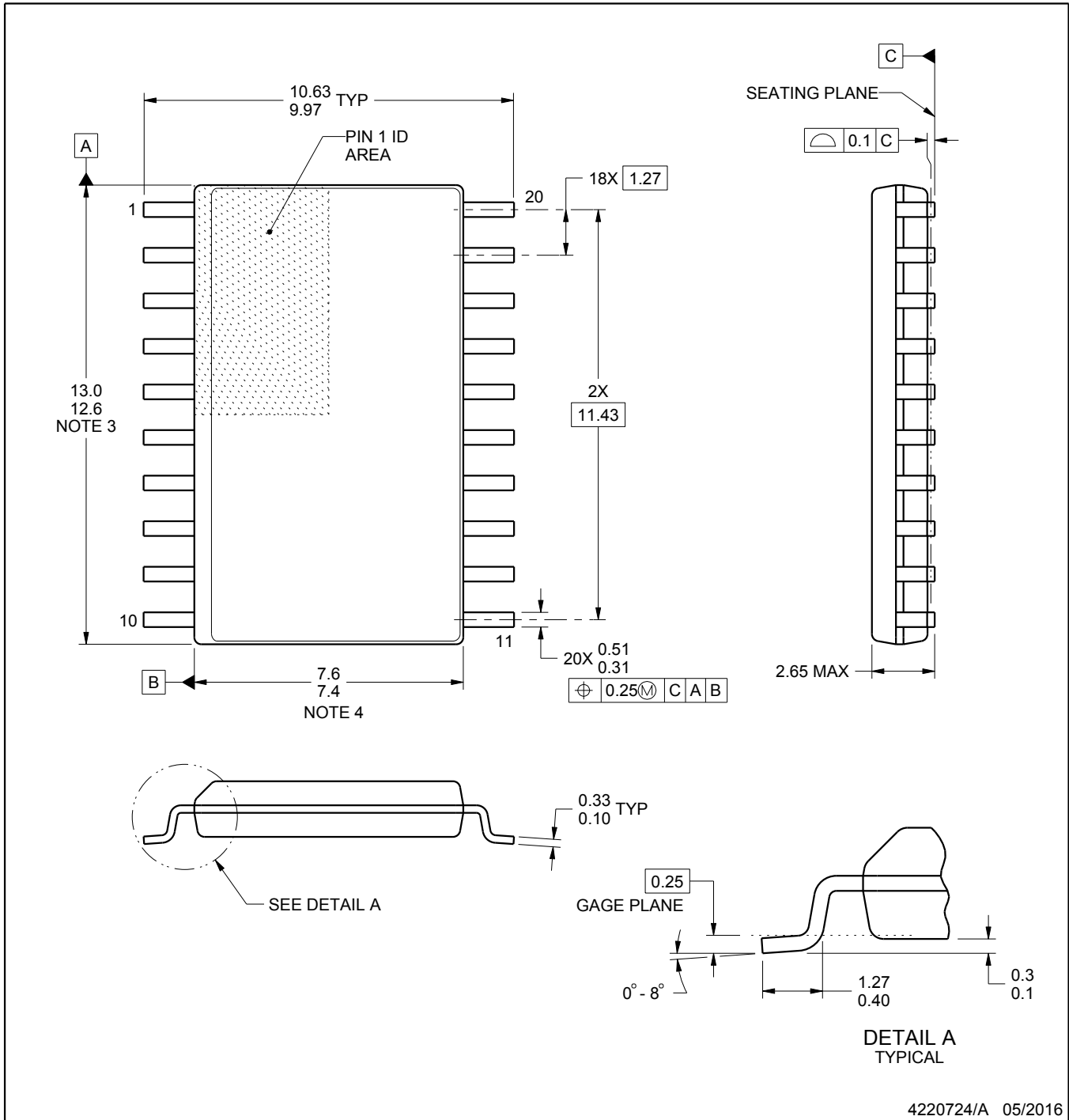
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

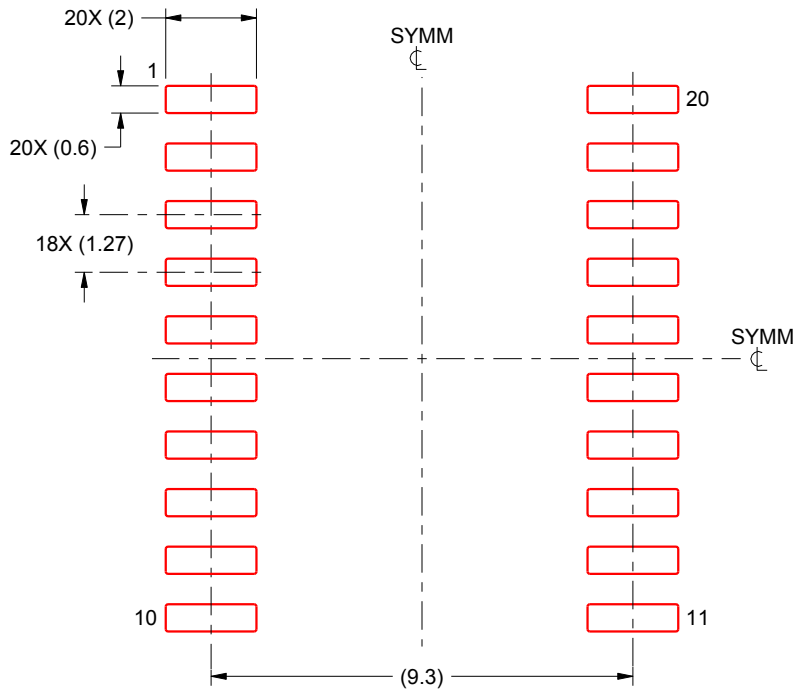
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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