SN74HCT595 3 ステート出力レジスタ付き 8 ビット シフト・レジスタ

1 特長

- LSTTL 入力ロジック互換
  - $V_{IL(max)}$ = 0.8V、$V_{IH(min)}$ = 2V
- CMOS 入力ロジック互換
  - $I_I \leq 1\mu A$ (V_{OL}、V_{OH})
- 4.5V～5.5V で動作
- 最大 10 個の LSTTL 負荷ファンアウトに対応
- シフト・レジスタはダイレクト・クリアを装備
- 拡張周囲温度範囲：–40℃～+125℃、T_A

2 アプリケーション

- 出力拡張
- LED マトリクス制御
- 7 セグメント・ディスプレイ制御
- 8 ビット・データ・ストレージ

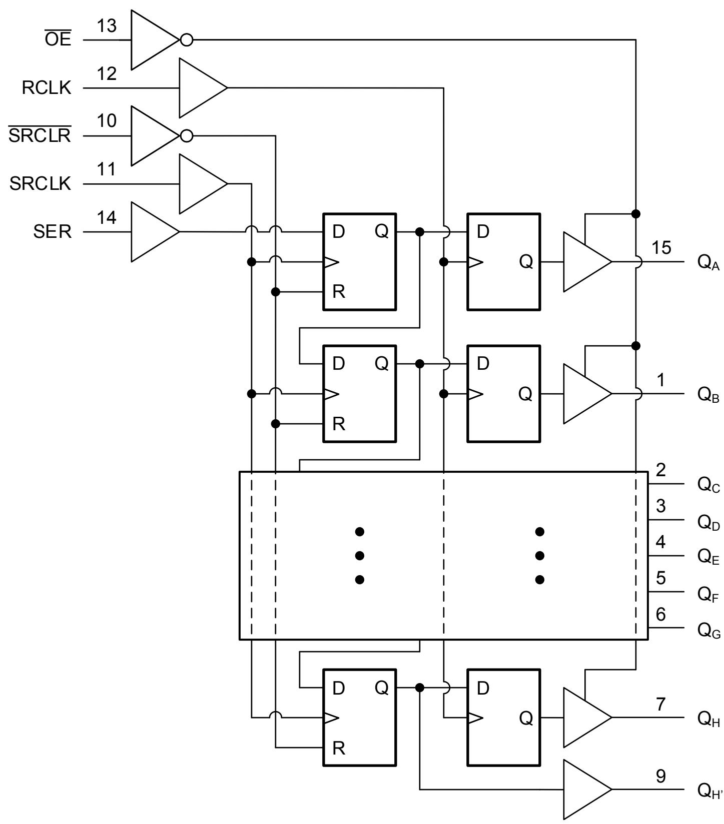
3 概要

SN74HCT595 デバイスには 8 ビットのシリアル・イン、パラレル・アウトのシフト・レジスタが搭載されており、8 ビットの D タイプ・ストレージ・レジスタへデータを供給します。ストレージ・レジスタはパラレルの 3 ステート出力を備えています。シフト・レジスタとストレージ・レジスタの両方に、それぞれ独立したクロックが供給されます。シフト・レジスタはダイレクト・オーバーライディング・クリア ($\overline{SRCLR}$) 入力、シリアル (SER) 入力、カスケード用シリアル出力 ($Q_{H'}$) を備えています。出力イネーブル ($\overline{OE}$) 入力が High のとき、出力は高インピーダンス状態になります。内部レジスタ・データおよびシリアル出力 ($Q_{H'}$) は、$\overline{OE}$ 入力の動作による影響を受けません。

製品情報[(1)]

部品番号	パッケージ	本体サイズ (公称)
SN74HCT595PW	TSSOP (16)	5.00mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2021) to Revision A (December 2021)	**Page**
• データシートのステータスを事前情報から*量産データに更新*	1

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5 Pin Configuration and Functions

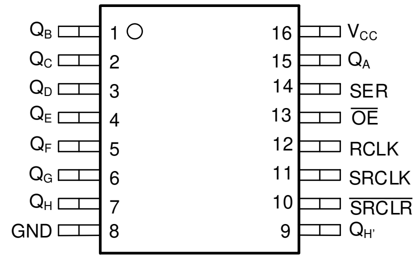

図 5-1. PW Package 16-Pin TSSOP Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
Q_B	1	O	Q_B O
Q_C	2	O	Q_C O
Q_D	3	O	Q_D O
Q_E	4	O	Q_E O
Q_F	5	O	Q_F O
Q_G	6	O	Q_G O
Q_H	7	O	Q_H O
GND	8	—	Ground
$Q_{H'}$	9	O	Serial O, can be used for cascading
$\overline{SRCLR}$	10	I	Shift register clear, active low
SRCLK	11	I	Shift register clock, rising edge triggered
RCLK	12	I	O register clock, rising edge triggered
$\overline{OE}$	13	I	O Enable, active low
SER	14	I	Serial I
Q_A	15	O	Q_A O
V_{CC}	16	—	Positive supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current[(2)]	$V_I < 0$ or $V_I > V_{CC} + 0.5$ V	–20	20	mA
I_{OK}	Output clamp current[(2)]	$V_O < 0$ or $V_O > V_{CC} + 0.5$ V	–20	20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	–35	35	mA
I_{CC}	Continuous output current through V_{CC} or GND		–70	70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Δt/Δv	Input transition rise and fall rate	V_{CC} = 4.5 V to 5.5V			500	ns/V
T_A	Ambient temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		SN74HCT595 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	76.1	°C/W

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6.4 Thermal Information (continued)

THERMAL METRIC[1]		SN74HCT595 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	-40°C to 125°C MIN	-40°C to 125°C TYP	-40°C to 125°C MAX	UNIT
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OH} = -20 uA, V_{CC} = 4.5 V	4.4			4.4			V
			I_{OH} = -6 mA, V_{CC} = 4.5 V	3.98			3.84			V
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 uA, V_{CC} = 4.5 V			0.1			0.1	V
			I_{OL} = 6 mA, V_{CC} = 4.5 V			0.26			0.33	V
I_I	Input leakage current	$V_I = V_{CC}$ or 0	V_{CC} = 5.5 V			±100			±1000	nA
I_{OZ}	Off-State (High-Impedance State) Output Current	$V_O = V_{CC}$ or 0, Q_A-Q_H	V_{CC} = 5.5 V			±0.5			±5	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, I_O = 0	V_{CC} = 5.5 V			8			80	µA
ΔI_{CC}	Additional Quiescent Device Current Per Input Pin	$V_I = V_{CC}$ - 2.1V	V_{CC} = 4.5V to 5.5V			126.2			157.5	µA
		V_I = 0.5 V or 2.4V	V_{CC} = 5.5V			2.4			2.9	mA
C_i	Input capacitance	V_{CC} = 4.5V to 5.5V	V_{CC} = 4.5V to 5.5V			10				pF
C_O	Output capacitance	V_{CC} = 4.5V to 5.5V	V_{CC} = 4.5V to 5.5V			20				pF
C_{pd}	Power dissipation capacitance per gate	No load				50				pF

6.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITION	V_{CC}	T_A = 25°C MIN	T_A = 25°C MAX	-40°C to 125°C MIN	-40°C to 125°C MAX	UNIT
f_{clock}	Clock frequency		4.5 V		31		25	MHz
t_w	Pulse duration	SRCLK or RCLK high or low	4.5 V	16		20		ns
			5.5 V	16		20		
		$\overline{\text{SRCLR}}$ low	4.5 V	16		20		
			5.5 V	16		20		

6.6 Timing Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITION	V_{CC}	T_A = 25°C MIN	T_A = 25°C MAX	-40°C to 125°C MIN	-40°C to 125°C MAX	UNIT
t_{su}	Setup time	SER before SRCLK↑	4.5 V	20		25		ns
			5.5 V	20		25		
		SRCLK↑ before RCLK↑	4.5 V	16		20		
			5.5 V	16		20		
		$\overline{SRCLR}$ low before RCLK↑	4.5 V	10		13		
			5.5 V	10		13		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	4.5 V	10		12		
			5.5 V	10		12		
t_h	Hold time	SER after SRCLK↑	4.5 V	0		0		ns
			5.5 V	0		0		

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	-40°C to 125°C MIN	-40°C to 125°C TYP	-40°C to 125°C MAX	UNIT
f_{max}				4.5 V	31			25			MHz
t_{pd}	Propogation delay	SRCLK	$Q_{H'}$	4.5 V			42			53	ns
				5.5 V			42			53	
		RCLK	Q_A - Q_H	4.5 V			40			50	
				5.5 V			40			50	
t_{PHL}	Propogation delay	$\overline{SRCLR}$	$Q_{H'}$	4.5 V			40			50	ns
				5.5 V			40			50	
t_{en}	Enable time	$\overline{OE}$	Q_A - Q_H	4.5 V			35			44	ns
				5.5 V			35			44	
t_{dis}	Disable time	$\overline{OE}$	Q_A - Q_H	4.5 V			30			38	ns
				5.5 V			30			38	
t_t	Transition-time		Any output	4.5 V			12			15	ns
			Any output	5.5 V			14			17	

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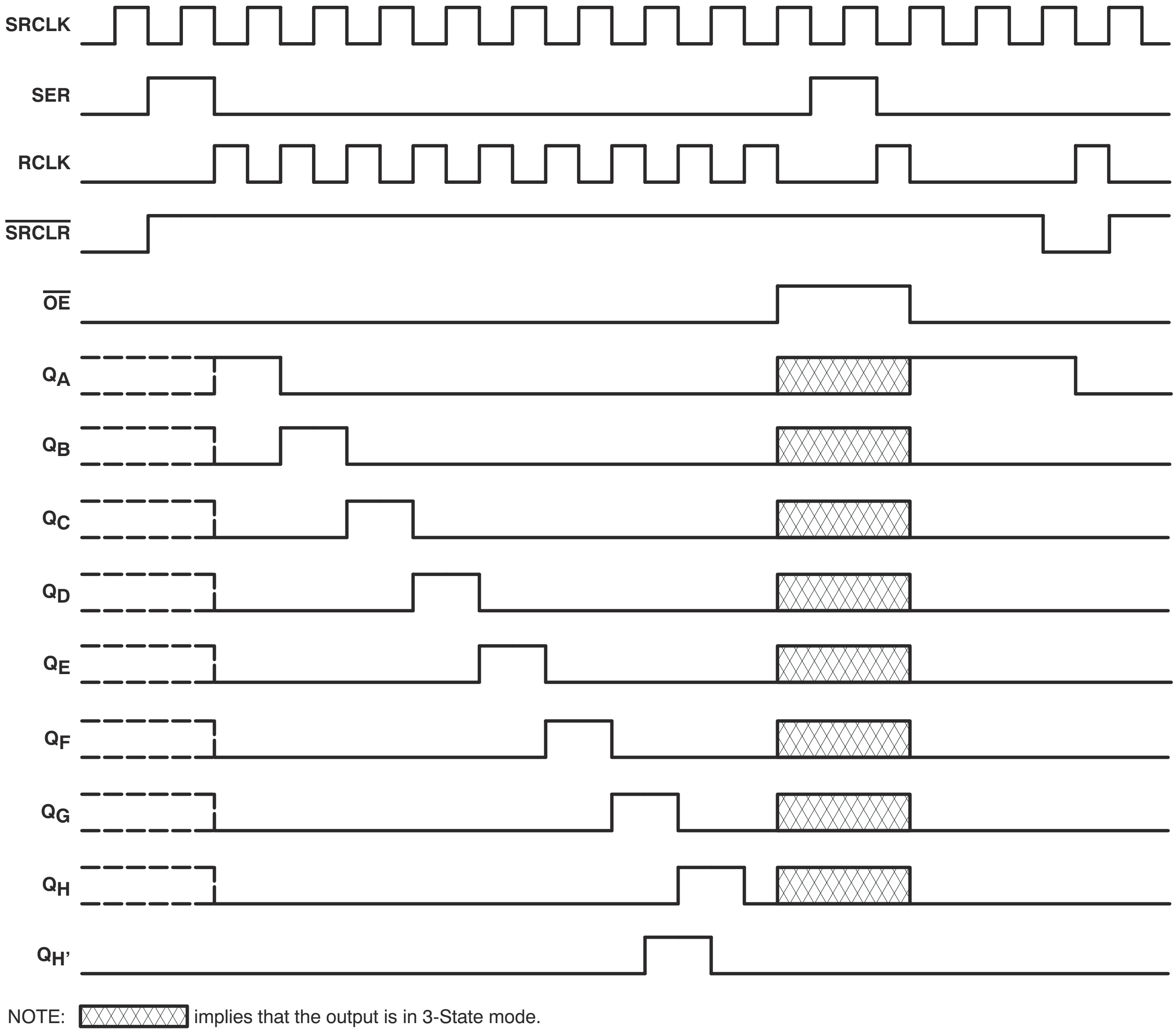

NOTE: implies that the output is in 3-State mode.

図 6-1. Timing Diagram

6.8 Typical Characteristics

T_A = 25°C

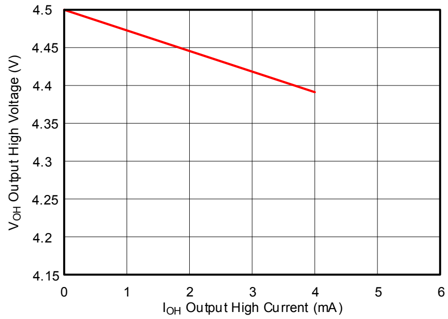

図 6-2. Typical Output Voltage in the High State (V_{OH})

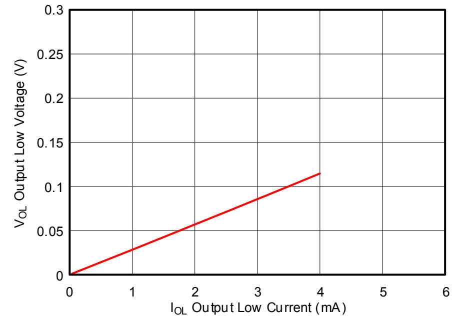

図 6-3. Typical Output Voltage in the Low State (V_{OL})

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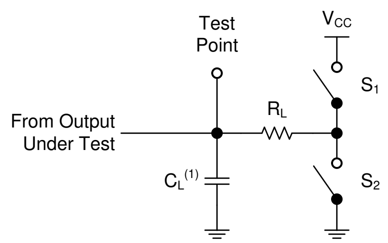
7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

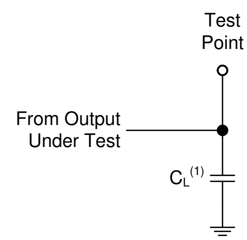
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

図 7-1. Load Circuit for 3-State Outputs



(1) C_L includes probe and test-fixture capacitance.

図 7-2. Load Circuit for Push-Pull Outputs

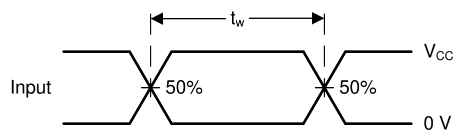


図 7-3. Voltage Waveforms, Pulse Duration

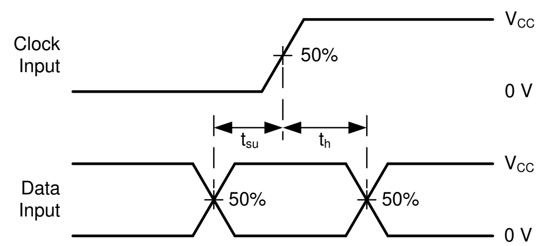
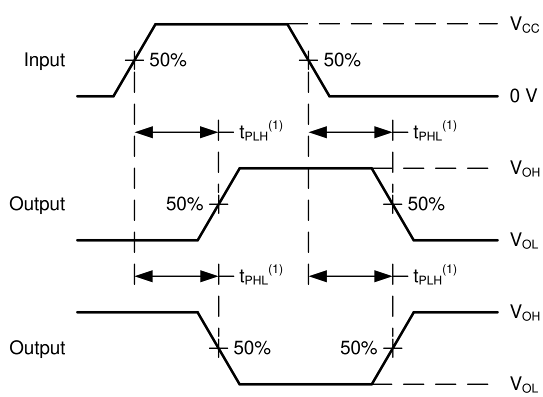


図 7-4. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 7-5. Voltage Waveforms Propagation Delays

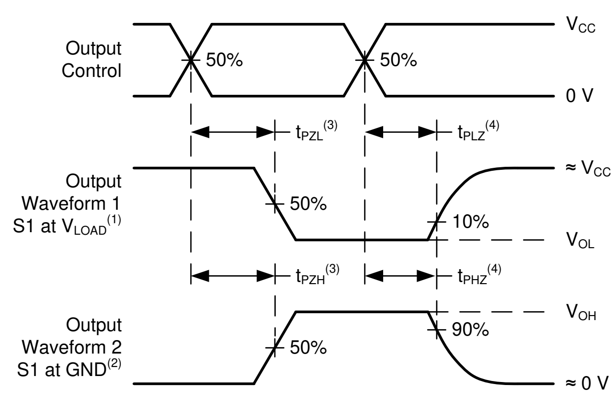
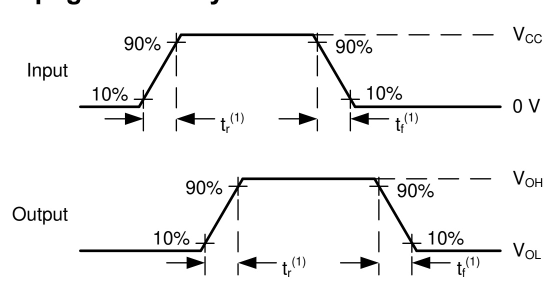


図 7-6. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

図 7-7. Voltage Waveforms, Input and Output Transition Times

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8 Detailed Description

8.1 Functional Block Diagram

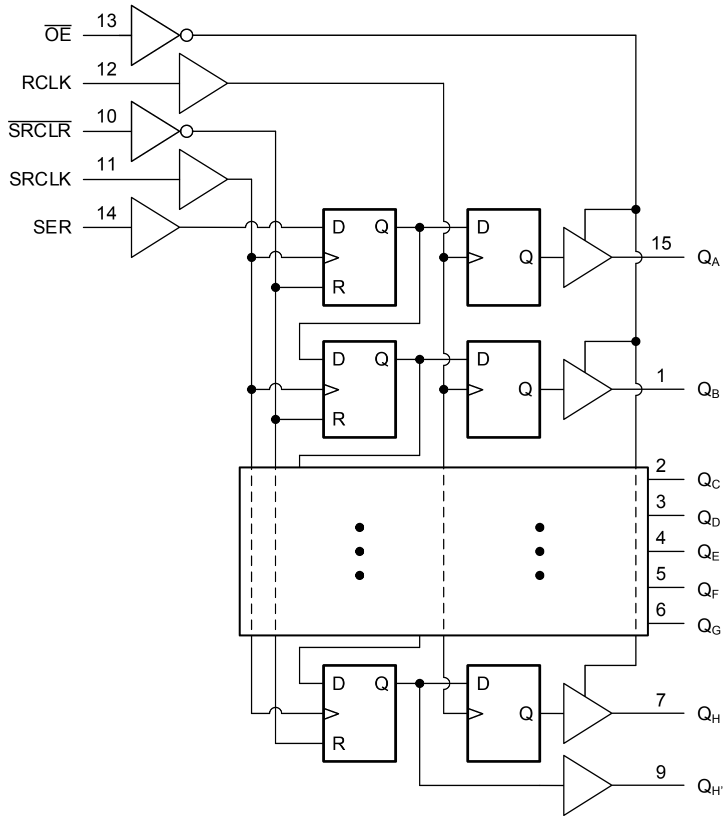

図 8-1. Logic Diagram (Positive Logic) for the SN74HCT595

8.2 Feature Description

8.2.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-State outputs. The three states that these outputs can be in are driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10 kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

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8.2.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.2.3 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

8.2.4 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

8.2.5 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 図 8-2.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

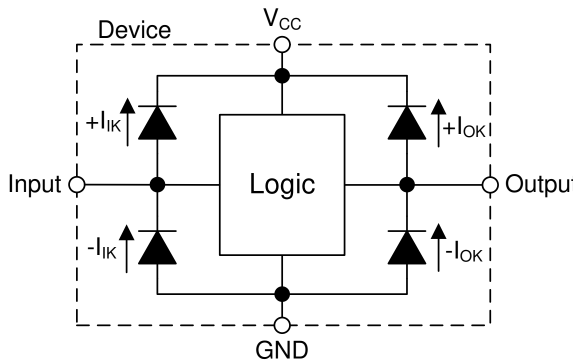

図 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.3 Device Functional Modes

Function Table lists the functional modes of the SN74HCT595.

表 8-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{SRCLR}$	RCLK	$\overline{OE}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	H	↑	X	Shift-register data is stored in the storage register.
X	↑	H	↑	X	Data in shift register is stored in the storage register, the data is then shifted through.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

In this application, the SN74HCT595 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74HCT595 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

The OE pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the SN74HCT595 can be controlled accordingly to turn off all the outputs reducing the I/O needed to three. There is no practical limitation to how many SN74HCT595 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, the shift register needs to be cleared and then clocked into the output register.

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9.2 Typical Application

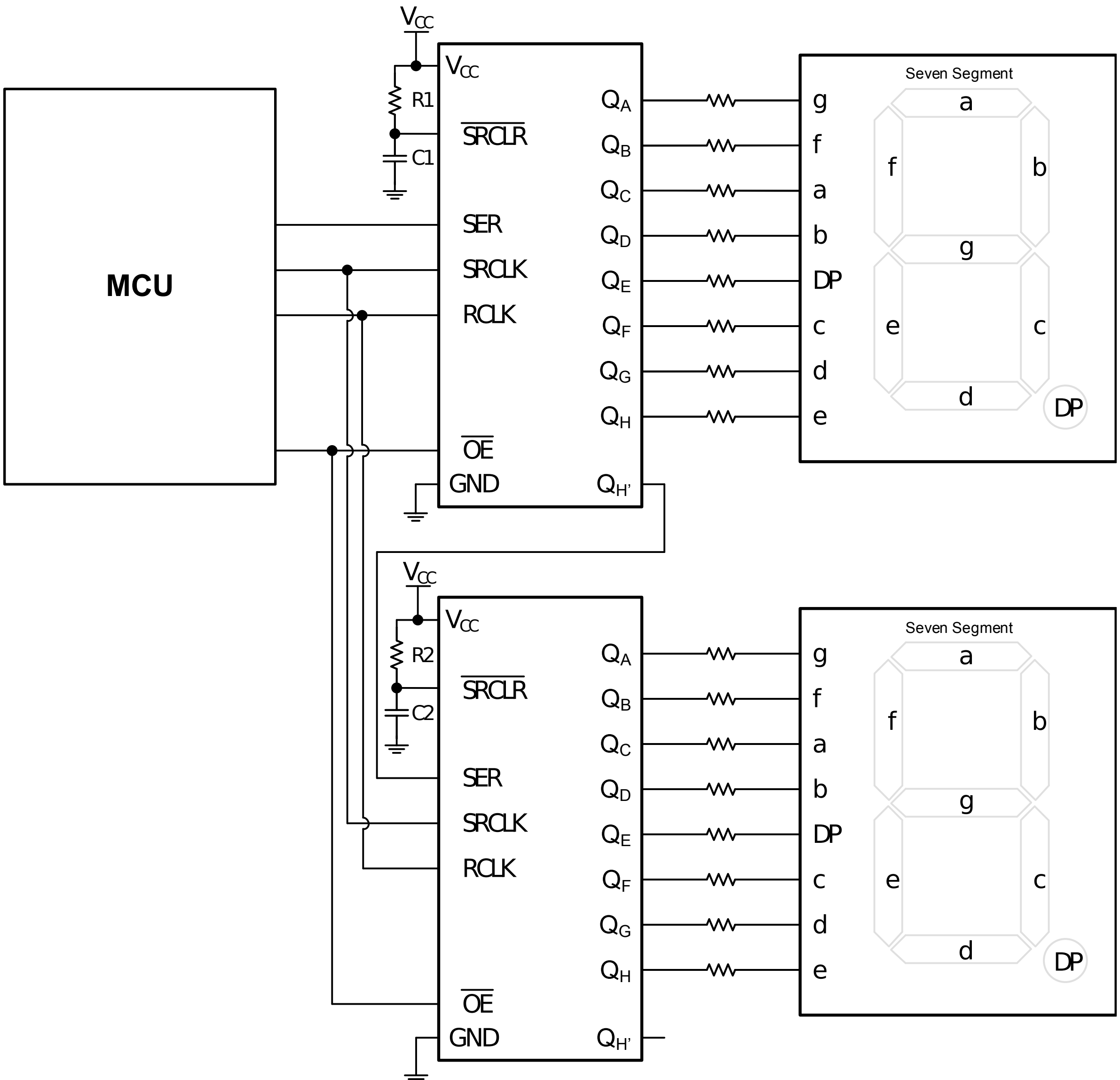

図 9-1. Typical Application Block Diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCT595 plus the maximum static supply current, I_{CC}, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

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The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCT595 plus the maximum supply current, I_{CC}, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCT595 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74HCT595 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCT595, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HCT595 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

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9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCT595 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.

9.2.3 Application Curve

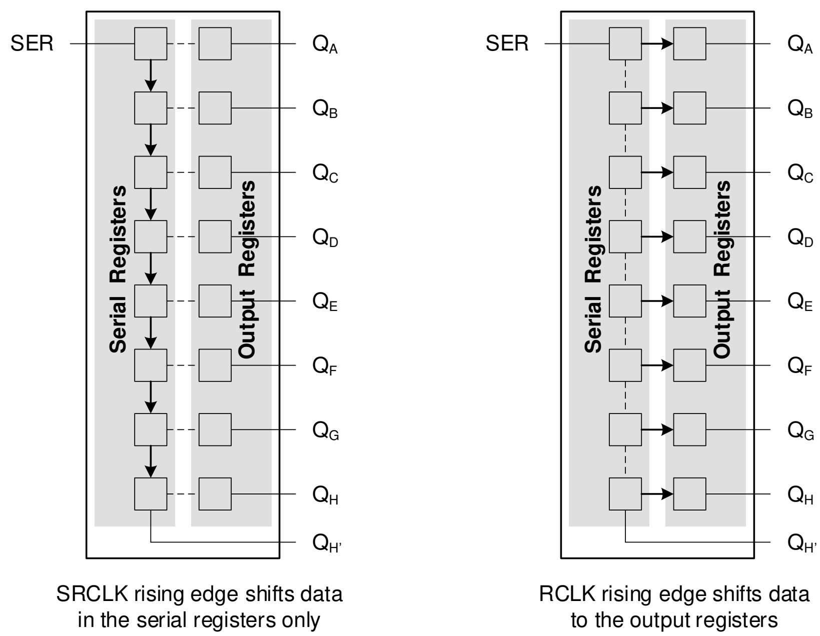

図 9-2. Simplified Functional Diagram Showing Clock Operation

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10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

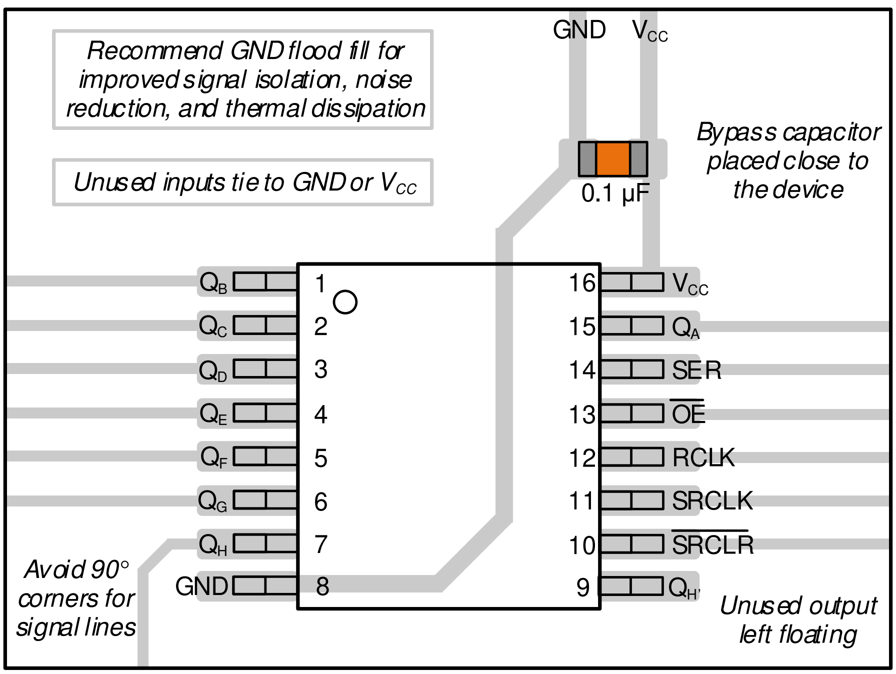

図 11-1. Example Layout for the SN74HCT595

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *HCMOS Design Considerations* application report
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCT595PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HT595
SN74HCT595PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HT595

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74HCT595 :

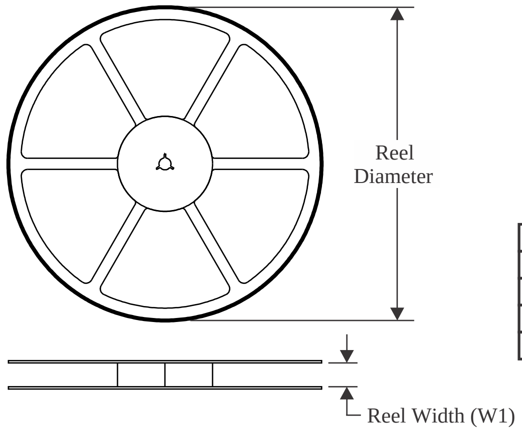
- Automotive : SN74HCT595-Q1

NOTE: Qualified Version Definitions:

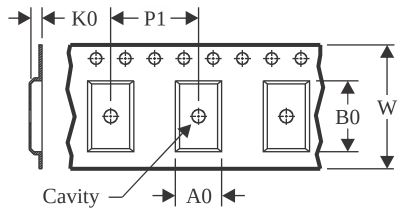
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

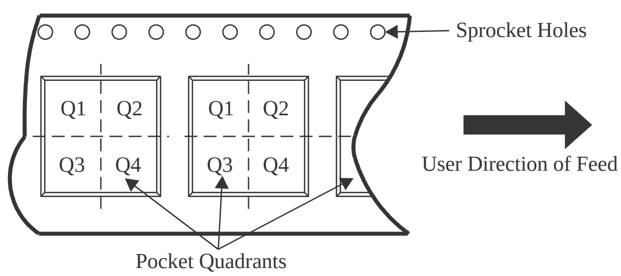


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

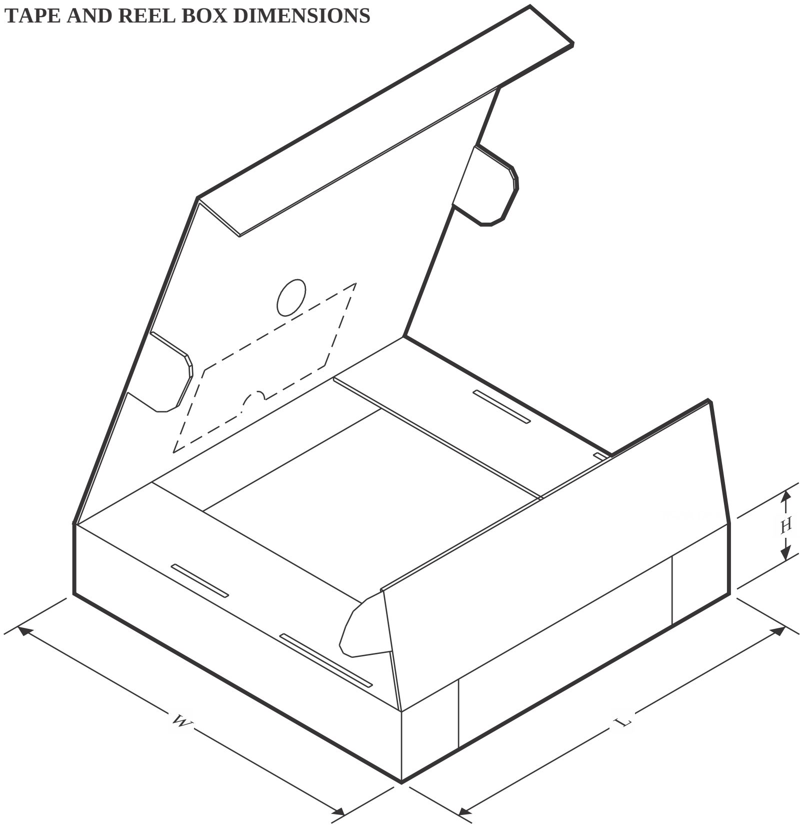
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

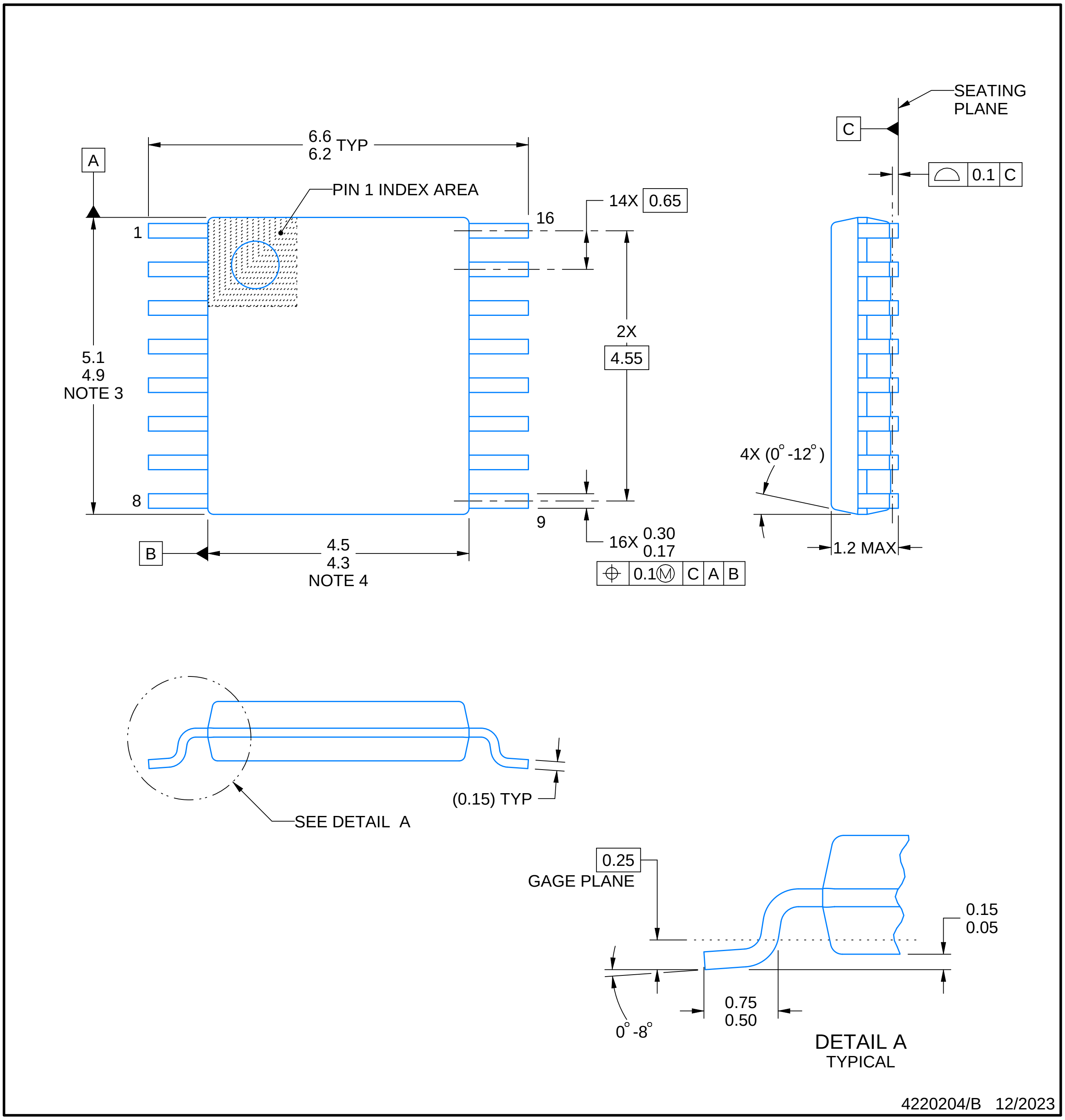
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT595PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



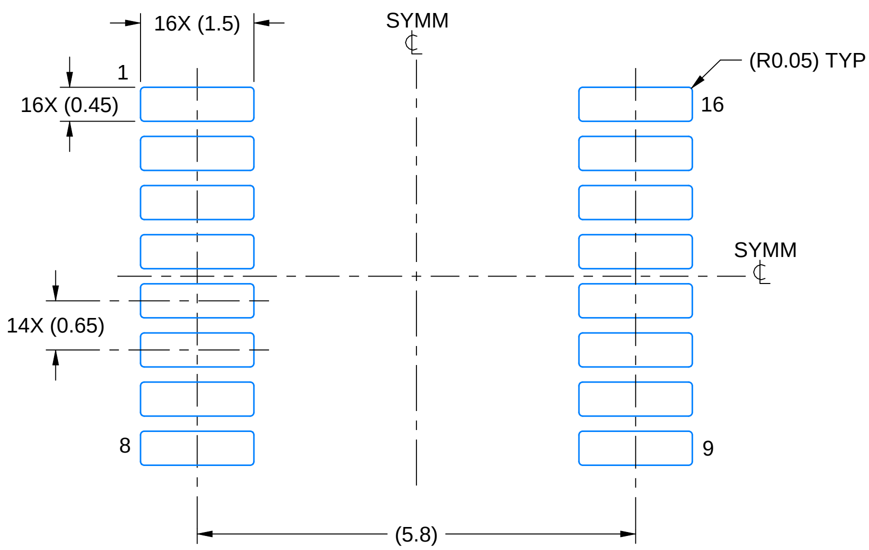
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT595PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

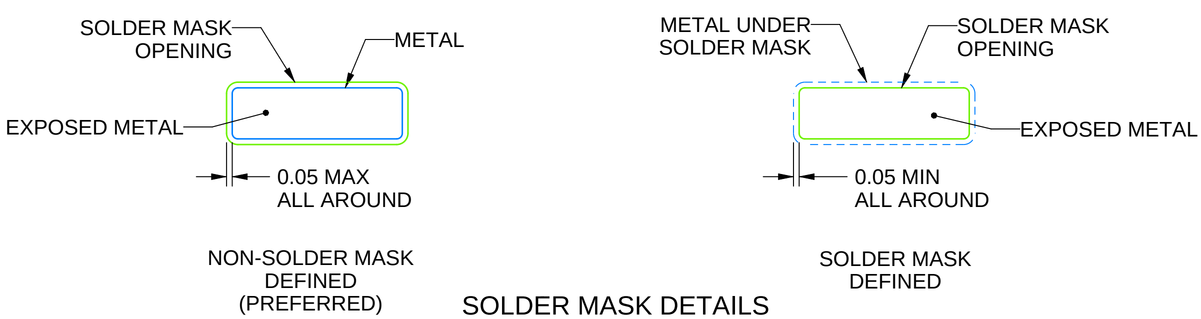


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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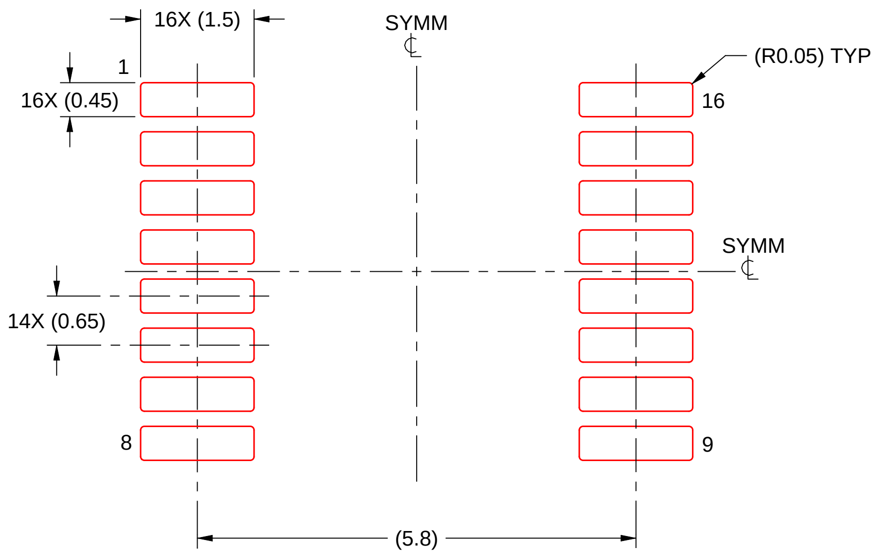
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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