

SN74LV06A オープン・ドレイン出力、ヘキサ・インバータ・バッファ/ドライバ

1 特長

- 2V~5.5V の V_{CC} で動作
- 最大 t_{pd} 6.5ns (5V 時)
- 標準 V_{OLP} (出力グランド・バウンス) $< 0.8V$ ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- 標準 V_{OHV} (出力 V_{OH} アンダーシュート) $> 2.3V$ ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- 入力を V_{CC} に接続すると、電源オン時に出力がディセーブルされます
- すべてのポートで混在モード電圧動作をサポート
- I_{off} により活線挿抜、部分的パワーダウン・モード、バック・ドライブ保護をサポート
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- サーバー
- テレコム・インフラストラクチャ
- TV セットトップ・ボックス
- UPS
- プリンタ
- エレベータ / エスカレータ
- EPOS (POS システム)、ECR、レジ
- 自動販売 / 支払い / 現金支払機

3 説明

これらのヘキサ・インバータ・バッファ/ドライバは、2V~5.5V V_{CC} 動作向けに設計されています。

SN74LV06A デバイスはブール関数 $Y = \bar{A}$ を正論理で実行します。

オープン・ドレイン出力が正常に動作するにはプルアップ抵抗が必要であり、他のオープン・ドレイン出力に接続してアクティブ Low のワイヤード OR 関数またはアクティブ High のワイヤード AND 関数を実装できます。

パッケージ情報

部品番号 ⁽¹⁾	パッケージ	本体サイズ (公称)
SN74LV06A	DGV (TVSOP, 14)	3.60mm × 4.40mm
	D (SOIC, 14)	8.65mm × 3.90mm
	NS (SO, 14)	10.20mm × 5.30mm
	DB (SSOP, 14)	6.20mm × 5.30mm
	PW (TSSOP, 14)	5.00mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略回路図



Table of Contents

1 特長	1	8.1 Overview.....	8
2 アプリケーション	1	8.2 Functional Block Diagram.....	8
3 説明	1	8.3 Feature Description.....	9
4 Revision History	2	8.4 Device Functional Modes.....	9
5 Pin Configurations and Functions	3	9 Application and Implementation	10
6 Specifications	4	9.1 Application Information.....	10
6.1 Absolute Maximum Ratings.....	4	9.2 Typical Application.....	10
6.2 ESD Ratings.....	4	9.3 Power Supply Recommendations.....	11
6.3 Recommended Operating Conditions.....	4	9.4 Layout.....	11
6.4 Thermal Information.....	5	10 Device and Documentation Support	12
6.5 Electrical Characteristics.....	5	10.1 Documentation Support.....	12
6.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	5	10.2 ドキュメントの更新通知を受け取る方法.....	12
6.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	5	10.3 サポート・リソース.....	12
6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6	10.4 Trademarks.....	12
6.9 Noise Characteristics.....	6	10.5 静電気放電に関する注意事項.....	12
6.10 Operating Characteristics.....	6	10.6 用語集.....	12
6.11 Typical Characteristics.....	7	11 Mechanical, Packaging, and Orderable Information	12
7 Parameter Measurement Information	8		
8 Detailed Description	8		

4 Revision History

Changes from Revision J (January 2016) to Revision K (March 2023) Page

- ドキュメントの構造レイアウトと表のフォーマットを更新..... 1

Changes from Revision I (February 2015) to Revision J (January 2016) Page

- Added T_J Junction temperature to the [セクション 6.1](#) table 4
- Changed [図 9-2](#) 11

5 Pin Configurations and Functions

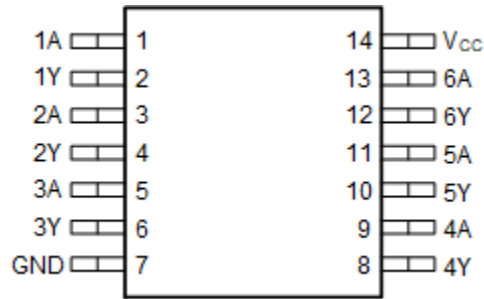


图 5-1. SN74LV06A D, DB, DGV, NS, or PW Package (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	1A	I	Input 1
2	1Y	O	Output 1
3	2A	I	Input 2
4	2Y	O	Output 2
5	3A	I	Input 3
6	3Y	O	Output 3
8	4Y	O	Output 4
9	4A	I	Input 4
10	5Y	O	Output 5
11	5A	I	Input 5
12	6Y	O	Output 6
13	6A	I	Input 6
7	GND	GND	Ground Pin
14	V _{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, GND = Ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	7	V
V _I	Input voltage range ⁽²⁾	–0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	7	V
I _{IK}	Input clamp current	V _I < 0	–20	mA
I _{OK}	Output clamp current	V _O < 0	–50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	–35	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature range	–65	150	°C
T _J	Junction Temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Machine Model (MM), per JEDEC specification	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74LV06A		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	5.5	V
I _{OL}	Low level output current	V _{CC} = 2 V	20	mA
		V _{CC} = 2.3 V to 2.7 V	2	
		V _{CC} = 3 V to 3.6 V	8	
		V _{CC} = 4.5 V to 5.5 V	16	
Δt/Δv	Input transition rise and fall rate	V _{CC} = 2.3 V to 2.7 V	200	ns/V
		V _{CC} = 3 V to 3.6 V	100	
		V _{CC} = 4.5 V to 5.5 V	20	

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74LV06A		UNIT
		MIN	MAX	
T _A	Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV06A					UNIT
		D	DB	DGV	NS	PW	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	100.6	112.5	135.2	95.4	128.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.8	65.0	57.9	52.9	57.2	
R _{θJB}	Junction-to-board thermal resistance	54.9	59.9	68.3	51.2	70.7	
ψ _{JT}	Junction-to-top characterization parameter	25.0	25.0	9.2	17.9	9.3	
ψ _{JB}	Junction-to-board characterization parameter	54.7	59.3	67.6	53.8	70.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LV06A			-40°C to 85°C SN74LV06A			-40°C to 125°C SN74LV06A		UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V			0.1			0.1		0.1	V
	I _{OL} = 2 mA	2.3 V			0.4			0.4		0.4	
	I _{OL} = 8 mA	3 V			0.44			0.44		0.44	
	I _{OL} = 16 mA	4.5 V			0.55			0.55		0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1			±1		±1	μA
I _{OH}	V _I = V _{IL} , V _{OH} = V _{CC}	5.5 V			±2.5			±2.5		±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20			20		20	μA
I _{off}	V _I or V _O = 0 to 5.5 V	0			5			5		5	μA
C _i	V _I = V _{CC} or GND	3.3 V		1.6			1.6			1.6	pF

6.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			-40°C to 85°C SN74LV06A		-40°C to 125°C SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF		5.4 ⁽¹⁾	10.4 ⁽¹⁾	1 ⁽¹⁾	13 ⁽¹⁾	1	14	ns
t _{PHL}					7.2 ⁽¹⁾	10.4 ⁽¹⁾	1 ⁽¹⁾	13 ⁽¹⁾	1	14	
t _{PLH}	A	Y	C _L = 50 pF		9.7	15.2	1	18	1	19	ns
t _{PHL}					9.3	15.2	1	18	1	19	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			-40°C to 85°C SN74LV06A		-40°C to 125°C SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF		4.1 ⁽¹⁾	7.1 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	9.5	ns
t _{PHL}					4.9 ⁽¹⁾	7.1 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	9.5	

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 85°C SN74LV06A		–40°C to 125°C SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 50 pF	7.1	10.6	1	12	1	13	ns	
t _{PHL}	A	Y		6.4	10.6	1	12	1	13		

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 85°C SN74LV06A		–40°C to 125°C SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF	3 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	7	ns	
t _{PHL}	A	Y		3.3 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	7		
t _{PLH}	A	Y	C _L = 50 pF	4.8	7.5	1	8.5	1	9	ns	
t _{PHL}	A	Y		4.4	7.5	1	8.5	1	9		

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER ⁽¹⁾		MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.5	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		–0.1	–0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		3.3		V
V _{IH(D)}	High-level dynamic input voltage	2.31			V
V _{IL(D)}	Low-level dynamic input voltage			0.99	V

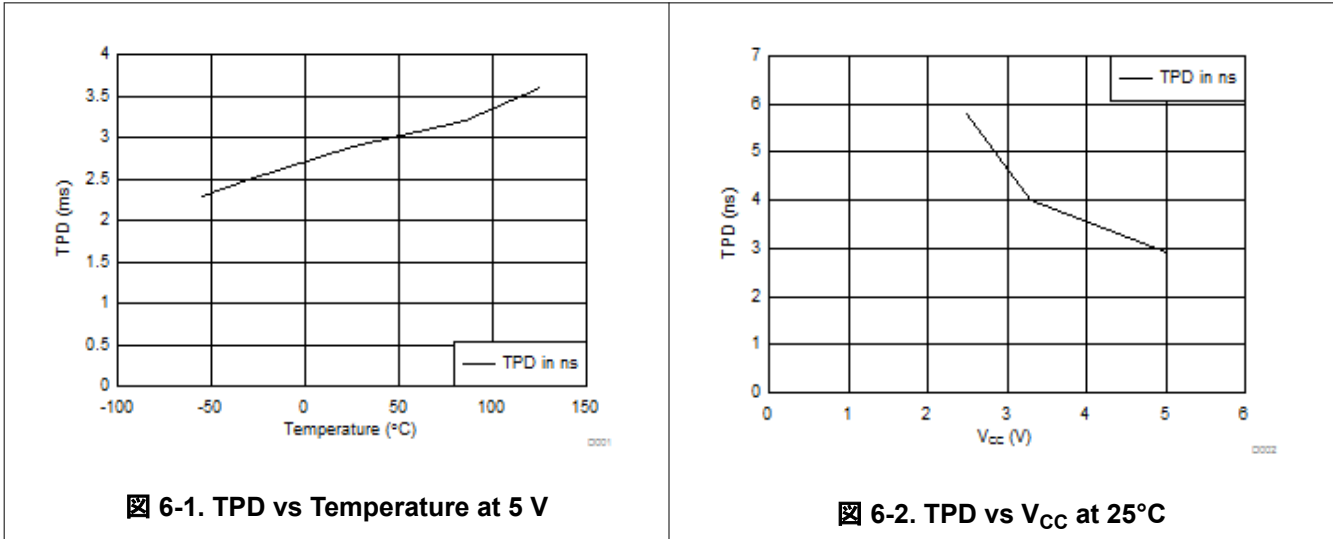
(1) Characteristics are for surface-mount packages only.

6.10 Operating Characteristics

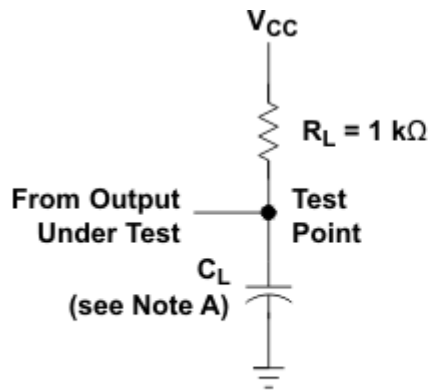
T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT	
C _{pd}	Power dissipation capacitance	C _L = 50 pF f = 10 MHz	3.3 V	2.6	pF
			5 V	4.7	

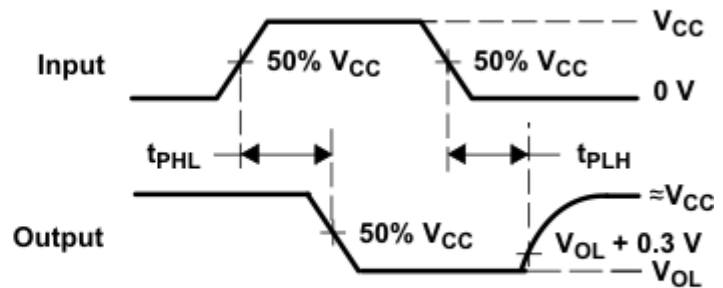
6.11 Typical Characteristics



7 Parameter Measurement Information



**LOAD CIRCUIT FOR
OPEN-DRAIN OUTPUTS**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

- C_L includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- The outputs are measured one at a time, with one input transition per measurement.

FIG 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

These hex inverter buffers/drivers are designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV06A device performs the Boolean function $Y = \bar{A}$ in positive logic.

The open-drain output require pull-up resistors to perform correctly and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current back-flow through the devices when they are powered down.

8.2 Functional Block Diagram



FIG 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows up or down voltage translation
 - Inputs and outputs accept voltages to 5.5 V
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V

8.4 Device Functional Modes

**表 8-1. Function Table
(Each Inverter)**

INPUT ⁽¹⁾ A	OUTPUT ⁽²⁾ Y
H	L
L	H

- (1) H = High Voltage Level, L = Low Voltage Level
(2) H = Driving High, L = Driving Low

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SN74LV06A is a low drive Open drain CMOS device that can be used for a multitude of buffer type functions. The inputs are 5.5 V tolerant and the outputs open drain and 5.5 V tolerant allowing it to translate up to 5.5 V or down to any other voltage between GND and 5.5 V.

9.2 Typical Application

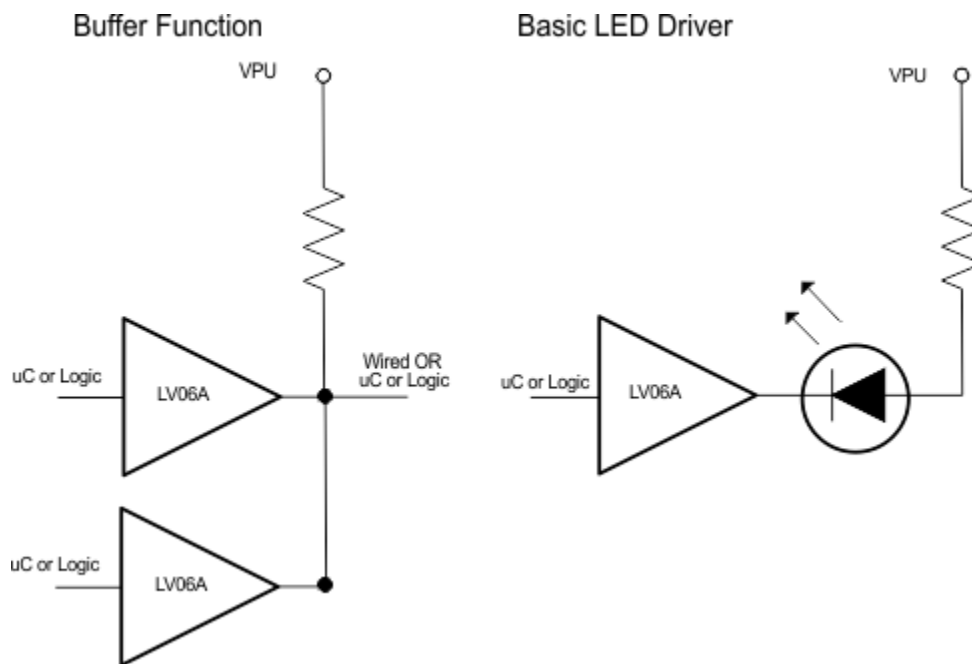


図 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and is open drain so it has low output drive only. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The parallel output drive can create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended Input Conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [セクション 6.3](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [セクション 6.3](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommended Output Conditions:
 - Load currents should not exceed 35 mA per output and 50 mA total for the part.

9.2.3 Application Curves

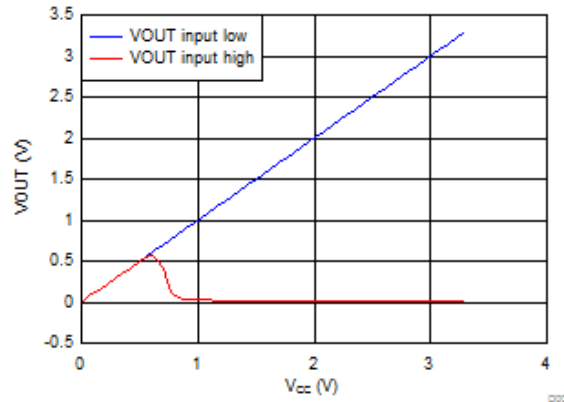


図 9-2. Output During Power Up with 4 k Pull-up at 3.3 V

9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [セクション 6.3](#). Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF capacitor is recommended for each power terminal. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver.

9.4.2 Layout Example

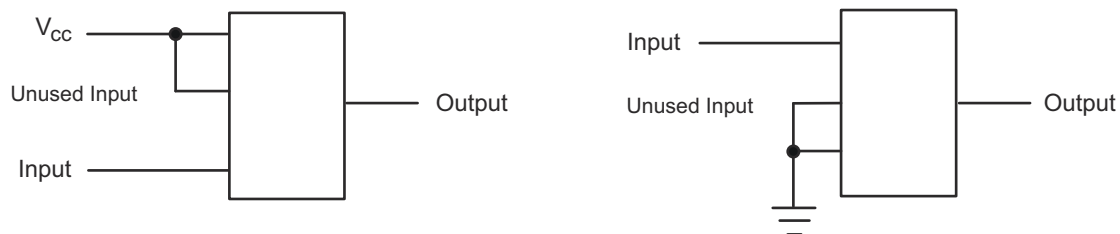


図 9-3. Layout Diagram

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV06A	Click here	Click here	Click here	Click here	Click here

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV06AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LV06A	
SN74LV06ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06ANSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV06A	Samples
SN74LV06APW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	LV06A	
SN74LV06APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06APWT	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	LV06A	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

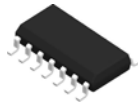

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV06ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV06ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV06ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV06ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV06ADRE4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV06ADRE4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV06ANSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74LV06ANSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV06APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV06APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV06ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV06ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV06ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV06ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV06ADRE4	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV06ADRE4	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV06ANSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74LV06ANSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74LV06APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV06APWR	TSSOP	PW	14	2000	356.0	356.0	35.0

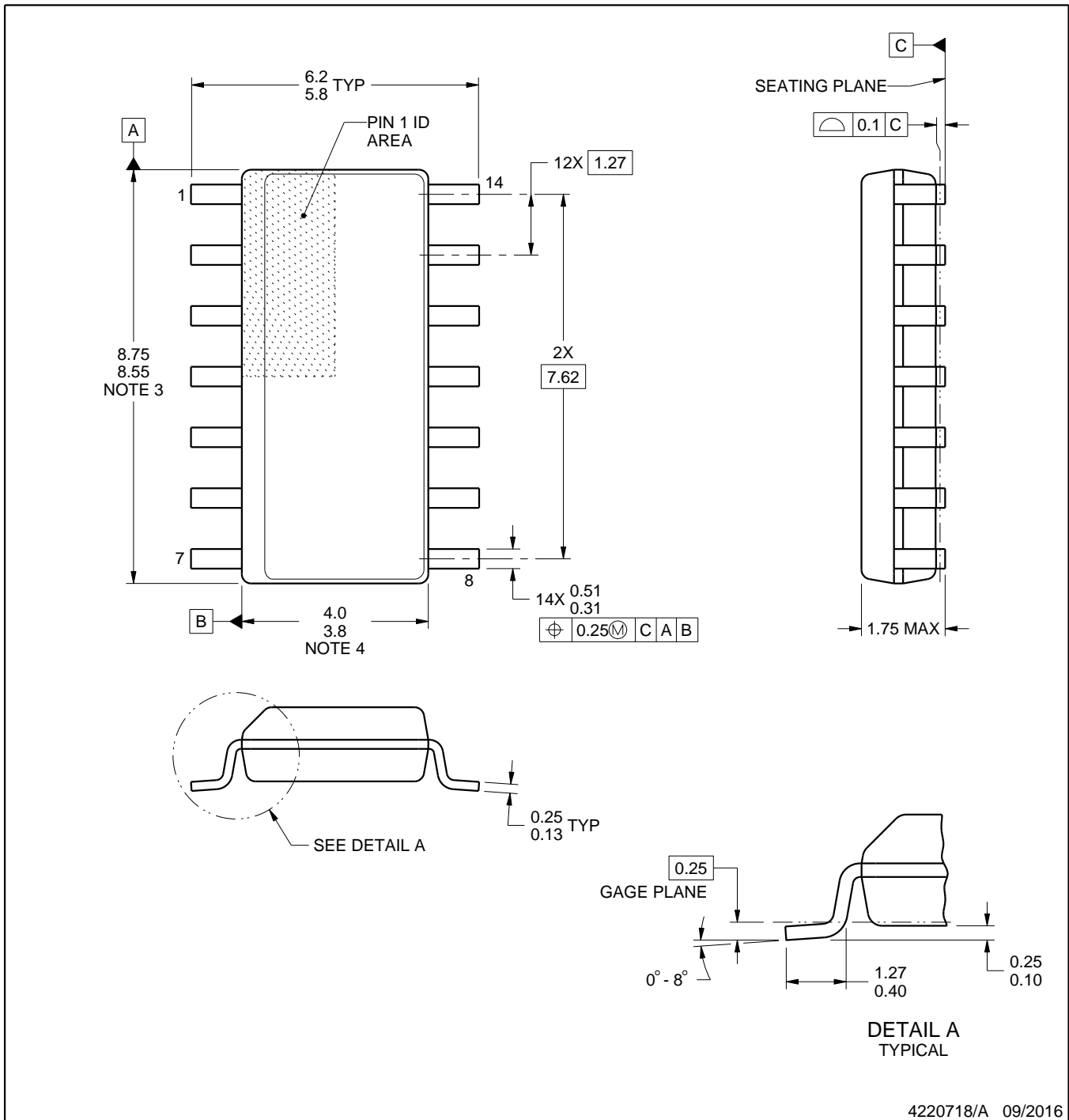


D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

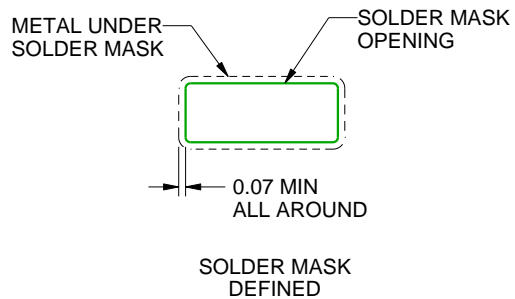
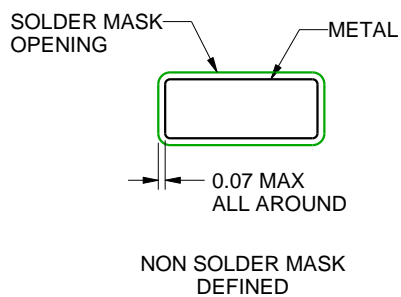
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

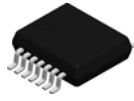
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

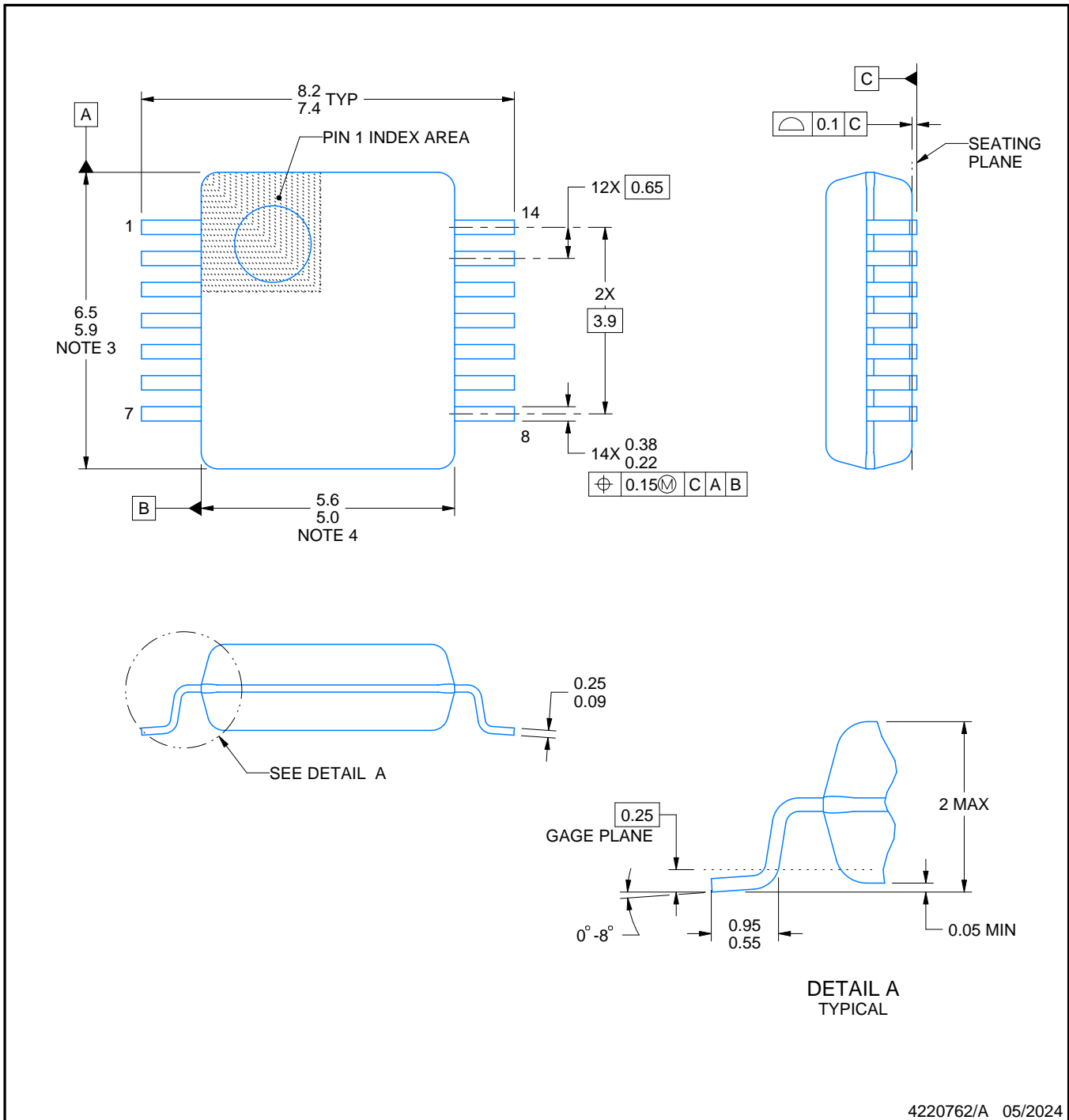
DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

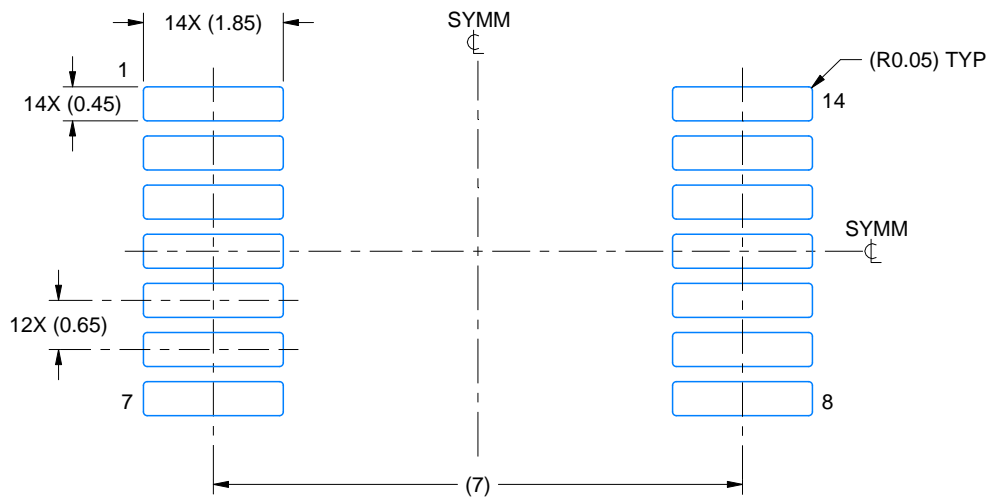
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

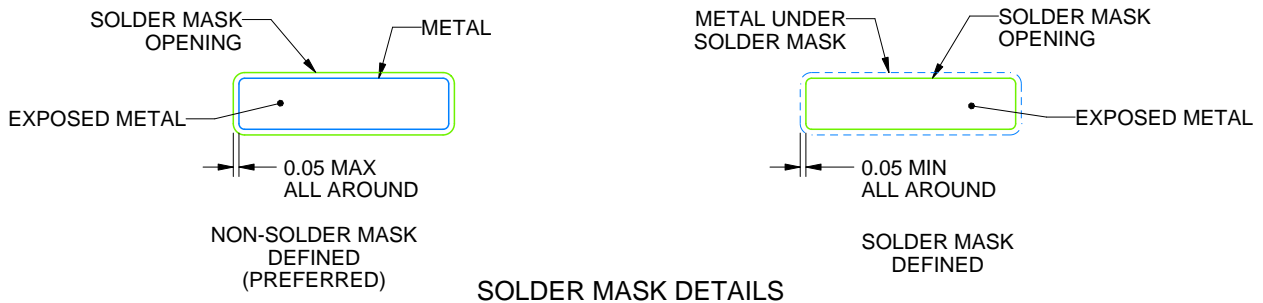
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

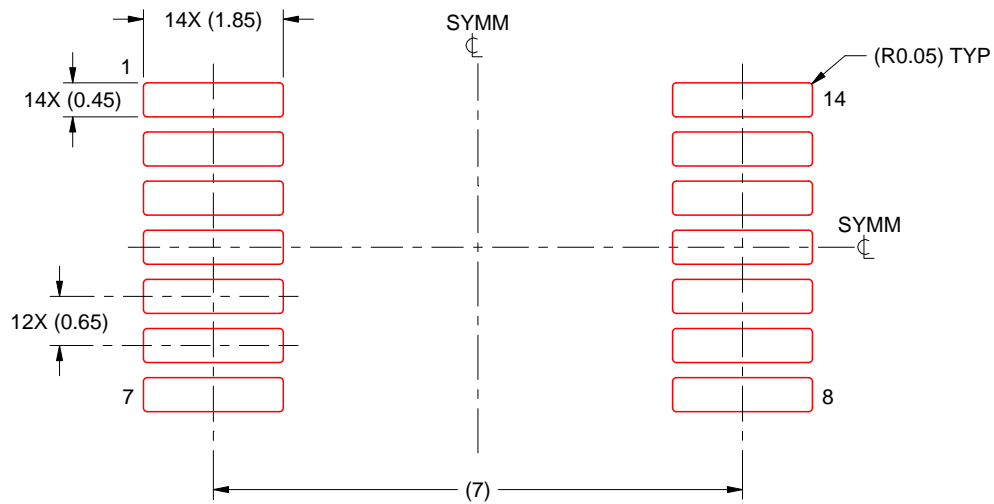
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

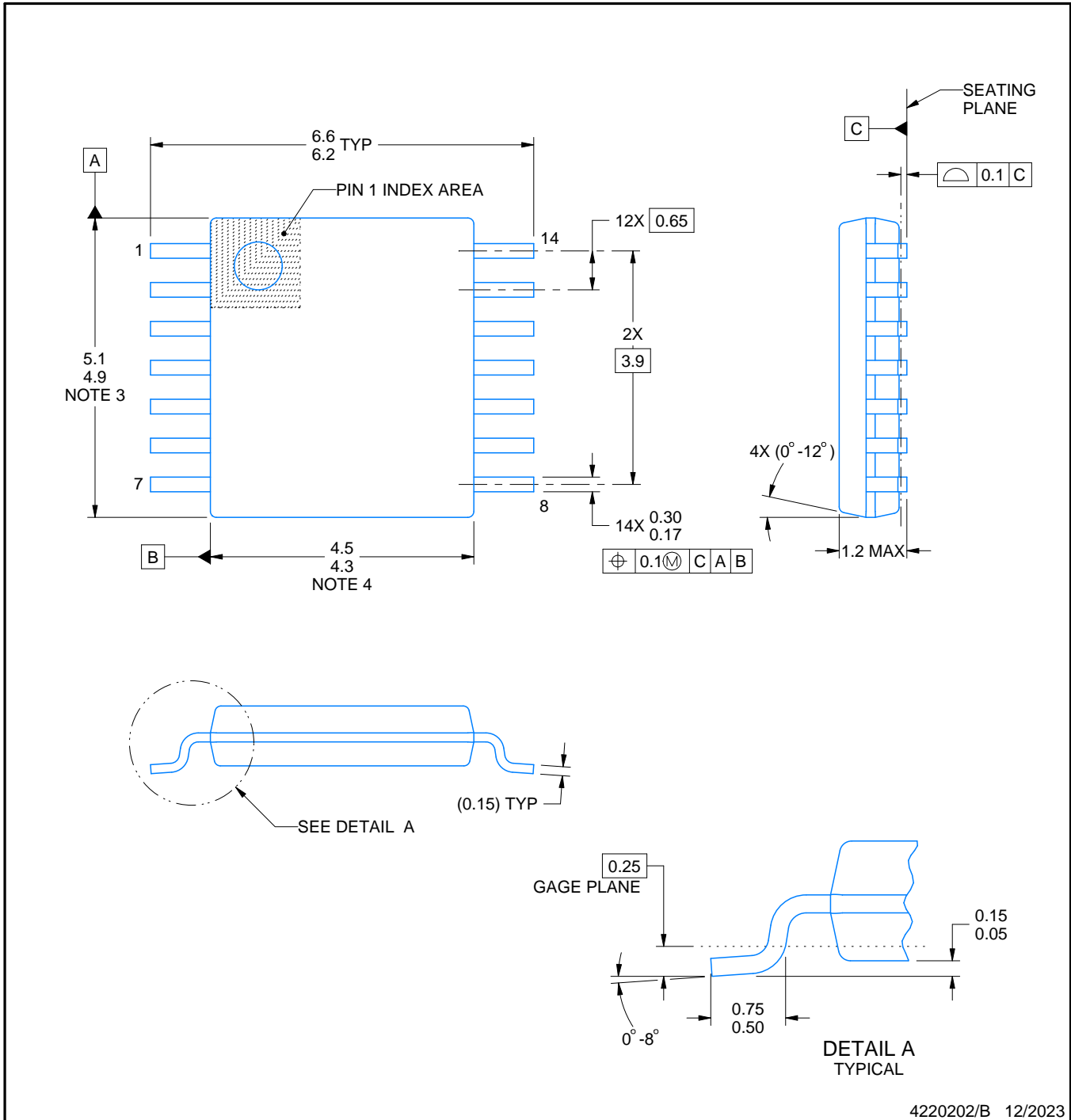


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

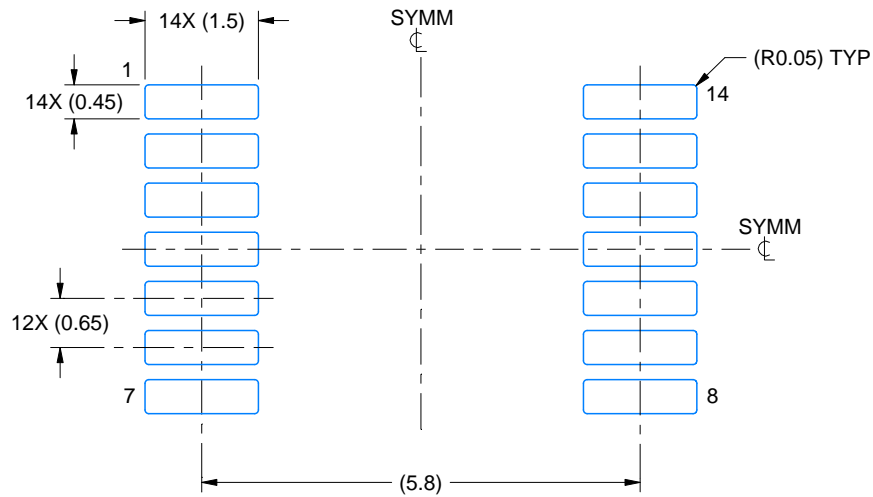
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

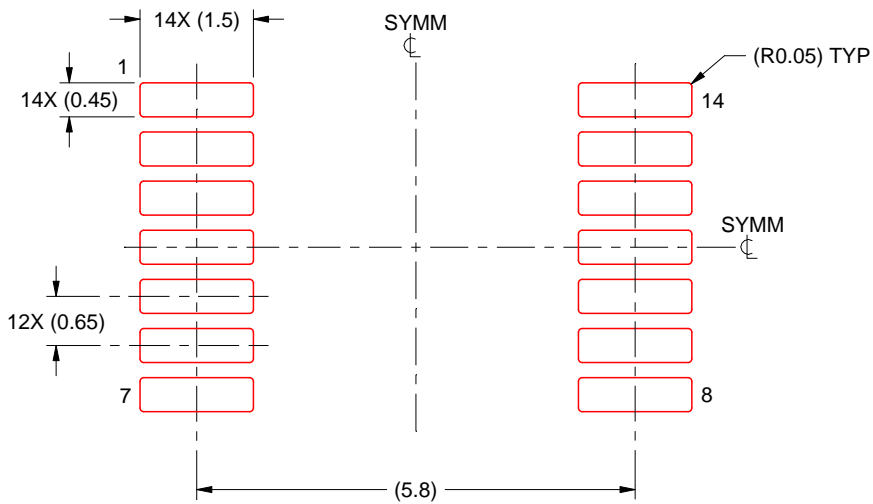
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated