



SN74LV165A パラレル・ロード(並列読み込み)、8ビット・シフト・レジスタ

1 特長

- 2V～5.5V の V_{CC} で動作
- 最大 t_{pd} 10.5ns (5V 時)
- すべてのポートで混在モード電圧動作をサポート
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- JESD 17 準拠で 250mA 超のラッチャップ性能

2 アプリケーション

マイクロコントローラの入力数拡張

3 説明

SN74LV165A デバイスは、2V～5.5V の V_{CC} で動作するように設計された、パラレル・ロード（並列読み込み）8 ビット・シフト・レジスタです。

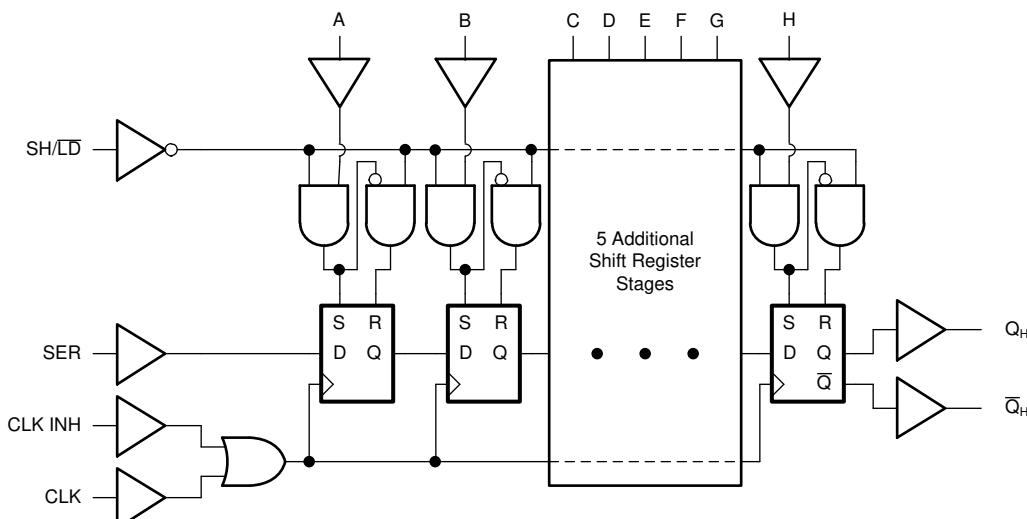
デバイスにクロックが供給されると、データはシリアル出力 Q_H にシフトされます。各段のパラレル入力へのアクセスは、8 つの個別の直接データ入力によって提供されます。これらのデータ入力は、シフト / ロード (SH/LD) 入力が Low レベルのときイネーブルになります。LV165A デバイスは、クロック禁止機能と、反転したシリアル出力 \overline{Q}_H を備えています。

このデバイスは、 I_{off} を使った部分的パワーダウン・アプリケーション用の動作が完全に規定されています。 I_{off} 回路が output をディスエーブルにするので、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

パッケージ情報⁽¹⁾

| 部品番号 | パッケージ | 本体サイズ(公称) |
|------------|----------------|------------------|
| SN74LV165A | D (SOIC、16) | 9.90mm × 3.90mm |
| | DB (SSOP、16) | 6.20mm × 5.30mm |
| | NS (SO、16) | 10.20mm × 5.30mm |
| | PW (TSSOP、16) | 5.00mm × 4.40mm |
| | DGV (TVSOP、16) | 3.60mm × 4.40mm |
| | RGY (VQFN、16) | 4.00mm × 3.50mm |
| | BQB (WQFN、16) | 3.60mm × 2.60mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)



英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table of Contents

| | | | |
|--|---|--|----|
| 1 特長 | 1 | 7 Parameter Measurement Information | 10 |
| 2 アプリケーション | 1 | 8 Detailed Description | 11 |
| 3 説明 | 1 | 8.1 Overview | 11 |
| 4 Revision History | 2 | 8.2 Functional Block Diagram | 11 |
| 5 Pin Configuration and Functions | 3 | 8.3 Feature Description | 11 |
| 6 Specifications | 4 | 8.4 Device Functional Modes | 13 |
| 6.1 Absolute Maximum Ratings | 4 | 9 Application and Implementation | 14 |
| 6.2 ESD Ratings | 4 | 9.1 Application Information | 14 |
| 6.3 Recommended Operating Conditions | 5 | 9.2 Typical Application | 14 |
| 6.4 Thermal Information | 5 | 9.3 Power Supply Recommendations | 16 |
| 6.5 Electrical Characteristics | 6 | 9.4 Layout | 16 |
| 6.6 Timing Requirements, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | 6 | 10 Device and Documentation Support | 17 |
| 6.7 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 6 | 10.1 Documentation Support | 17 |
| 6.8 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | 7 | 10.2 Receiving Notification of Documentation Updates | 17 |
| 6.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | 7 | 10.3 サポート・リソース | 17 |
| 6.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 7 | 10.4 Trademarks | 17 |
| 6.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | 8 | 10.5 静電気放電に関する注意事項 | 17 |
| 6.12 Timing Diagrams | 8 | 10.6 用語集 | 17 |
| 6.13 Operating Characteristics | 9 | 11 Mechanical, Packaging, and Orderable | |
| 6.14 Typical Characteristics | 9 | Information | 17 |

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision Q (December 2022) to Revision R (March 2023) | Page |
|--|------|
| • ドキュメントの構造レイアウトとフォーマットされた表を現在の標準に更新 | 1 |
| <hr/> | |
| Changes from Revision P (June 2022) to Revision Q (December 2022) | Page |
| • データシートのステータスを「事前情報」から「量産データ」に変更 | 1 |
| <hr/> | |
| Changes from Revision O (November 2016) to Revision P (June 2022) | Page |
| • 「製品情報」、「ピン構成」、「熱に関する情報」の表に BQB (WQFN) パッケージの情報を追加 | 1 |
| • 文書全体にわたって表、図、相互参照の採番方法を更新 | 1 |
| • Updated specifications table formatting | 6 |
| <hr/> | |
| Changes from Revision N (July 2013) to Revision O (November 2016) | Page |
| • 「アプリケーション」セクション、「デバイス情報」表、「目次」、「ピン構成および機能」セクション、「仕様」セクション、「ESD 定格」表、「熱に関する情報」表、「代表的特性」セクション、「詳細説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加 | 1 |
| <hr/> | |

5 Pin Configuration and Functions

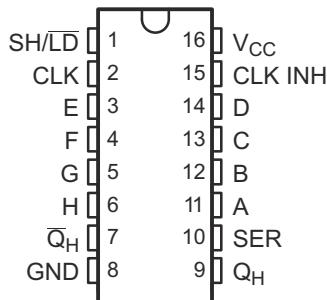


図 5-1. D, DB, DGV, N or PW Package,
16-Pin SOIC, SSOP, TSSOP, SOP or TSSOP
(Top View)

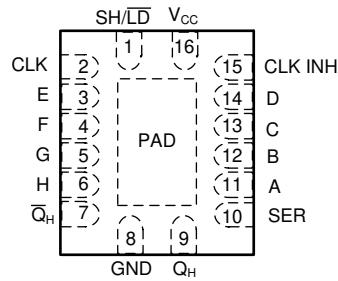


図 5-2. RGY or BQB Package,
16-Pin VQFN or WQFN
(Top View)

表 5-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-----------------|-----|---------------------|----------------------------|
| NAME | NO. | | |
| A | 11 | I | Serial input A |
| B | 12 | I | Serial input B |
| C | 13 | I | Serial input C |
| CLK | 2 | I | Storage clock |
| CLK INH | 15 | I | Storage clock |
| D | 14 | I | Serial input D |
| E | 3 | I | Serial input E |
| F | 4 | I | Serial input F |
| G | 5 | I | Serial input G |
| GND | 8 | G | Ground pin |
| H | 6 | I | Serial input H |
| Q _H | 7 | O | Output H, inverted |
| Q _H | 9 | O | Output H |
| SH/ LD | 1 | I | Load Input |
| SER | 10 | I | Serial input |
| V _{CC} | 16 | P | Power pin |
| PAD | | — | Thermal Pad ⁽²⁾ |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) RGY and BQB Package Only

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------|---|-----------------------|------|----------------|------|
| V_{CC} | Supply voltage | | -0.5 | 7 | V |
| V_I | Input voltage ⁽²⁾ | | -0.5 | 7 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | | -0.5 | 7 | V |
| V_O | Output voltage ^{(2) (3)} | | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | | -20 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | | -50 | mA |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | | ± 25 | mA |
| | Continuous current through V_{CC} or GND | | | ± 50 | mA |
| T_{jmax} | Maximum virtual junction temperature | | | 150 | °C |
| T_{stg} | Storage temperature | | -65 | 150 | °C |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|---|------------|------|
| $V_{(ESD)}$ | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ± 2000 | V |
| | Machine Model (MM), per JEDEC specification | ± 200 | |
| | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ± 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|---------------------|------------------------------------|---|---------------------|----------|---------------|
| V_{CC} | Supply voltage | | 2 | 5.5 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | 1.5 | | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.7$ | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.7$ | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.7$ | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2\text{ V}$ | 0.5 | | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.3$ | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.3$ | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.3$ | | |
| V_I | Input voltage | | 0 | 5.5 | V |
| V_O | Output voltage | | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 2\text{ V}$ | -50 | | μA |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | -2 | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | -6 | | mA |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | -12 | | |
| I_{OL} | Low-level output current | $V_{CC} = 2\text{ V}$ | 50 | | μA |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 2 | | mA |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | 6 | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 12 | | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 200 | | ns/V |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | 100 | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 20 | | |
| T_A | Operating free-air temperature | | -40 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#)

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74LV165A | | | | | | | UNIT |
|-------------------------------|--|-------------|--------------|------------|---------------|----------------|---------------|---------------|------|
| | | D (SOIC) | DB (SSOP) | NS (SO) | PW (TSSOP) | DGV (TWSOP) | RGY (VQFN) | BQB (WQFN) | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 86.2 | 102.8 | 89.4 | 113.3 | 125.9 | 48.8 | 85.9 | °C/W |
| $R_{\theta JC(\text{top})}$ | Junction-to-case (top) thermal resistance | 46.1 | 53.3 | 47.9 | 48.3 | 51 | 46.7 | 82.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 43.8 | 53.5 | 49.8 | 58.4 | 57.7 | 24.9 | 55.6 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 13.2 | 16.6 | 16.6 | 6.4 | 5.7 | 2 | 9.4 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 43.5 | 52.9 | 49.5 | 57.8 | 57.2 | 24.9 | 55.6 | °C/W |
| $R_{\theta JC(\text{bot})}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | 11.7 | 33.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#)

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | V _{CC} | -40°C to 85°C | | | -40°C to 125°C | | | UNIT | |
|------------------|----------------------------|---|-----------------|-----------------------|-----|-----|-----------------------|-----|-----|------|--|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| V _{OH} | High-level output voltage | I _{OH} = -50 mA | 2 V to 5.5 V | V _{CC} – 0.1 | | | V _{CC} – 0.1 | | | V | |
| | | I _{OH} = -2 mA | 2.3 V | 2 | | | 2 | | | | |
| | | I _{OH} = -6 mA | 3 V | 2.48 | | | 2.48 | | | | |
| | | I _{OH} = -12 mA | 4.5 V | 3.8 | | | 3.8 | | | | |
| V _{OL} | Low-level output voltage | I _{OL} = 50 mA | 2 V to 5.5 V | 0.1 | | | 0.1 | | | V | |
| | | I _{OL} = 2 mA | 2.3 V | 0.4 | | | 0.4 | | | | |
| | | I _{OL} = 6 mA | 3 V | 0.44 | | | 0.44 | | | | |
| | | I _{OL} = 12 mA | 4.5 V | 0.55 | | | 0.55 | | | | |
| I _I | Input leakage current | V _I = 5.5 V or GND | 0 V to 5.5 V | ±1 | | | ±1 | | | µA | |
| I _{CC} | Static supply current | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | 20 | | | 20 | | | µA | |
| I _{off} | Partial power down current | V _I or V _O = 0 to 5.5 V | 0 | 5 | | | 5 | | | µA | |
| C _i | Input capacitance | V _I = V _{CC} or GND | 3.3 V | 1.7 | | | 1.7 | | | pF | |

6.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [图 7-1](#))

| PARAMETER | TEST CONDITION | 25°C | | -40°C to 85°C | | -40°C to 125°C | | UNIT | |
|-----------------|----------------|--|------|---------------|-----|----------------|-----|------|--|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| t _w | Pulse duration | CLK high or low | 8.5 | 9 | | 9 | | ns | |
| | | SH/ \overline{LD} low | 11 | 13 | | 13 | | | |
| t _{su} | Setup time | SH/ \overline{LD} high before CLK \uparrow | 7 | 8.5 | | 8.5 | | ns | |
| | | SER before CLK \uparrow | 8.5 | 9.5 | | 9.5 | | | |
| | | CLK INH before CLK \uparrow | 7 | 7 | | 7 | | | |
| | | Data before SH/ \overline{LD} \uparrow | 11.5 | 12 | | 12 | | | |
| t _h | Hold time | SER data after CLK \uparrow | -1 | 0 | | 0 | | ns | |
| | | Parallel data after SH/ \overline{LD} \uparrow | 0 | 0 | | 0 | | | |
| | | SH/ \overline{LD} high after CLK \uparrow | 0 | 0 | | 0 | | | |

6.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [图 7-1](#))

| PARAMETER | TEST CONDITION | 25°C | | -40°C to 85°C | | -40°C to 125°C | | UNIT | |
|-----------------|----------------|--|-----|---------------|-----|----------------|-----|------|--|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| t _w | Pulse duration | CLK high or low | 6 | 7 | | 7 | | ns | |
| | | SH/ \overline{LD} low | 7.5 | 9 | | 9 | | | |
| t _{su} | Setup time | SH/ \overline{LD} high before CLK \uparrow | 5 | 6 | | 6 | | ns | |
| | | SER before CLK \uparrow | 5 | 6 | | 6 | | | |
| | | CLK INH before CLK \uparrow | 5 | 5 | | 5 | | | |
| | | Data before SH/ \overline{LD} \uparrow | 7.5 | 8.5 | | 8.5 | | | |
| t _h | Hold time | SER data after CLK \uparrow | 0 | 0 | | 0 | | ns | |
| | | Parallel data after SH/ \overline{LD} \uparrow | 0.5 | 0.5 | | 0.5 | | | |
| | | SH/ \overline{LD} high after CLK \uparrow | 0 | 0 | | 0 | | | |

6.8 Timing Requirements, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [图 7-1](#))

| PARAMETER | TEST CONDITION | 25°C | | -40°C to 85°C | | -40°C to 125°C | | UNIT |
|-----------|--|------|-----|---------------|-----|----------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | CLK high or low | 4 | | 4 | | 4 | | ns |
| | SH/ \overline{LD} low | 5 | | 6 | | 6 | | |
| t_{su} | SH/ \overline{LD} high before CLK \uparrow | 4 | | 4 | | 4 | | ns |
| | SER before CLK \uparrow | 4 | | 4 | | 4 | | |
| | CLK INH before CLK \uparrow | 3.5 | | 3.5 | | 3.5 | | |
| | Data before SH/ \overline{LD} \uparrow | 5 | | 5 | | 5 | | |
| t_h | SER data after CLK \uparrow | 0.5 | | 0.5 | | 0.5 | | ns |
| | Parallel data after SH/ \overline{LD} \uparrow | 1 | | 1 | | 1 | | |
| | SH/ \overline{LD} high after CLK \uparrow | 0.5 | | 0.5 | | 0.5 | | |

6.9 Switching Characteristics, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over operating free-air temperature range (unless otherwise noted), (see [图 7-1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAP | 25°C | | | -40°C to 85°C | | | -40°C to 125°C | | | UNIT |
|-----------|---------------------|----------------------------------|-----------------------|------|------|-----|---------------|------|-----|----------------|------|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| f_{max} | | | $C_L = 15 \text{ pF}$ | 50 | 80 | | 45 | | | 45 | | | MHz |
| | | | | 40 | 65 | | 35 | | | 35 | | | |
| t_{pd} | CLK | Q _H or \overline{Q} | $C_L = 15 \text{ pF}$ | 12.2 | 19.8 | | 1 | 22 | | 1 | 22 | | ns |
| | SH/ \overline{LD} | | | 13.1 | 21.5 | | 1 | 23.5 | | 1 | 23.5 | | |
| | H | | | 12.9 | 21.7 | | 1 | 24 | | 1 | 24 | | |
| t_{pd} | CLK | Q _H or \overline{Q} | $C_L = 50 \text{ pF}$ | 15.3 | 23.3 | | 1 | 26 | | 1 | 26 | | ns |
| | SH/ \overline{LD} | | | 16.1 | 25.1 | | 1 | 28 | | 1 | 28 | | |
| | H | | | 15.9 | 25.3 | | 1 | 28 | | 1 | 28 | | |

6.10 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over operating free-air temperature range (unless otherwise noted), (see [图 7-1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAP | 25°C | | | -40°C to 85°C | | | -40°C to 125°C | | | UNIT |
|-----------|---------------------|----------------------------------|-----------------------|------|------|-----|---------------|------|-----|----------------|------|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| f_{max} | | | $C_L = 15 \text{ pF}$ | 65 | 115 | | 55 | | | 55 | | | MHz |
| | | | | 60 | 90 | | 50 | | | 50 | | | |
| t_{pd} | CLK | Q _H or \overline{Q} | $C_L = 15 \text{ pF}$ | 8.6 | 15.4 | | 1 | 18 | | 1 | 18 | | ns |
| | SH/ \overline{LD} | | | 9.1 | 15.8 | | 1 | 18.5 | | 1 | 18.5 | | |
| | H | | | 8.9 | 14.1 | | 1 | 16.5 | | 1 | 16.5 | | |
| t_{pd} | CLK | Q _H or \overline{Q} | $C_L = 50 \text{ pF}$ | 10.9 | 14.9 | | 1 | 16.9 | | 1 | 16.9 | | ns |
| | SH/ \overline{LD} | | | 11.3 | 19.3 | | 1 | 22 | | 1 | 22 | | |
| | H | | | 11.1 | 17.6 | | 1 | 20 | | 1 | 20 | | |

6.11 Switching Characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range (see [图 7-1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAP | 25°C | | | −40°C to 85°C | | | −40°C to 125°C | | | UNIT |
|-----------|---------------------|----------------------------------|-----------------------|------|-----|------|---------------|------|-----|----------------|------|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| f_{max} | | | $C_L = 15 \text{ pF}$ | 110 | 165 | | 90 | | | 90 | | | MHz |
| | | | $C_L = 50 \text{ pF}$ | 95 | 125 | | 85 | | | 85 | | | |
| t_{pd} | CLK | Q _H or \overline{Q} | $C_L = 15 \text{ pF}$ | | 6 | 9.9 | 1 | 11.5 | | 1 | 11.5 | | ns |
| | SH/ \overline{LD} | | | | 6 | 9.9 | 1 | 11.5 | | 1 | 11.5 | | |
| | H | | | | 6 | 9.9 | 1 | 10.5 | | 1 | 10.5 | | |
| t_{pd} | CLK | Q _H or \overline{Q} | $C_L = 50 \text{ pF}$ | | 7.7 | 11.9 | 1 | 13.5 | | 1 | 13.5 | | ns |
| | SH/ \overline{LD} | | | | 7.7 | 11.9 | 1 | 13.5 | | 1 | 13.5 | | |
| | H | | | | 7.6 | 11 | 1 | 12.5 | | 1 | 12.5 | | |

6.12 Timing Diagrams

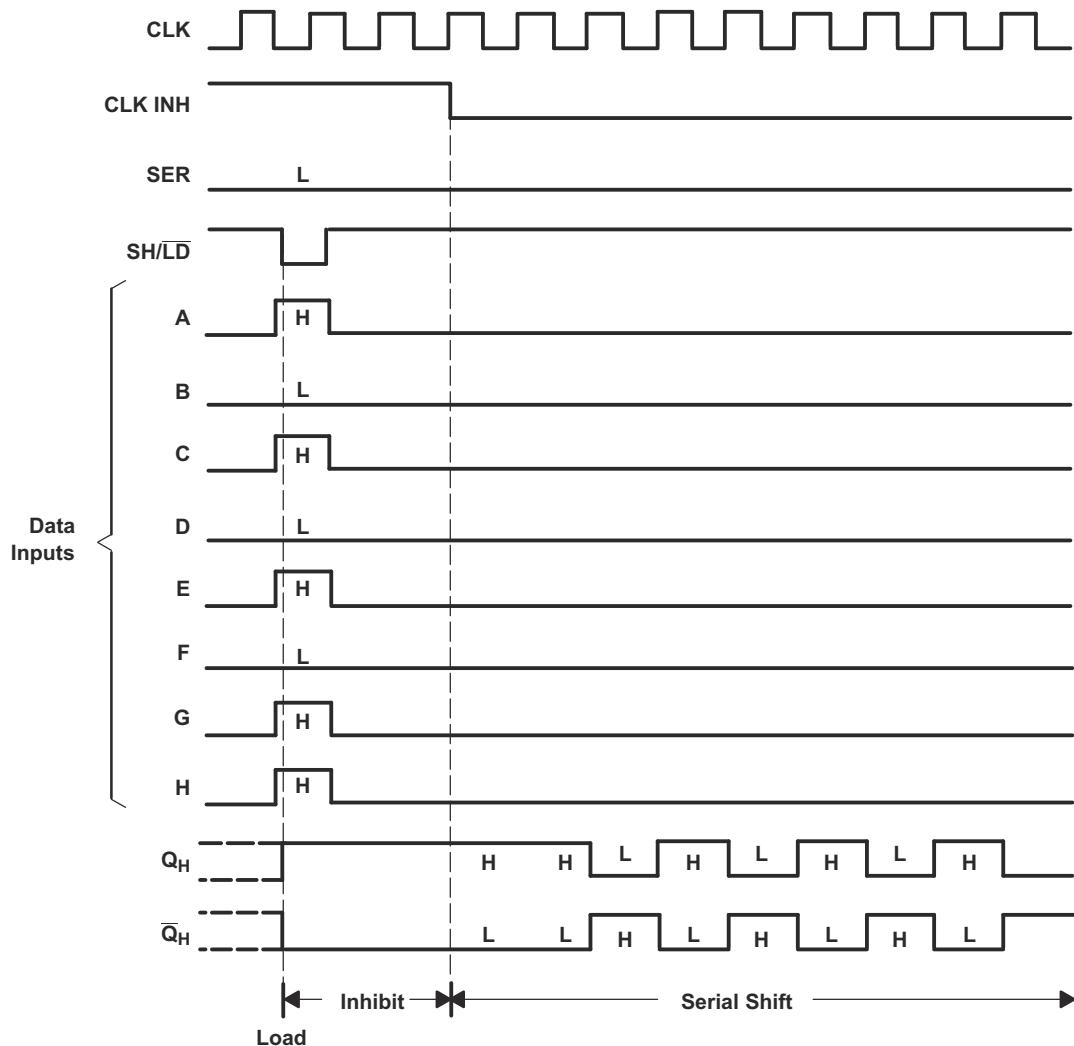


图 6-1. Typical Shift, Load, and Inhibit Sequences

6.13 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | V_{cc} | TYP | UNIT |
|--|--|----------|------|------|
| C_{pd} Power dissipation capacitance | $C_L = 50 \text{ pF}$ $f = 10 \text{ MHz}$ | 3.3 V | 36.1 | pF |
| | | 5 V | 37.5 | |

6.14 Typical Characteristics

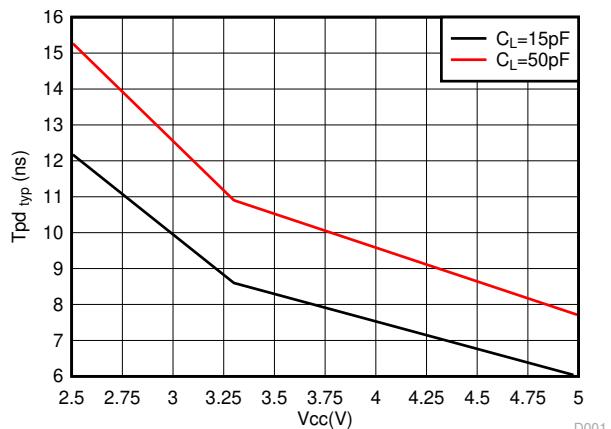
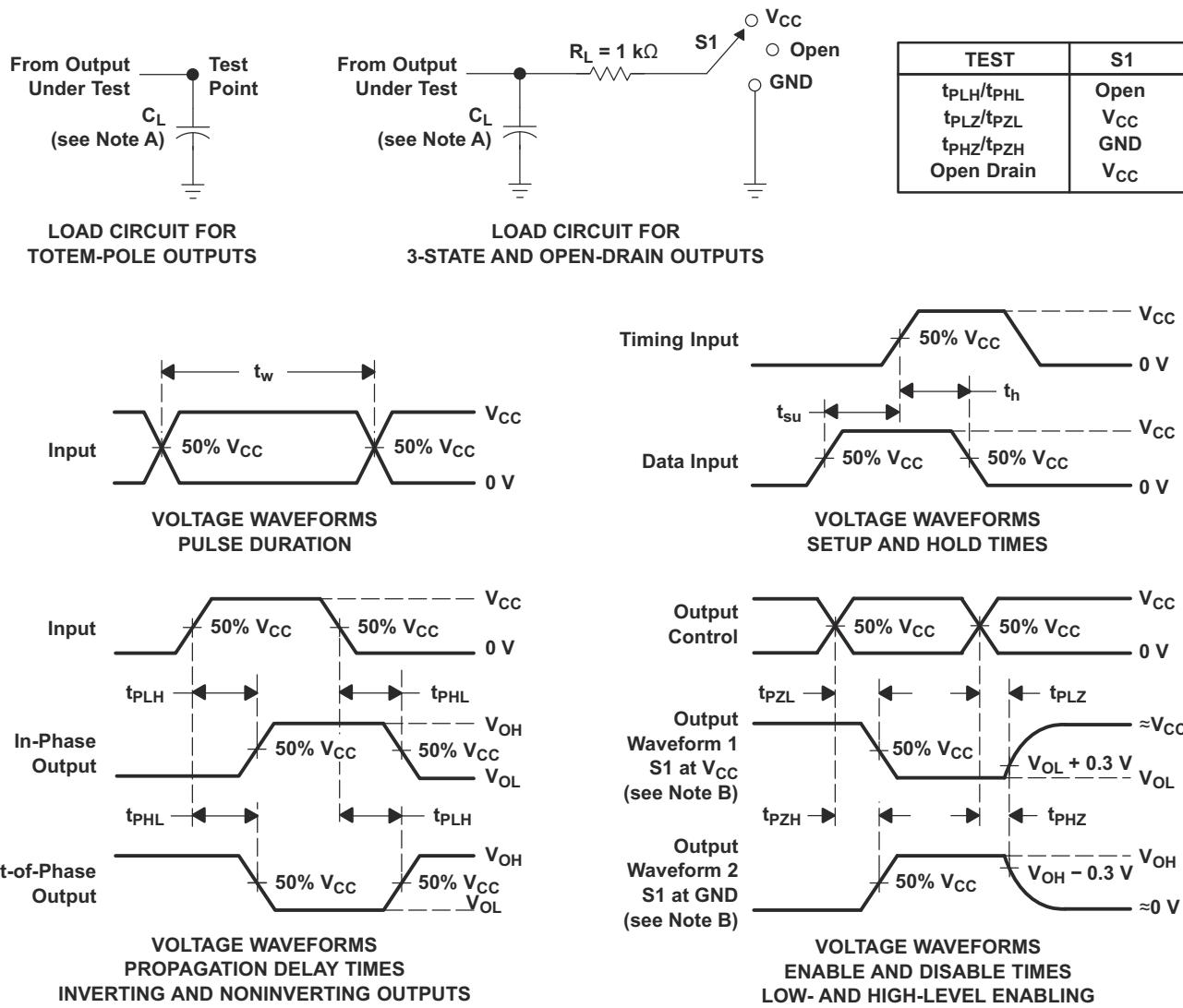


図 6-2. T_{PD} Typical (25°C) vs V_{cc}

7 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

FIG 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

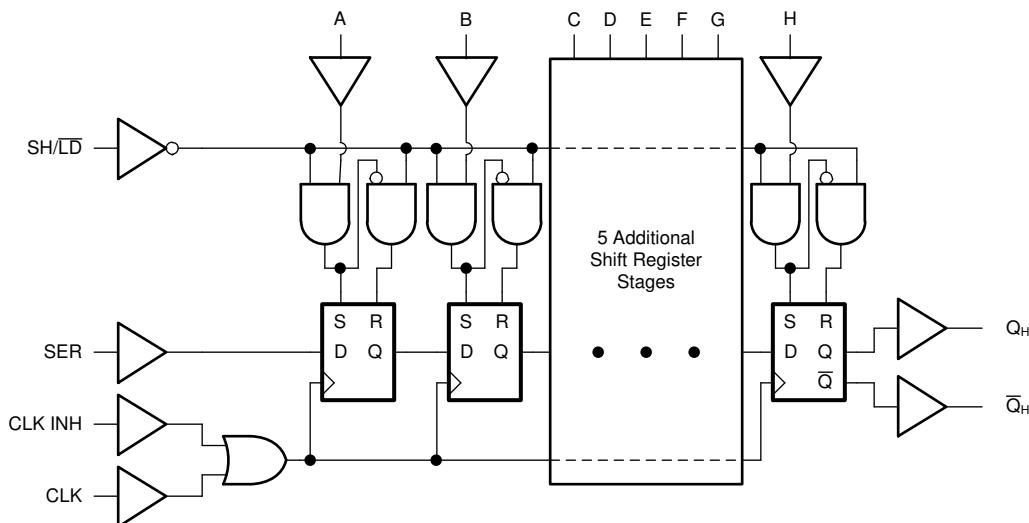
The SN74LV165A device is a parallel-load, 8-bit shift registers designed for 2 V to 5.5 V V_{CC} operation.

When the device is clocked, data is shifted toward the serial output Q_H . Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load (SH/ \overline{LD}) input. The 'LV165A devices feature a clock-inhibit function and a complemented serial output, \overline{Q}_H .

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/ \overline{LD} is held high and clock inhibit (CLK INH) is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH accomplishes clocking, CLK INH must be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/ \overline{LD} is held high. The parallel inputs to the register are enabled while SH/ \overline{LD} is held low, independently of the levels of CLK, CLK INH, or SER.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

8.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

8.3.4 Clamp Diode Structure

図 8-1 shows the inputs and outputs to this device have negative clamping diodes only.

注意

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

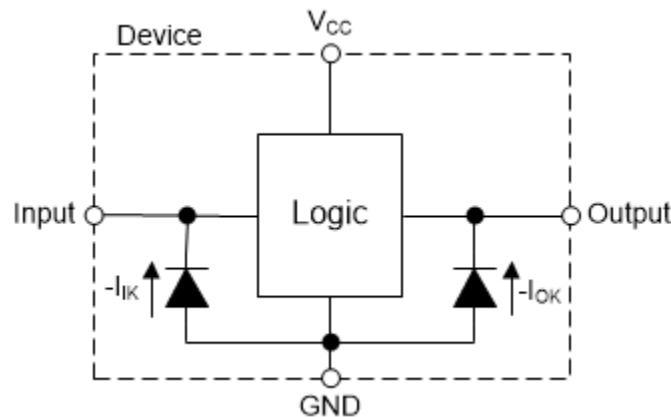


図 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

The [Operating Mode Table](#) and the [Output Function Table](#) list the functional modes of the SN74LV165A.

表 8-1. Operating Mode Table

| INPUTS ⁽¹⁾ | | | FUNCTION |
|-----------------------|-----|---------|----------------------|
| SH/LD | CLK | CLK INH | |
| L | X | X | Parallel load |
| H | H | X | No change |
| H | X | H | No change |
| H | L | ↑ | Shift ⁽²⁾ |
| H | ↑ | L | Shift ⁽²⁾ |

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, ↑ = Low to High transition

(2) Shift : Content of each internal register shifts towards serial output Q_H . Data at SER is shifted into the first register.

表 8-2. Output Function Table

| INTERNAL REGISTERS ^{(1) (2)} | | OUTPUTS ⁽²⁾ | |
|---------------------------------------|---|------------------------|-----------|
| A — G | H | Q | \bar{Q} |
| X | L | L | H |
| X | H | H | L |

(1) Internal registers refer to the shift registers inside the device. These values are set by either loading data from the parallel inputs, or by clocking data in from the serial input.

(2) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The SN74LV165A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low-drive and slow-edge rates minimize overshoot and undershoot on the outputs.

9.2 Typical Application

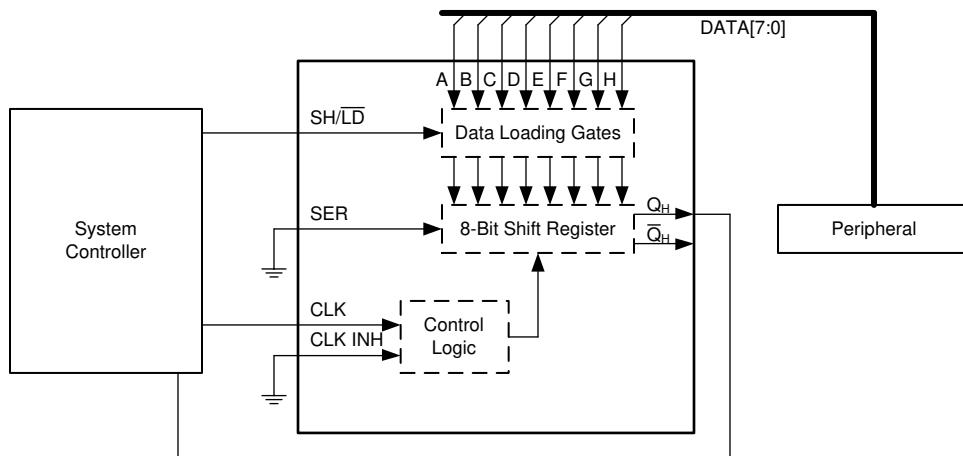


図 9-1. Input Expansion with Shift Registers

9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV165A plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV165A plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV165A can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV165A can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

注意

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV165A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

The SN74LV165A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV165A to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

9.2.5 Application Curve

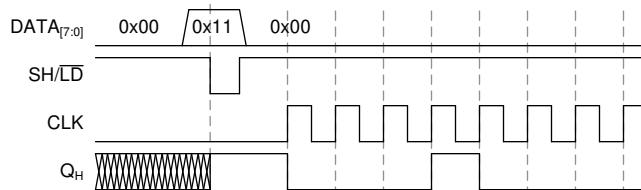


図 9-2. Application Timing Diagram

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [セクション 6.1](#) section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μ F capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01- μ F or 0.022- μ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

9.4.2 Layout Example

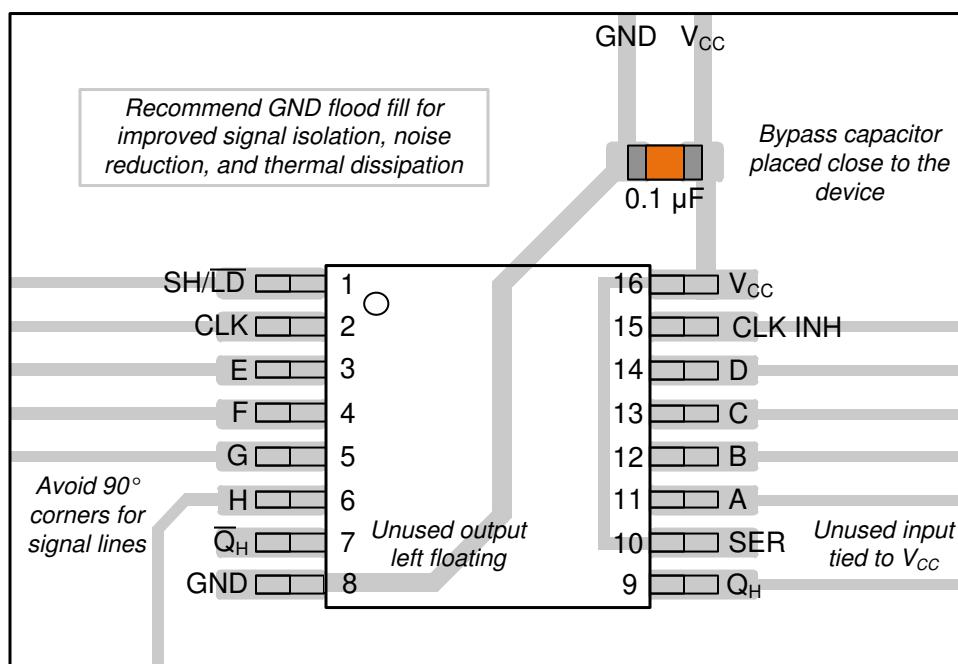


図 9-3. Example Layout for the SN74LV165A in the PW Package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN74LV165A | Click here |

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

10.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74LV165ABQBR | Active | Production | WQFN (BQB) 16 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ABQBR.A | Active | Production | WQFN (BQB) 16 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165AD | Obsolete | Production | SOIC (D) 16 | - | - | Call TI | Call TI | -40 to 125 | LV165A |
| SN74LV165ADBR | Active | Production | SSOP (DB) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ADBR.A | Active | Production | SSOP (DB) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ADGVR | Active | Production | TVSOP (DGV) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ADGVR.A | Active | Production | TVSOP (DGV) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ADR | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ADR.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ADRG3 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ADRG3.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ADRG4 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ADRG4.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ANSR | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV165A |
| SN74LV165ANSR.A | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV165A |
| SN74LV165APW | Obsolete | Production | TSSOP (PW) 16 | - | - | Call TI | Call TI | -40 to 125 | LV165A |
| SN74LV165APWR | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165APWR.A | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165APWRG3 | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165APWRG3.A | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165APWRG4 | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165APWRG4.A | Active | Production | TSSOP (PW) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ARGYR | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ARGYR.A | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |
| SN74LV165ARGYRG4 | Active | Production | VQFN (RGY) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV165A |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

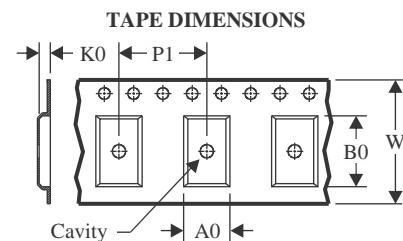
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV165A :

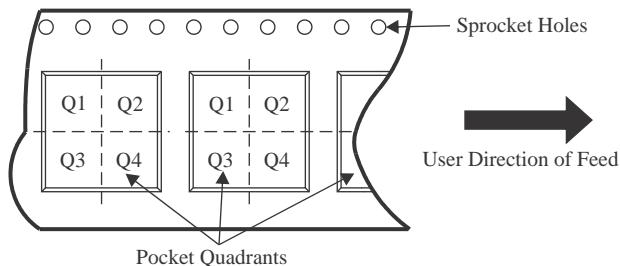
- Automotive : [SN74LV165A-Q1](#)
- Enhanced Product : [SN74LV165A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

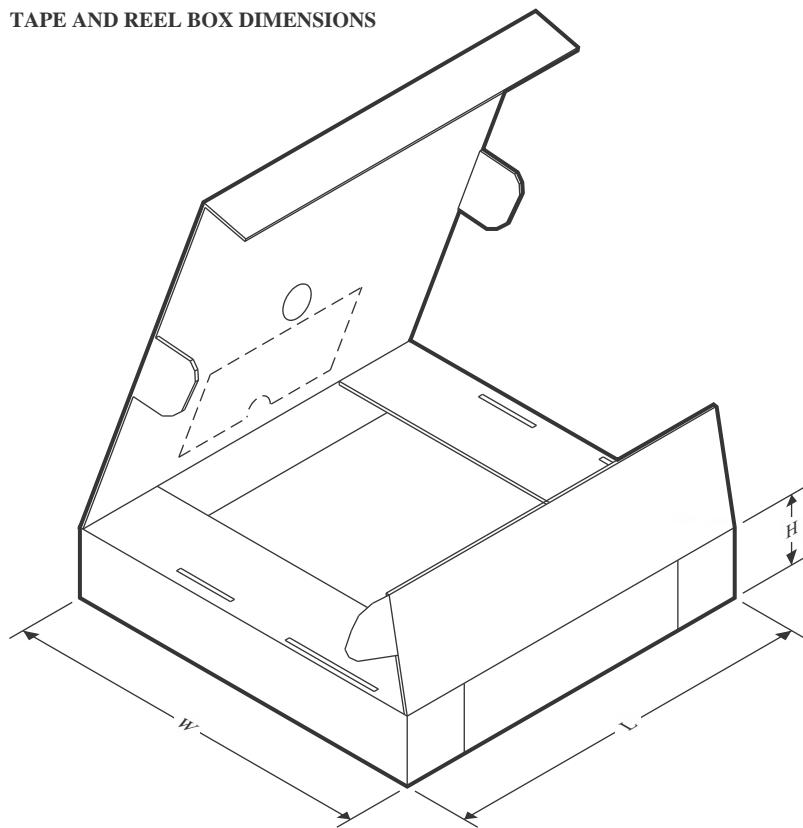
TAPE AND REEL INFORMATION

| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV165ABQBR | WQFN | BQB | 16 | 3000 | 180.0 | 12.4 | 2.8 | 3.8 | 1.2 | 4.0 | 12.0 | Q1 |
| SN74LV165ADBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV165ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV165ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV165ADRG3 | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV165ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV165ANSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV165APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.3 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV165APWRG3 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.85 | 5.45 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV165APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV165APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV165ARGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

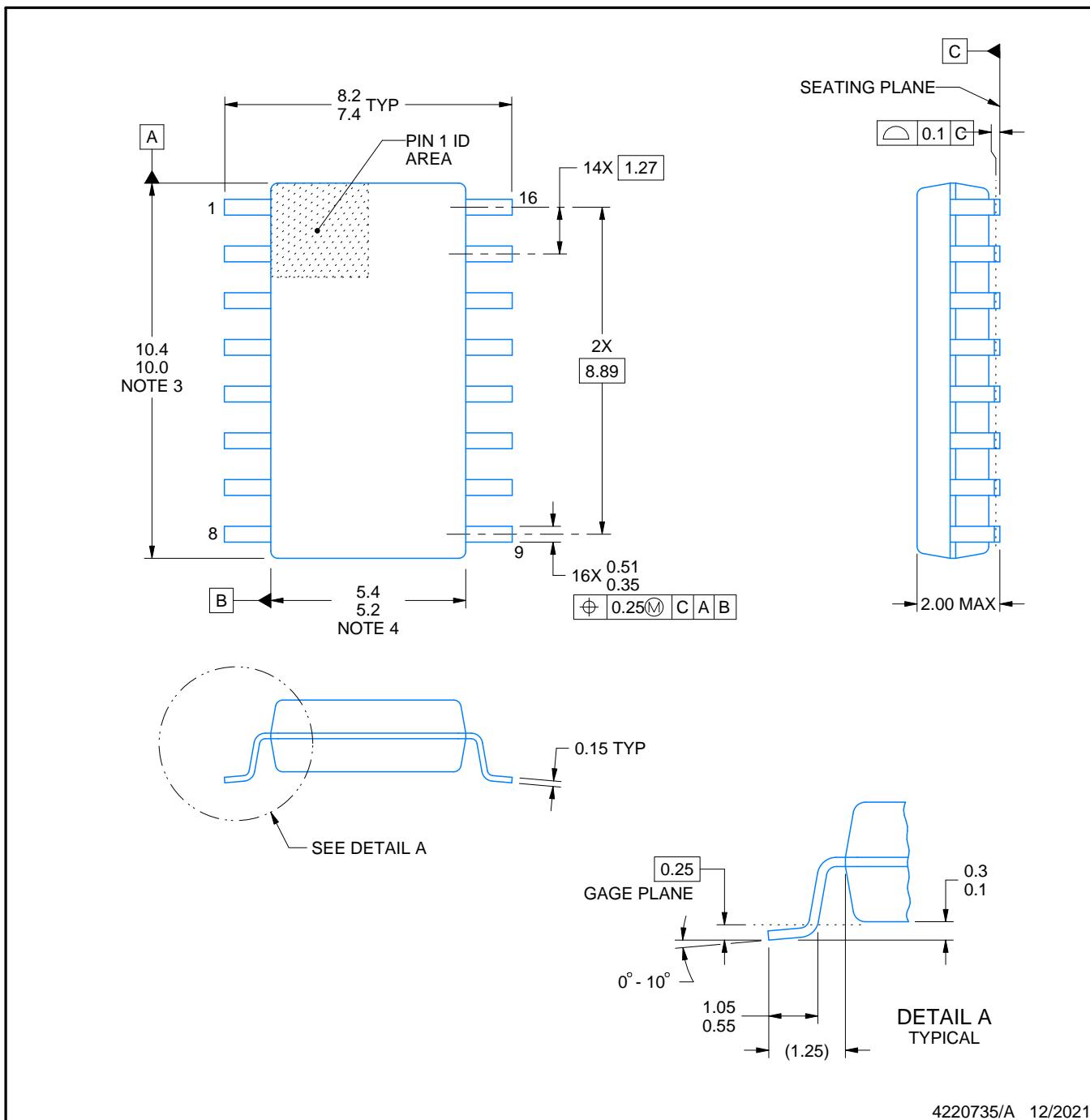
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV165ABQBR | WQFN | BQB | 16 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LV165ADBR | SSOP | DB | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV165ADGVR | TVSOP | DGV | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV165ADR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74LV165ADRG3 | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74LV165ADRG4 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LV165ANSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV165APWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV165APWRG3 | TSSOP | PW | 16 | 2000 | 366.0 | 364.0 | 50.0 |
| SN74LV165APWRG4 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV165APWRG4 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LV165ARGYR | VQFN | RGY | 16 | 3000 | 360.0 | 360.0 | 36.0 |



PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

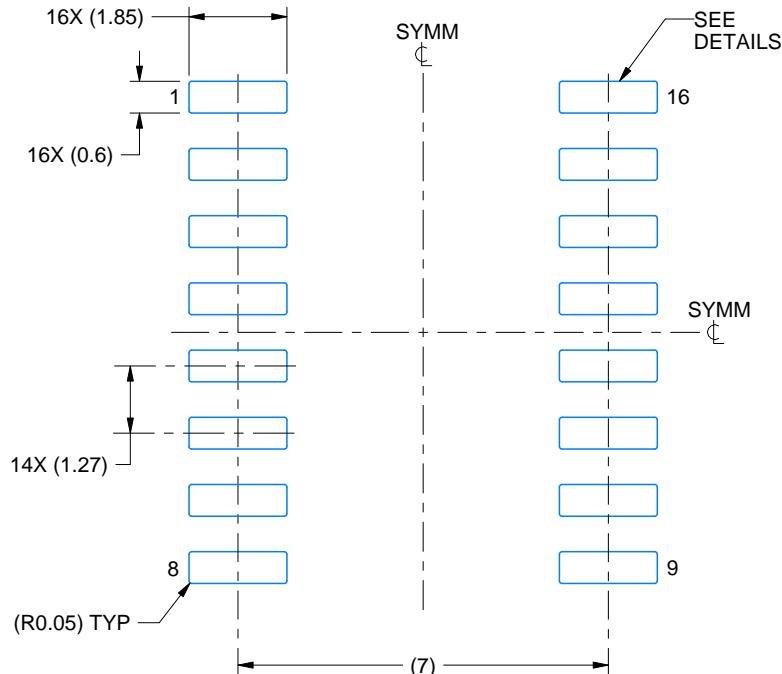
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

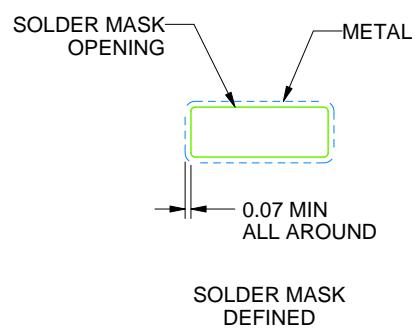
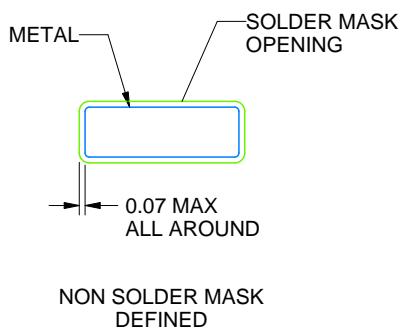
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

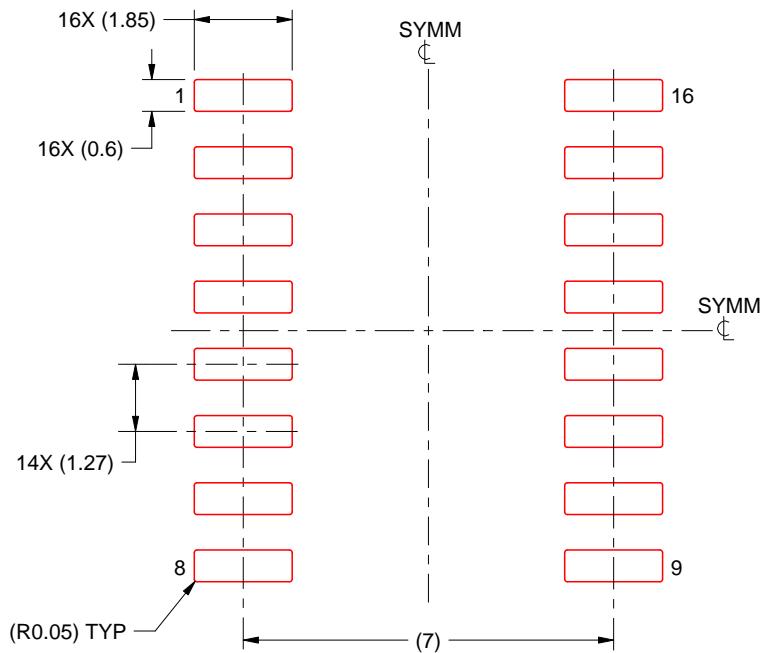
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

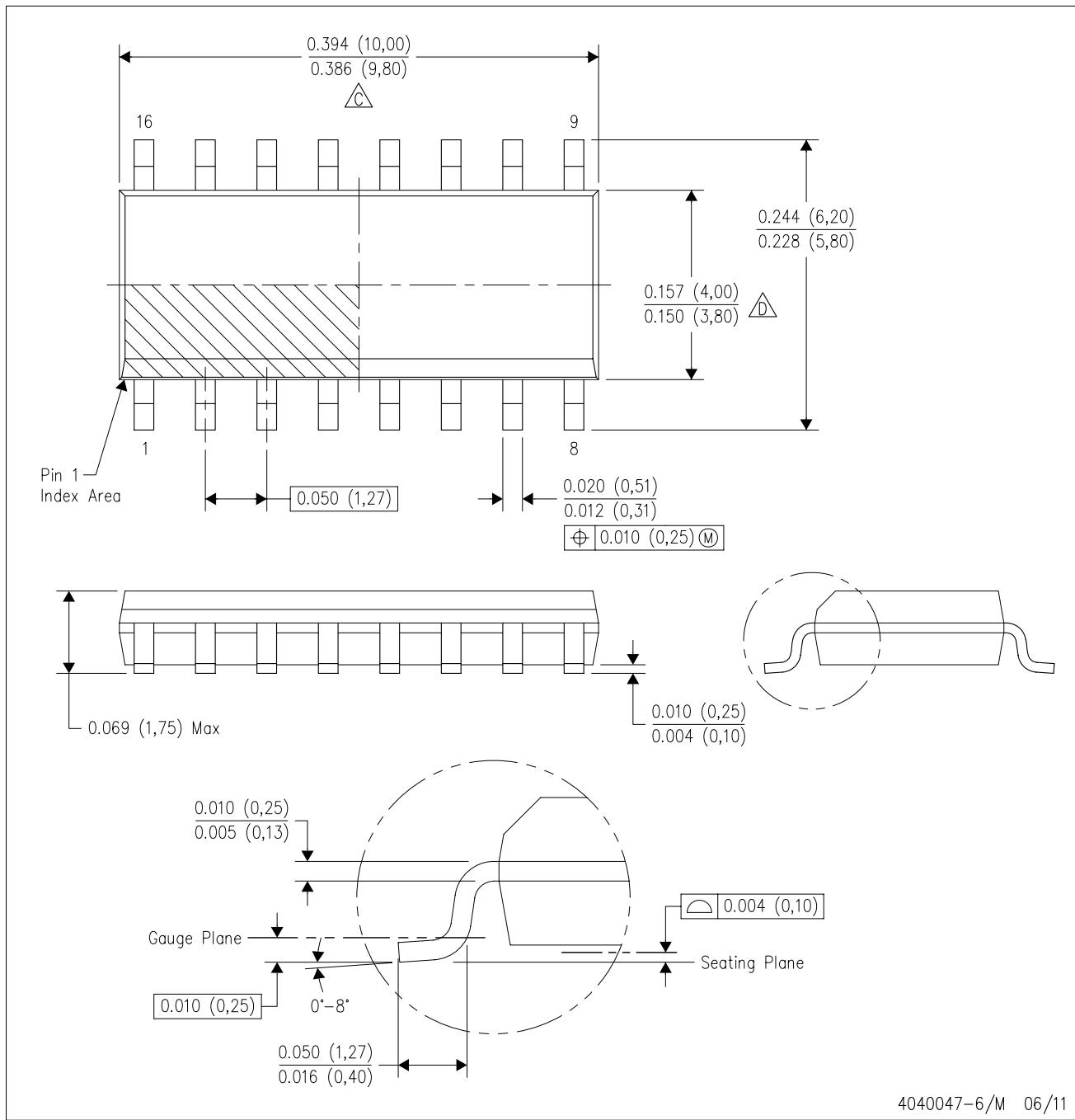
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

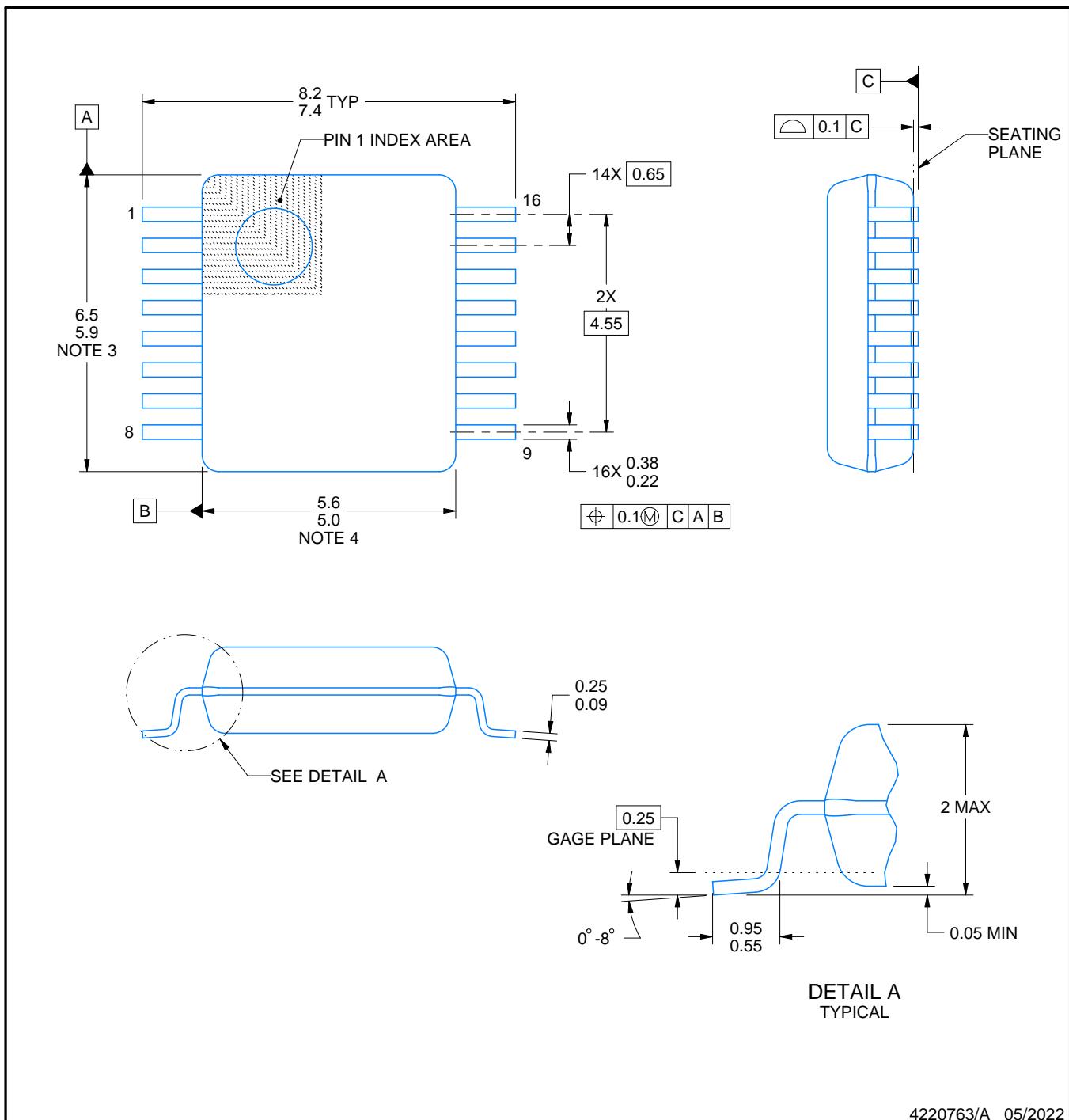
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

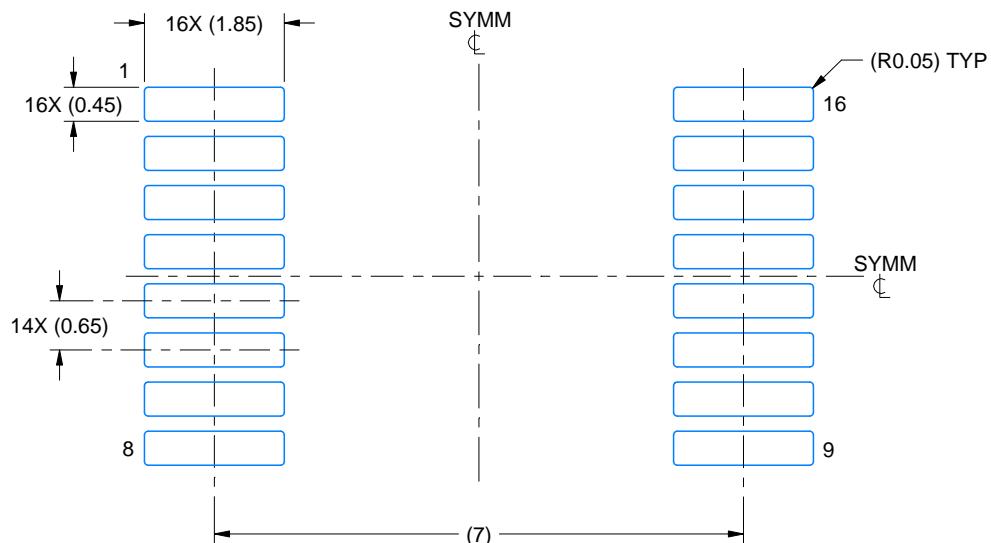
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

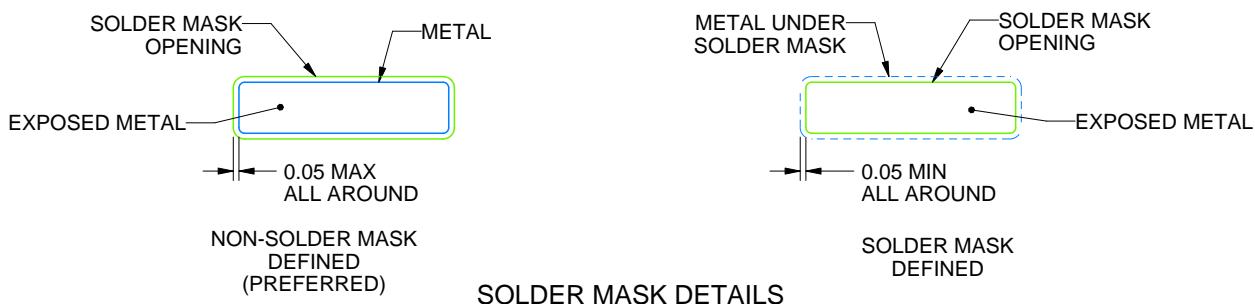
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

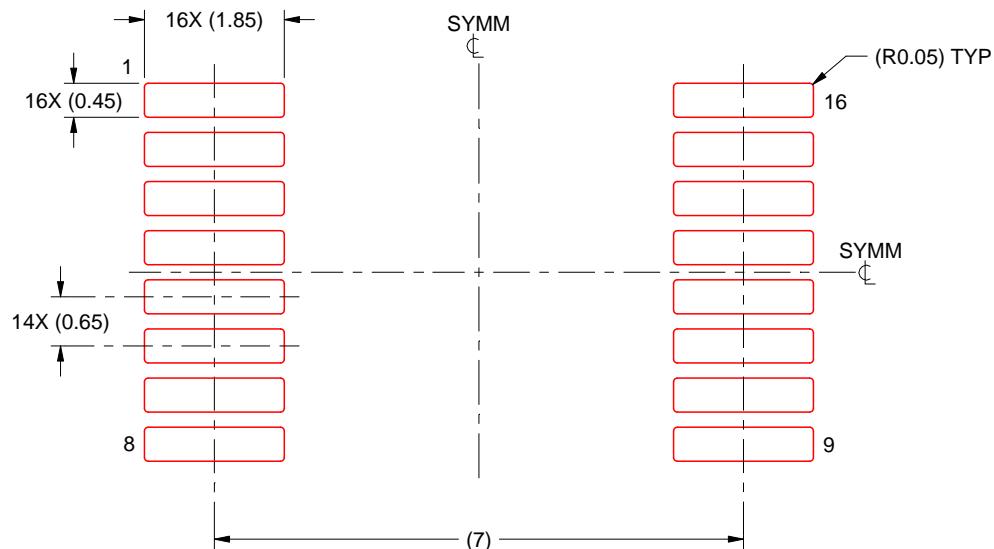
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

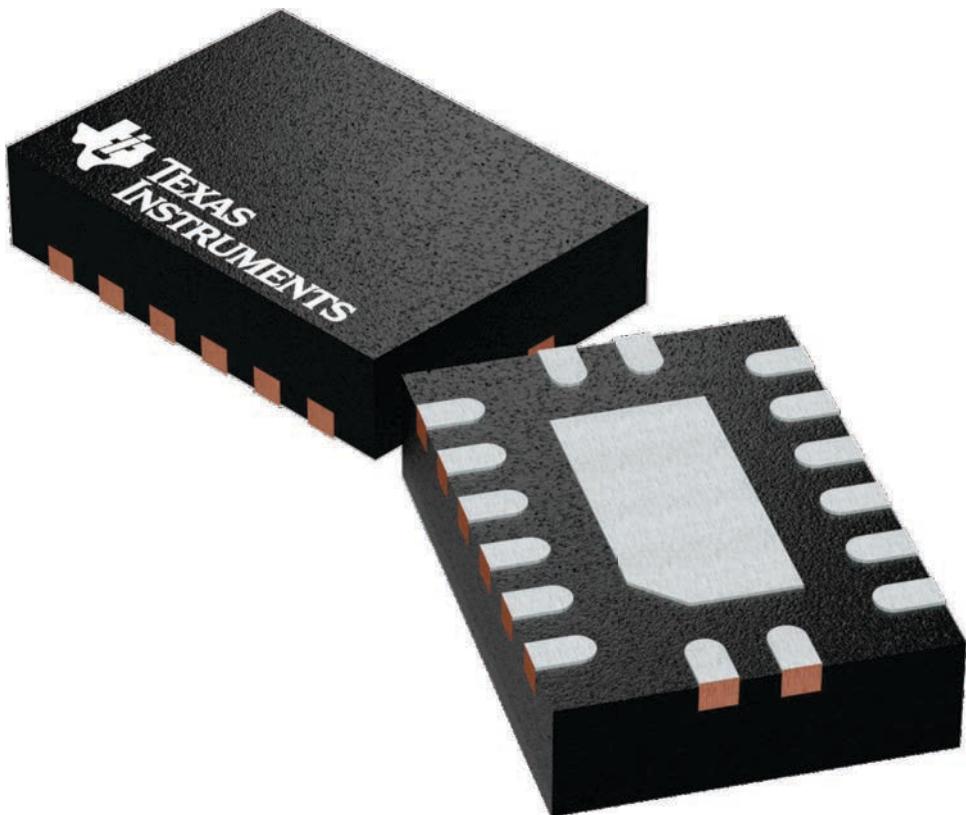
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



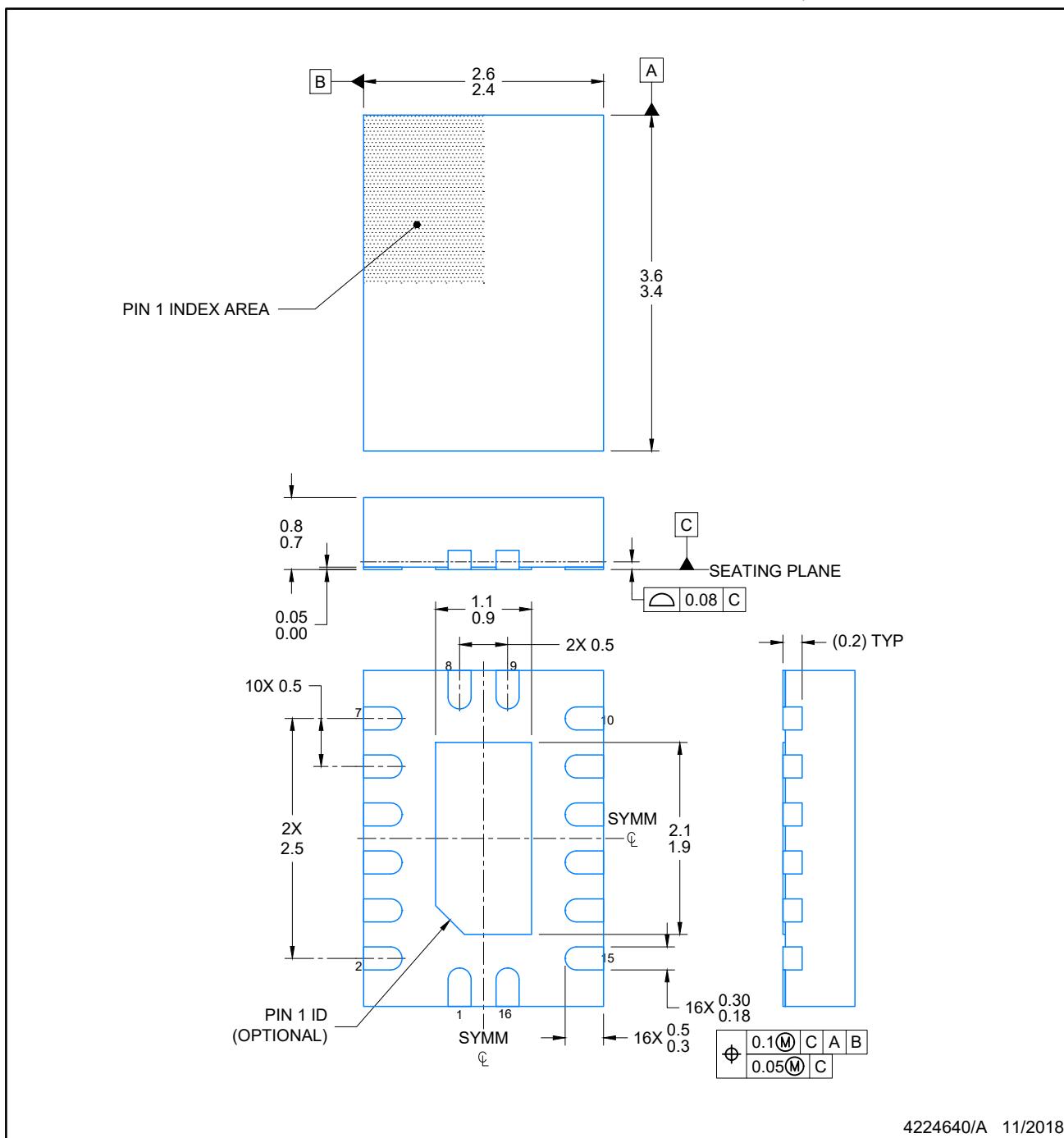
4226161/A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

BQB0016A

PLASTIC QUAD FLAT PACK-NO LEAD



4224640/A 11/2018

NOTES:

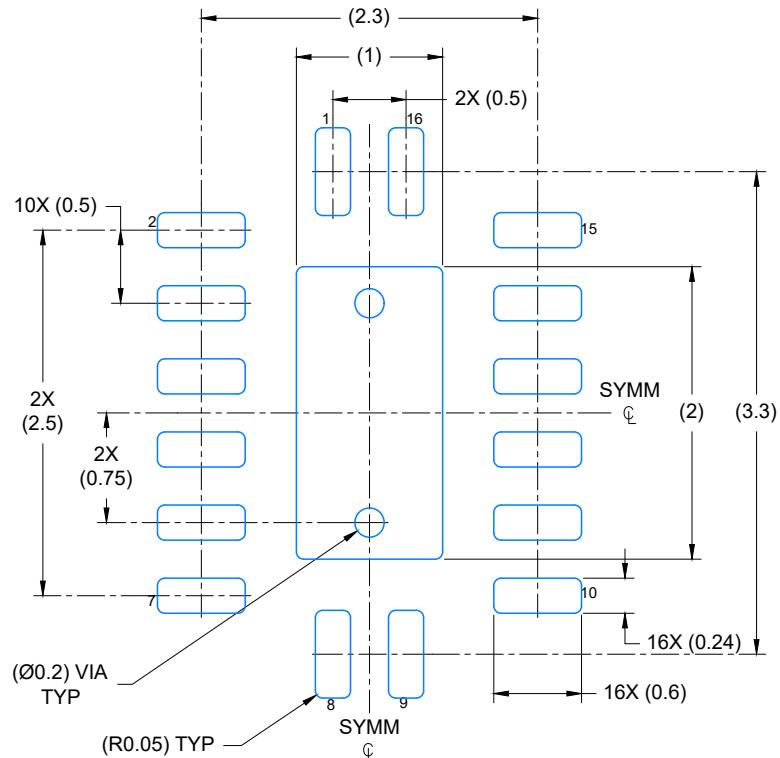
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

BQB0016A

WQFN - 0.8 mm max height

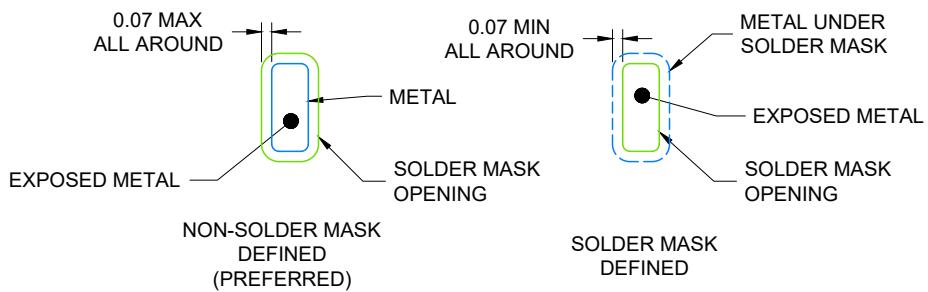
PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

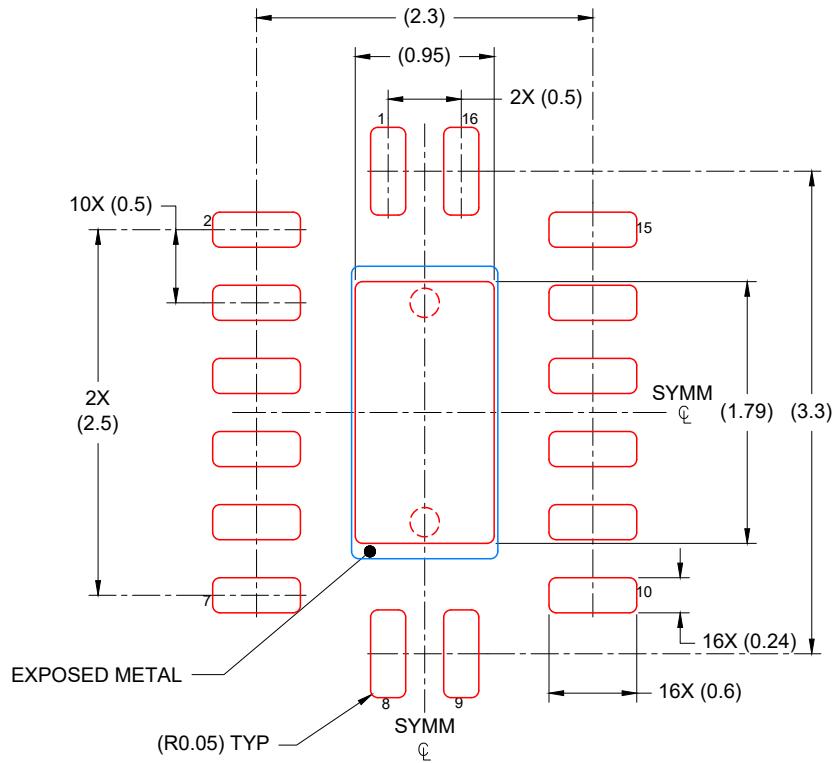
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQB0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

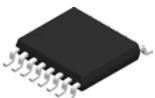
4224640/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

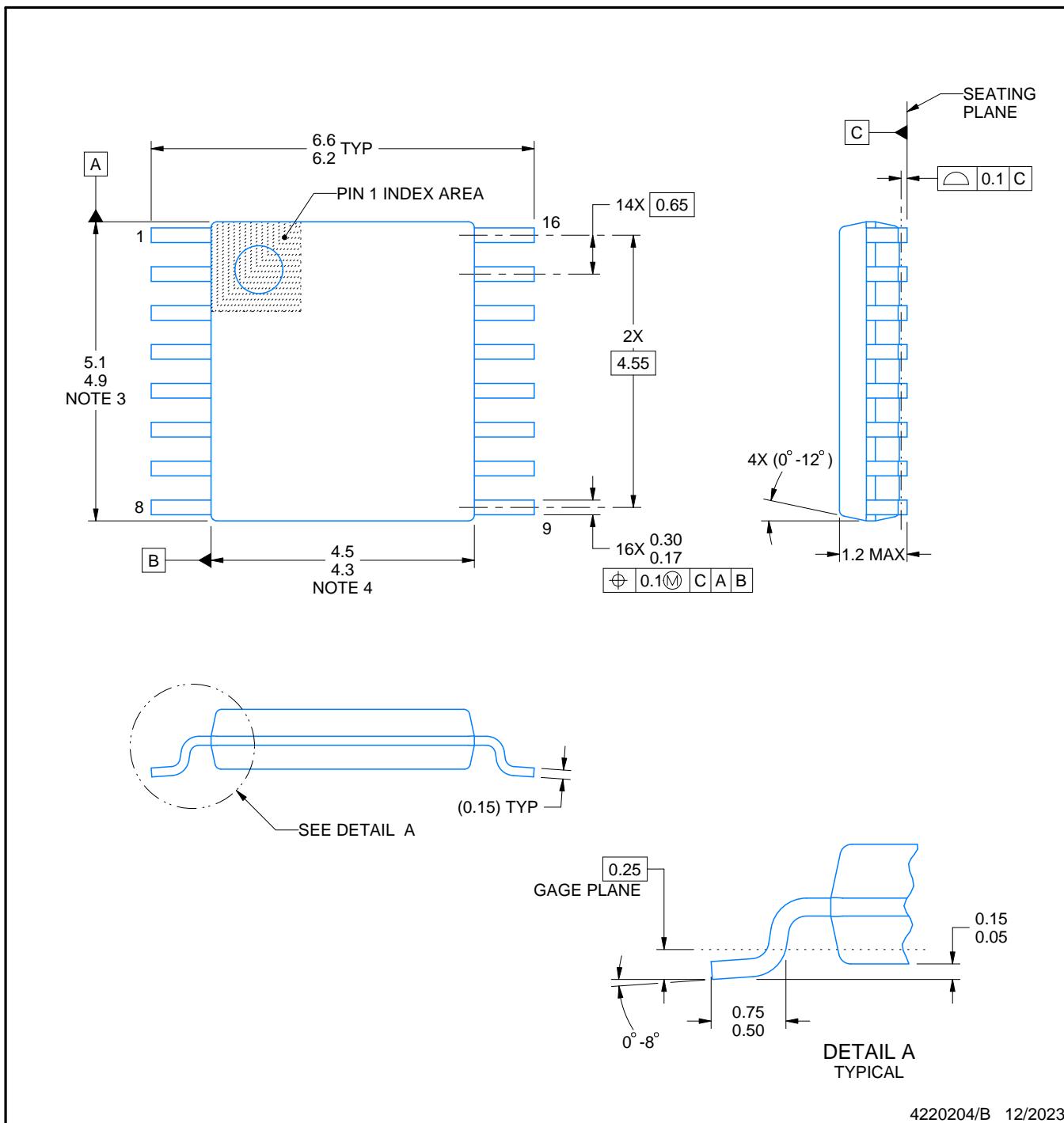
PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

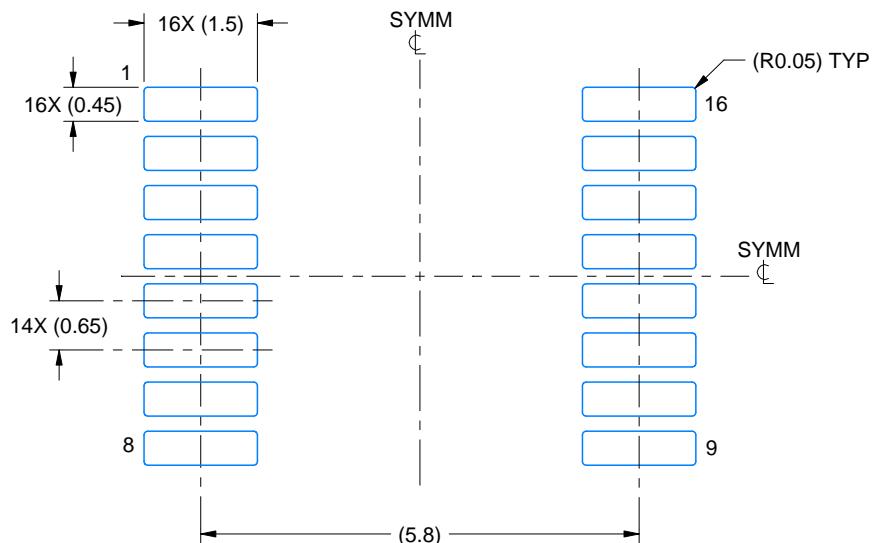
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

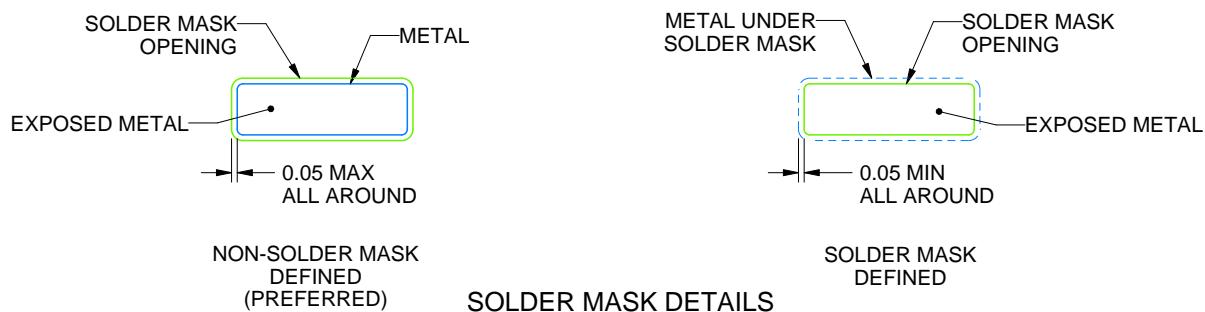
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

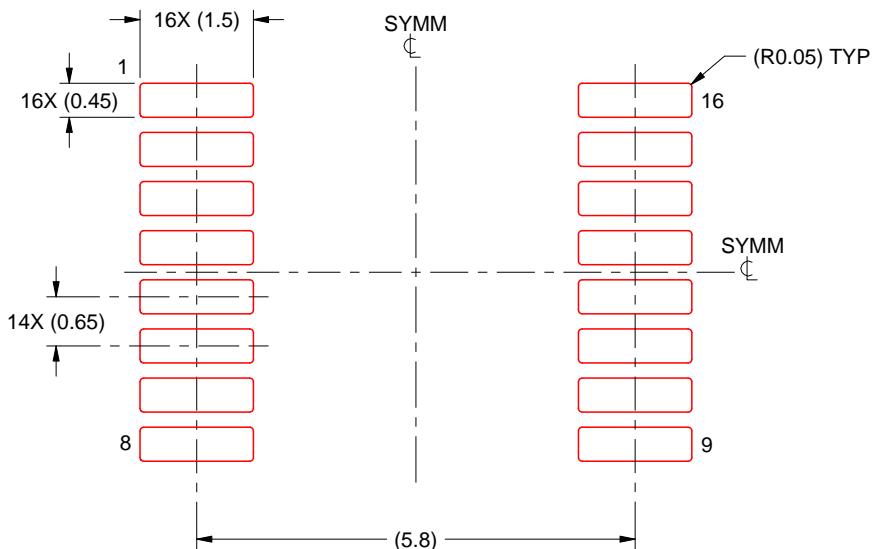
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

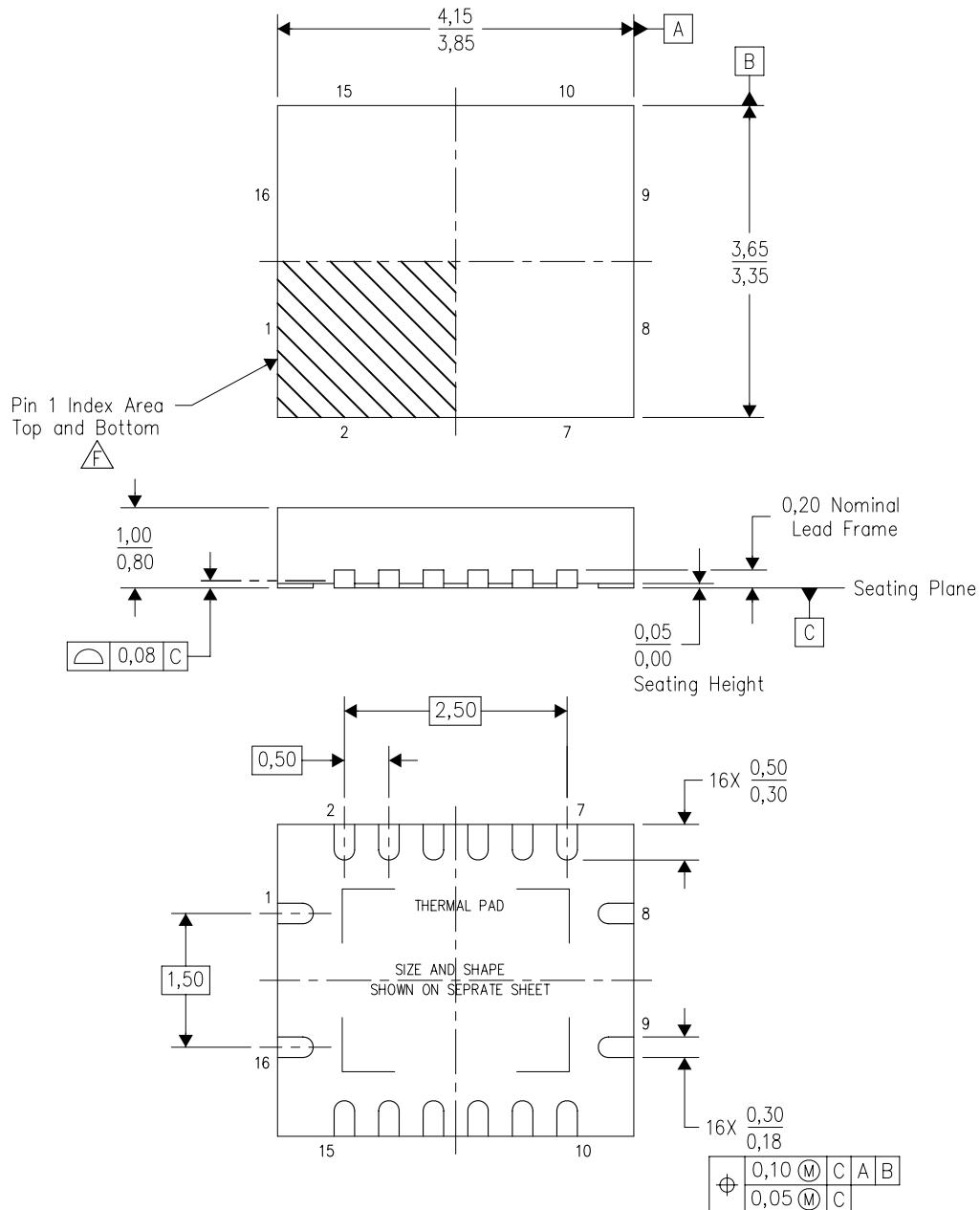
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-3/l 06/2011

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

 F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
The Pin 1 identifiers are either a molded, marked, or metal feature.

- G. Package complies to JEDEC MO-241 variation BA.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の默示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または默示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したもので、(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月