SN74LV374A 3 ステート出力、オクタル・エッジ・トリガ D タイプ・フリップ・フロップ

1 特長

- 2V～5.5V の V_{CC} で動作
- 最大 t_{pd} 9.5ns (5V 時)
- 代表値 V_{OLP} (出力グランド・バウンス) < 0.8V (V_{CC} = 3.3V、T_A = 25℃)
- 代表値 V_{OHV} (出力 V_{OH} アンダーシュート) > 2.3V (V_{CC} = 3.3V、T_A = 25℃)
- すべてのポートで混在モード電圧動作をサポート
- I_{off} により部分的パワーダウン・モード動作をサポート
- JESD 17 準拠で 250mA 超のラッチアップ性能

2 アプリケーション

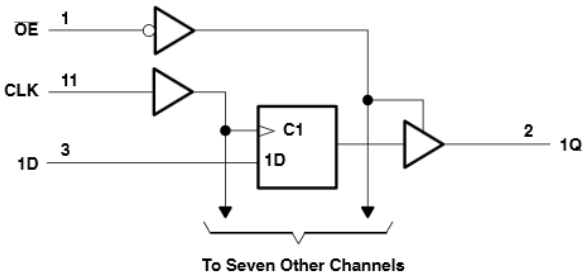
- プログラマブル・ロジック・コントローラ (PLC)
- DCS と PAC:アナログ入力モジュール
- 電車、路面電車、地下鉄の車両
- AC インバータ・ドライブ
- プリンタ

3 概要

SN74LV374A デバイスは、2V～5.5V の V_{CC} で動作するように設計されたオクタル・エッジ・トリガ D タイプ・フリップ・フロップです。

パッケージ情報

部品番号	パッケージ	本体サイズ (公称)
SN74LV374A	DB (SSOP、20)	7.20mm × 5.30mm
	DW (SOIC、20)	12.80mm × 7.50mm
	NS (SO、20)	12.60mm × 5.30mm
	PW (TSSOP、20)	6.50mm × 4.40mm



ここに示すピン番号は DB、DW、NS、PW、RGY の各パッケージのものです。

論理図 (正論理)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision K (December 2022) to Revision L (March 2023) — **Page**

- ドキュメントの構造的レイアウトと表のフォーマットを更新 ... 1
- Updated thermal values for DW package from RθJA = 79.2 to 102.3, RθJC(top) = 43.7 to 69.9, RθJB = 47 to 70.8, ΨJT =18.6 to 46.4, ΨJB = 46.5 to 70.4, all values in °C/W ... 5

Changes from Revision J (March 2015) to Revision K (December 2022) — **Page**

- 文書全体にわたって表、図、相互参照の書式を更新 ... 1

Changes from Revision I (March 2015) to Revision J (October 2016) — **Page**

- Added Junction temperature, T_J ... 4
- Deleted "V_{CC} × 0.3" from MIN and added "V_{CC} × 0.3" to MAX for SN54LV374A and SN74LV374A ... 5
- Changed "SN54LV384A" to "SN54LV374A" in *Electrical Characteristics* table ... 6
- Added *Related Links* section, *Receiving Notification of Documentation Updates* section, and *Community Resources* section ... 15

Changes from Revision H (April 2005) to Revision I (March 2015) — **Page**

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1

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5 Pin Configuration and Functions

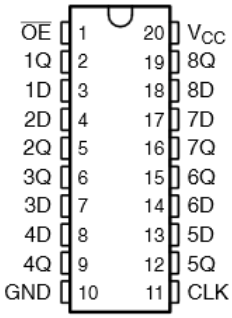

図 5-1. DB, DW, NS, or PW Package 20-PIN SSOP, SOIC, SO, or TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	I	Enable pin
1Q	2	O	Output 1
1D	3	I	Input 1
2D	4	I	Input 2
2Q	5	O	Output 2
3Q	6	O	Output 3
3D	7	I	Input 3
4D	8	I	Input 4
4Q	9	O	Output 4
GND	10	–	Ground pin
CLK	11	I	Clock pin
5Q	12	O	Output 5
5D	13	I	Input 5
6D	14	I	Input 6
6Q	15	O	Output 6
7Q	16	O	Output 7
7D	17	I	Input 7
8D	18	I	Input 8
8Q	19	O	Output 8
V_{CC}	20	–	Power pin

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
V_I	Input voltage(2)		−0.5	7	V
V_O	Voltage applied to any output in the high-impedance or power-off state (2)		−0.5	7	V
V_O	Output voltage(2) (3)		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0)		–20	mA
I_{OK}	Output clamp current	(V_O < 0)		–50	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			SN74LV374A		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.77		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–8	
		V_{CC} = 4.5 V to 5.5 V		–16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		8	
		V_{CC} = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV374A				UNIT
		DB (SSOP)	DW (SOIC)	NS (SO)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	94.5	102.3	76.7	102.4	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	56.4	69.9	43.2	36.5	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	49.7	70.8	44.2	53.6	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	18.5	46.4	16.8	2.4	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	49.3	70.4	43.8	52.9	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN74LV374A –40°C to +85°C			SN74LV374A –40°C to +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC}−0.1			V_{CC}−0.1			V
	I_{OH} = −2 mA	2.3 V	2			2			
	I_{OH} = −8 mA	3 V	2.48			2.48			
	I_{OH} = −16 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 8 mA	3 V			0.44			0.44	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±5			±5	µA
I_{CC}	V_I = V_{CC} or GND , I_O = 0	5.5 V			20			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		2.9			2.9		pF

6.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV374A –40°C to +85°C		SN74LV374A –40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	60[1]	105[1]		50		50		MHz
			C_L = 50 pF	50	85		40		40		
t_{pd}	CLK	Q	C_L = 15 pF		9.7[1]	16.3[1]	1	19	1	20.5	ns
t_{en}	$\overline{OE}$	Q			8.9[1]	15.9[1]	1	19	1	20.5	
t_{dis}	$\overline{OE}$	Q			6.3[1]	12.6[1]	1	15	1	16.5	
t_{pd}	CLK	Q	C_L = 50 pF		11.8	19.3	1	23	1	24.5	ns
t_{en}	$\overline{OE}$	Q			10.9	18.8	1	22	1	23.5	
t_{dis}	$\overline{OE}$	Q			8.2	17.3	1	19	1	20.5	
$t_{sk(o)}$						2		2			

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

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6.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV374A –40°C to +85°C		SN74LV374A –40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80[1]	150[1]		70		70		MHz
			C_L = 50 pF	55	110		50		50		
t_{pd}	CLK	Q	C_L = 15 pF		6.8[1]	12.7[1]	1	15	1	16	ns
t_{en}	$\overline{OE}$	Q			6.3[1]	11[1]	1	13	1	14	
t_{dis}	$\overline{OE}$	Q			4.7[1]	10.5[1]	1	12.5	1	13.5	
t_{pd}	CLK	Q	C_L = 50 pF		8.3	16.2	1	18.5	1	19.5	ns
t_{en}	$\overline{OE}$	Q			7.7	14.5	1	16.5	1	17.5	
t_{dis}	$\overline{OE}$	Q			5.9	14	1	16	1	17	
$t_{sk(o)}$						1.5		1.5			

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV374A –40°C to +85°C		SN74LV374A –40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	130[1]	205[1]		110		110		MHz
			C_L = 50 pF	85	1705		75		75		
t_{pd}	CLK	Q	C_L = 15 pF		4.9[1]	8.1[1]	1	9.5	1	10.5	ns
t_{en}	$\overline{OE}$	Q			4.6[1]	7.6[1]	1	9	1	10	
t_{dis}	$\overline{OE}$	Q			3.4[1]	6.8[1]	1	8	1	9	
t_{pd}	CLK	Q	C_L = 50 pF		5.9	10.1	1	11.5	1	12.5	ns
t_{en}	$\overline{OE}$	Q			5.5	9.6	1	11	1	12	
t_{dis}	$\overline{OE}$	Q			4	8.8	1	10	1	11	
$t_{sk(o)}$						1		1			

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Timing Requirements

over recommended operating free-air temperature range, (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

		T_A = 25°C		SN74LV374A –40°C to +85°C		SN74LV374A –40°C to +125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC} = 2.5 V ± 0.2 V								
t_w	Pulse duration, CLK high or low	6		7		7		ns
t_{su}	Setup time, data before CLK ↑	5		5.5		6		ns
t_h	Hold time, data after CLK ↑	2.5		2.5		3		ns
V_{CC} = 3.3 V ± 0.3 V								
t_w	Pulse duration, CLK high or low	5		5.5		5.5		ns
t_{su}	Setup time, data before CLK ↑	4.5		4.5		5		ns
t_h	Hold time, data after CLK ↑	2		2		2.5		ns
V_{CC} = 5 V ± 0.5 V								
t_w	Pulse duration, CLK high or low	5		5		5		ns
t_{su}	Setup time, data before CLK ↑	3		3		3.5		ns
t_h	Hold time, data after CLK ↑	2		2		2.5		ns

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6.10 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (1)

PARAMETER		SN74LV374A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.5	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	2.9	2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.11 Operating Characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 10 MHz	3.3 V	21.1	pF
					5 V	22.8	

6.12 Typical Characteristics

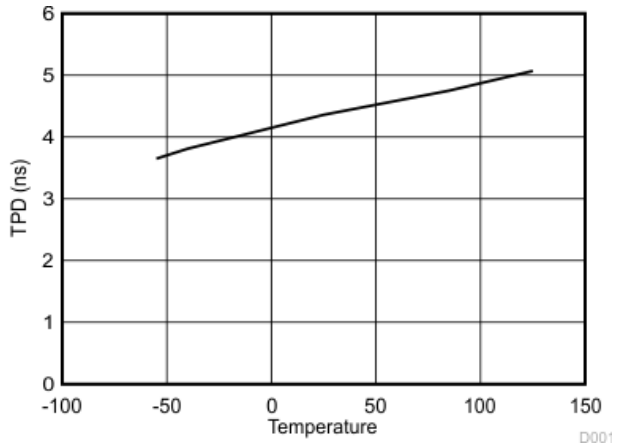

図 6-1. TPD vs. Temperature at 5 V

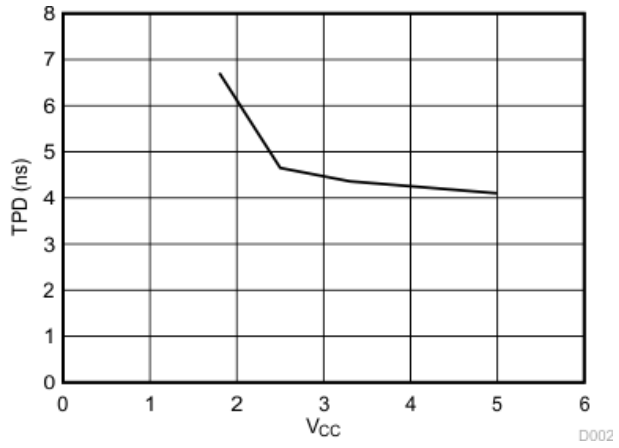

図 6-2. TPD vs. V_{CC} at 25°C

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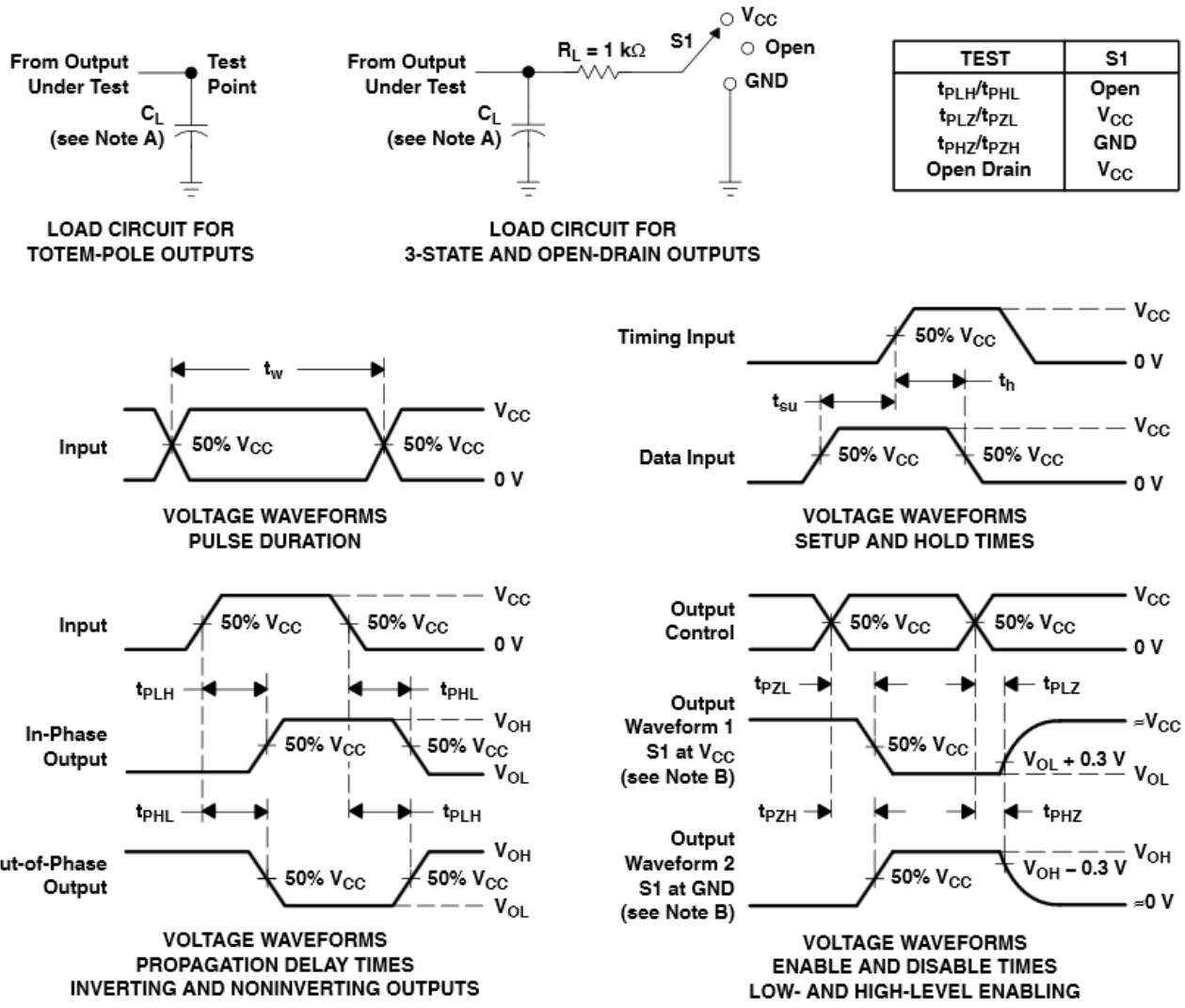
7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

図 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LV374A devices are octal edge-triggered D-type flip-flops designed for 2 V to 5.5 V V_{CC} operation. These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bi-directional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs. A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the latch.

Old data can be retained or new data can be entered while the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The output of the device is unknown until the first valid rising clock edge occurs while V_{CC} is within the *セクション 6.3* range.

8.2 Functional Block Diagram

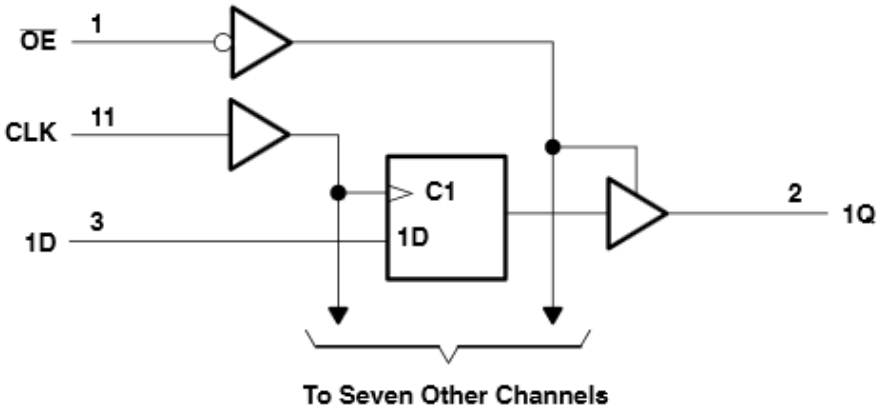


図 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The device's wide operating range allows it to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SN74LV374A devices.

表 8-1. Function Table (Each Flip-Flop)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q_0

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表 8-1. Function Table (Each Flip-Flop) (continued)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
H	X	X	Z

9 Application and Implementation

注

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9.1 Application Information

The SN74LV374A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V allowing down translation to the V_{CC} level.

9.2 Typical Application

図 9-1 shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

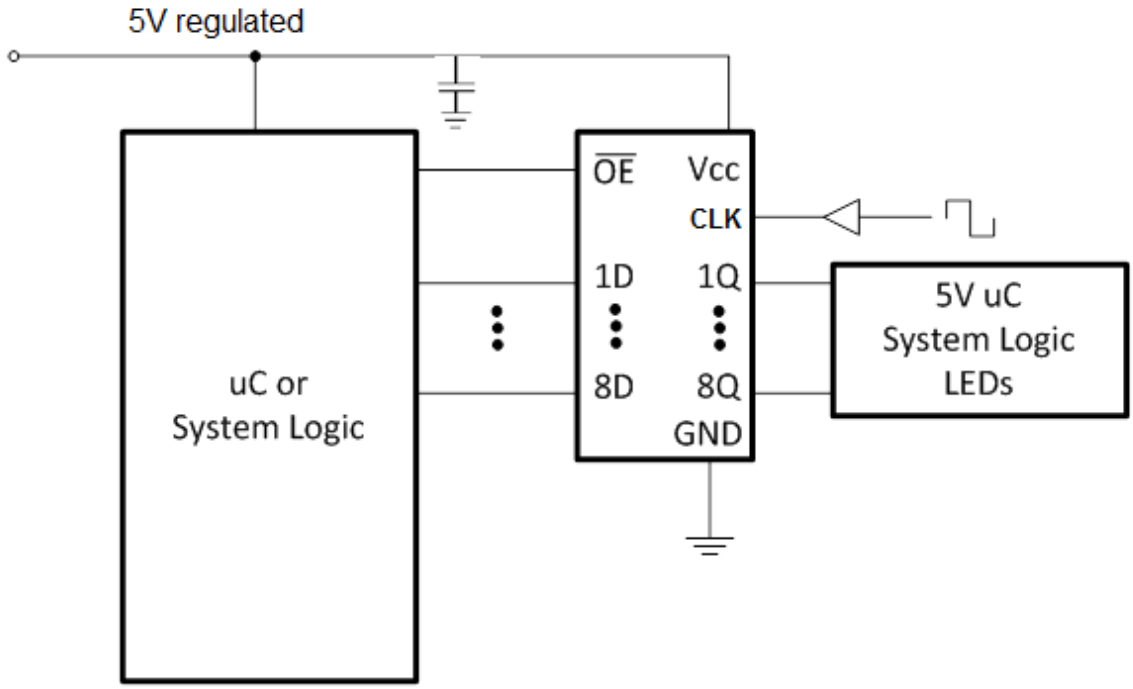

図 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

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9.2.2 Detailed Design Procedure

- Recommended Input conditions:
  - Rise time and fall time specs see (Δt/ΔV) in セクション 6.3.
  - Specified High and low levels. See (V_{IH} and V_{IL}) in セクション 6.3.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- Recommended output conditions:
  - Load currents should not exceed 35 mA per output and 70 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curve

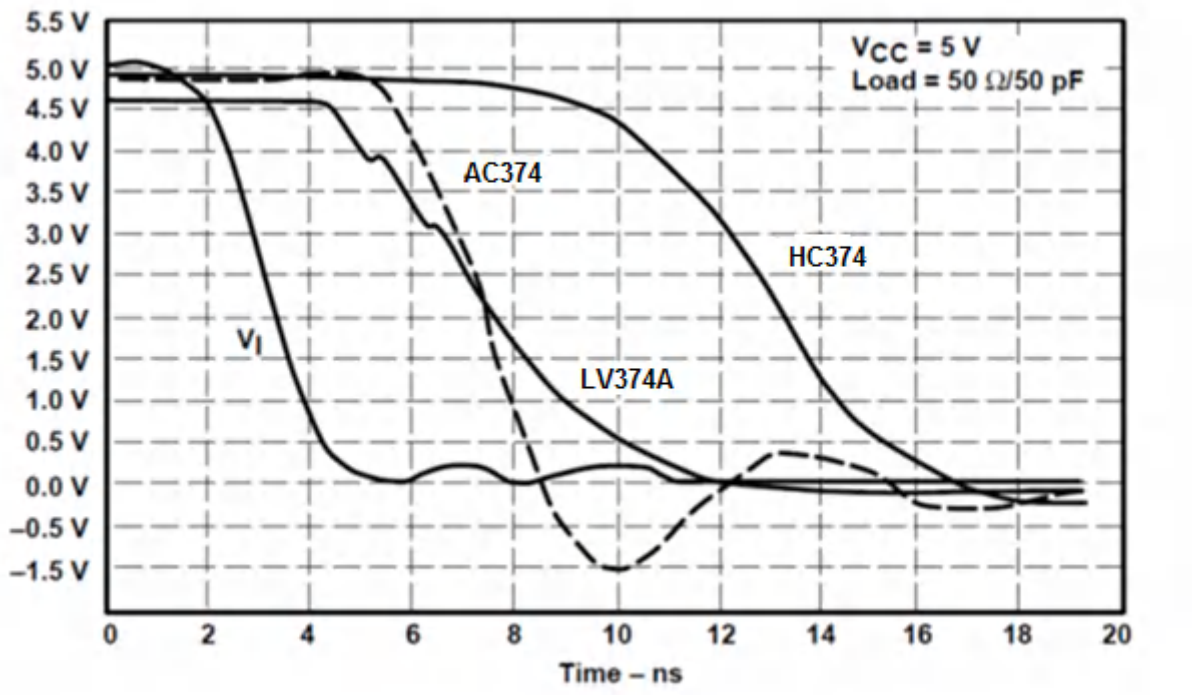

図 9-2. Switching Characteristics Comparison

9.3 Power Supply Recommendations

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

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9.4.1.1 Layout Example

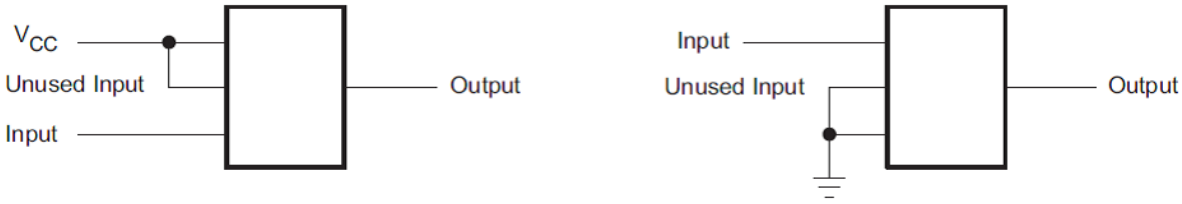

図 9-3. Layout Example

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.4 Trademarks

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10.5 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV374ADBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A
SN74LV374ADBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A
SN74LV374ADW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 125	LV374A
SN74LV374ADWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A
SN74LV374ADWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A
SN74LV374ANSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV374A
SN74LV374ANSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV374A
SN74LV374APW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 125	LV374A
SN74LV374APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A
SN74LV374APWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV374A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV374A :

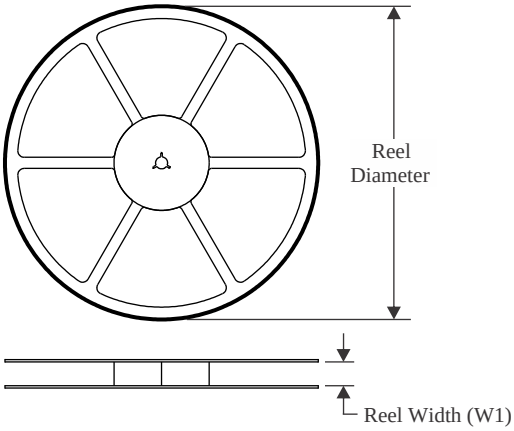
- Automotive : SN74LV374A-Q1
- Enhanced Product : SN74LV374A-EP

NOTE: Qualified Version Definitions:

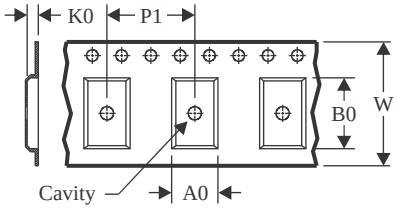
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

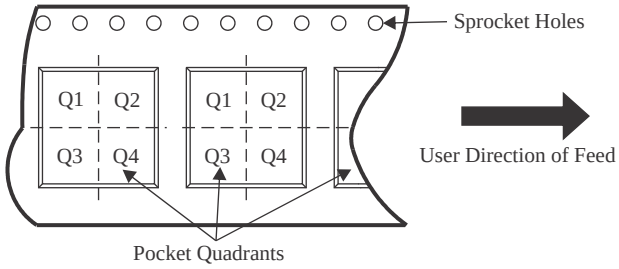


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

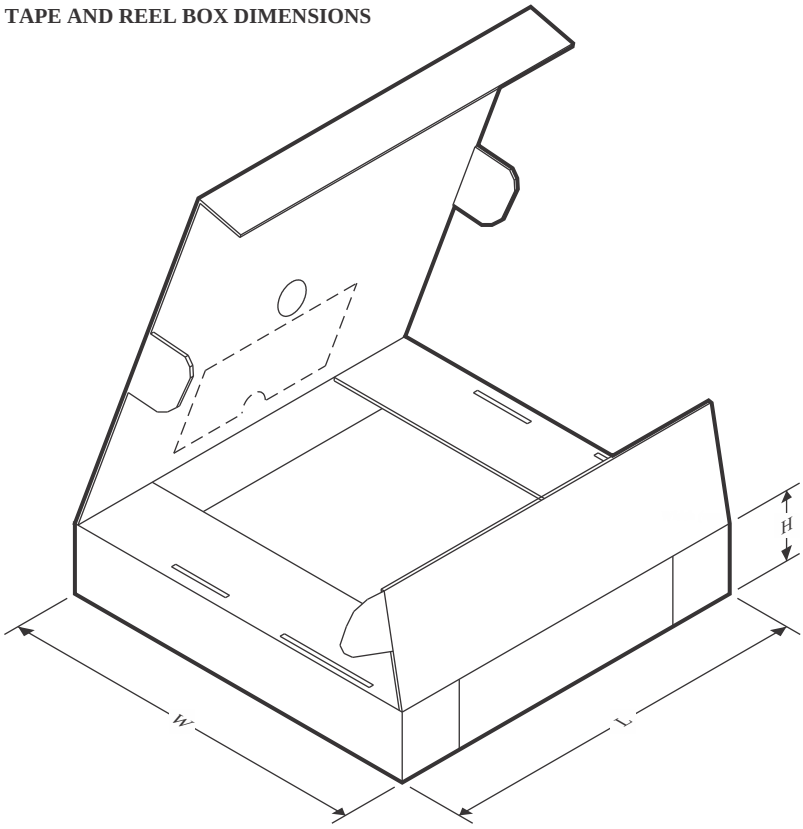
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV374ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV374ADWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74LV374ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV374ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV374APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

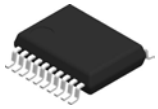
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV374ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LV374ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV374ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV374ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LV374APWR	TSSOP	PW	20	2000	353.0	353.0	32.0

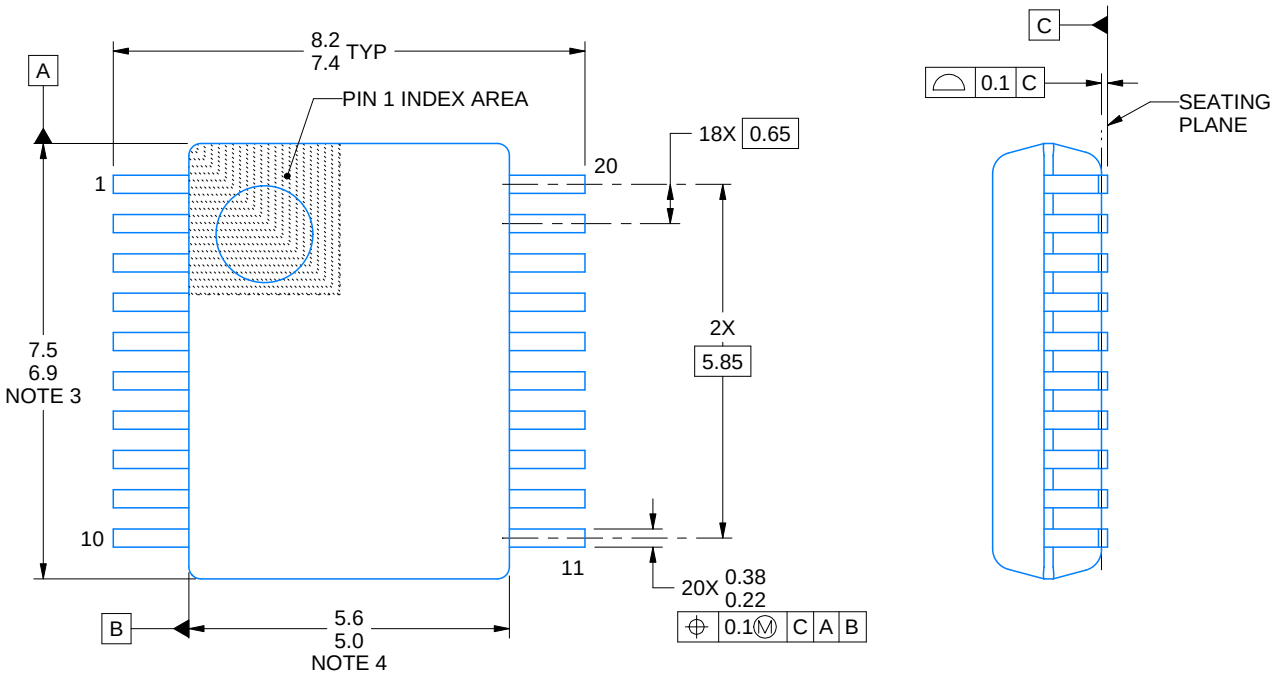
DB0020A

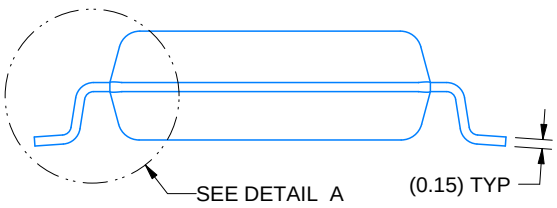


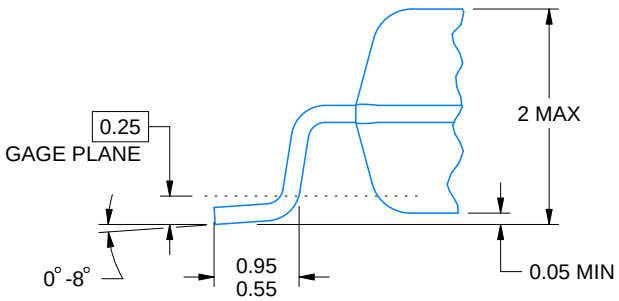
PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE





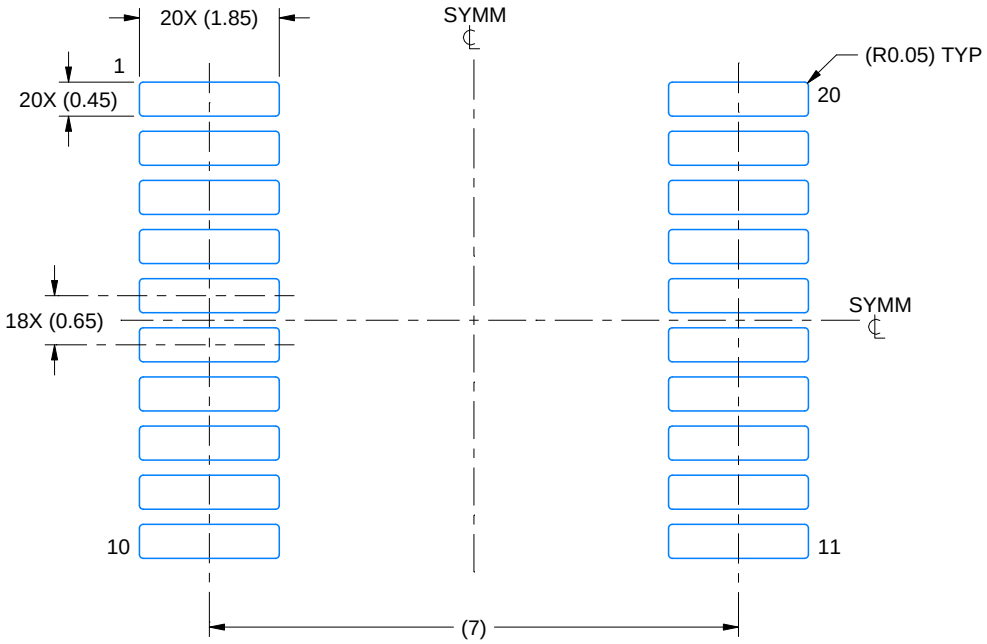


DETAIL A
TYPICAL

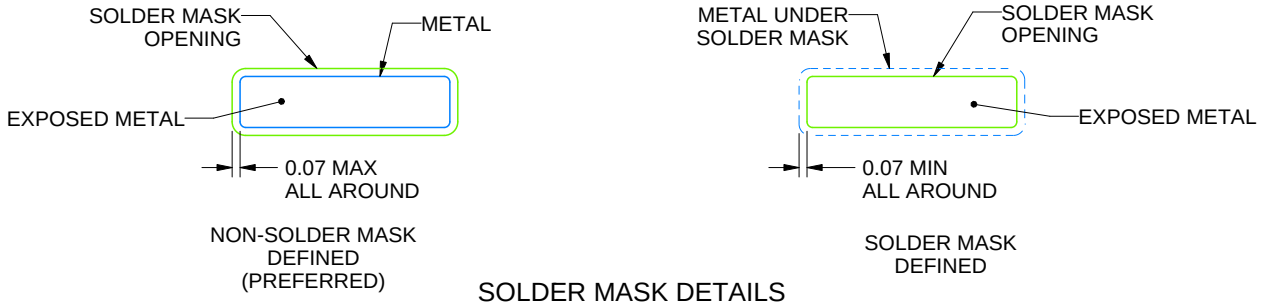
4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

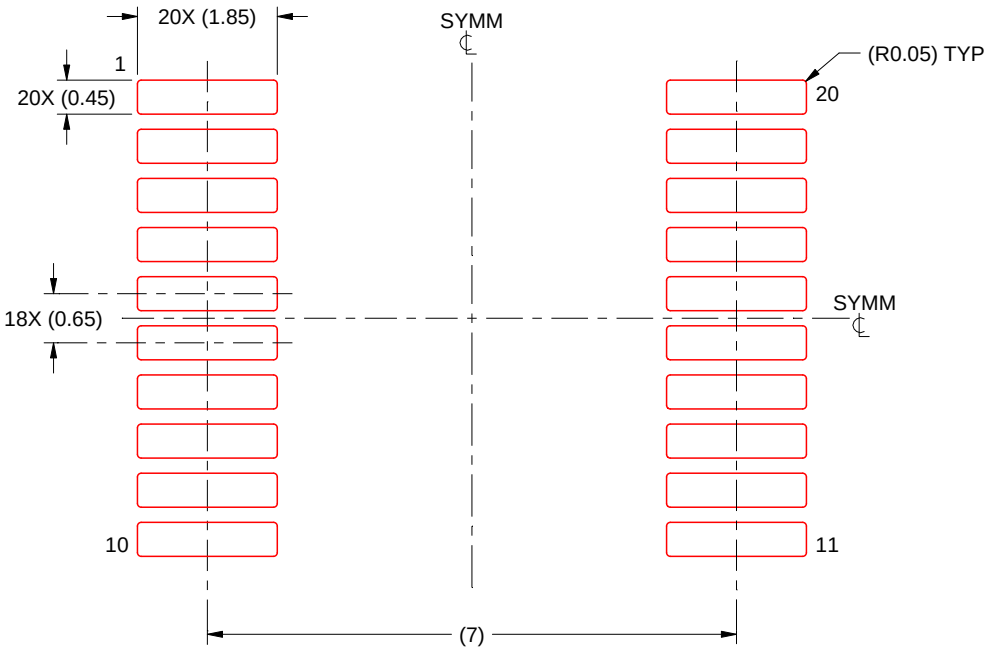
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

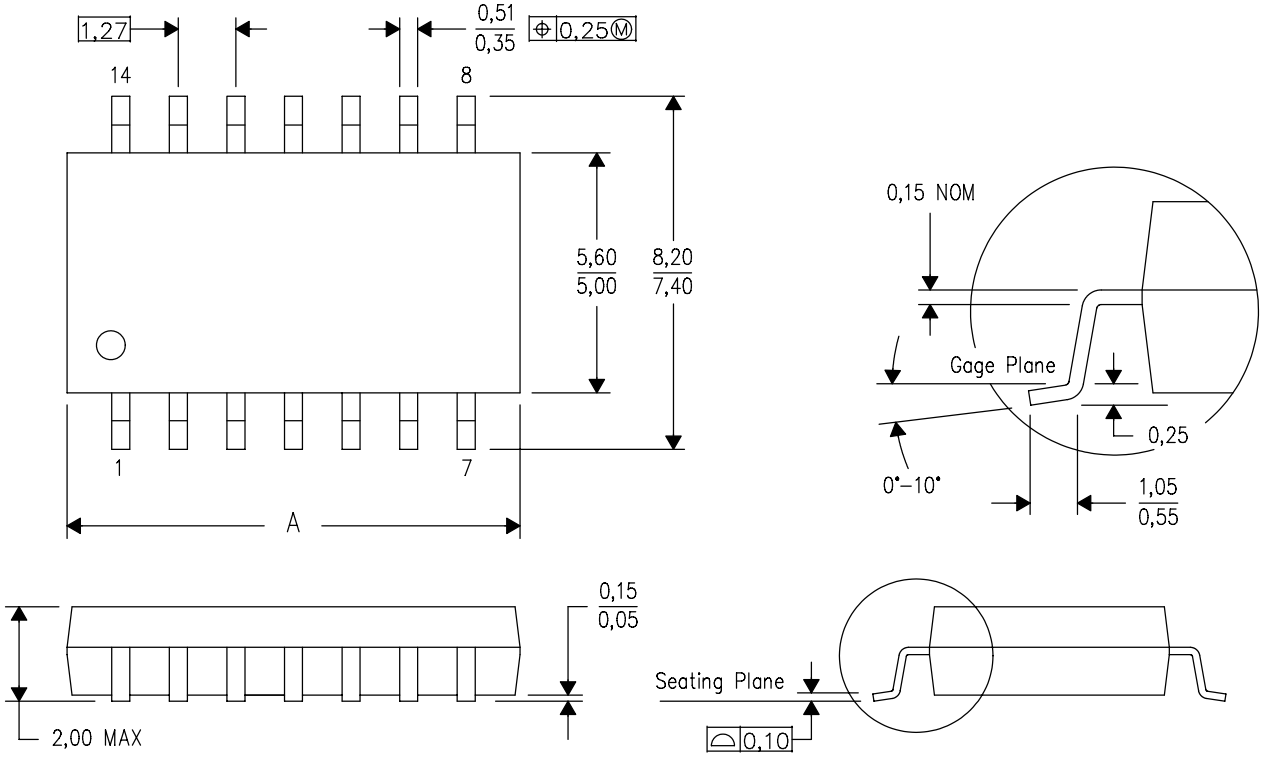
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

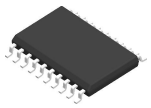
14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

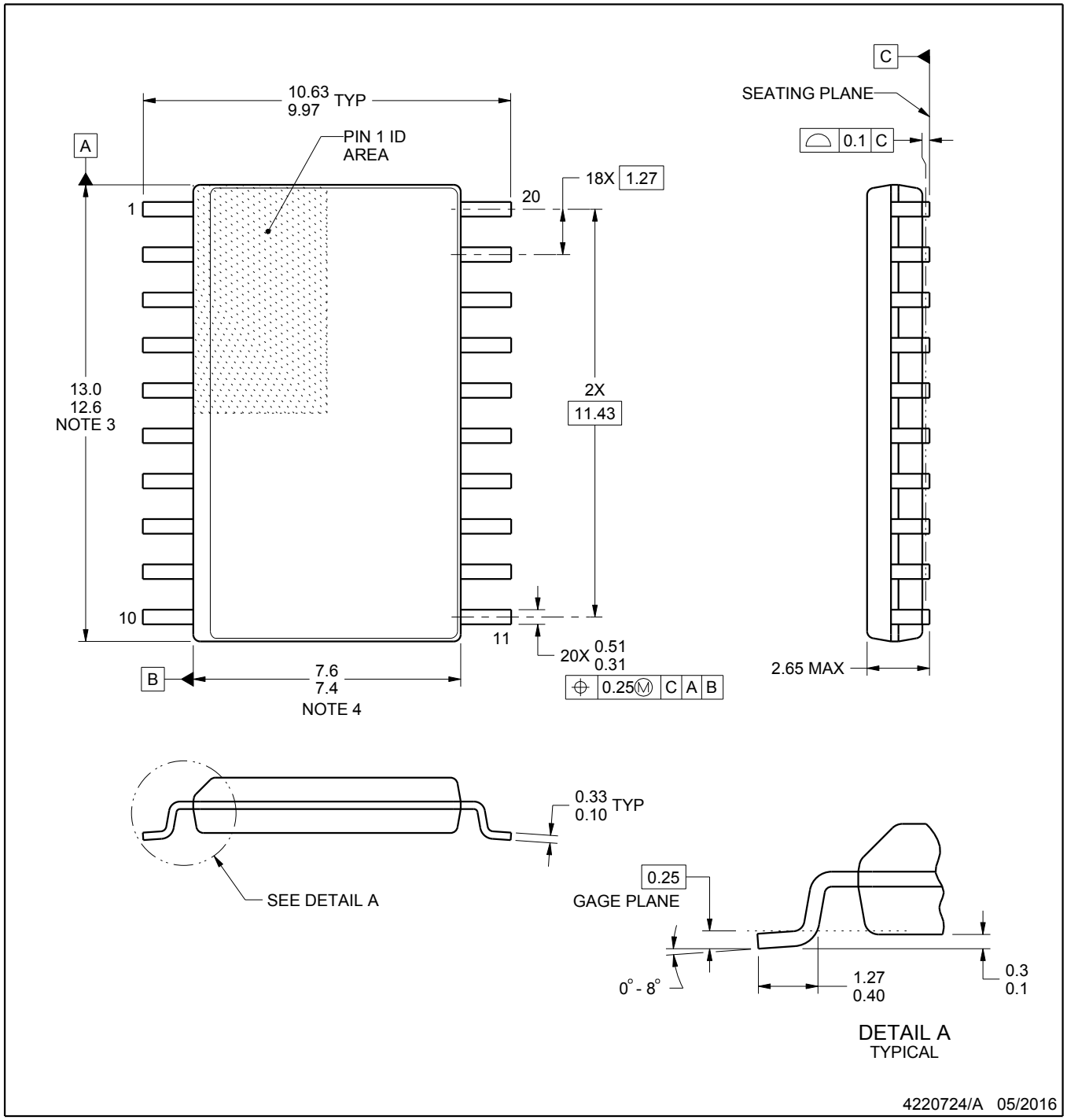


PACKAGE OUTLINE

DW0020A

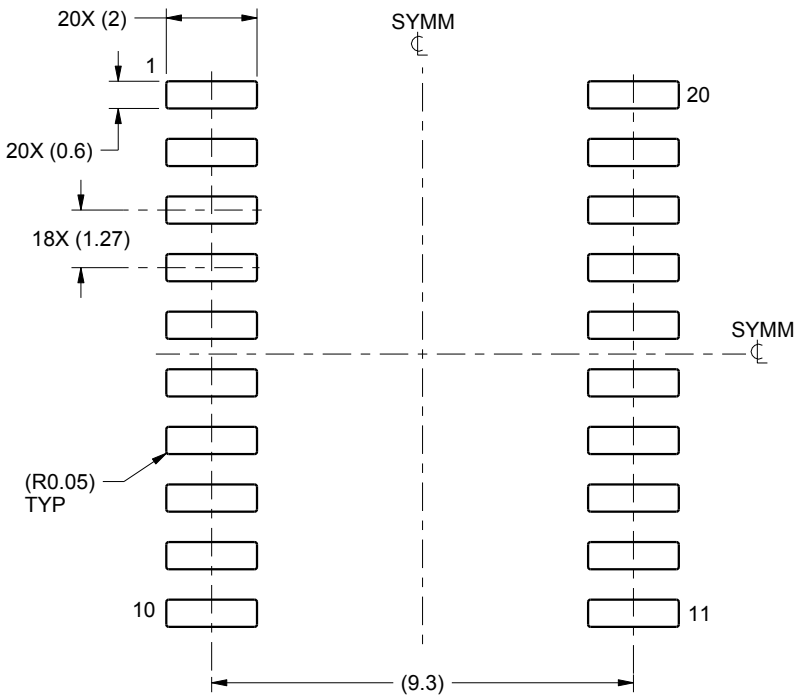
SOIC - 2.65 mm max height

SOIC

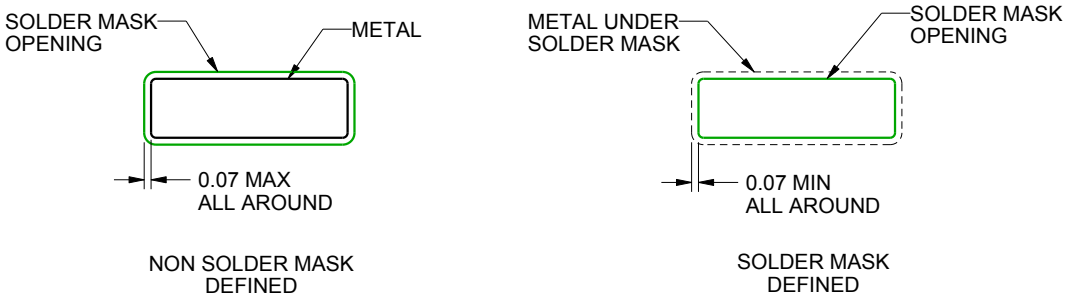


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

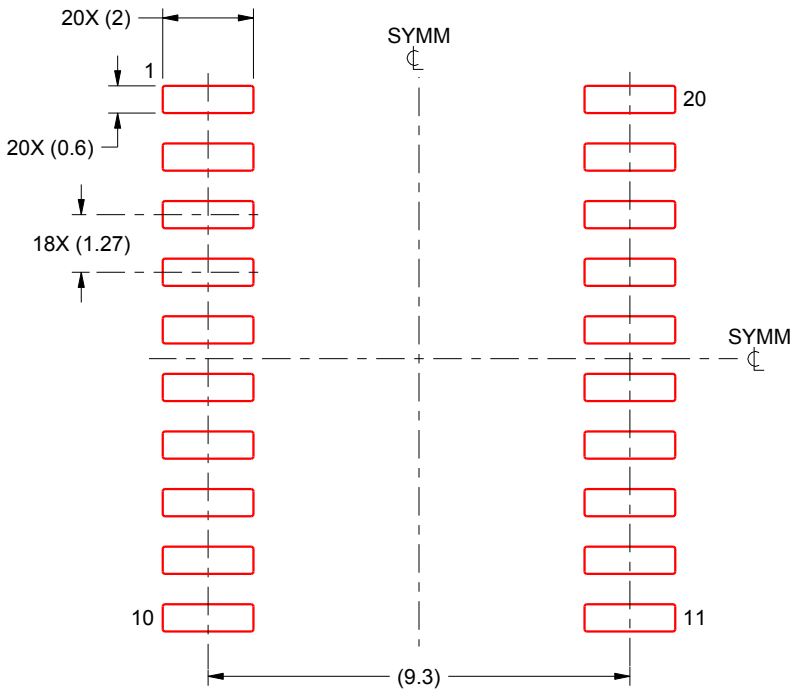


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

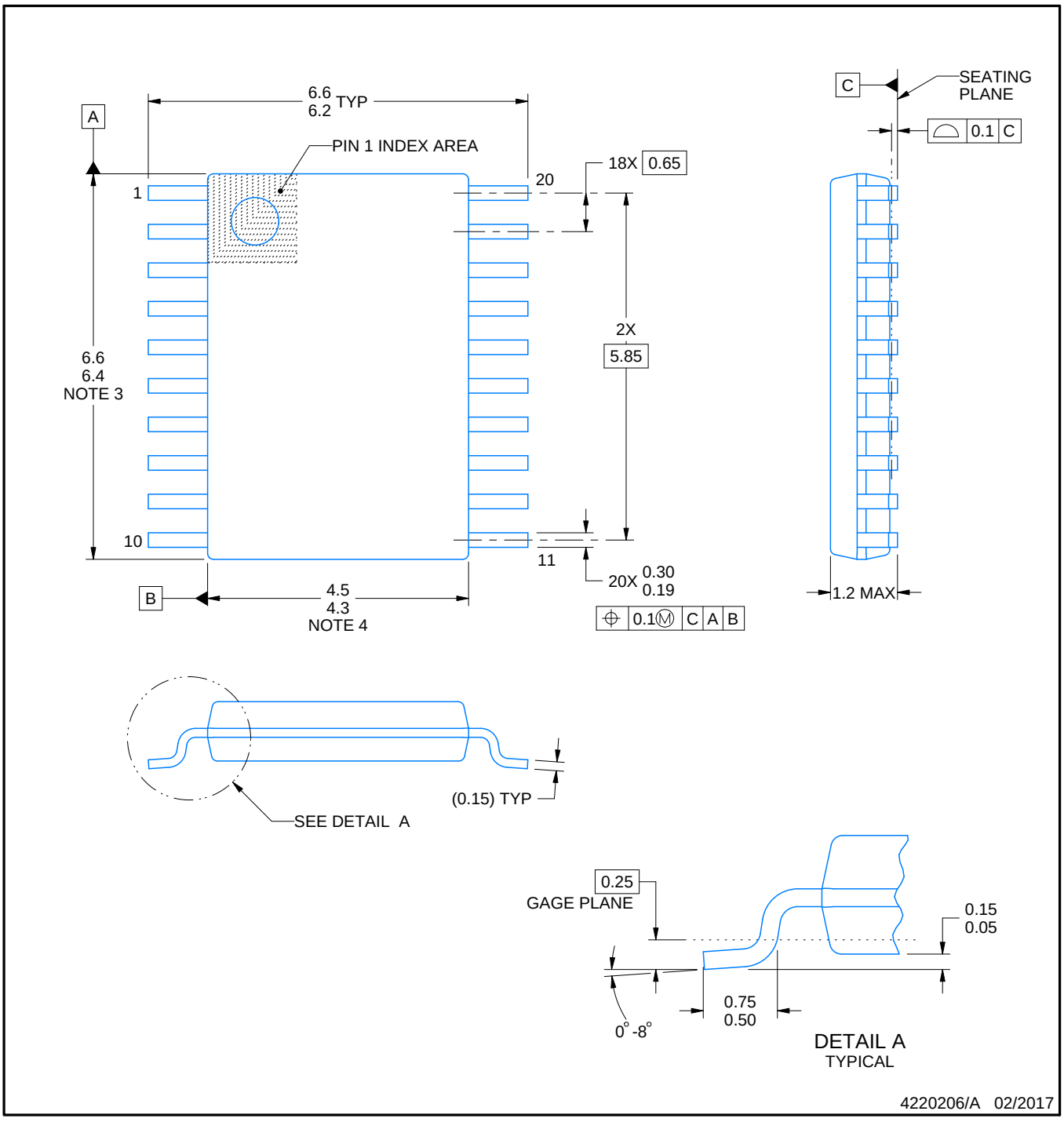
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

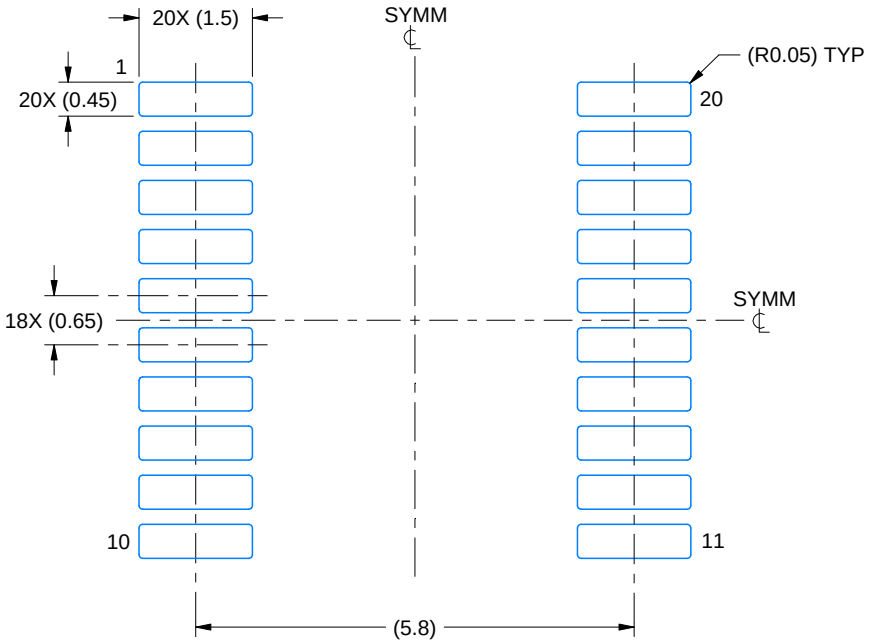
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

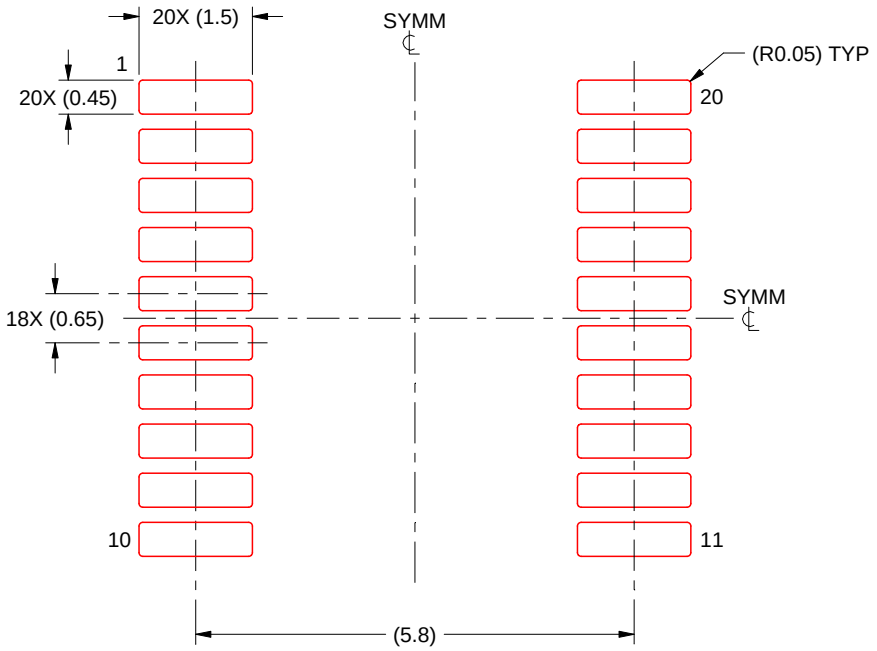
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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